

EMC Performance Evaluation of Various PCB Designs through Simulation and
Measurements

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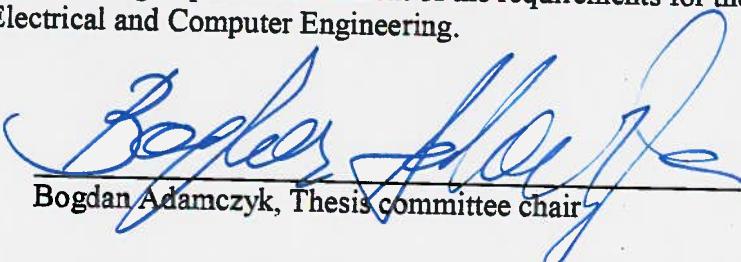
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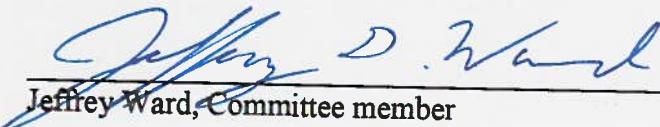


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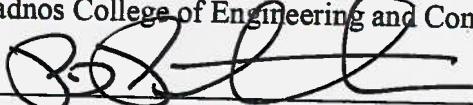
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Dedication

I thank Dr. Prof. Bogdan Adamczyk and Dr. Prof. Karl Frederick Brakora for their dedication to inspire me to be my best. For their belief in me to accomplish what I become without questioning or pressure at any moment. This can only be done by dedicated people who see the best in others.

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Preface

This thesis is based on the research performed of Dimitri Häring. The research was focused on several EMC aspects related to printed circuit board design and RF performance. All PCB's and circuitry were designed by Dimitri Häring in consultation with Dr. Bogdan Adamczyk and Dr. Karl Brakora of GVSU, and Scott Mee of E3 Compliance LLC. All simulations and measurements where done under the supervision of Dr. Bogdan Adamczyk and Dr. Karl Brakora. The VHF auto tuner design was performed by D. Häring with various revisions in different design stations performed by Dr. Prof. Karl Brakora who also supervised the project executed for R.A. Miller Industries Inc. Furthermore, I would like to thank for the support on my thesis by the following people, Daniel Jilote, Bilguun Baatar, Brian Collins. The thesis starts with a broad background in the introduction section.

Abstract

The applied research presented in this thesis is intended to deepen the understanding of various concepts related to PCB design with respect to EMC and RF performance. The first topic addressed is embedded capacitance of a PCB. The work includes decoupling capacitors and their placement relative to the IC in a combination of three different PCB stack-ups. The evaluation is performed in the frequency domain and time domain. The next topic discussed is the EMC/ EMI filters which are essential measurements to protect a device or subsystem from EMI. The circuit's load is usually unknown. A generic filter design is built, which allows the placement of various PCB structures to evaluate filters under different load and source impedance. To convert voltage efficiently, SMPS buck converters are widely used. To suppress EMI, various counter measures for differential mode, and common mode are discussed and measured with a conducted emission (CE) voltage method (V) to evaluate their performance. The designed snubber is evaluated in the time domain by measuring the ringing and the suppressed target frequency content. The results of the above four topics are utilized in a VHF auto tuner design. The results of the embedded capacitance frequency domain evaluation show that the two evaluated 6-layer designs outperform the 4-layer design. Additionally, the 6-layer design with far spaced power plane outperforms the 6-layer version 3 design with not-far spaced power plane referenced to the top signal layer. Grouped capacitors outperform the not grouped capacitors. For not grouped capacitors on a 6-layer design, the evaluation in time and frequency domain shows that the 6-layer designs are particularly enhancing higher frequency content suppression regardless if the capacitors are grouped or not. The filter evaluation showed that for a 2nd order filter the capacitor placed close to the high impedance side shows increased performance. The 3rd order structures π and T show that there is no significant performance decrease if the filter is mounted one way or another. The correlation of the measured and simulated data showed that the ideal case simulations are valid for the ideal behavior of the filter. Due to the bandwidth of a π filter, large components with lower self-

resonance frequencies are favorable. In real-world applications, a π is favorable because there never is just an LC or CL structure due to bulk or decoupling capacitors. The SMPS evaluation showed that the snubber could be designed with Adamczyk's and Spence's approach. The tested EMC filter structures showed clearly that a single component shows an impact on the CE (V) measurement and can be identified by its self-resonant frequency. The filter can be designed for different target frequency ranges, and depending on the design, it will show better or worse results. The shield was added, and the measured interference dropped mainly to the ambient level. On the VHF auto tuner each evaluated topic is discussed and shows that around 50 % of the used components are related to EMC. The presented work illustrates the multidisciplinary character of electromagnetic compatibility (EMC).

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Abbreviations

AC	Alternating Current
AM	Amplitude Modulation
BGA	Ball Grid Array
BOM	Bill of Materials
CE	Conducted Emmissions
CM	Common Mode
CMC	Common Mode Choke
CW	Continuous Waveform
DC	Direct Current
DM	Differential Mode
DMM	Digital Multimeter
DUT	Device Under Test
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
ESL	Equivalent Series Inductance
FB	Feedback
FET	Field Effect Transistor
FFT	Fast Fourier Transform
FR-4	Glass Epoxy Material
GND	Ground
GPIO	General Purpose Input/Output
IC	Integrated Circuit
IL	Insertion Loss
JTAG	Joint Test Action Group
LDO	Linear Drop-out Regulator
LISN	Line Impedance Stabilization Network
LQFP	Low Profile Quad Flat Pack
LVD	Low-Voltage Detect
μ C	Microcontroller

MEDIC	Marshall Space Flight Center Electromagnetic Compatibility Design and Interference Control
NASA	National Aeronautics and Space Administration
OSL	Open, Short, and Load
OSLT	Open, Short, Load, and Through
PCB	Printed Circuit Board
PDN	Power Distribution Network
PWM	Pulse Width Modulation
PWR	Power
QFN	Quad Flat No-leads
RBW	Resolution Bandwidth
RE	Radiated Emmissions
RF	Radio Frequency
RI	Radiated Immunity
SMA	SubMiniature version A
SMPS	Switched Mode Power Supply
SRF	Self-Resonant Frequency
SWD	Serial Wire Debug
SWR	Standing Wave Ratio
TI	Texas Instruments Incorporated
UART	Universal Asynchronous Receiver/Transmitter
V_{DD}	Direct Current Supply Voltage [1]
V_{DDA}	Direct Current Analog Supply Voltage [1]
VHF	Very High Frequency
(V)	Voltage Method
VNA	Vector Network Analyzer

Chapter - 1 Introduction

1.1 Background

A system is electromagnetically compatible with its environment if it satisfies three criteria [2].

1. It does not cause interference with other systems.
2. It is not susceptible to emissions from other systems.
3. It does not cause interference with itself.

A fundamental understanding of Electromagnetic Compatibility (EMC) can be described as a house placed in a sphere. Depending on the observation point lying on the sphere the house may not be recognized as a house because only earth can be seen. By changing the observation point on the sphere, the roof of the house might be seen. In moments of clarity, you might find the spot on the sphere which grants the view through a window into the house. With further investigation, you might find a window where you can see through allowing for this moment of clarity and a understanding of the inside, but in most cases you just see the house. To bring it back to EMC, most often a capacitor is just a capacitor, but depending on the goals and test performed, the capacitor serves different purposes. To give the reader a better understanding of the importance of EMC, this thesis will discuss various EMC case studies under different conditions. The thesis is complicated by the fact that every device has different needs and test conditions. Rao describes in a case study of a complex system like a modern fighter aircraft [3]. The modern fighter aircraft has various subsystems, where every electronically functional system in the aircraft has to be EMC tested. Tests are only valid as long as the tests show reproducible results. On the magnitude of a fighter aircraft, it clearly can be seen that to do so documentation has to be made which describes the hazards, test setup, and test limits. To achieve comparable results meaningful standards are created based on the experience of case studies which describe failures or interference issues. The purpose of this work is to advance

the knowledge and understanding of the techniques and designs which enhance EMC performance. Enhancing EMC performance first usually requires understanding the operation of the circuit and its functionality. Second, to understand the boundaries which limit the capabilities. The further investigations are important because of the increased use of electronic devices, systems, or subsystems. The overall focus on the work rests on the understanding of fundamental principals of various electromagnetic compatibility PCB best practice designs. The first evaluation is done with embedded capacitance, in both the frequency domain then in the time domain. The designs are evaluated by simulations with ideal components and verified and proven with measurements. Therefore various concepts will be discussed, and aspects of them will be investigated in further detail. This is of interest for suppression of EMI and their application to a Very High Frequency (VHF) auto tuner. The next section presents the defined research objectives as approved by the thesis committee. The research objectives defined are shown below.

- Evaluate the embedded capacitance of a PCB with and without decoupling capacitors in frequency and time domain.
- Evaluate common EMC filters under various loads and source conditions.
- Quantify embedded capacitances for EMC filter applications.
- Apply embedded capacitance to EMC filters and snubbers for SMPS circuitry.
- Propose a set of design rules using the knowledge gathered in the above objective.
- Apply EMI suppression techniques to the design of a VHF auto tuner.

It will be shown that the results of these studies can be used to shorten complex simulation processes. This can be used for fast and raw estimations. This helps product designers to make early design choices with respect to EMC in their products. This will result in fewer design iterations and hence reduce costs.

1.2 Embedded Capacitance of a PCB

Embedded capacitance of a PCB is often discussed in terms of Power Distribution Network (PDN). The embedded capacitance is a fundamental measure to lower power bus noise. A capacitor is basically constructed by stacking a non-conductive material between two conductive plates, which is commonly known as plate capacitor. By examining the construction of a printed circuit board closely, the similarity to a plate capacitor can be drawn. In fact a two layer PCB is a capacitor. The embedded capacitance studies is done once for frequency domain and once for the time domain.

1.3 EMC Filters - Source and Load Impedance

Naturally, embedded capacitance is not enough to limit unwanted interference caused by high current flows. A filter, most common a low pass filter because of the use of DC voltage, is used. The filters are usually designed to suppress interference for a specific frequency range and consist usually out of large components with large values.

The applied research will show the effect of different EMC filter structures with reactive passive components. The evaluation of the filters will be mainly on the structure and their use in circuitry with relation to performance, in terms of impedance to ground, lower being better (within a defined frequency range). Lower impedance will lead to a short at a specific frequency and close the current loop. Therefore, EMC filters were simulated, designed, and measured.

1.4 SMPS EMI Suppression Techniques

A common circuit in active electronics is a Switched Mode Power Supply (SMPS), which is an efficient DC/DC down-converter. The fast switching transistors with high currents leads to high-frequency radiated EMI. The main reason is the switching, so the rise or fall

time of the edges from a low to high, or high to low state, process with transistors. A common way to reduce the interference is to slow down the rise and fall time with resistors. This method is only applicable to the point where the functionality starts being affected. Snubber, EMC filter, shielding, and Common Mode Choke (CMC), will be studied as effective suppression techniques. Purposed strategies will be applied and measurements in the time domain with a high-frequency oscilloscope and conducted emissions testing is performed to evaluate if the purposed strategies will protect or suppress generated noise of the switching. Snubber, EMC filter, shielding, and CMC, will be studied as effective suppression techniques.

1.5 VHF Auto Tuner Applied EMC in Design

To apply the gained knowledge of the previously introduced topics, a VHF auto tuner was designed. The tuner design was brought to prototype stage where two fully functional boards were built. The tuner matches the antenna impedance of a VHF whip antenna designed by R.A. Miller Industries Inc. to an 50Ω system over. The frequency range 30 MHz to 50 MHz. The design requirements demand a power handling of 50 W continuous wave. A match is defined as an Standing Wave Ratio (SWR) below 2.0. The tuner is used in combination with the TFM-30 – Technisonic Industries Ltd. radio. The maximum output power of the radio is 10 W. The radio is used in avionics. The intended use of the tuner is in a helicopter. Due to the rugged environment and avionics regulations there are high demands on the design.

Chapter - 2 Review of Literature

2.1 Embedded capacitance of a PCB

Embedded capacitance have been studied by many researchers. The topic is not new, however the increased use of electronics pushes the limits of interference further and tightens the requirements on EMC. Kaiser provides detailed mathematical closed form formulas for various geometric structures regarding embedded capacitance [4]. Capacitance of a plate capacitor is defined according to Eq. 2.1 according to Koris and Schmidt-Walter [5].

$$C = \epsilon \frac{A}{d} \quad (2.1)$$

According to Ott there are two ways to increase the embedded capacitance [6]. First, decrease the height of the dielectric. Second, increase the dielectric constant. This finding corresponds to Koris. This leads to the question why can we not increase the area A. According to Ott there is only a specific area that is effective for interplane coupling [6]. The reason is that the charge has to be moved to be effective this needs time, hence the area cannot be increased to gain increased embedded capacitance. Another way to increase PCB capacitance is proposed by 3M [7], which developed embedded capacitive materials which can be added to the layer stack. This will add capacitance to the board and therefore enhance noise suppression beyond the capabilities of what is achievable by stack-up design. Furthermore, it may allow to reduce number of surface mount components. Ott discusses power supply decoupling in where he explains the reason for decoupling by showing in examples that most power distribution systems do not provide low impedance [6]. Hubing et al. presents in his paper "An experimental investigation of 4-layer printed circuit board decoupling" experiment results with fully populated circuit boards [8]. His experiments ended with the conclusion that closely spaced power and ground planes require different decoupling strategies than a 4-layer stack-up where the two inner layers commonly ground and power are 40 mils spaced apart. Hubing et al. states in his paper

"Power Bus Decoupling on Multilayer Printed Circuit Boards" that the decoupling strategies used for 2 layer boards should not be applied to boards with low impedance due to dedicated power and ground planes inside the board which reduces the inductivity of the board compared to two layers. A analytical discussion with models of multilayer board power distribution are presented [9]. Paul states in his paper "Effectiveness of Multiple Decoupling Capacitors" states that the decoupling capacitors are effective well beyond this self resonant frequency. In his paper Paul presents LTSpice simulation and models of decoupling capacitors [10]. Hubing et al. states in his paper "Effective Strategies for Choosing and Locating Printed Circuit Board Decoupling Capacitors" that the power bus design of PCB is important [11]. The decoupling strategy are depending on various factors. Hubing describes three different decoupling strategies depending on three cafeteria. Hubing, Paul and Ott focusing mainly on general decoupling strategies and there improvement. Erdin and Achar present in there paper "Decoupling Capacitor Placement on Resonant Parallel-Plates Via Driving Point Impedance" a semi-analytical method o evaluate the effectiveness of a decoupling capacitor on resonance power and ground planes [12]. Furthermore an iterative technique is purposed to calculate the effective radius of a decoupling capacitor. EMISTream is a EMI suppression support tool which is specifically designed to analyze PCB on common EMI issues. The tool provides various analysis for power and ground resonance analysis and an EMI design rule checker [13].

This thesis will present on defined cases, the difference of embedded capacitance of closely spaced power and ground planes with respect to no capacitors, not grouped capacitors (one inch distant placed capacitors to the microcontroller) and grouped capacitors (not distant placed capacitors to the microcontroller) placed to the power supply pin. Measurements in time frequency domain are performed with defined ports on the test trace. To test the described cases a fast switching Integrated Circuit (IC) is used which toggles as many pins as possible at the same time. This allows time domain measurements with a differential probe to evaluate the difference of grouped and not grouped capacitors on the

4-layer stack and the 6-layer stack. This research provides valuable information for design and EMC engineers in form of validation of existing concepts. It can also be used from here on to derive closed form models and analytical approaches to further investigate the matter.

2.2 EMC Filters - Source and Load Impedance

Filters are widely used in various disciplines. Filters are used to separate or attenuate voltage and current over a frequency range. In communications systems, boundaries, input impedances, and output impedances are often well known. Where most filters can be calculated with absolute numbers, an Electromagnetic Interference (EMI) filter is relative to the desired frequency range. The frequency range to suppress unwanted emissions is usually based on estimations of previous designs, known harmonics of switchers or based on measurements. The fundamental understanding of the key components of a filter and the filter structure is important for proper design, cost optimization, and fast fixes on end products. The discussion around different filter structures is not new according to Clark and McCullom who is affiliated with National Aeronautics and Space Administration (NASA) at the Marshall Space Flight Center Electromagnetic Compatibility Design and Interference Control (MEDIC) and wrote the MEDIC Handbook [14]. Discussed is that the filtering shall prevent the entrance and exit of EMI from equipment. The types of noise which shall be suppressed are Differential Mode (DM) and Common Mode (CM) noise. The DM noise is defined by a noise current that exits with reference between positive and negative power lines and is generated or coupled in most commonly on the PCB. DM noise is usually minimal above 2 MHz since the line inductance and capacitance line-to-line and ground-to-ground acts as low pass filter. The CM noise travels out of the device over the wires in the same direction and returns over the ground and is capacitively coupled to ground. Due to this coupling, usually common mode noise can be

expected with higher frequency content than differential mode noise, above 2 MHz. The filter discussed in this document is intended to suppress DM noise. According to the filter overview provided by Clark and McCullom shows the overview of 1st and 2nd order filter for high and low impedance configurations of load and source applied to the different possible filter structures. Different examples of filter structures are shown in Fig. 2.1. According to the document, EMI filters are single-section filters or several-section filters which are cascaded to increase attenuation. Furthermore, the stability of an SMPS is discussed with reference to the filter design. The input impedance of the filter consists of the wiring and the impedance of the voltage source supplying the device. During testing the main impedance is defined by the Line Impedance Stabilization Network (LISN) which is in between voltage source and device and operates as known impedance to ensure repeatable results and a measurement port of 50Ω for the spectrum analyzer. Furthermore, the LISN acts as a low pass filter to suppress interference generated by the voltage supply or coupled in from outside cabling of the used test chamber. Adamzyk discusses filter in his books and compares simple filter structures with ideal models.

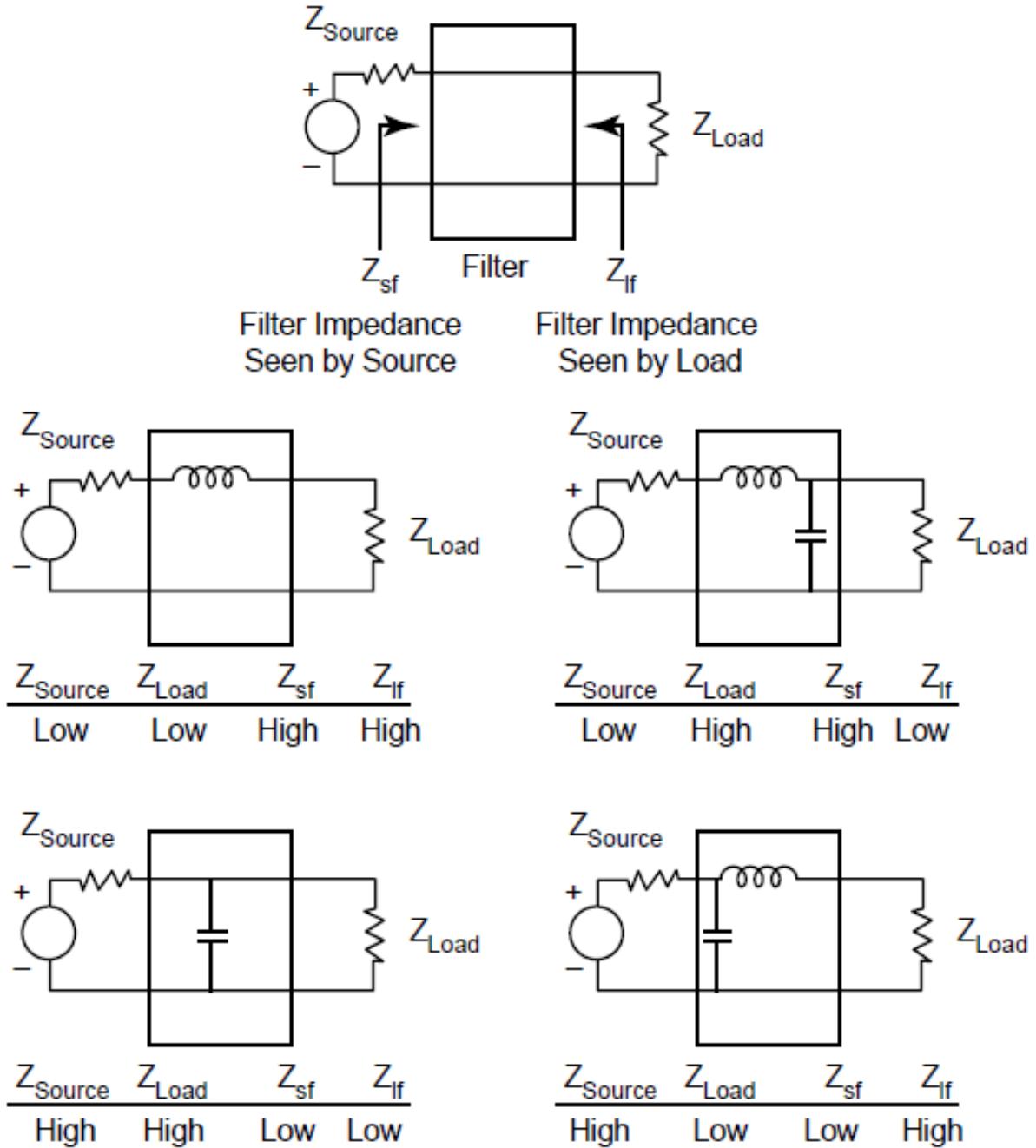


Figure 2.1: EMC Filter configuration examples [14]

The impact of source and load impedance is shown based on ideal models with no parasitic influence [15]. Ott presents insight into the basic filter design in where he discusses briefly filter structures and the advantage of using an ferrite bead over high Q inductors [6]. Furthermore the parasitic effects of filters are discussed. The boundary conditions for

EMC filters are described.

Based on the presented literature a generic filter model is designed to evaluate the effects of load and source impedance of EMC filters. The models will be compared to the ideal simulations. Based on the comparison of simulated and measured results a simple feasible approach of designing an EMC/EMI Filter is presented.

2.3 SMPS EMI Suppression Techniques

Texas instruments wrote a specific guide on how to design snubbers for audio amplifiers, which is named Class-D Output Snubber Design Guide [16]. An output snubber is an RC network placed at the output of a switching audio amplifier. The snubber dampens any ringing or overshoot on the Pulse Width Modulation (PWM) output waveform. The stray inductance in the IC leads, IC bond wires, and PCB traces causes the overshoot and ringing. Having an output snubber provides a low- impedance drainage path to ground for the energy stored in these inductances. Without a provided path, the stored current finds a path through parasitic capacitance on the PCB and causes the overshoot and ringing. Falin wrote an application report on Minimizing Ringing at the Switch Node of a Boot Converter [17]. In the results, he states that the ringing is gone and the overshoot is reduced at the cost of only 2 ns increased switching time of the FET. This implies that there is always a trade-off between reducing ringing and overshoot to switching time. Taylor and Manack wrote a report on controlling switch-node ringing in synchronous buck converters [18]. The report covers three methods on how to reduce ringing in a buck converter. To control rise time of the FETs a series resistor can be used. To improve the behavior of the high side, a boot circuit RC filter is suggested in parallel to the FET. For the low side, an RC circuit is used to build a snubber in parallel to the FET.

According to Clark and McCullom the use of switched mode power supplies is ideal for use on NASA experiments and space platforms [14]. He also points out that a SMPS improp-

erly designed can be a source of EMI and can degrade other systems. According to Adamczyk and Spence a snubber circuit is traditionally designed by measuring the ringing and placing a capacitor until the ringing drops to half of its original magnitude [19]. By using the value of the capacitor found calculations can be performed to calculate the required resistor. However, this can be a time consuming step with try and fail especially when small package size are involved and a differential probe has to be soldered in and out. In the second part of the publication a more practical approach is introduced and demonstrated by an example [20]. A SMPS buck converter is designed and various footprints are placed to evaluate the following EMI suppression techniques a snubber circuit, various EMC filter structures, common mode choke, and shielding. The design itself provides beyond that the option to place a boot circuit, and gate series resistor. The effect of snubber is measured once in time domain and once in frequency domain with a Conducted Emissions (CE) Voltage Method (V) measurement. The effects of various filter designs from 1st to 3rd order are measured with CE (V). The effect of shielding is evaluated in time domain by CE (V) measurement.

Originally only the evaluation of snubbers was planned, during the time and progress of the thesis it got clear a broader discussion will provided not more insight on specific case or idealistic approach with simulations but data and knowledge direct related to measurement and design. The new approach further more supports the previous topic EMC filter in a realistic case.

2.4 VHF Auto Tuner Applied EMC in Design

Multiple auto tuning techniques exist typically the measure the SWR and use then an algorithm to determine the best switching state of the matching circuit [21] - [22]. Litwinczuk presents problems which occur with computer aided automatic tuning designs [22]. A purposed structure of an automatic antenna matching device is shown in Fig. 1 which con-

sists of an attenuator, measurement section VSWR, EMP protection, matching network, EMP protection, antenna, CPU, and driver. The matching circuit is based on tuneable inductor and switched capacitors. A flow chart diagram shows the used computer aided algorithm. Simulations were performed to define and test the quantization of the matching network. As software representation a 8-bit value was used to state the switched capacitance or inductance. Furthermore, the values of used inductance and capacitance are provided in Tab. 1 and Tab. 2. The frequency range used was 18 MHz to 45 MHz. PIN diode Hand Book by Doherty and Joos presents the different circuits of PIN diodes which are commonly used [23]. It describes there benefits in terms of electrical characteristics. Most designs are used as antenna switches. Guzel presents in his master thesis the design and application of PIN switches for X-band and high power application [24].

As the literature review shows no literature on auto tuners in the desired frequency and power range which is based on a state of the art solid state design could be found. Therefore, a whole system design was done to build an VHF auto tuner. The system itself does not seriously differ then the one of the resources. Major points of the design where the design of the directional coupler and the PIN diode RF switch. The driving circuit for the PIN diode RF switch was designed from sketch. The goal is to present a fully functional VHF auto tuner. The finished design which is a prototype is then evaluated and discussed with respect to EMI suppression techniques gathered through out the previous four evaluated topics and there results.

Chapter - 3 Methodology

In this chapter, the applied methods are defined. The defined methods include simulations, Printed Circuit Board (PCB) design, and purposed measurement setup.

3.1 Embedded Capacitance of a PCB

This section will discuss the method used to perform the proof of the relative difference in impedance due to increased inductance and the resulting resonant frequency of different PCB stack-up designs. The suggested method is to define two different layer stack-ups with a well defined spacing between power (PWR) and ground (GND) planes with known ratio. This is a passive measurement conducted with a Vector Network Analyzer (VNA) which will measure the board impedance over a defined trace.

3.1.1 Terms and Definitions

This section provides insight into the used terms and definition throughout this document.

Embedded capacitance The capacitance that exists between a ground and power plane in a printed circuit board.

Closely and not closely spaced Closely spaced (coupled) power and ground planes refers to a distance of a smaller or equal than 5 mil spaced power and ground planes, as shown in Fig. 3.1. Not closely spaced power and ground planes refers to a distance of greater than 10 mil, as shown in Fig. 3.2.

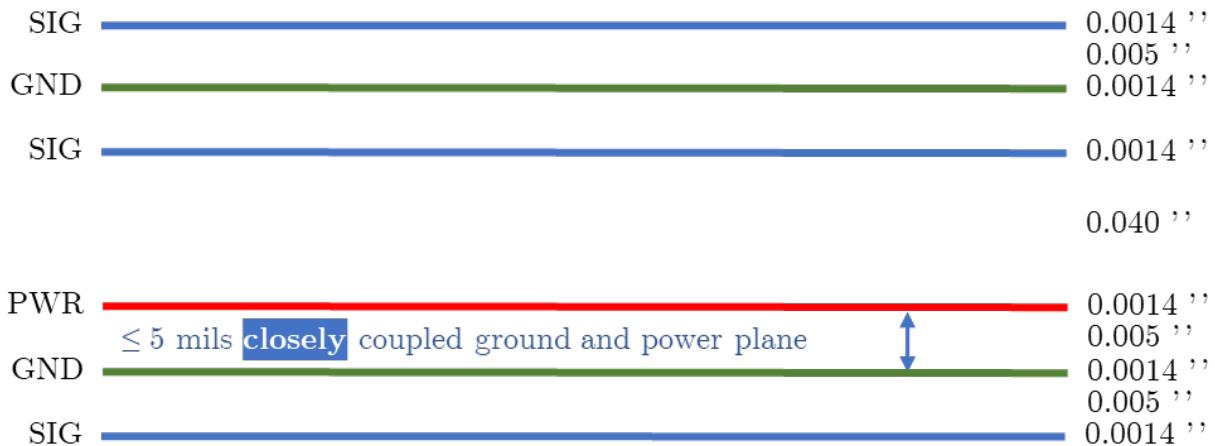


Figure 3.1: Definition of closely spaced (coupled) power and ground planes.

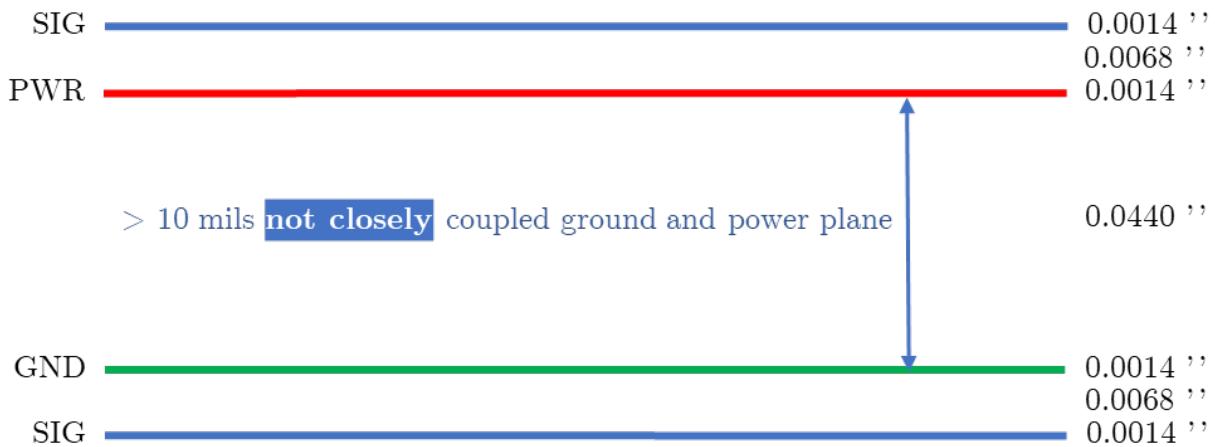


Figure 3.2: Definition of not closely spaced (coupled) power and ground planes.

Far and not-far spaced Far refers to the power plane spacing referenced to the top signal layer, as shown in Fig. 3.3. Not-far refers to the power plane spacing referenced to the top signal layer, as shown in Fig. 3.4.

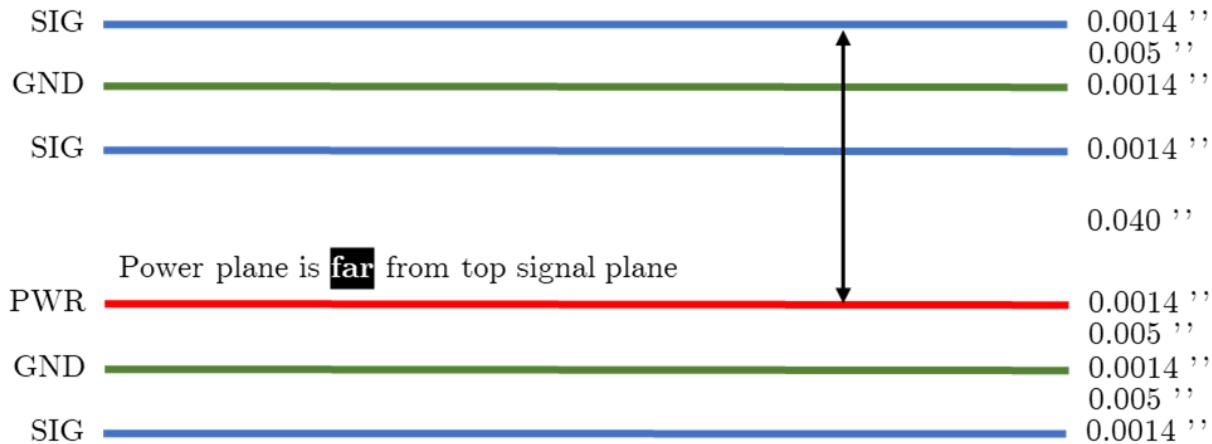


Figure 3.3: Definition of far spaced power plane (layer) measured from top signal layer.

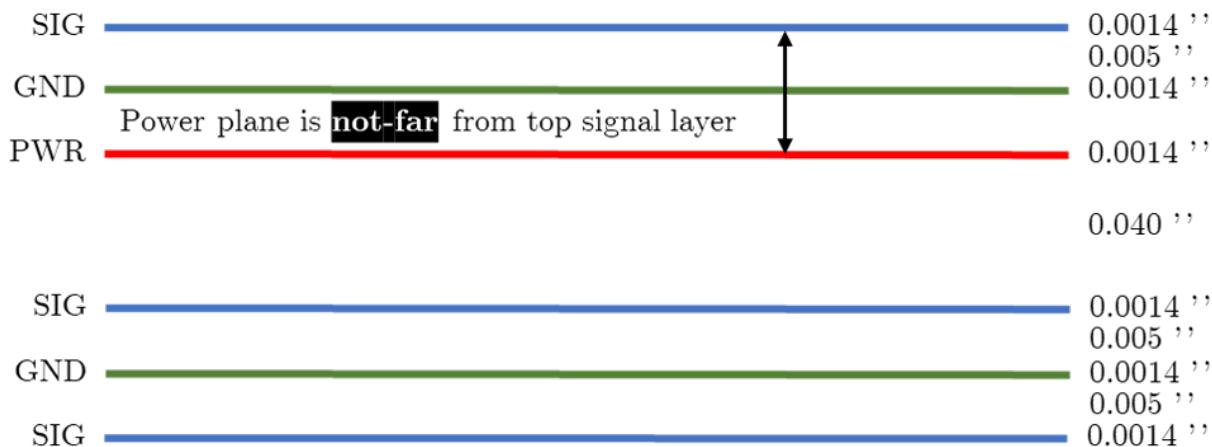


Figure 3.4: Definition of not-far spaced power plane (layer) measured from top signal layer.

Grouped and not Grouped Grouped refers to the distance of the decoupling capacitors to the IC, as shown in Fig. 3.5. Not grouped refers to the distance of the decoupling capacitors to the IC, as shown in Fig. 3.6.

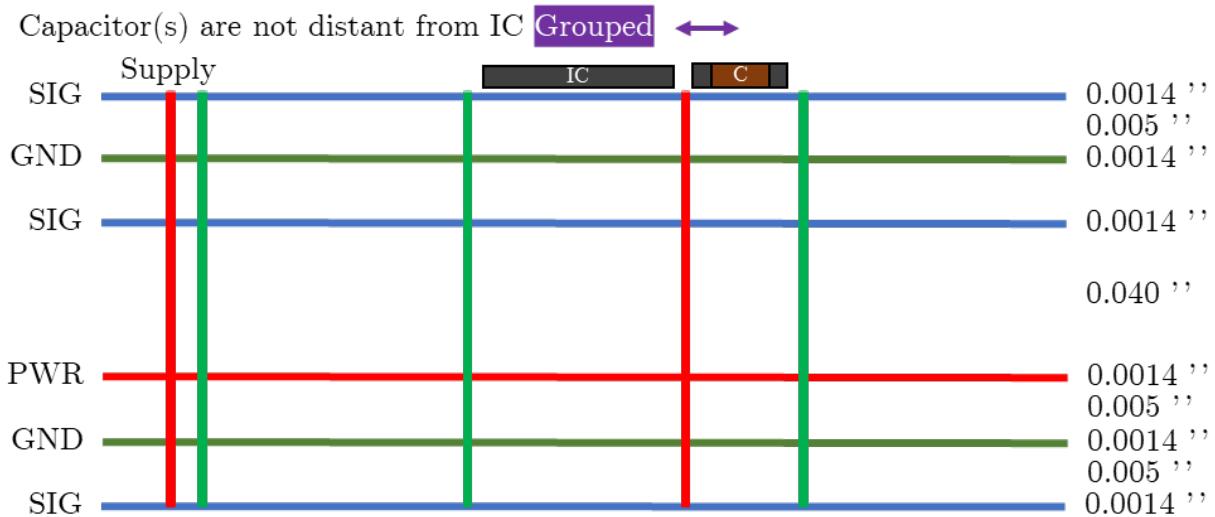


Figure 3.5: Definition of grouped capacitor(s) to the integrated circuit (IC).

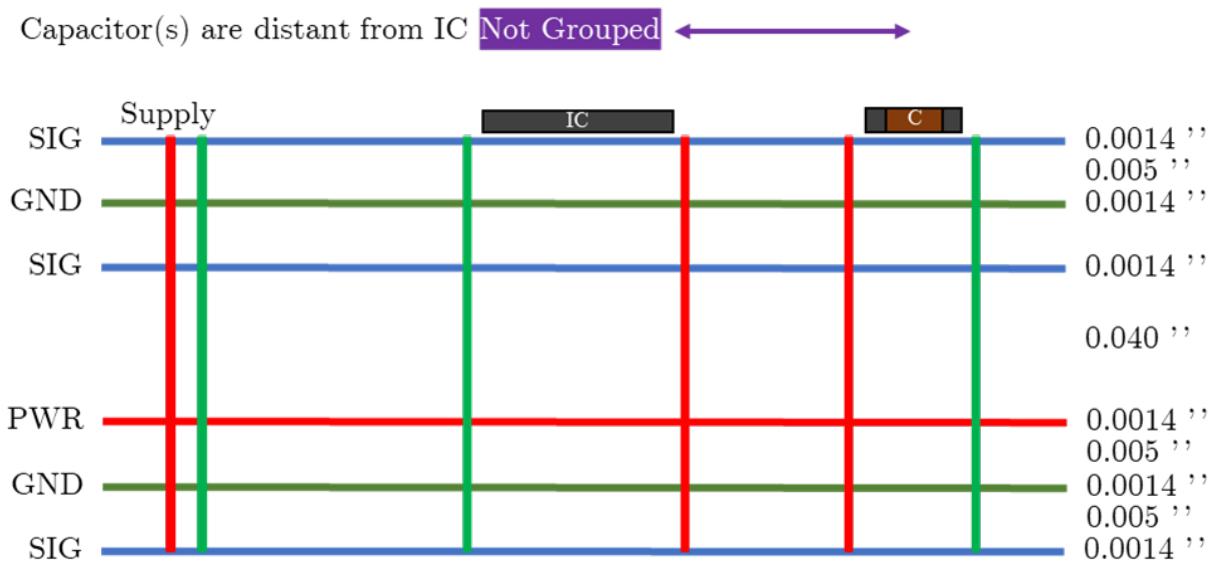


Figure 3.6: Definition of not grouped capacitor(s) to the integrated circuit (IC).

Loop area The loop area is defined by the forward and return path of the current. Fig. 3.7 shows the cross section of a PCB and the discussed definitions.

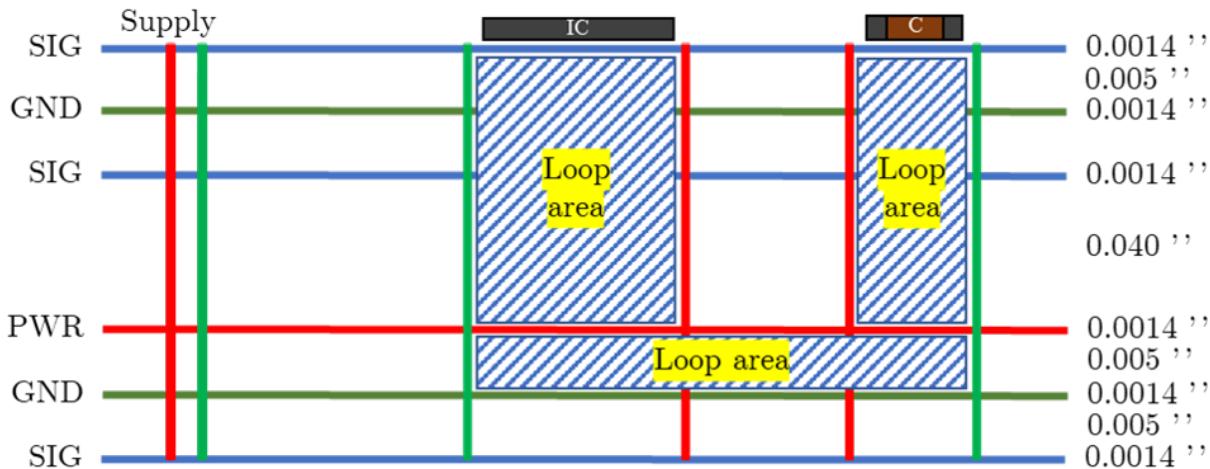


Figure 3.7: Definition of loop areas.

3.1.2 PCB Stack-up

To research the effect of embedded capacitance a four layer stack and a six layer stack were designed. The four layer stack has a 44.9 mil spacing between GND plane and PWR plane, shown in Fig. 3.8. The six layer stack has a 5 mil spacing between GND plane and PWR plane , shown in Fig. 3.9. As dielectric glass epoxy material (FR-4) is used. A big challenge was to find a manufacturer that could actually manufacture the 6-layer stack-up. An additional board with a 6-layer (L6) stack-up is designed that has a slight alteration in layer order and additional footprints intended to use for VNA calibration, shown in Fig. 3.10. In the stack-up 6-layer version 3 (v3), layer three and layer five were swapped compared to the previous 6-layer board. This presents the far-spaced power and ground planes.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.38mil		
4	Dielectric 1	1x 7628 AT05 47% Resin TG130	6.89mil	4.29	
5	GND	Copper	1.38mil		
6	Dielectric 2	6x 7628M 43% Resin TG150	44.49mil	3.96	
7	Signal Layer 1	Copper	1.38mil		
8	Dielectric 3	1x 7628 AT05 47% Resin TG130	6.89mil	4.29	
9	GND Bottom	Copper	1.38mil		
10	Solder Side	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

Figure 3.8: Layer stack 4-layer (L4) board.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric 1	Prepreg	5.00mil	4.2	
5	GND Internal Plane 1	Copper	1.40mil		
6	Dielectric 5		5.00mil	4.2	
7	Signal Layer 1	Copper	1.42mil		
8	Dielectric 4		40.00mil	4.2	
9	GND - Internal Plane 1	Copper	1.42mil		
10	Dielectric 3	FR-4	5.00mil	4.2	
11	PWR - Internal Plane 2	Copper	1.42mil		
12	Dielectric 2	Prepreg	5.00mil	4.2	
13	Bottom Layer	Copper	1.40mil		
14	Bottom Solder	Solder Resist	0.40mil	3.5	
15	Bottom Overlay				

Figure 3.9: Layer stack 6-layer (L6) board.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric 1	Prepreg	5.00mil	4.2	
5	GND Internal Plane 1	Copper	1.40mil		
6	Dielectric 5		5.00mil	4.2	
7	PWR - Internal Plane 2	Copper	1.42mil		
8	Dielectric 4		40.00mil	4.2	
9	Signal Layer 3	Copper	1.42mil		
10	Dielectric 2	Prepreg	5.00mil	4.2	
11	GND - Internal Plane 4	Copper	1.42mil		
12	Dielectric 3	FR-4	5.00mil	4.2	
13	Bottom Layer	Copper	1.40mil		
14	Bottom Solder	Solder Resist	0.40mil	3.5	
15	Bottom Overlay				

Figure 3.10: Layer stack 6-layer version 3 (v3) board with alternative stack-up for far-spaced power and ground planes.

3.1.3 PCB Features

The PCB features are shown in Fig. 3.11. The PCB has four mounting holes, one in each corner. To attach a power supply two footprints for banana jacks are provided to feed the GND plane and the PWR trace to the Linear Drop-out Regulator (LDO) with a positive 5 V supply voltage.

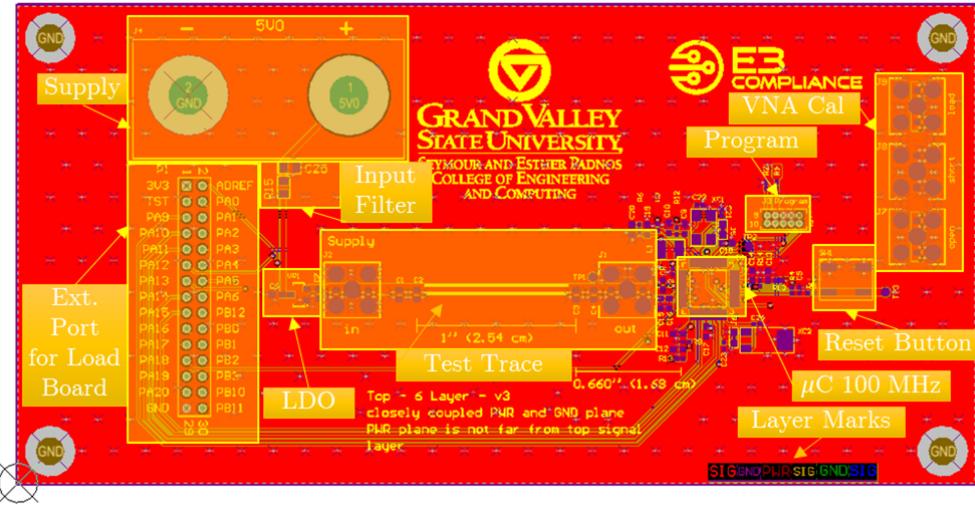


Figure 3.11: Top of the PCB with highlighted features.

The capacitor C25 and R15 can be used as input filter if required. The LDO VR1 is used to provide a stable supply voltage to the μ C with a voltage output of 3.3 V. C6 and C7 are used as bypass capacitors for the LDO and have been chosen according to the requirements described in the LDO's data sheet [25]. The test trace is placed between the LDO out pin and the microcontroller (μ C) V_{in} pin. The test trace consists of two Molex female through hole SubMiniature version A (SMA) connectors and the capacitor footprints C1, C2, C3, and C4. The capacitors C1 and C2 are not grouped. The capacitors C3 and C4 are grouped. The distance between C2 and C3 is one inch. The microcontroller is an ATMEL - ATSAM4S2AAU in an Low Profile Quad Flat Pack (LQFP) 48 package with a clock frequency of 100 MHz [26]. The components around the μ C are chosen according to the reference design of the development kit. The header J3 is used to program the μ C

with a Segger J-Link probe over a Serial Wire Debug (SWD) or Joint Test Action Group (JTAG) interface. A button is used to reset the μ C. The General Purpose Input/Output (GPIO) are routed over the different signal layers from the μ C to the header P1. On the top overlay or silkscreen a distinguished description is printed that allows the separation between the 4-layer board and the 6-layer board. Keep out area on each layer with a text describing the current layer is placed on the right bottom side which serves the purpose to avoid Gerber files or stack-up failures. The dimensions of the board are three inches by six inches.

Due to recognized issues during calibration with the VNA, a new version of the 6-layer stack-up was designed. The board is generally mentioned just as "v3". The main difference is the stack-up as discussed in Section 3.1.2 and the VNA calibration footprints marked in white as shown in Fig. 3.11. The calibration was done for Open, Short, and Load (OSL). The through for a two port calibration is intended to be done with an SMA through connector female to female, which allows to perform a Open, Shot, Load, and Through (OSLT) calibration.

3.1.4 PCB Frequency Domain

To measure embedded impedance of a PCB trace and the impedance change caused by decoupling capacitors, the PCB shown in Fig. 3.12 was designed. The blue boards consist of 6-layers with 5 mil spacing and the green boards consist of 4-layers with 40 mil spacing between the signal top layer and the ground plane. The full Altium Designer project can be found under the following path / < *ProjectRepository* > /01_Altium/ or the hardware documentation is shown in Appendix A.2. The test trace between grouped and not grouped capacitors is one inch long. The surface mount SMA through hole connector was a specially designed to simplify the combination of the two designs. Table 3.1 shows the evaluated cases with no capacitors, grouped capacitors, and not grouped capacitors versus the closely spaced GND and PWR planes of the 6-layer stack-up and the not closely

spaced GND and PWR planes of the 4-layer stack-up.



Figure 3.12: PCB designed for frequency domain measurements.

Table 3.1: No capacitor, not grouped capacitor, and grouped capacitor case.

Case	Top View
No capacitor	

Continuation of Table 3.1	
Case	Top View
Not grouped capacitor	
Grouped capacitor	

Schematic

Fig. 3.13 shows the two SMA connectors J1 and J2 that are connected with a single undisturbed trace to each other. On the trace are four capacitors placed that are grounded on the second side which are designed to be decoupling capacitors. Capacitor C1 and C2 are placed one inch apart of capacitor C3 and C4. This configuration as shown here is used to measure the impedance of the three test cases which are no capacitors, grouped capacitors and not grouped capacitors.

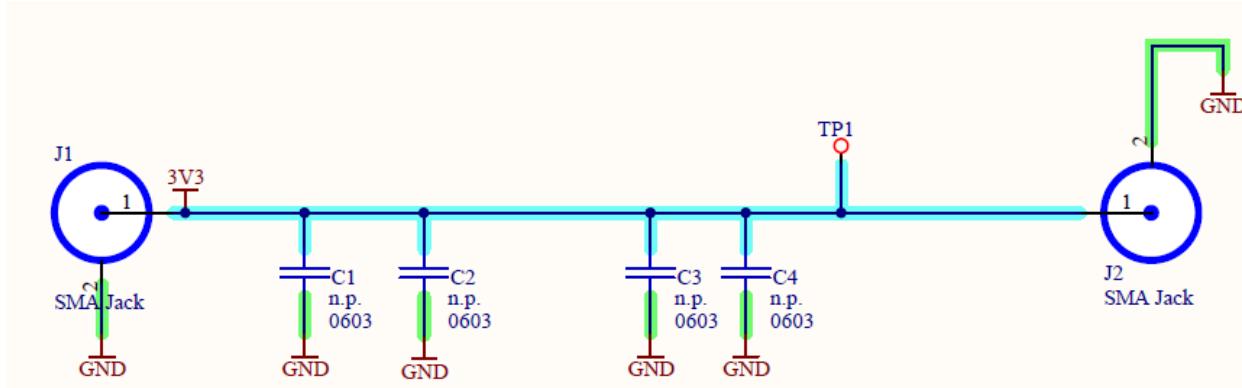


Figure 3.13: Schematic test trace used for VNA measurements in frequency domain.

Bill of Materials

For the connectors, a SMA through hole connector is used. The connector is only soldered onto the top layer of the PCB surface. The reason to do so is that it represents best a real world measurement.

- TE Connectivity female through hole SMA connector 5-1814832-1

Table 3.3 shows which type of capacitor is soldered on to the specific land pattern named by the reference designator. Fig. 3.13 shows the schematic presentation of the physical board as it is designed.

Table 3.3: Placement of decoupling capacitors based on the three defined cases, and their nominal values.

Ref. Designator	no Capacitor	Grouped Capacitor	not Grouped Capacitor
C1	-	-	0603 25V 0.1 μ F CGA3E2X8R1E104K080AA
C2	-	-	0603 25V 0.1 μ F CGA3E2X8R1E104K080AA
C3	-	0603 25V 0.1 μ F CGA3E2X8R1E104K080AA	-
C4	-	0603 25V 0.1 μ F CGA3E2X8R1E104K080AA	-

The capacitor CGA3E2X8R1E104K080AA used for testing in Tab. 3.3 have according to the manufacturer TDK the flowing characteristics, as shown in Fig. 3.14. Presented is the impedance vs. frequency plot. The resonant frequency is around 20 MHz.

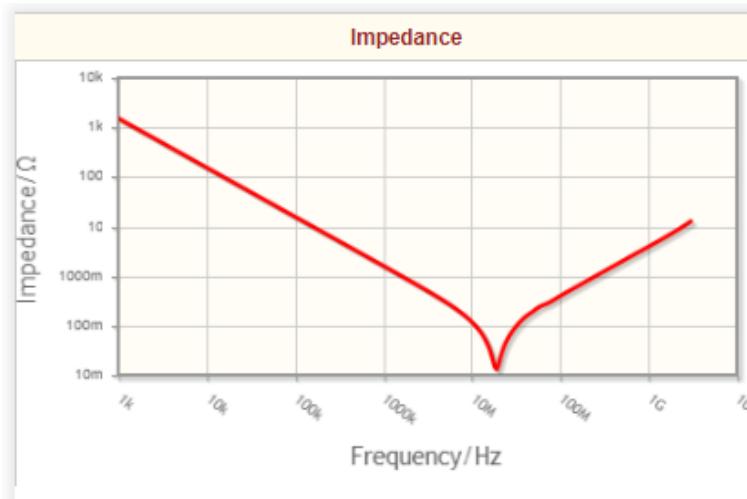


Figure 3.14: TDK CGA3E2X8R1E104K080AA capacitor characteristics [27].

3.1.5 PCB Transient Response

To measure the time domain behavior, a μ C is placed after the test trace of the frequency domain testing which is fed by an LDO. Test point TP1 in the traces allows to measure with an oscilloscope the noise difference between the three different test cases and the comparison between 4-layer and 6-layer PCB. To run the μ C, embedded software is written in C language to toggle the GPIO as fast as possible which will cause additional noise that should be to a certain point prevented with an advanced decoupling strategy. Fig. 3.15 shows a populated board with a μ C and all components related to it.

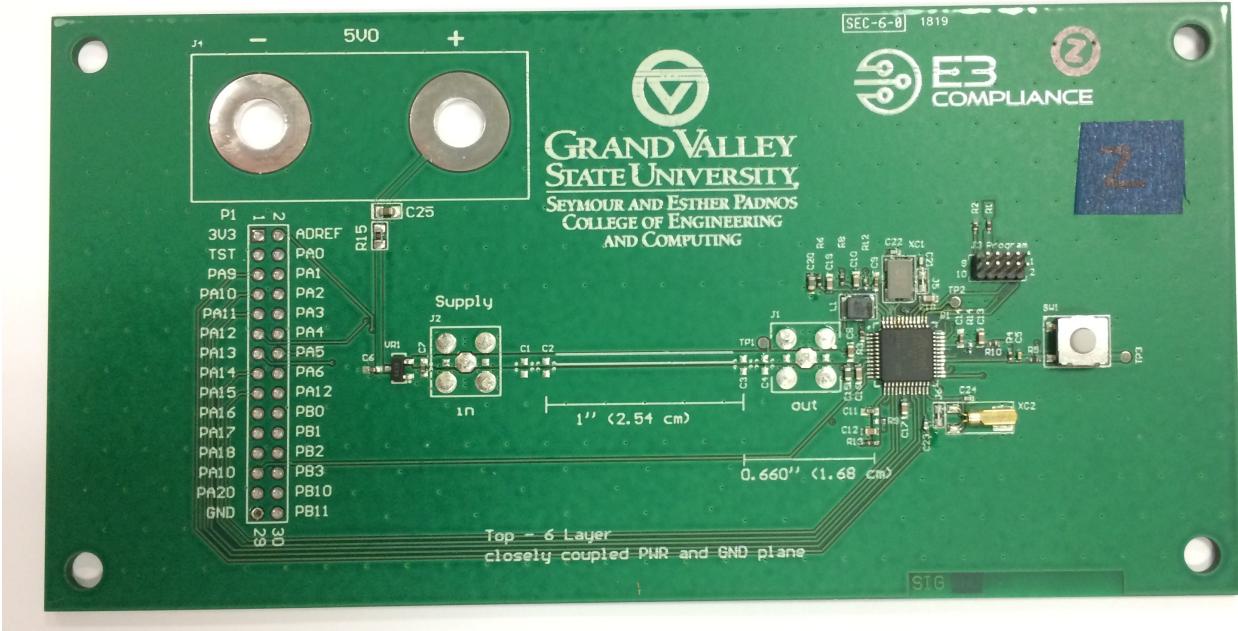


Figure 3.15: PCB populated with μ C.

Microcontroller

The requirements for the microcontroller (μ C) are that it has to be fast switching, which means a high clock. The chosen microcontroller was an Atmel SAM4S having a clock speed of 100 MHz which allows toggling all GPIO with a switching frequency of approximately 3.15 MHz with a duty cycle of 50% [26].

Bill of Materials

This full bill of material is shown in Appendix A.7.

3.1.6 Costs

The costs of the boards and equipment including components are shown in Tab. 3.4. The total price includes stencil for reflow assembly. The price increase from a 4-layer board standard available stack-up manufactured in China to a 6-layer board custom stack-up manufactured in the United States is 3.35. The costs of components are not compared.

The components on the each board are exactly the same.

Table 3.4: Embedded capacitance PCB costs.

Description	Price/Unit in \$	No of Units	Total in \$
4-Layer PCB	15.40	10	154.00
6-Layer	51.68	15	775.10
6-Layer version 3	51.68	15	775.10

3.2 EMC Filters - Source and Load Impedance

To investigate the frequency domain behavior of EMC filters, the following techniques are proposed: simulation in LTSpice, and the empirical approach of building a generic filter which will illustrate the impact of different load, and source combinations. One of the main issues of designing a filter is that the load might not be known precisely enough to switching of active components or unknown frequency content which changes load impedance. The unknown frequency content can be coupled or generated by active circuitry. The impact of the topology which leads to design symmetries or asymmetries is therefore essential. A filters topology is heavily impacted due to its requirements which inherent often that a Direct Current (DC) current has to pass through. The requirement limits the choice of topology that no capacitor can be used in series. The topology variation is limited to 3rd order because a filter higher order can be represented as a combination of two or more filter. The economic desire of having the most effective filter for the lowest possible cost leads to the argument that the lowest amount of discrete components should be used to reach the specification. Therefore, an asymmetric filter design might be used. In the asymmetric case, the best performance of a filter is attained by choosing the topology in which the capacitor is placed in parallel next to the high impedance site. Fig. 3.16 gives an overview on the important components and the placement of the filter. It also defines the naming of

the filter structures. The first letter to the left is next to the source while the letter to the right is next to the load, as shown in the figure is an LC filter which means L is next to the source and C is next to the load.

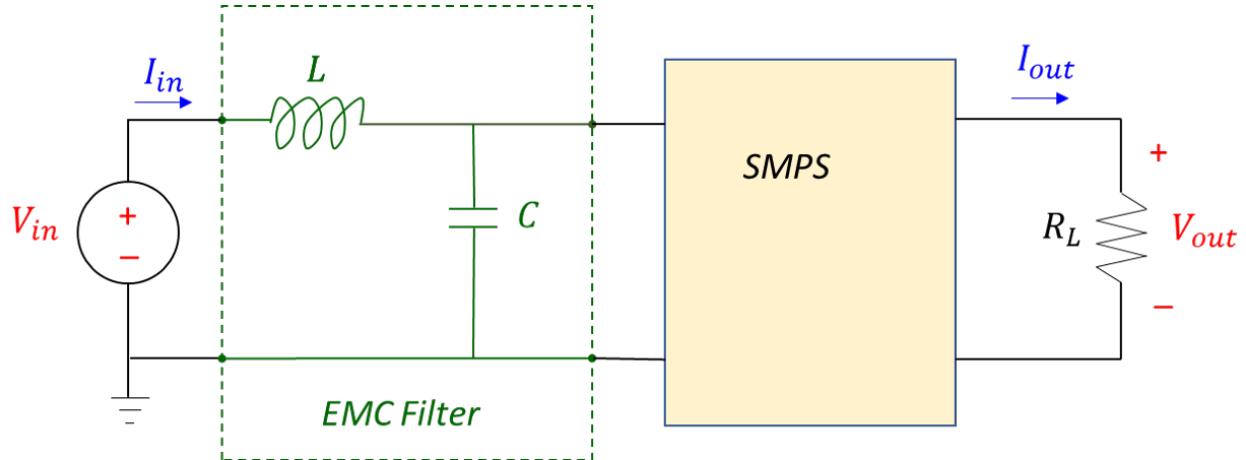


Figure 3.16: Example of an EMC filter placement on a SMPS.

The reason for using low-pass is that DC has to pass through. The 1st and 2nd order low-pass filter structures were discussed in Section 2.2. Fig. 3.17a shows a 3rd order filter structure consisting of an inductor, capacitor, and inductor (LCL), due the shape the filter is named T filter structure. Fig. 3.17b shows a 3rd order filter structure consisting of a capacitor, inductor, and capacitor (CLC), due the shape the filter is named pi (π) filter structure.

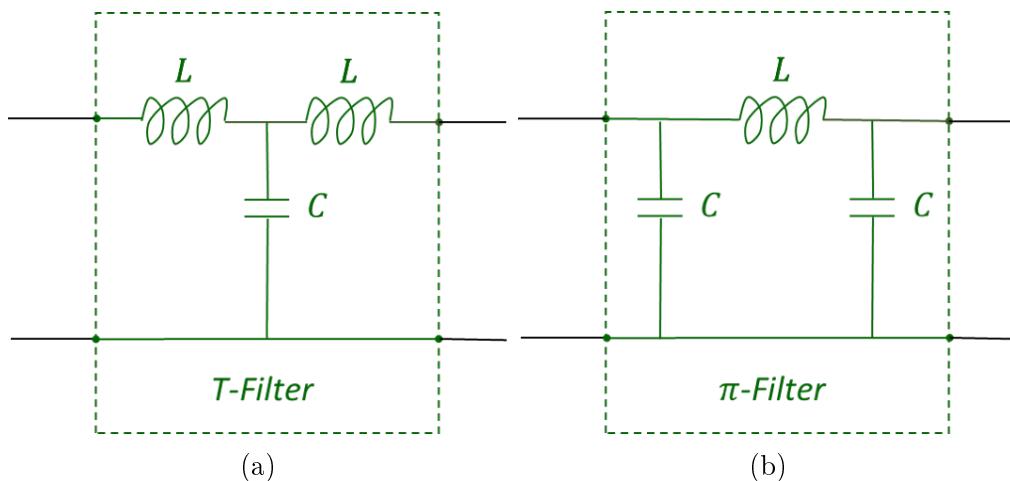


Figure 3.17: EMC filter typologies 3rd order, low pass.

Each order adds an additional slope of 20 dB per decade which can be computed by multiplying the filters order with 20 dB to calculate the estimated largest slope of the filter type.

3.2.1 Filter design

In this section the design and decisions that were made to achieve the EMC filter PCB design are discussed. The software package used to design the PCB is Altium Designer. The schematic is designed to allow a variety of filter designs, the designs are based on the theory presented in Adamczyk book [15]. The filter layout is based on a generic design which allows to build C, L, CL, LC, PI, and T filter structures. The filter can be measured with a VNA with SMA connectors. Due to the decision made to use different package sizes a slight asymmetry in the design occurs which might be seen in the measurements.

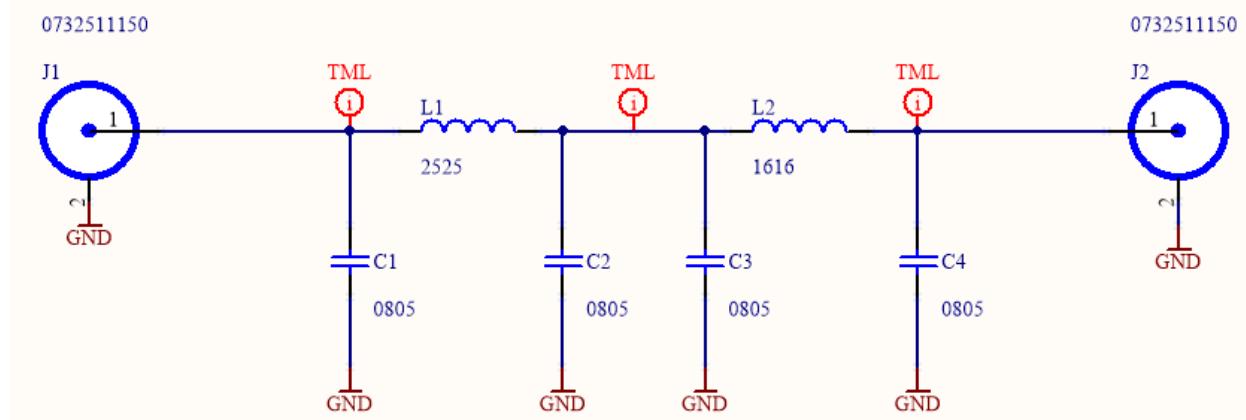


Figure 3.18: Generic EMC Filter schematic.

The designed PCB is shown in Fig. 3.19. J1 and J2 are equipped with straight female edge mount SMA connectors. L1 and L2 can be either populated with an inductor or a 0Ω resistor. C1 to C4 can be equipped with a capacitor or with a resistor depending on the desired filter structure and circuit which shall be analyzed.

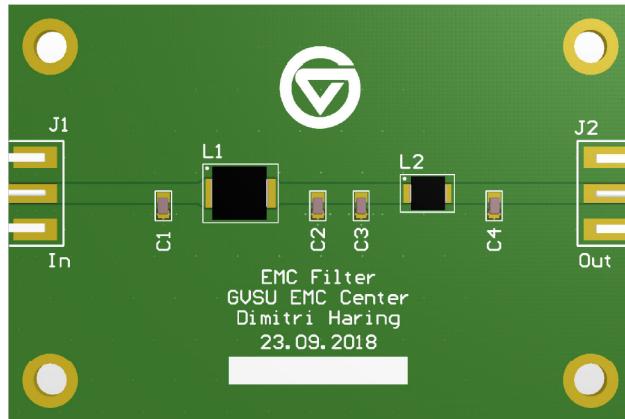


Figure 3.19: EMC filter 3D PCB top view.

PCB Stack-up

The stack-up is a two layer design with 62 mils spacing between top and bottom layer with 1 oz copper. FR-4 is used as dielectric.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric 1	FR-4	59.20mil	4.2	
5	Bottom Layer	Copper	1.40mil		
6	Bottom Solder	Solder Resist	0.40mil	3.5	
7	Bottom Overlay				

Figure 3.20: EMC filter stack-up 2-layer design 62 mil board height 1 oz copper.

PCB Features

The PCB consists of multiple pads that allows to populate different filter typologies. The footprints vary in size. L1 is 2525 package size and L2 is 1616 package size which allows to test not only filter structures beyond that the impact of different components size can be shown. The design was kept as simple as possible to avoid unwanted influence on the measurements.

Bill of Materials

Table 3.5 shows a list of the used parts used to implement different designed filter structures.

Table 3.5: Parts List EMC Filter.

Part	Value	Manufacturer	Part Number
Resistor	0 Ω	Panasonic Electronic Components	ERJ-12Y0R00U
Resistor	1 k Ω	Stackpole Electronics Inc.	RMCF0603JT1K00
Resistor	10 k Ω	Stackpole Electronics Inc.	RMCF0603JT10K0
Resistor	91 k Ω	Stackpole Electronics Inc.	RMCF0603JT91K0
Capacitor	10 nF	KEMET	C0603C103J5RACTM
Inductor	4.7 μ H	Vishay / Dale	IHLP1616BZER4R7M5A
Connector		Molex	0732511150

3.2.2 LTspice Simulations of different filter typologies in ideal case

The simulations show the ideal case of different filter typologies simulated in LTspice with ideal components. These ideal simulations can be used to verify the measurements.

The simulations are normalized to unity voltage of 1 VAC voltage source. The source impedance RS is 50 Ω . The inductor value is 4.7 uH. The capacitor value is 10 nF. The load impedance varies from 50 Ω to 91 k Ω .

For filter comparison, the insertion loss is plotted in LTspice with a log scale in frequency, x-axis, and magnitude, y-axis.

Simulation LC - R 1 k Ω Vs. CL - R 1 k Ω Filter Structure

The literature review indicates a good way to compare two filter structures is to use the Insertion Loss (IL) which can be simulated and measured with a VNA. The IL is calcu-

lated according to Eq. 3.1.

$$s_{21} = \frac{b_2}{a_1} = \frac{V_2^-}{V_1^+} \quad (3.1)$$

Fig. 3.21 shows three circuits. To the left is the circuit with no filter and no additional load used to normalize the circuit with filter. To the right top is the circuit with filter and load, LC - R 1 kΩ. To the right bottom is the circuit with filter and load, CL - R 1 kΩ.

Fig. 3.22 shows the plotted IL. The compared structures are LC - R 1 kΩ (green) versus CL - R 1 kΩ(royal blue). Points where the magnitude and frequencies are similar are marked light blue. The curves start at an offset of -21.2 dB. At 1 MHz both graphs have a magnitude of -30.8 dB. At 10 MHz the CL-R structure has a magnitude of -50.7 dB. At 10 MHz the LC-R structure has a magnitude of -65.8 dB. The slope per decade in the frequency range of 1 MHz to 10 MHz is -19.9 dB for the CL-R structure, and -35 dB for the LC - R structure. By subtracting slope CL-R of slope LC-R, the deviation at 10 MHz is 15.1 dB. Beyond a frequency of 40 MHz, both graphs show similar behavior.

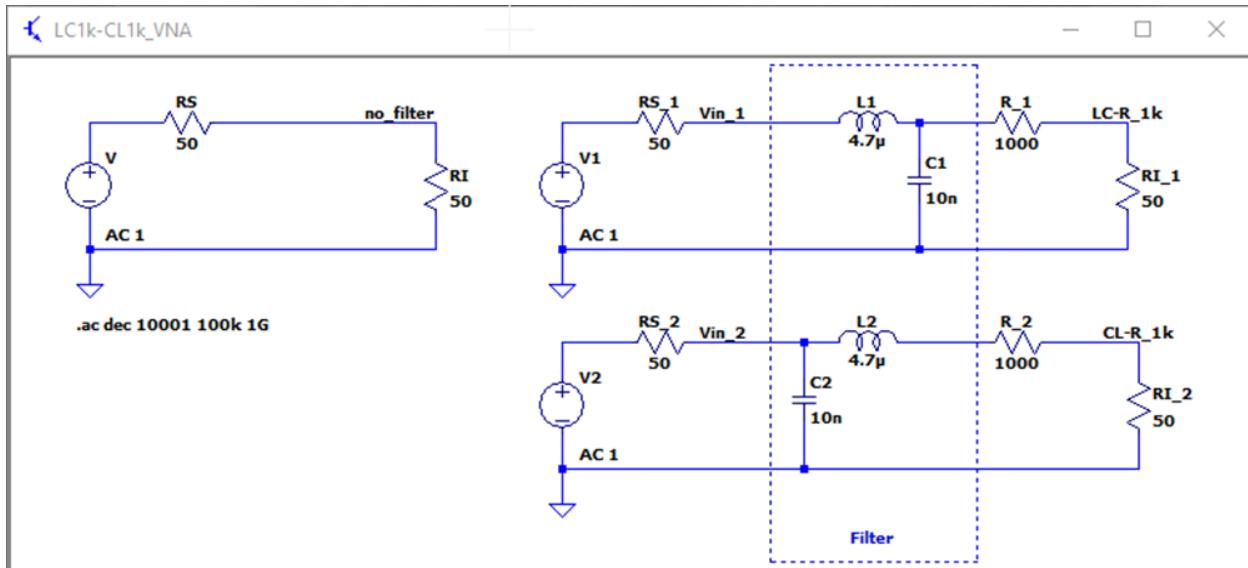


Figure 3.21: EMC filter simulation LC - R 1 kΩ vs. CL - R 1 kΩ, schematic

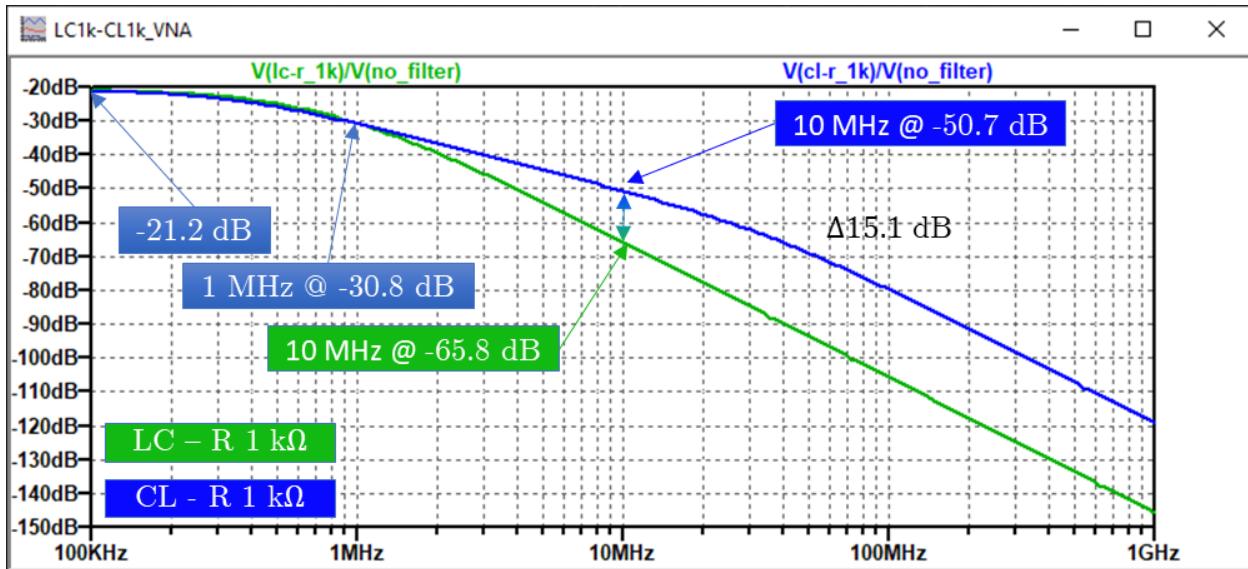
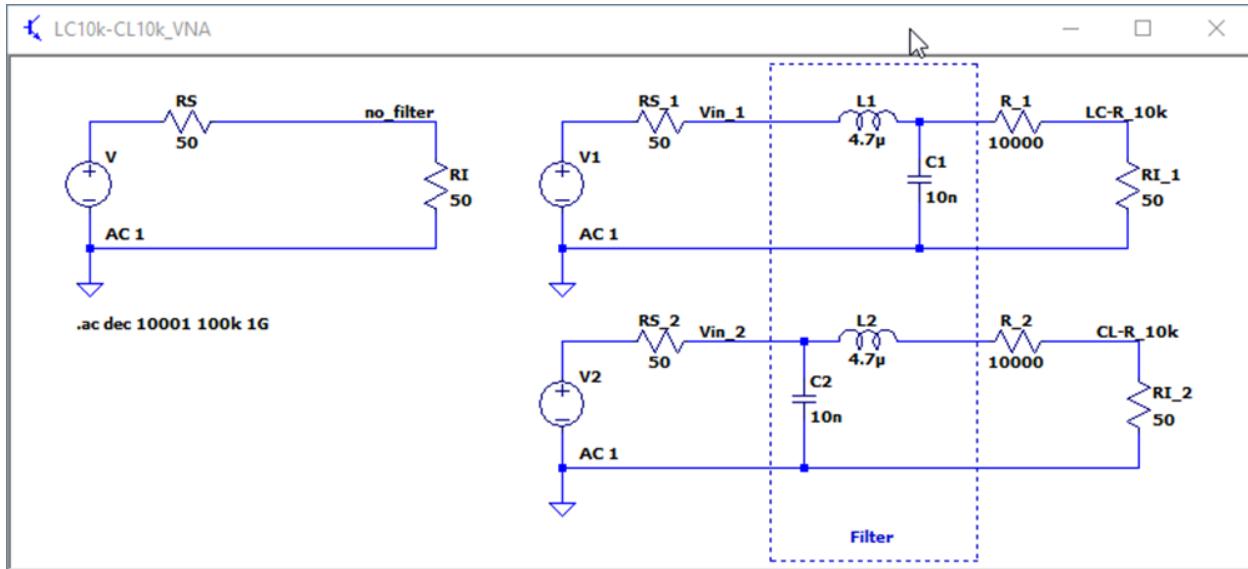
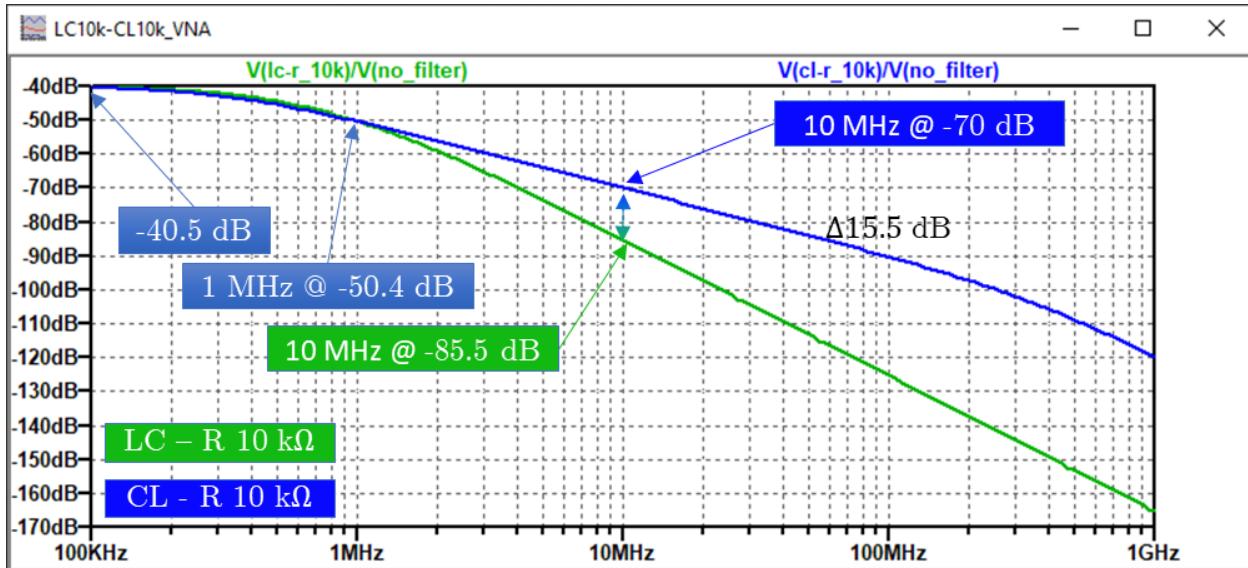


Figure 3.22: EMC filter simulation LC - R 1 kΩ vs. CL - R 1 kΩ, plot

Simulation LC - R 10 kΩ Vs. CL - R 10 kΩ Filter Structure

Fig. 3.23 shows three circuits. To the left is the circuit with no filter and no additional load used to normalize the circuit with filter. To the right top is the circuit with filter and load, LC - R 10 kΩ. To the right bottom is the circuit with filter and load, CL - R 10 kΩ. Fig. 3.24 shows the plotted IL. The compared structures are LC - R 10 kΩ (green) versus CL - R 10 kΩ(royal blue). Points where the magnitude and frequencies are similar are marked light blue. The curves start at an offset of -40.5 dB. At 1 MHz both graphs have a magnitude of -50.4 dB. At 10 MHz the CL-R structure has a magnitude of -70 dB. At 10 MHz the LC-R structure has a magnitude of -85.5 dB. The slope per decade in the frequency range of 1 MHz to 10 MHz is -19.6 dB for the CL-R structure, and -35.1 dB for the LC - R structure. By subtracting slope CL-R of slope LC-R, the deviation at 10 MHz is 15.5 dB. Beyond a frequency of 800 MHz, both graphs show similar behavior.

Figure 3.23: EMC filter simulation LC - R 10 k Ω vs. CL - R 10k Ω , schematic.Figure 3.24: EMC filter simulation LC - R 10 k Ω vs. CL - R 10k Ω , plot.

Simulation LC - R 91 k Ω Vs. CL - R 91 k Ω Filter Structure

Fig. 3.25 shows three circuits. To the left is the circuit with no filter and no additional load used to normalize the circuit with filter. To the right top is the circuit with filter and load, LC - R 91 k Ω . To the right bottom is the circuit with filter and load, CL - R 91 k Ω .

Fig. 3.26 shows the plotted IL. The compared structures are LC - R 91 k Ω (green) ver-

sus CL - R 91 k Ω (royal blue). Points where the magnitude and frequencies are similar are marked light blue. The curves start at an offset of -59.5 dB. At 1 MHz both graphs have a magnitude of -69.6 dB. At 10 MHz the CL-R structure has a magnitude of -89.1 dB. At 10 MHz the LC-R structure has a magnitude of -104.6 dB. The slope per decade in the frequency range of 1 MHz to 10 MHz is -28.5 dB for the CL-R structure, and -35 dB for the LC - R structure. By subtracting slope CL-R of slope LC-R, the deviation at 10 MHz is 15.5 dB. Beyond the frequency of 10 MHz, both graphs show similar behavior and extrude.

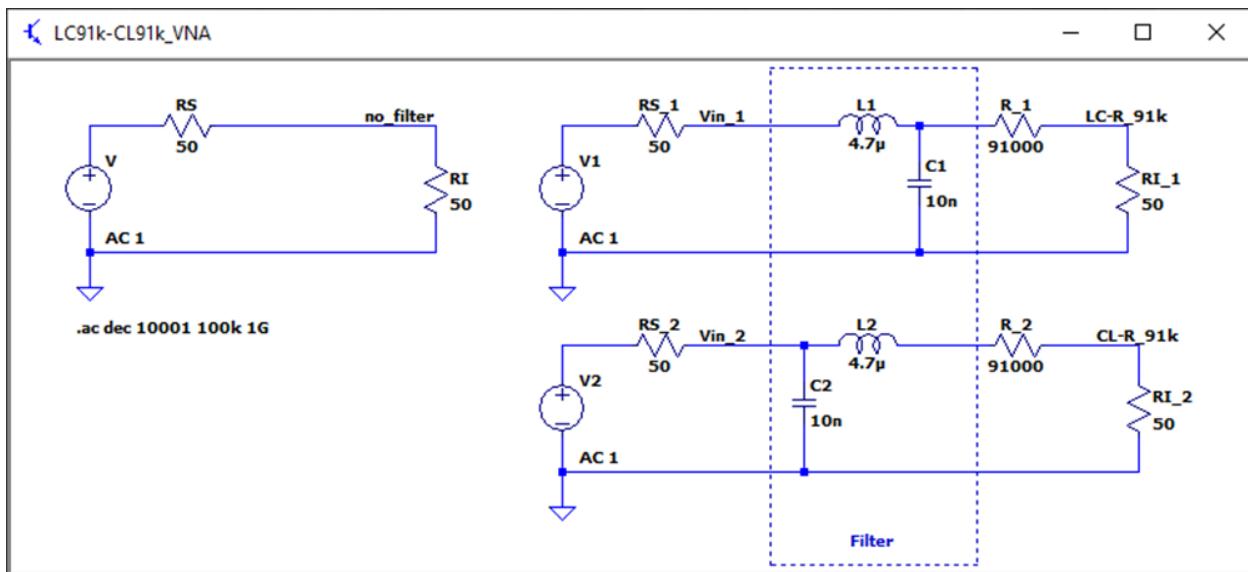


Figure 3.25: EMC filter simulation LC - R 91 k Ω vs. CL - R 91 k Ω , schematic.

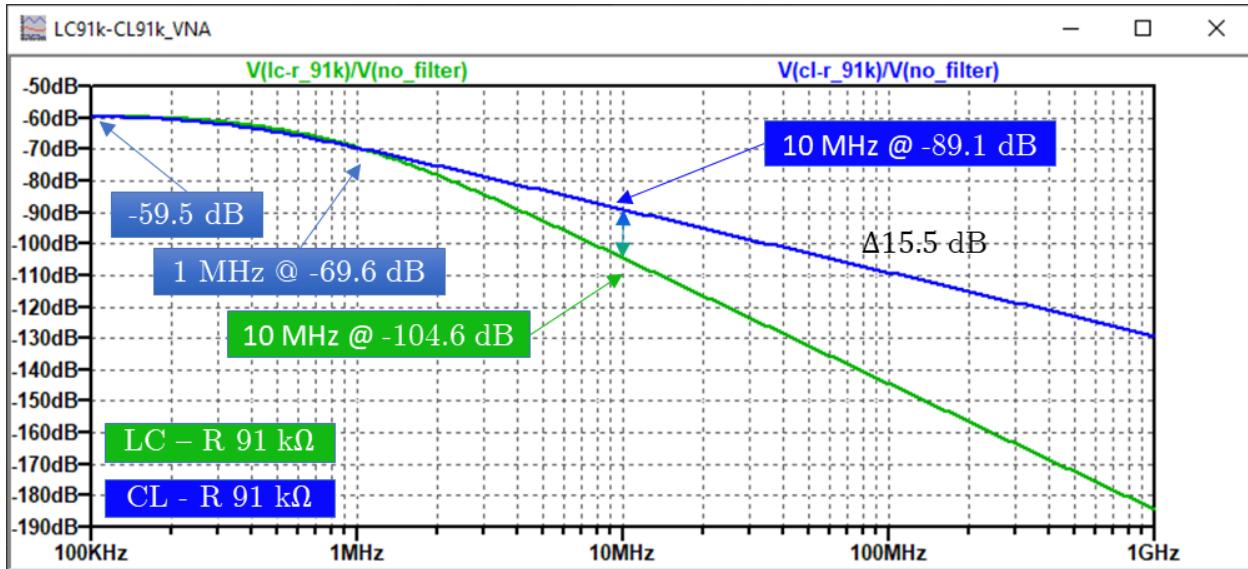
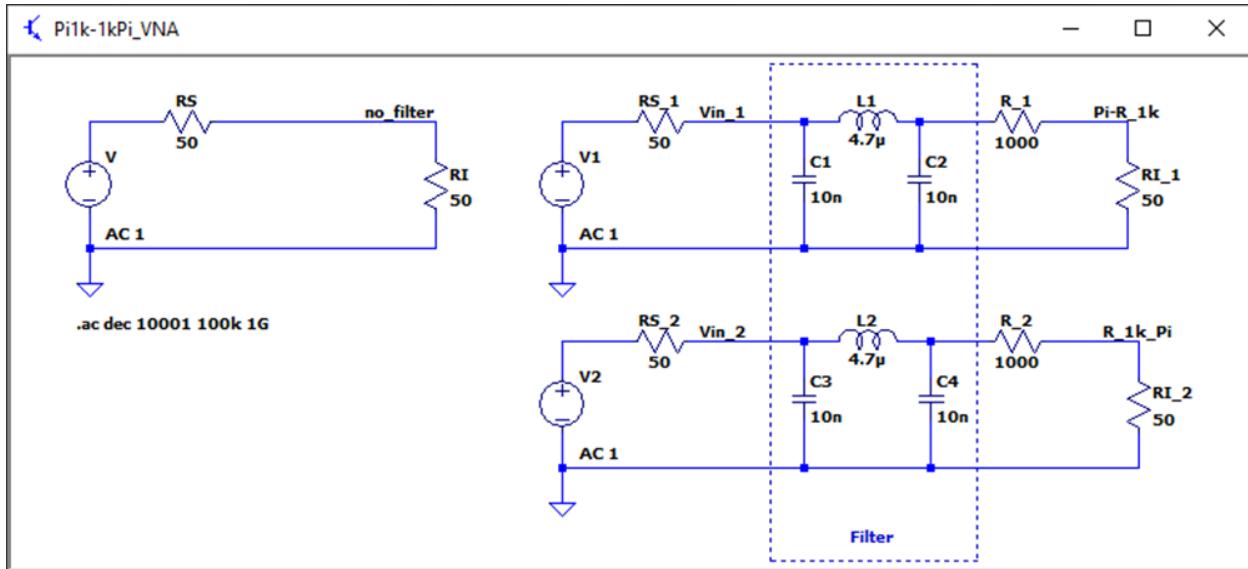
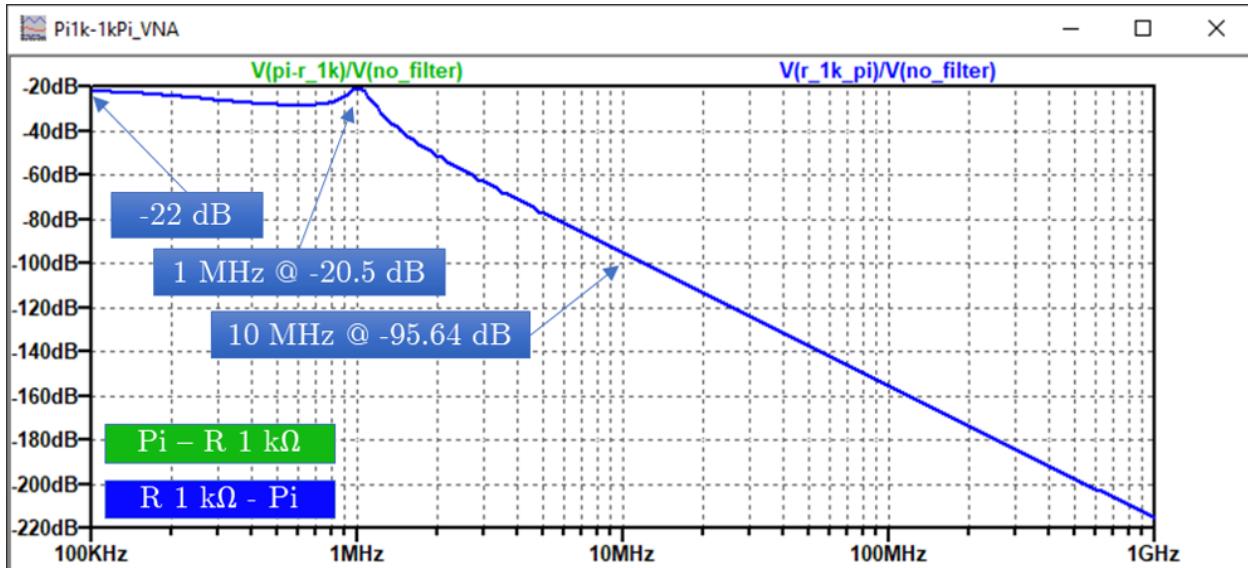


Figure 3.26: EMC filter simulation LC - R 91 k Ω vs. CL - R 91 k Ω , plot.

Simulation π - R 1 k Ω Vs. R 1 k Ω - π Filter Structure

Fig. 3.27 shows three circuits. To the left is the circuit with no filter and no additional load used to normalize the circuit with filter. To the right top is the circuit with filter and load, π - R 1 k Ω . To the right bottom is the circuit with filter and load, R 1 k Ω - π . Fig. 3.28 shows the plotted IL. The compared structures are π - R 1 k Ω (green) versus R 1 k Ω - π (royal blue). Points where the magnitude and frequencies are similar are marked light blue. The curves start at an offset of -22 dB. At 1 MHz both graphs have a magnitude of -20.5 dB. At 10 MHz both graphs have a magnitude of -95.64 dB. The slope per decade in the frequency range of 1 MHz to 10 MHz is -75.14 dB for both graphs. Both graphs show equal behavior.

Figure 3.27: EMC filter simulation π - R 1 k Ω vs. R 1 k Ω - π , schematic.Figure 3.28: EMC filter simulation π - R 1 k Ω vs. R 1 k Ω - π , plot.

Simulation T - R 1 k Ω Vs. R 1 k Ω - T Filter Structure

Fig. 3.27 shows three circuits. To the left is the circuit with no filter and no additional load used to normalize the circuit with filter. To the right top is the circuit with filter and load, T - R 1 k Ω . To the right bottom is the circuit with filter and load, R 1 k Ω - T. Fig. 3.28 shows the plotted IL. The compared structures are T - R 1 k Ω (green) versus R 1 k Ω

- T (royal blue). Points where the magnitude and frequencies are similar are marked light blue. The curves start at an offset of -21 dB. At 1 MHz both graphs have a magnitude of -30.7 dB. At 10 MHz both graphs have a magnitude of -66.2 dB. The slope per decade in the frequency range of 1 MHz to 10 MHz is -35.5 dB for both graphs. Both graphs show equal behavior.

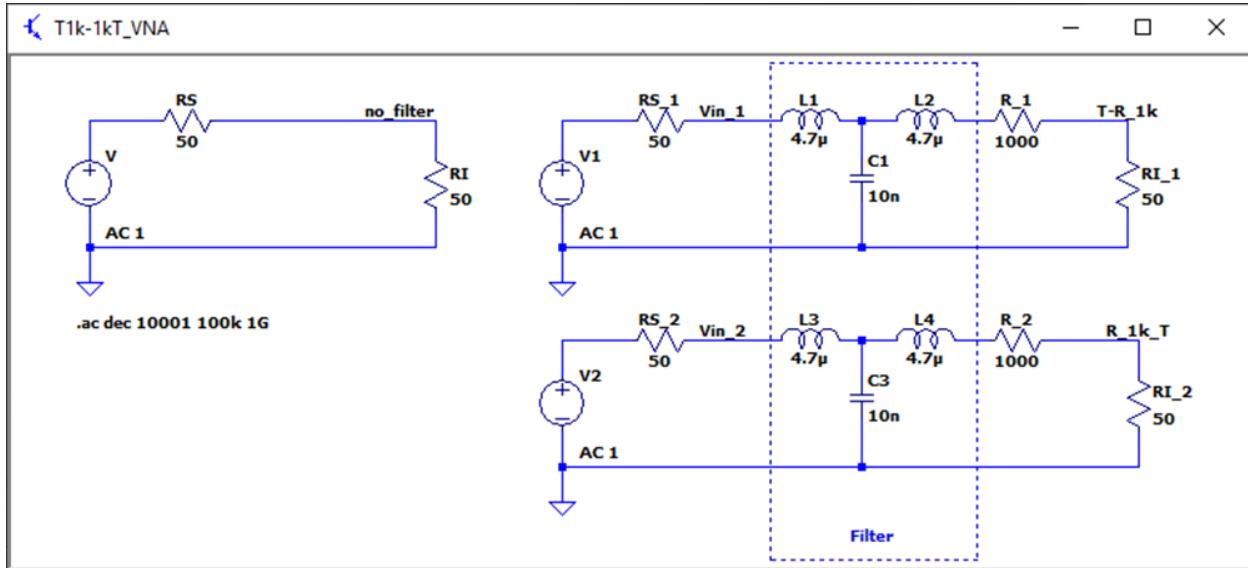


Figure 3.29: EMC filter simulation T - R 1 k Ω vs. R 1 k Ω - T, schematic.

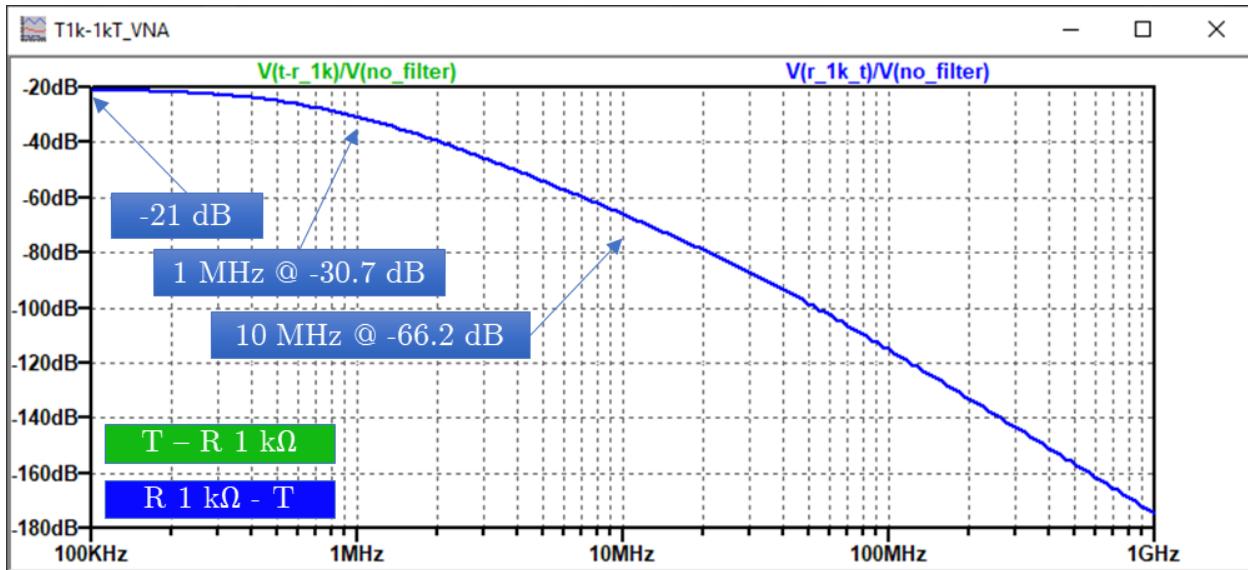


Figure 3.30: EMC filter simulation T - R 1 k Ω vs. R 1 k Ω - T, plot.

Simulation T - R 1 kΩ Vs. CL - R 1 kΩ Filter Structure

Fig. 3.31 shows three circuits. To the left is the circuit with no filter and no additional load used to normalize the circuit with filter. To the right top is the circuit with filter and load, T - R 1 kΩ. To the right bottom is the circuit with filter and load, CL - R 1 kΩ. Fig. 3.32 shows the plotted IL. The compared structures are T - R 1 kΩ (green) versus CL - R 1 kΩ (royal blue). Points where the magnitude and frequencies are similar are marked light blue. The curves start at an offset of -21.2 dB. At 1 MHz both graphs have a magnitude of -30.7 dB. At 10 MHz the T-R structure has a magnitude of -66.2 dB. At 10 MHz the CL-R structure has a magnitude of -50.7 dB. The slope per decade in the frequency range of 1 MHz to 10 MHz is -35.5 dB for the T-R structure, and -20 dB for the CL - R structure. By subtracting slope T-R of slope CL-R, the deviation at 10 MHz is 15.5 dB. Beyond a frequency of 40 MHz, both graphs show similar behavior.

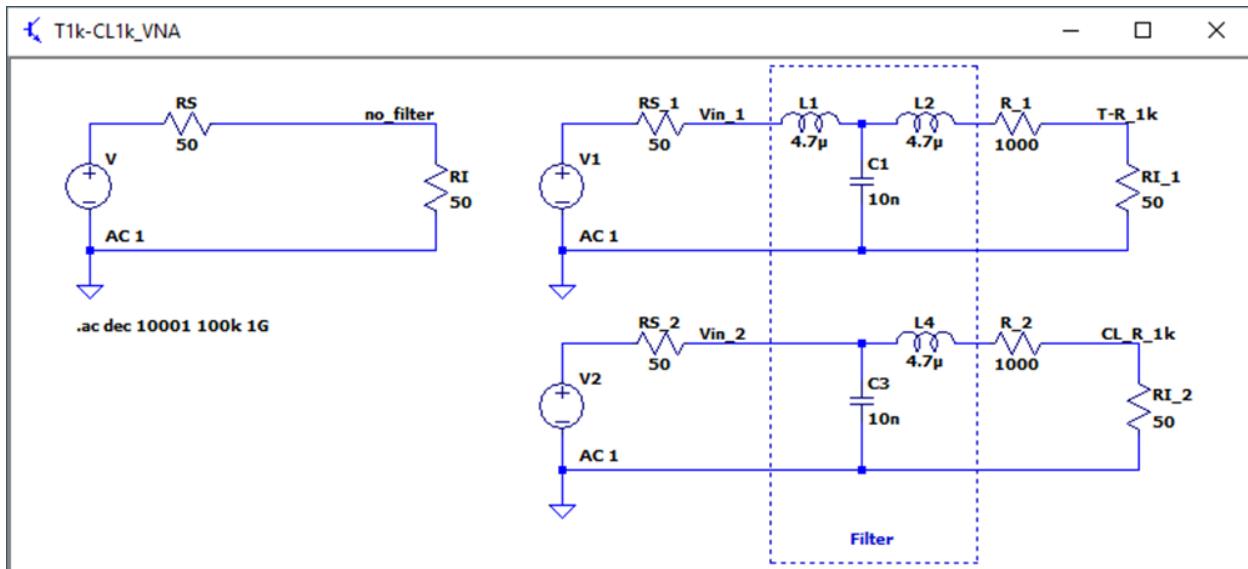


Figure 3.31: EMC filter simulation T - R 1 kΩ vs. CL - R 1 kΩ, schematic.

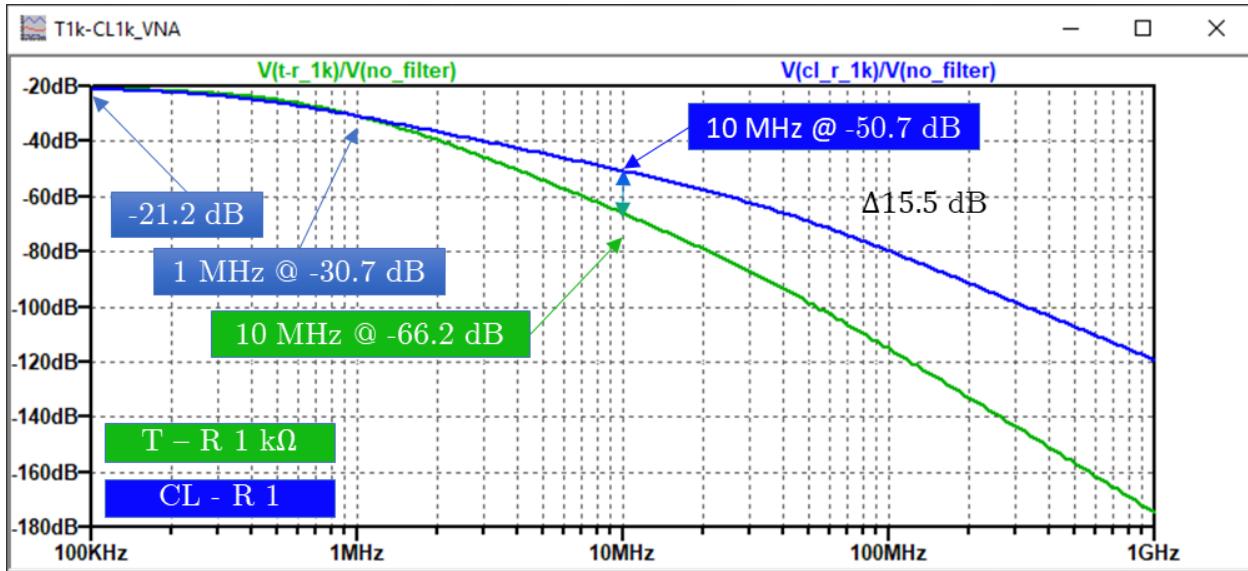


Figure 3.32: EMC filter simulation T - R 1 kΩ vs. CL - R 1 kΩ, plot.

Summary Simulations

Tab. 3.6 presents the summarized key points highlighted in the simulation of various filter structures of the previous sections.

Table 3.6: Summary of simulated results EMC filter.

Filter	100 kHz	1 MHz	10 MHz
LC - R 1 kΩ	-21.2 dB	-30.8 dB	-65.8 dB
CL - R 1 kΩ	-21.2 dB	-30.8 dB	-50.7 dB
LC - R 10 kΩ	-40.5 dB	-50.4 dB	-85.5 dB
CL - R 10 kΩ	-40.5 dB	-50.4 dB	-70 dB
LC - R 91 kΩ	-59.5 dB	-69.6 dB	-104.6 dB
CL - R 91 kΩ	-59.5 dB	-69.6 dB	-89.1 dB
π - R 1 kΩ	-22 dB	-20.5 dB	-95.64 dB
R 1 kΩ - π	-22 dB	-20.5 dB	-95.64 dB
T - R 1 kΩ	-21 dB	-30.7 dB	-66.2 dB
R 1 kΩ - T	-21 dB	-30.7 dB	-66.2 dB

Continuation of Table 3.6			
Filter	100 kHz	1 MHz	10 MHz
T - R 1 kΩ	-21 dB	-30.7 dB	-66.2 dB
CL - R 1 kΩ	-21.2 dB	-30.8 dB	-50.7 dB

3.3 SMPS EMI Suppression Techniques

This section presents the design and test planes for the Switched Mode Power Supply (SMPS) buck converter. To avoid high frequency content during switching multiple precautions can be taken. One way to deal with high frequency ringing caused by fast switching is to slow the rise time of the switch, which can be done with a resistor in series with the gate of a N-MOSFET (for example) which is one of the most effective ways to suppress it or change the frequency range. However, often this can only be done to a certain degree until the actual performance time wise is affected. This is the case with a Switched Mode Power Supply (SMPS) where a large timing mismatch will cause an incorrect output voltage in the best case and in the worst the SMPS would lose functionality completely. Therefore, another strategy is needed to suppress high frequency ringing caused by switching. To evaluate the effect and applied strategies on snubber circuits a SMPS is designed. A step-down DC/DC controller LTC3878 from Analog Device is used. This device has the switching elements external and therefore is suitable to use. To achieve comparable results it is important to define a load. The load is chosen to be 50Ω . The following section presents the design.

3.3.1 SMPS Buck Converter Design with LTC3878

PCB Stack-up

The layer stack of the switched mode power supply is shown in Fig. 3.33. The first design was based on a two layer design without having a single route on the bottom layer. A two

layer design like this would theoretically be sufficient. However, industry does not use a single SMPS, most likely multiple components will be placed on the board which requires additional routes. Therefore, a realistic design is a four layer design with a dedicated GND plane.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.38mil		
4	Dielectric 1	1x 7628 AT05 47% Resin TG130	6.89mil	4.29	
5	GND	Copper	1.38mil		
6	Dielectric 2	6x 7628M 43% Resin TG150	44.49mil	3.96	
7	Signal Layer 1	Copper	1.38mil		
8	Dielectric 3	1x 7628 AT05 47% Resin TG130	6.89mil	4.29	
9	GND Bottom	Copper	1.38mil		
10	Solder Side	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

Figure 3.33: SMPS layer stack 4-layer board.

PCB Features

The PCB features are shown in Fig. 3.34. On the top silk screen the description of the voltage input is printed. Notice, there is no reverse bias protection on the board. Instead, a common-mode choke (L2) is placed at the input. For differential mode suppression a input filtering of a two π structure is placed with bypass capacitors. The input is directed into the high side FET. After the filtering the supply voltage is taken for the dc/dc buck converter IC LTC3878. The expected return current paths are marked on the top overlay to avoid unwanted interruption in the ground plane which might caused increased radiated emissions. R5 and C8 could be used as boot circuit for the high side FET. After the high side FET the low side FET in parallel to high side output and ground is placed. In parallel to the low side FET the snubber circuit is placed that consists out of the following components C11, C12, R13, and R18. The two FETs are followed by a series inductor and output filtering with bypass capacitors. A C1206 capacitor footprint is mounted which shall especially help by ripple suppression of the voltage output. Two different loads can be equipped $50\ \Omega$ with R20 and $100\ \Omega$ with R17. The expected voltage output is marked

on the top overlay with +5 VDC. Banana jack connectors are used to interface the PCB with voltage power supplies or measuring devices for input and output. An opening in the solder mask is provided that allows shielding of the switched mode power supply as needed. Notice, the in and output tracks are covered with solder mask to prevent a short caused by the shielding. Four mounting holes in the form of larger vias which are grounded are placed on the outer edge of the PCB to provide a method of mounting to a case.

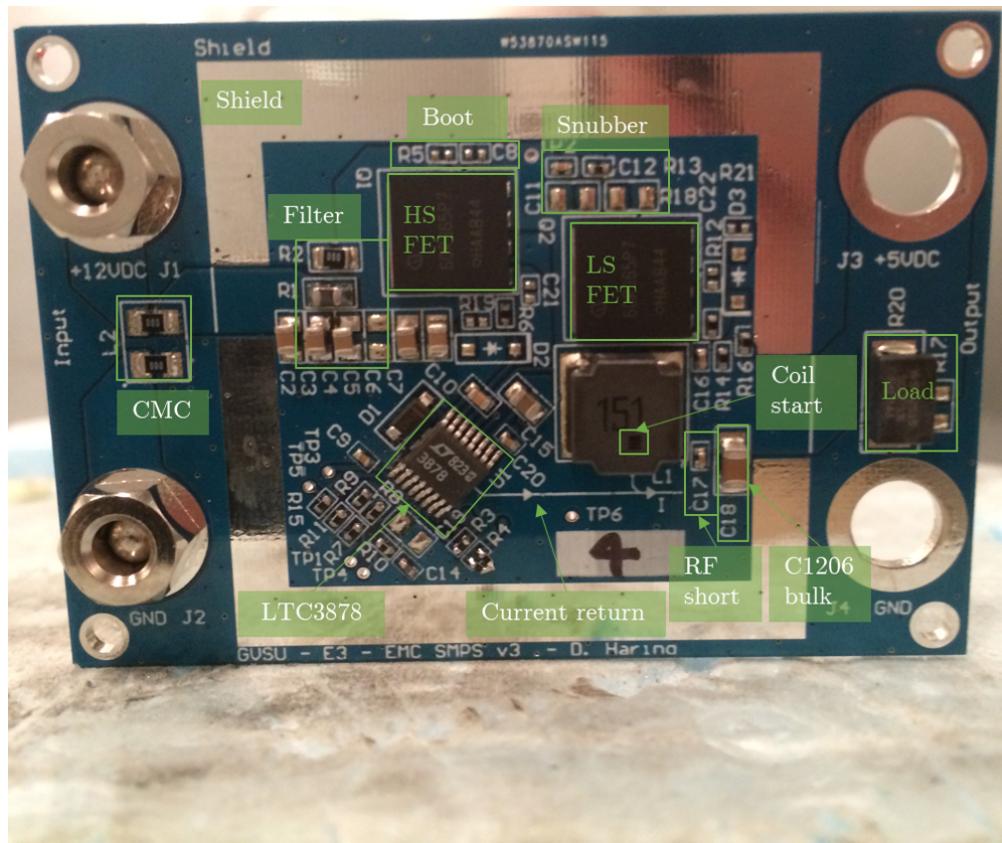


Figure 3.34: SMPS PCB features and top view.

Schematic

Specially highlighted are the snubber test circuit. The test circuit is in parallel to the low side FET, shown in Appendix C.1.1. Two different footprint sizes were chosen to allow a bigger variety of components and values that can be chosen to design the snubber circuit. Furthermore, a resistor in series to the gate of the FET is placed, which allows to

define rise time. A boot circuit is placed in parallel to the high side FET. Most of the schematic is based on the data sheet of the LTC3878] [28].

Snubber

The snubber was designed based on the measurements of the high frequency ringing. According to Adamczyk and Spence the snubber can be designed with a simple procedure presented in his monthly column "EMC Concepts Explained" under the title "RC Snubber Design for SMPS Protection" [19]. The first step is to measure the ringing frequency. Then, place a known capacitor parallel to drain and gate pin of the FET and measure the ringing again. Use Eq. 3.2 to calculate the parasitic capacitance of the FET [20].

$$C_{\sum \text{parasitics}} = \frac{C_{ADD}}{\left(\frac{f_r}{f_r}\right)^2 - 1} \quad (3.2)$$

Then calculate the parasitic inductance with Eq. 3.3.

$$L_{\sum \text{parasitics}} = \frac{1}{(C_{\sum \text{parasitics}})(2\pi f_r)^2} \quad (3.3)$$

Then calculate the minimum snubber capacitor value with Eq. 3.4.

$$C_{\text{snubber minimum}} = \frac{3}{(L_{\sum \text{parasitics}})(2\pi f_r)^2} \quad (3.4)$$

Then calculate the resistor value with Eq. 3.5.

$$R = \sqrt{\frac{L_{\sum \text{parasitics}}}{\left(\frac{C_{\sum \text{parasitics}}}{3}\right)}} \quad (3.5)$$

The procedure will be used in Section 4.4.1.

Filter

The filter design was initially based on a communications filter assuming both sides are $50\ \Omega$ terminated. From there the effect of increasing or decreasing values of capacitance and inductance is tested, this is shown in Fig. 3.35. It can be seen that a large inductance is favorable. In the filter circuit with $22\ \mu H$ capacitor values were chosen which actually can be bought.

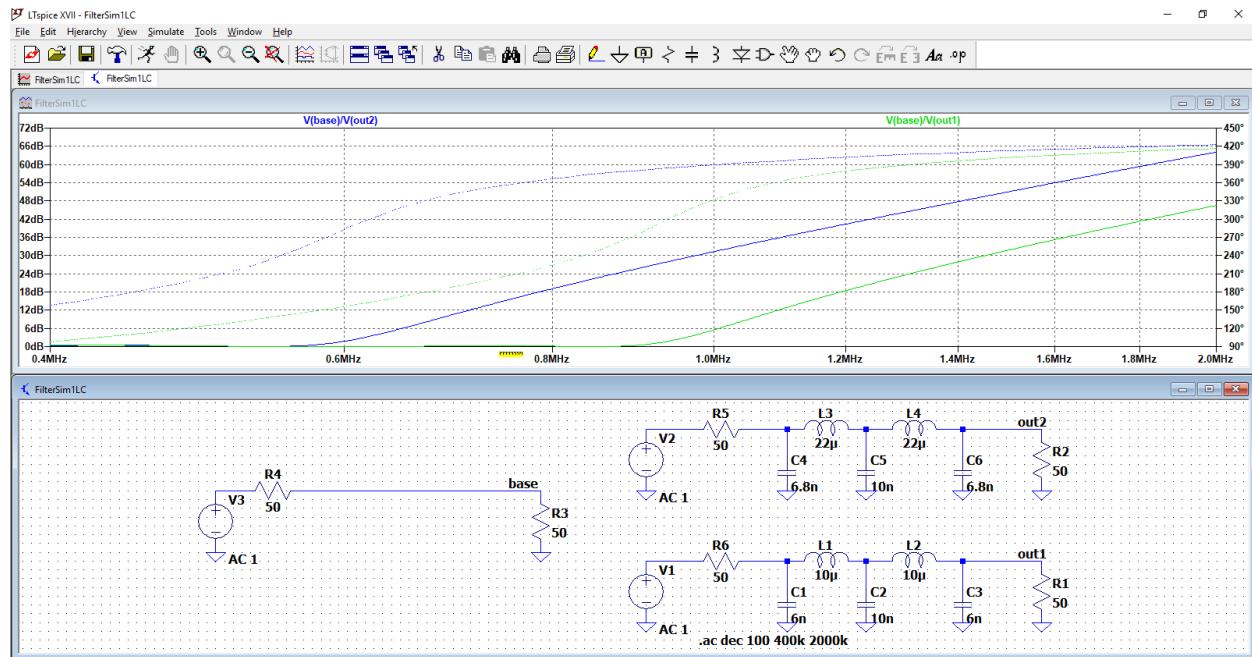


Figure 3.35: SMPS filter LTspice simulation results first approach based on communications filter.

New models were designed based on the investigation performed with the EMC filter and the measurement results gathered with conducted emissions of the SMPS. Fig. 3.36 shows the circuitry for the simulated results presented in Fig. 3.37. The model is still based on the communications filter but it shows the impact of reduction of components. It is desirable to have as few coils as possible for two reasons. One, coils are expensive. Two, usually the coil has to handle high current, which makes it hard to find in a small footprint. To reduce size one coil is favorable.

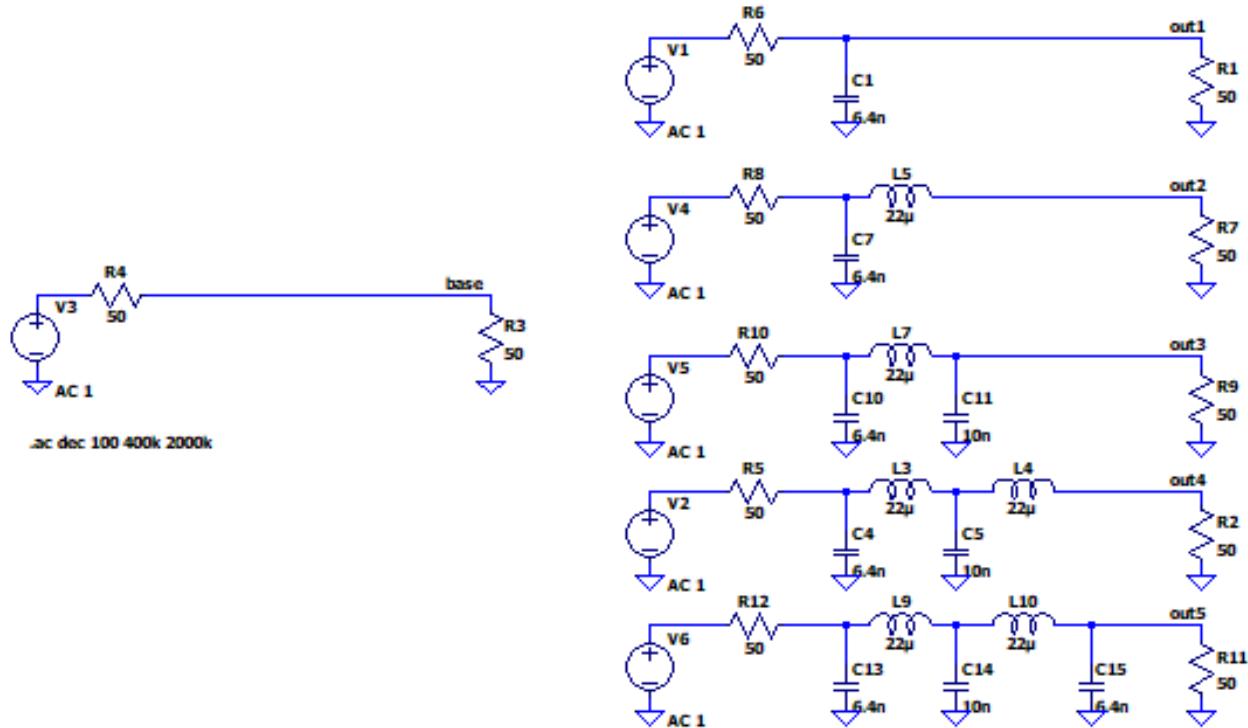


Figure 3.36: SMPS filter LTspice simulation results extended approach based on communications filter, schematic.

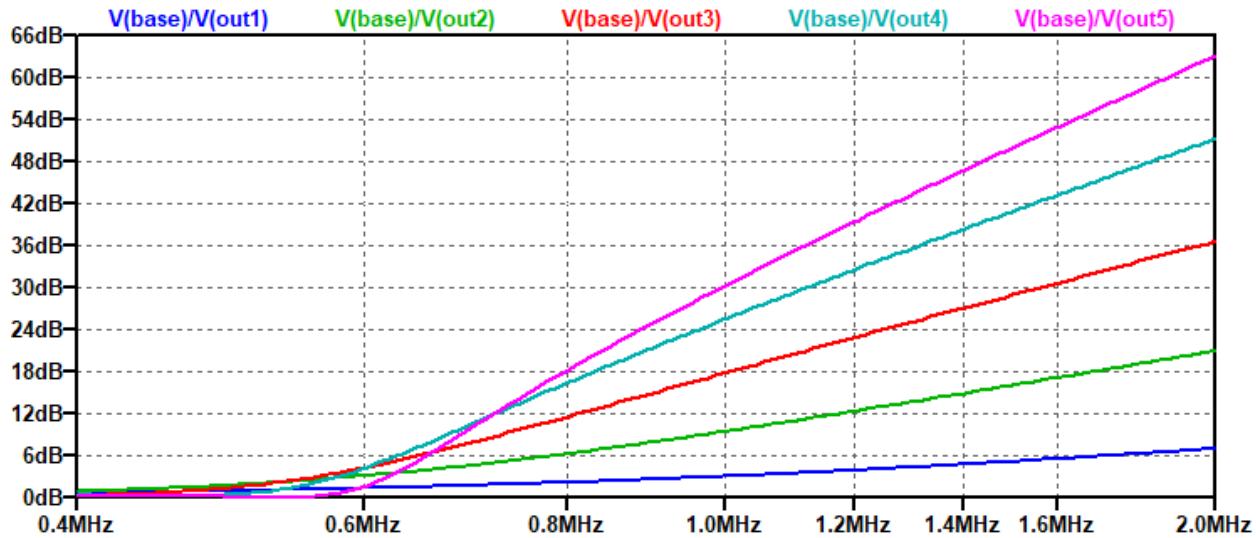


Figure 3.37: SMPS filter LTspice simulation results extended approach based on communications filter, plots.

As shown in plot of Fig. 3.37 the fundamental frequency of around 400 kHz cannot really be damped. The next approach used higher capacitor values in a magnitude of 10x

higher. The schematic is shown in Fig. 3.38. The resulting plots are shown in Fig. 3.39 where clearly can be seen that the previous cut off frequency of 0.6 MHz is shifted down to about 0.2 MHz. This shows the filter design is on the right track but there is still a low attenuation for a 3rd order filter at 400 kHz. Keep in mind this simulation is under ideal conditions no Equivalent Series Inductance (ESL) accounted for and symmetric load.

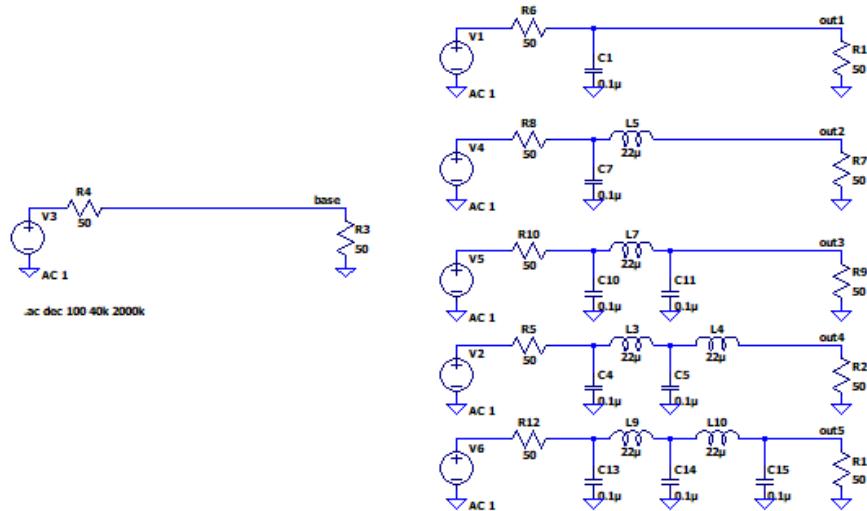


Figure 3.38: SMPS EMI filter LTspice simulation results second approach with 10 times higher capacitors.

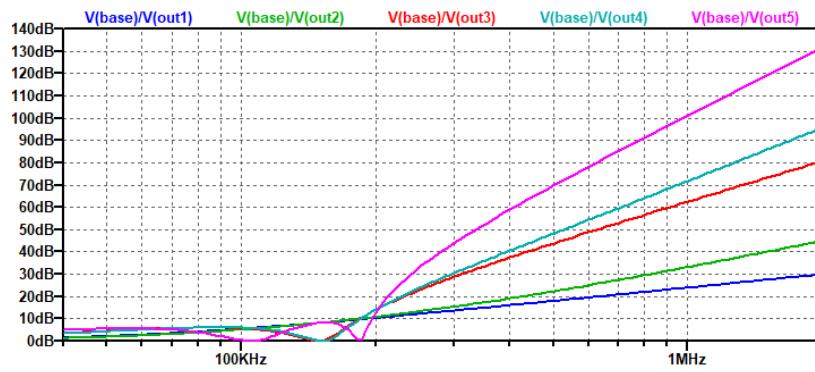


Figure 3.39: SMPS EMI filter LTspice simulation results second approach with 10 times higher capacitors.

3.3.2 Hardware Test Plan

A hardware test plan is usually made during the design of the hardware where test points and measurements made with it are defined in. This is very important for troubleshooting and later design optimization of a product. The test plan for the first PCB prototype is shown in Tab. 3.7.

Table 3.7: Snubber circuitry test plan PCB.

No.	Test	Task	Result
1	Short	Before applying voltage measure the resistance between GND and PWR 12VDC.	
	Fault	Find short and open it, use Digital Multimeter (DMM)	
2	Voltage	Apply 12 VDC and measure the voltage with a oscilloscope and DMM.	
	Fault	No voltage, check if power supply output is on.	
	Fault	No voltage, check if all connectors are connected with correct polarity.	
3	Voltage	Measure the voltage with a oscilloscope and DMM after common mode choke L2.	
	Fault	No voltage, check data sheet and design if the part is correct mounted.	
4	Voltage	Measure SMPS Vout check if +5V and voltage ripple at P2	
	Fault	No voltage, check if voltage at C20 or R5 is 12DC.	
	Fault	No voltage, check INTVCC.	
	Fault	No voltage, check voltage on TP2?	
	Fault	No voltage, check SMPS RUN/SS on TP3.	
	Fault	No voltage, check SMPS voltage at TP4.	
	Fault	STILL No voltage, might be damaged IC? Try a second one	
	Fault	STILL No voltage, read FET data sheet because it was switched.	
	Fault	STILL No voltage, start praying and continue search!	

Continuation of Table 3.7			
No.	Test	Task	Result
	Fault	STILL No voltage, I believe in you! You can do it!	
	Fault	De-solder and change components one by one until faulty one is found.	
5	Current	Check current supplied by the power supply	
	Fault	More then 100 mA going, mhhh.	
	Fault	Is the correct load resistor mounted?.	
6	Voltage	Measure voltage output of J3 and J4 should be 5V out.	
	Fault	Wrong voltage, check voltage divider	
	Fault	Voltage ripples, check bypass capacitors on size and value.	
	Fault	Still not working, read the data sheet.	
	Fault	Change snubber circuit.	

3.3.3 EMC Test

The testing of conducted emissions is performed according to "CISPR 25:2016 Vehicles, boats and internal combustion engines - Radio disturbance characteristics - Limits and methods of measurement for the protection of on-board receivers" [29]. Two different methods to measure conducted emissions are stated, which are voltage method and current method. For current method the setup can be built to measure Differential Mode (DM) and Common Mode (CM) current. To measure the relative impact of component changes the Resolution Bandwidth (RBW) will be adjusted to increase performance. This setting should not be used to perform CISPER 25 conformance measurements.

3.3.4 EMC Test Plan

First, the measurement setup for CE voltage method is presented. Two boards, board three (B3) and board (B4) are tested. Board three is equipped with a Common Mode Choke (CMC). Board 4 no EMI suppression is applied. The reason to do so is to gather

more information in a single test run.

Measurement setup Conducted Emissions Voltage Method

Fig. 3.40 shows the set up used for battery line measured conducted emissions voltage method. The battery is supported by a DC power supply with low noise and minimal harmonics. For performing the ambient measurements, it is important to either have the battery supplied by the DC supply or to disconnect and shorten the cables on the battery lead. If the cables are attached to the supply, but the supply is turned off, it will cause interference because the battery will supply the DC supply. The setup is sensitive to changes. Therefore, it is important to have the right height and distances as defined in the specifications. The wire harness length in the shown figure is an estimate, not the actual standard length. In most standards, it will be a minimum of 20 cm with +/- 20 cm. The setup has to build upon a grounded metal plate which is connected to the wall of the chamber. The LISN and battery have to be grounded to the metal sheet. The battery minus pole is connected, therefore, to the chamber ground. The RF cable should not be routed close by to the device under test (DUT) because it is possible that fields can couple into the outer shielding and lead to an undesired current flow in the RF cable. The bench itself should be build up out of non-conductive material. To measure the DM and CM voltages at the same time a discriminator could be placed in between LISN and EMI receiver. Outside the chamber, the EMI receiver is connected to a computer which runs software to perform the test and manage and store the test results.

Fig. 3.41 shows the set up used for ground line measured conducted emissions voltage method. The setup is the same as discussed for the battery line with the exception that the RF cable is connected to the ground line LISN and the 50Ω port of the battery line LISN is terminated with a 50Ω impedance.

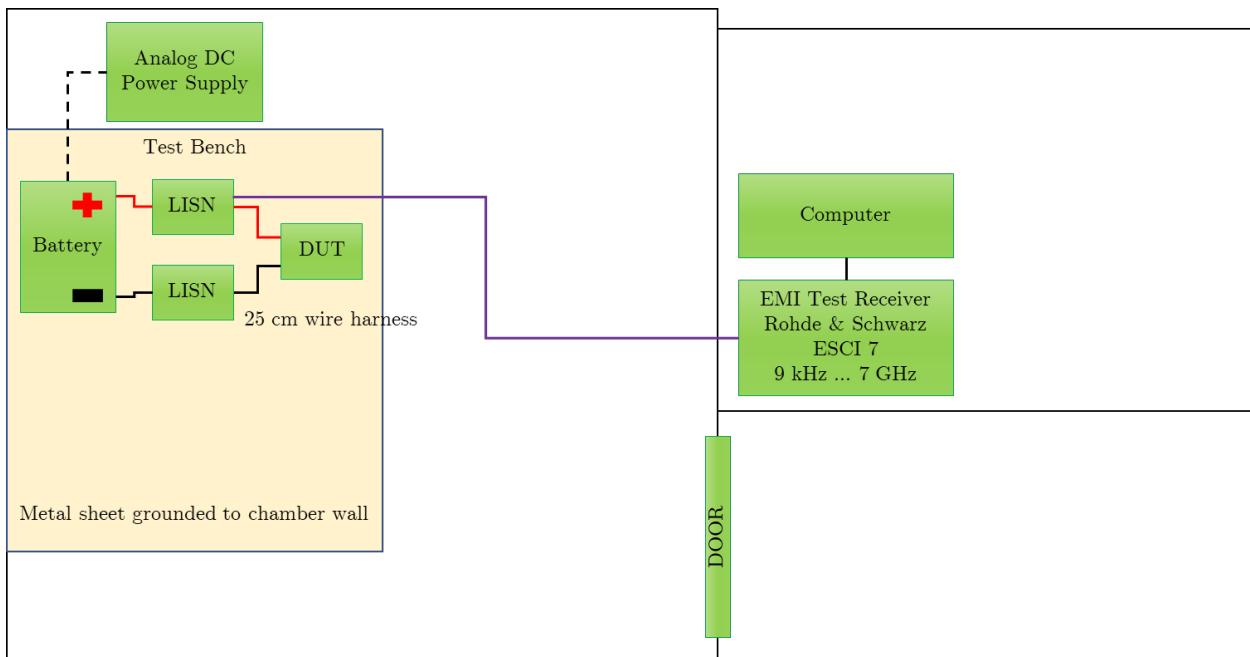


Figure 3.40: SMPSv3 CE test (V) battery line measurement setup.

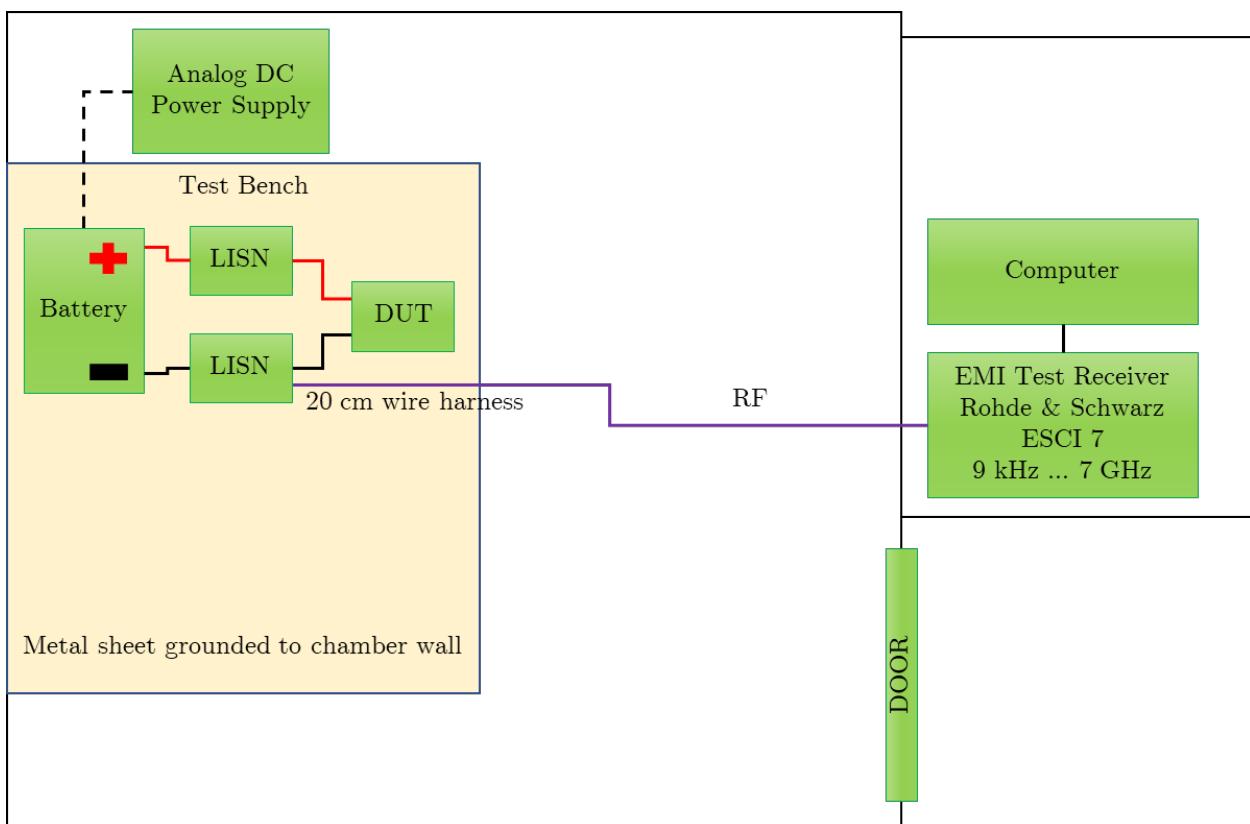


Figure 3.41: SMPSv3 CE test (V) ground line method measurement setup.

Tests Conducted Emissions Voltage Method

Tab. 3.8 shows an example of the tests organized in detail. The reason to make a test plan is it helps to counter issues upfront and not on the date of testing. It helps to prepare before testing by ordering components in case the original chosen ones do not perform as expected or if there is a better solution for the component set. Performance testing can also be done in a pre-compliance laboratory. In column result either pass or fail can be noted. The full featured test plan is presented in Appendix C.5.

Table 3.8: SMPS EMC test plan, CE (V).

No.	Test	Board	Result
1	Conducted Emissions Test voltage method		
1.1	Measure empty chamber to establish base line, Ambient		check
1.2	Measure baseline CE (V) Battery with CMC	Board 3	pass
1.3	Measure baseline CE (V) Battery	Board 4	fail

Components Used for Testing

Tab. 3.9 presents the components which were used for testing of the SMPS.

Table 3.9: Components list used for SMPS CE (V) testing.

Part	Value	Manufacturer	Part Number
Resistor	1 Ω	Yageo	RC0402FR-071RL
Capacitor	2200 pF +/- 10%	Wurth Electronics	885012205063
Capacitor	6.8 nF +/- 10%	Wurth Electronics	885012207121
Capacitor	0.01 μF	Wurth Electronics	885012207092
Inductor	22 μH	TDK	MLZ2012N220LTD25
CMC	45 Ohms @ 100 MHz 4.0 A	Murata Electronics	DLW5ATZ450TQ2L

Continuation of Table 3.9			
Part	Value	Manufacturer	Part Number
Shielding Board Level Shield	Mounting Clip	LeaderTech	TC-01
Shielding 1.326X1.45X0.2 IN 1PC NON- VENTED	Shield	LeaderTech	SMS-306
Shielding Surface Mnt Shields 1 Pc 1.326" x 1.450" VENTED	Shield	LeaderTech	SMS-106

Chapter - 4 Results

The measurement and test setups are provided for each measurement or test. The results are presented in the figures. The detailed numerical results are shown in several tables in Chapter 6.

4.1 Embedded capacitance of a PCB

In this section first the measurement setup is presented followed by the measurement results. The behavior in frequency domain of the embedded capacitance of the designed test boards was measured. The behavior of the time domain was measured.

4.1.1 Measurement Setup for Input Impedance and Insertion Loss

To measure the embedded impedance of the different board configurations a VNA is used to perform an s_{11} , s_{22} , and s_{33} measurement at the port of interest which is towards the μ C with the designator J1. The measurement setup is shown in Fig. 4.1. The measurement was performed with a frequency range of 100 kHz to 2 GHz, a power output of +10 dBm, at a number of 10001 points, and an IF frequency at 10 kHz. A calibration with OSL is performed for s_{11} , s_{22} , and s_{33} measurements. For s_{21} , s_{43} measurements a OSLT calibration was performed with the same setup used for s_{11} . To measure three boards for insertion loss with the VNA, first, two boards were measured, and one trace stored in memory. Then the third board was measured with s_{43} . To tighten the connectors and cable connections a PE Pasternack Fixed Click Type Torque Wrench With 5/16 Bit For SMA, 2.92mm, 3.5mm Connectors Pre-set to 8 in-lbs was used. The SMA cable has a length of 60 cm. Due to the top solder of the through-hole SMA connectors, shorted and open through-hole SMA connectors were used to calibrate the phase delay out added due to the standoff. Fig. 4.2 shows the measurement setup for s_{21} , s_{43} memory trace (dark blue), and s_{43} .

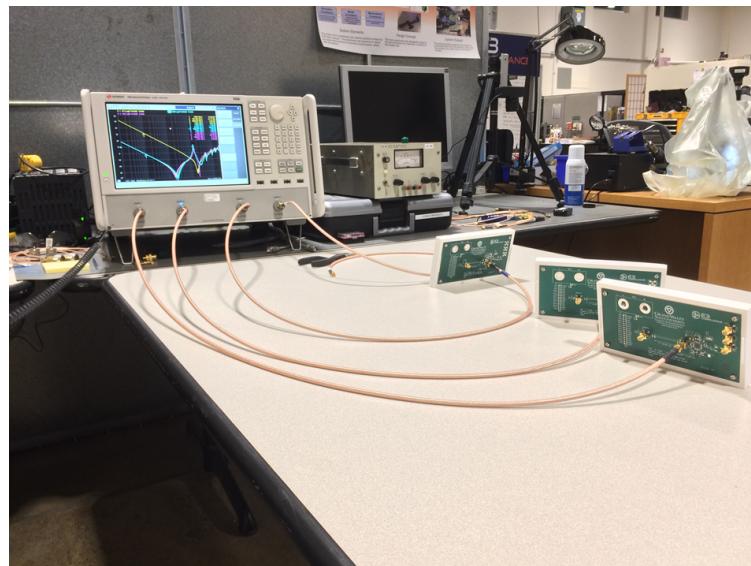


Figure 4.1: Measurement setup comparison three boards input impedance.

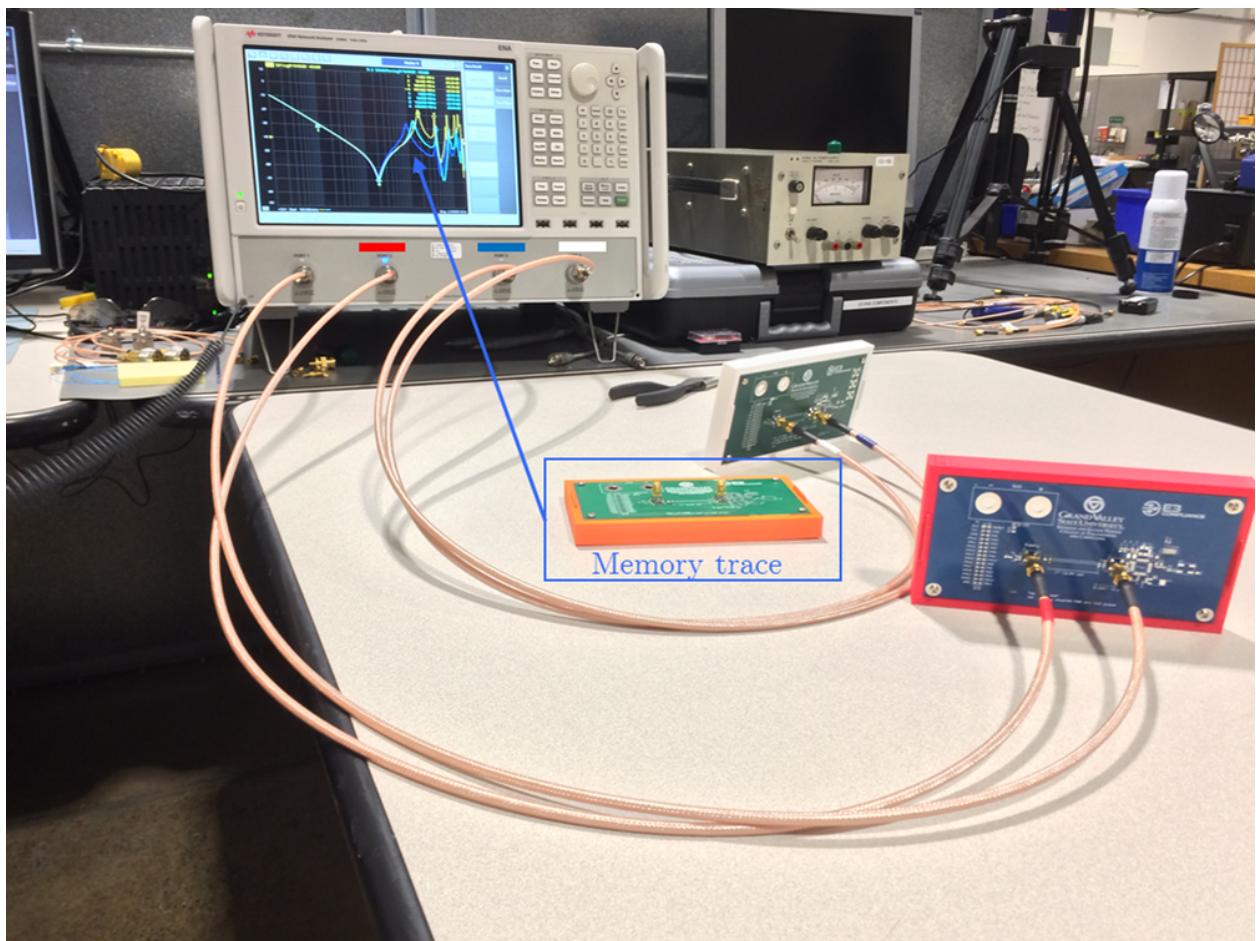


Figure 4.2: Measurement setup comparison three boards insertion loss.

4.1.2 Input Impedance Measurements

The input impedance measures the impedance between ground and power net. The impedance is measured on connector J1 next to the μ C supply pin. The μ C supply pin is the point of interest. Tab. A.1 shows the conversion from dB to Ohm.

4-Layer vs. 6-Layer vs. 6-Layer version 3 for No Capacitors

Fig. 4.3 shows the measurement of the input impedance for 4-layer (L4), 6-layer (L6), and 6-layer version 3 (v3) board for no capacitors populated. Three boards were measured, S_{11} (brown) shows the impedance of the board with 4-Layer stack-up. S_{22} (cyan) shows the impedance of the board with 6-Layer stack-up. S_{33} (magenta) shows the impedance of the board with 6-Layer v3 stack-up. The stack-ups are shown on the right side.

Up to the resonant frequency of the boards, based on the 4-layer input impedance, the 6-layer board outperforms the four layer board by 13.29 dB. The 6-layer board version 3 outperforms the four layer board by 8.59 dB. The 6-layer board outperforms the 6-layer version 3 by 4.64 dB. The 6-layer board sees the first resonant frequency at 142 MHz. The 6-layer version 3 boards resonant frequency is at 154 MHz. The 4-layer board's resonant frequency is at 230 MHz. At 434 MHz the 4-layer boards anti-resonance is at 6.6 dB, the 6-layer version 3 is at 1.22 dB, and the 6-layer is at -3.27 dB. The difference in magnitude between 4-layer and 6-layer board at 434 MHz is 9.87 dB. The difference in magnitude between 4-layer and 6-layer version 3 board at 434 MHz is 5.38 dB. The difference in magnitude between 6-layer and 6-layer version 3 board at 434 MHz is 4.49 dB. Beyond a frequency of 434 MHz, all three boards show the same trend — the boards with 6-layer stack-up show lower divergences than the 4-layer board.

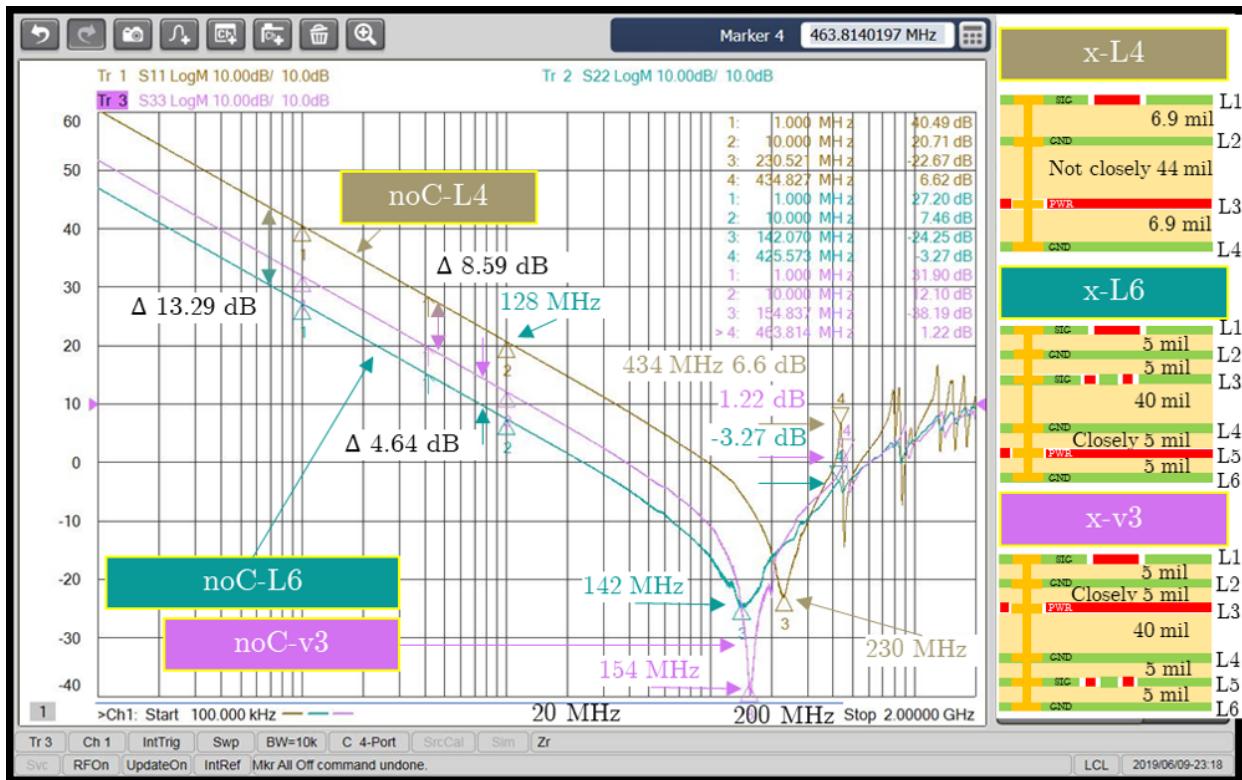


Figure 4.3: 4-layer vs. 6-layer vs. 6-layer v3 no capacitors input impedance measured on connector J1 with VNA.

6-Layer version 3 for No, Not Grouped, and Grouped Capacitors

Fig. 4.4 shows the measurement of the input impedance of board series six layer version 3 with closely coupled power and ground planes on layer two and layer three. Three boards were measured, S_{11} (brown) shows the impedance of the board with no capacitors placed. S_{22} (cyan) shows the impedance of the board with not grouped capacitors. S_{33} (magenta) shows the impedance of the board with grouped capacitors. The stack-up is shown on the right side.

The two populated boards outperform the not populated board by 33.29 dB for the lower frequency range up to the first resonant frequency of the populated boards, which is at 15 MHz. In a frequency range of 15 MHz to 128 MHz, the impedance of the populated board increases upon the anti-resonance. No marginal differences between the not grouped and grouped boards can be distinguished. Beyond 463 MHz no remarkable differences in

impedance can be seen through all three boards. The non-populated board's resonant frequency is at 168 MHz.

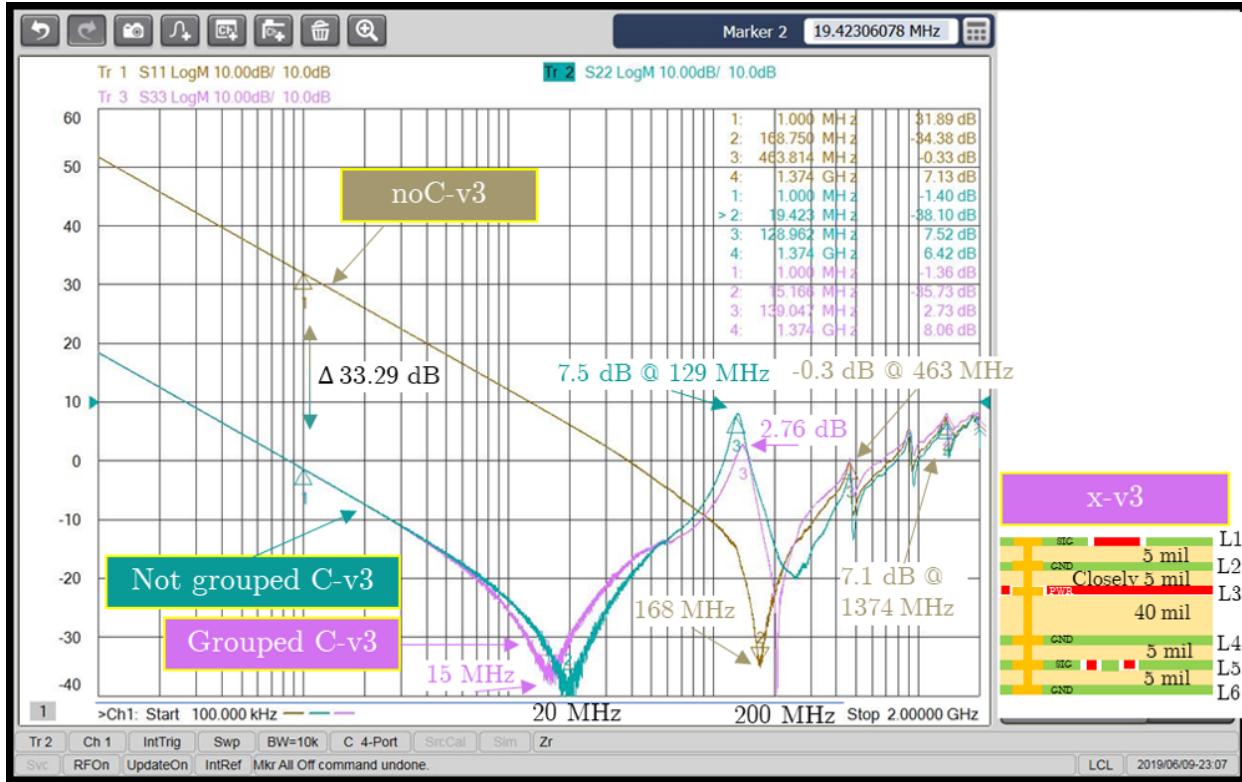


Figure 4.4: 6-layer v3 for no, not grouped, and grouped capacitors input impedance.

6-Layer for No, Not Grouped, and Grouped Capacitors

Fig. 4.5 shows the measured input impedance of board series six layer with closely coupled power and ground planes on layer four and layer five. Three boards were measured, S_{11} (brown) shows the impedance of the board with no capacitors placed. S_{22} (cyan) shows the impedance of the board with not grouped capacitors. S_{33} (magenta) shows the impedance of the board with grouped capacitors. The stack-up is shown on the right side. The two populated boards outperform the not populated board by 33.29 dB for the lower frequency range up to the first resonant frequency of the populated boards, which is at 15 MHz. In a frequency range of 15 MHz to 128 MHz, the impedance of the populated board increases upon the anti-resonance. No marginal differences between the not grouped

and group boards can be distinguished. Beyond 463 MHz no remarkable differences in impedance can be seen through all three boards. The non-populated board's resonant frequency is at 168 MHz.

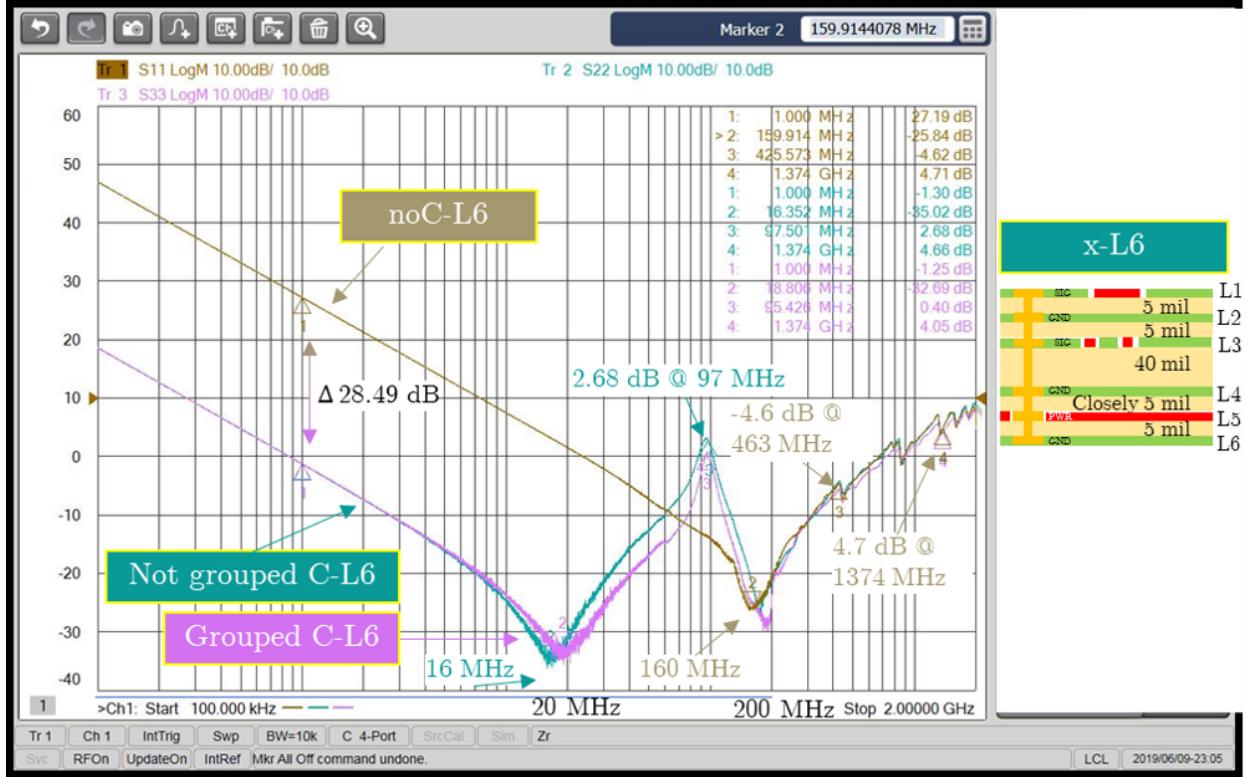


Figure 4.5: Measured data 6-layer with power and ground plane far from top layer for no, not grouped, and grouped capacitors input impedance.

4-Layer for No, Not Grouped, and Grouped Capacitors

Fig. 4.6 shows the measured input impedance for a 4-layer board with not closely coupled power and ground planes on layer two and layer three. Three boards were measured, S_{11} (brown) shows the impedance of the board with no capacitors placed. S_{22} (cyan) shows the impedance of the board with not grouped capacitors. S_{33} (magenta) shows the impedance of the board with grouped capacitors. The stack-up is shown on the right side. The two populated boards outperform the not populated board by 41.54 dB for the lower frequency range up to the first intercept point of populated and non-populated boards, which is at 120 MHz. In a frequency range of 15 MHz to 180 MHz, the impedance of the

populated board increases upon the anti-resonance. The populated impedance starts to deviate of each other at a frequency of 40 MHz. The impedance of the grouped capacitors outperforms the impedance of the not-grouped capacitors over a frequency range starting at 40 MHz and 284 MHz. The grouped capacitance converges with the no capacitor impedance from a frequency range of around 230 MHz. For a higher frequency range of 284 MHz to 434 MHz, the impedance of the not grouped capacitor outperforms the grouped capacitors impedance. Beyond the second anti-resonance, the discussion which is the best is highly depending on the frequency, and the frequency is on resonance or anti-resonance. However, it can be reasonably said that the performance of each board beyond 434 MHz is unstable with regards to impedance.

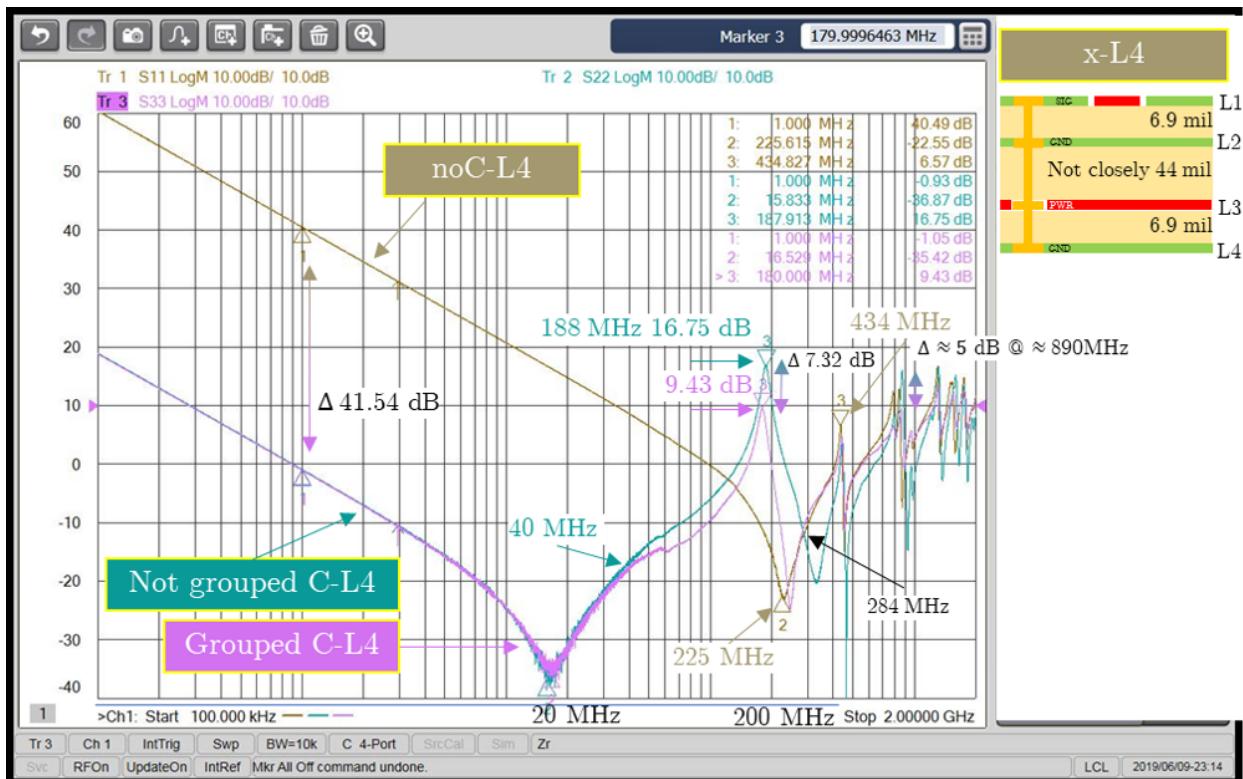


Figure 4.6: 4-layer with power and ground plane not closely spaced for no, not grouped, and grouped capacitors input impedance.

4-Layer, 6-Layer, and 6-Layer Version 3 for Not Grouped Capacitors

Fig. 4.7 shows the measured input impedance for not grouped capacitors. Three boards were measured, s_{11} (brown) shows the impedance of the board with 4-layer stack-up. S_{22} (cyan) shows the impedance of the board with 6-layer stack-up. S_{33} (magenta) shows the impedance of the board with 6-layer version 3 stack-up. The stack-up is shown on the right side.

Up to the frequency of 55 MHz, the impedance of all three stack-ups are similar and deviate only marginal in frequency on their self-resonant frequency from 15 MHz to 18 MHz. The next anti-resonance occurs for 6-layer stack-up at a frequency of 95 MHz at a magnitude of 3.1 dB. The 6-layer version 3 stack-up has an anti-resonance at a frequency of 132 MHz with a magnitude of 8.2 dB. The 4-layer stack-up has an anti-resonance at a frequency of 186 MHz with a magnitude of 16.8 dB. Hence, the following resonance peaks are shifted as well in frequency in a similar order as the anti-resonance. At a frequency range of 425 MHz to 463 MHz, the anti-resonance of each stack-up is synchronized in frequency and stays synchronized beyond this point. The magnitude around this synchronized frequency range are similar distributed as the previous anti-resonance with 23.76 dB for the 4-layer stack-up, -0.85 dB for the 6-layer stack-up version 3, and -5.9 dB for the 6-layer stack-up. Beyond 463 MHz, the pattern repeats with different frequencies and magnitudes. However, it can be stated that the 6-layer stack-ups are in terms of impedance stabler compared to the 4-layer stack-up.

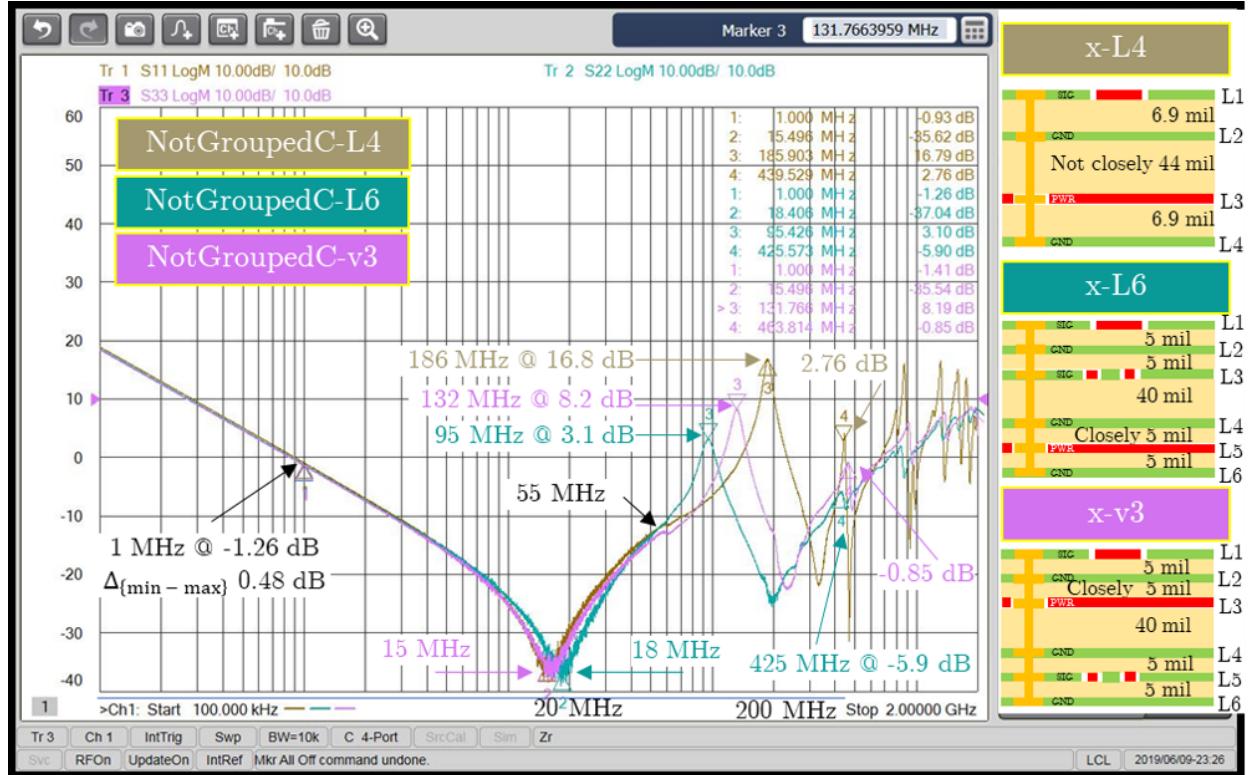


Figure 4.7: Input impedance 4-layer, 6-layer, and 6-layer Version 3 for Not Grouped Capacitors.

4-Layer, 6-Layer, and 6-Layer Version 3 for Grouped Capacitors

Fig. 4.8 shows the measured input impedance for grouped capacitors. Three boards were measured, S_{11} (brown) shows the impedance of the board with 4-layer stack-up. S_{22} (cyan) shows the impedance of the board with 6-layer stack-up. S_{33} (magenta) shows the impedance of the board with 6-layer version 3 stack-up. The stack-up is shown on the right side. Up to the frequency of 65 MHz, the impedance of all three stack-ups are similar and deviate only marginal in frequency on their self-resonant frequency from 15 MHz to 25 MHz. The next anti-resonance occurs for 6-layer stack-up at a frequency of 96 MHz at a magnitude of 0.45 dB. The 6-layer version 3 stack-up has an anti-resonance at a frequency of 142 MHz with a magnitude of 2.74 dB. The 4-layer stack-up has an anti-resonance at a frequency of 180 MHz with a magnitude of 9.42 dB. Hence, the following resonance peaks are shifted as well in frequency in a similar order as the anti-resonance. At a frequency range

of 425 MHz to 463 MHz, the anti-resonance of each stack-up is synchronized in frequency and stays synchronized beyond this point. The magnitude around this synchronized frequency range are similar distributed as the previous anti-resonance with 3.63 dB for the 4-layer stack-up, 0.77 dB for the 6-layer stack-up version 3, and -6.6 dB for the 6-layer stack-up. Beyond 463 MHz, the pattern repeats with different frequencies and magnitudes. However, it can be stated that the 6-layer stack-ups are in terms of impedance more stable compared to the 4-layer stack-up.

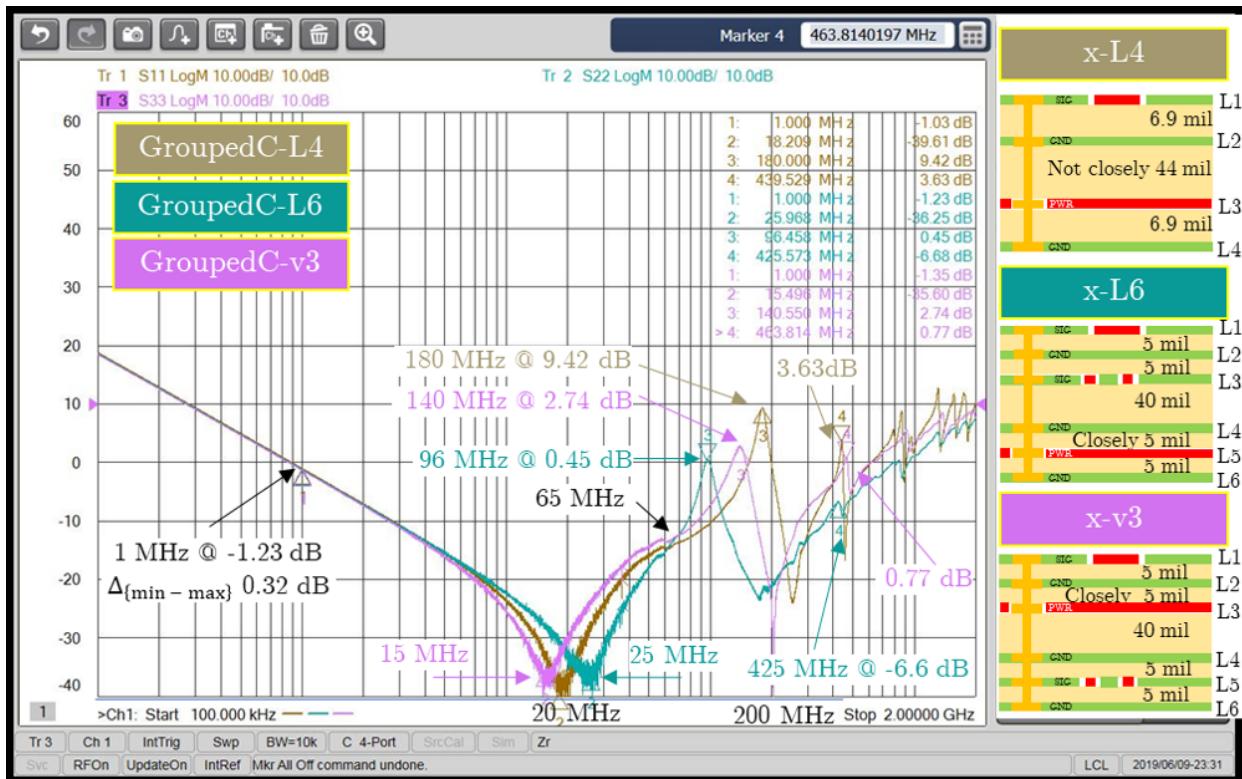


Figure 4.8: Input impedance 4-layer, 6-layer, and 6-layer Version 3 for Grouped Capacitors.

4.1.3 Insertion Loss Measurements

The following sub-sections present the insertion loss measured for each case. The insertion loss is the normalized measurement with both ports terminated to 50Ω impedance.

4-Layer, 6-Layer, and 6-Layer Version 3 for No Capacitors

Fig. 4.9 shows the measured insertion loss for no capacitors mounted. Three boards were measured, s_{21} (brown) shows the insertion loss of the board with 4-layer stack-up. S_{43} memory trace (aquamarine) shows the insertion loss of the board with 6-layer stack-up. S_{43} (cyan) shows the impedance of the board with 6-layer version 3 stack-up. The stack-up is shown on the right side.

Up to the frequency of 200 kHz, the insertion loss of all three stack-ups is similar. At a frequency of 10 MHz, the 4-layer stack-ups impedance is -8.07 dB. The 6-layer stack-up version three impedance is -15.89 dB. The impedance of the 6-layer stack-up is -20.54 dB. A resonant frequency can be seen at 339 MHz up to 347 MHz. The first anti-resonance occurs at a frequency of 433 MHz for 6-layer stack-up with a magnitude of -40.06 dB. The 6-layer version 3 has an anti-resonant frequency at 468 MHz at -31.29 dB. The 4-layer stack-up has an anti-resonant frequency at 439 MHz with magnitude -21.37 dB. The 6-layer stack-ups outperforms mainly the 4-layer stack-up. The 4-layer stack-up has a resonant frequency at 1873 MHz with a magnitude of -55 dB.

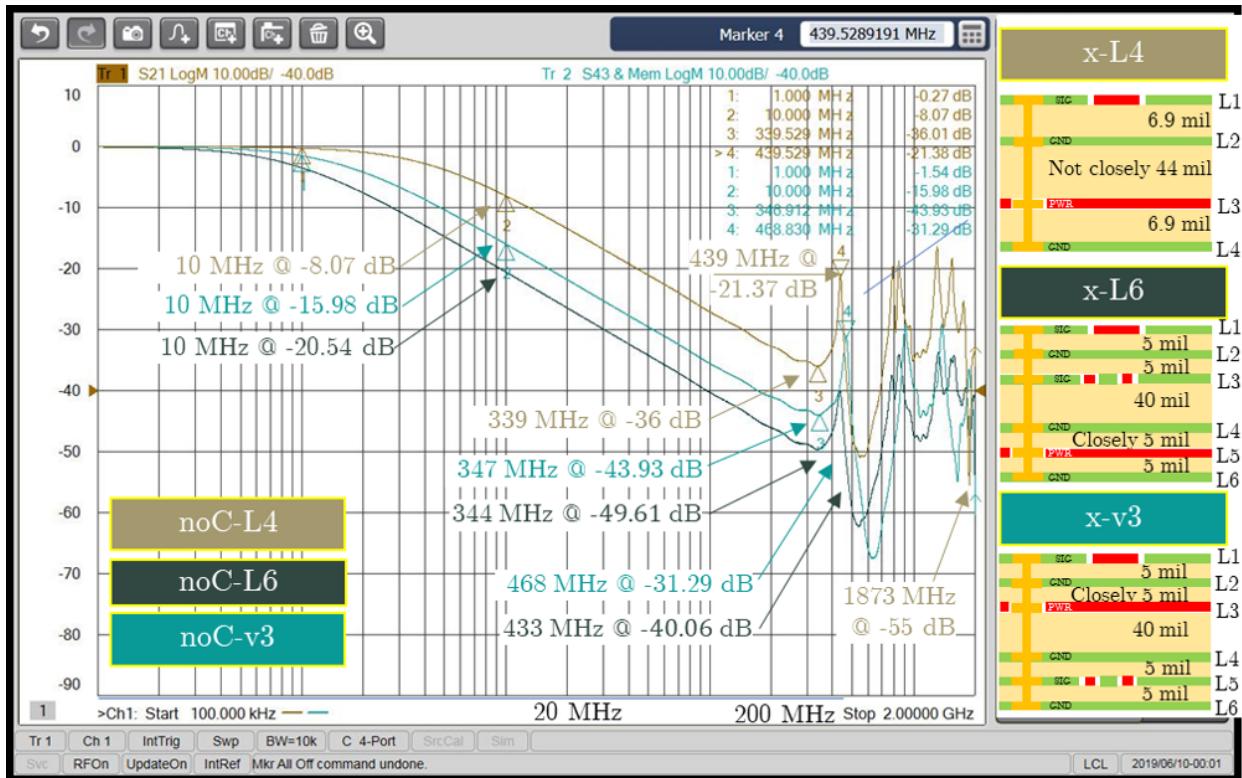


Figure 4.9: Insertion loss 4-layer, 6-layer, and 6-layer Version 3 for No Capacitors.

4-Layer, 6-Layer, and 6-Layer Version 3 for Not Grouped Capacitors

Fig. 4.10 shows the measured insertion loss for not grouped capacitors mounted. Three boards were measured, S_{21} (brown) shows the insertion loss of the board with 4-layer stack-up. S_{43} memory trace (aquamarine) shows the insertion loss of the board with 6-layer stack-up. S_{43} (cyan) shows the impedance of the board with 6-layer version 3 stack-up. The stack-up is shown on the right side.

At a frequency of 1 MHz, the insertion loss of all three stack-ups is similar at -29.22 dB. The slope is -20 dB. The first resonant frequency occurs at 18 MHz. The first anti-resonance occurs at a frequency of 96 MHz for 6-layer stack-up with a magnitude of -26.71 dB. The 6-layer version 3 has an anti-resonant frequency at 142 MHz at -24.18 dB. The 4-layer stack-up has at a frequency of 189 MHz with magnitude -16.30 dB. The second anti-resonance occurs at a frequency of 437 MHz for 6-layer stack-up with a magnitude of -40.03 dB. The

6-layer version 3 has an anti-resonant frequency at 474 MHz at -32.82 dB. The 4-layer stack-up has an anti-resonance at a frequency of 444 MHz with magnitude -22.8 dB. Beyond this point, the 6-layer stack-ups outperforms mainly the 4-layer stack-up. The 4-layer stack-up has a resonant frequency at 1893 MHz with a magnitude of -68 dB.

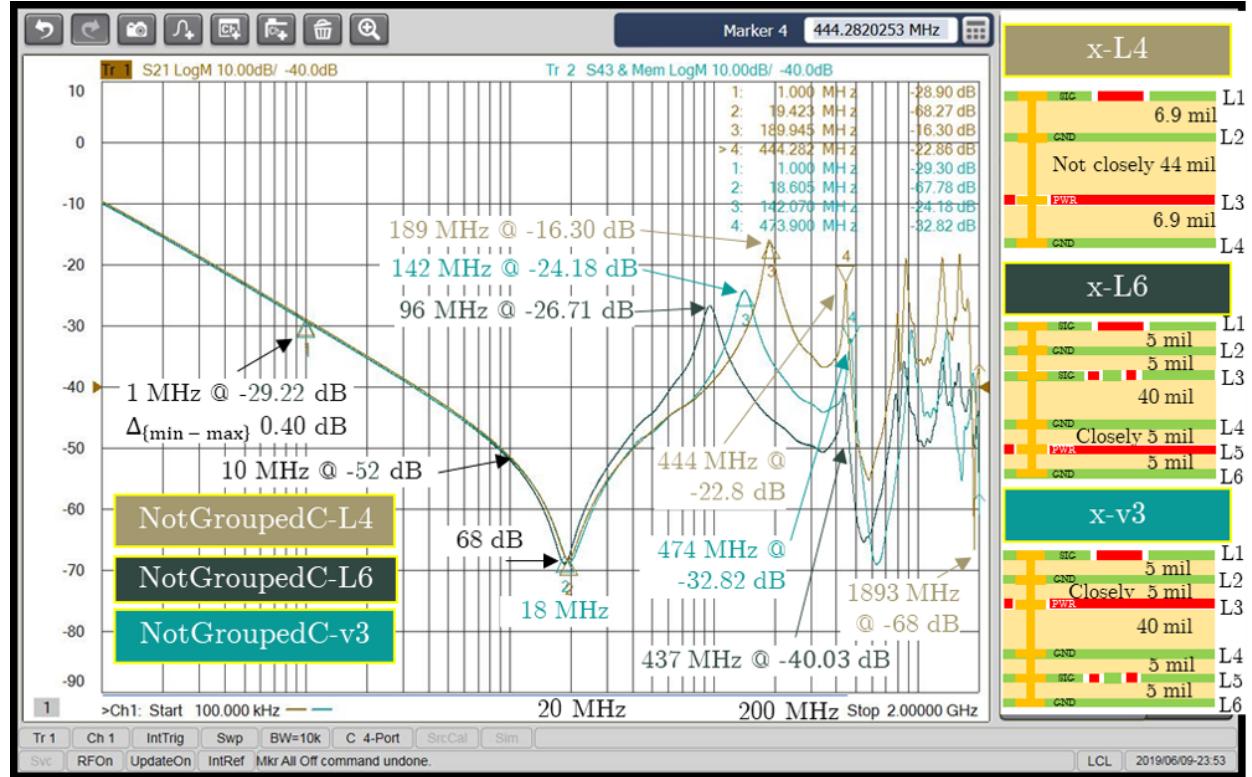


Figure 4.10: Insertion loss 4-layer, 6-layer, and 6-layer Version 3 for Not Grouped Capacitors.

4-Layer, 6-Layer, and 6-Layer Version 3 for Grouped Capacitors

Fig. 4.11 shows the measured insertion loss for grouped capacitors mounted. Three boards were measured, S_{21} (brown) shows the insertion loss of the board with 4-layer stack-up. S_{43} memory trace (aquamarine) shows the insertion loss of the board with 6-layer stack-up. S_{43} (cyan) shows the impedance of the board with 6-layer version 3 stack-up. The stack-up is shown on the right side.

At a frequency of 1 MHz, the insertion loss of all three stack-ups is similar at -29.01 dB. The slope is -20 dB. The first resonant frequency occurs between 18 MHz and 20 MHz.

The first anti-resonance occurs at a frequency of 86 MHz for 6-layer stack-up with a magnitude of -25.5 dB. The 6-layer version 3 has an anti-resonant frequency at 142 MHz at -24.18 dB. The 4-layer stack-up has at a frequency of 180 MHz with magnitude -16.60 dB. The second anti-resonance occurs at a frequency of 433.5 MHz for 6-layer stack-up with a magnitude of -41.02 dB. The 6-layer version 3 has an anti-resonant frequency at 469 MHz at -32.09 dB. The 4-layer stack-up has an anti-resonance at a frequency of 439.5 MHz with magnitude -24 dB. Beyond this point, the 6-layer stack-ups outperforms mainly the 4-layer stack-up.

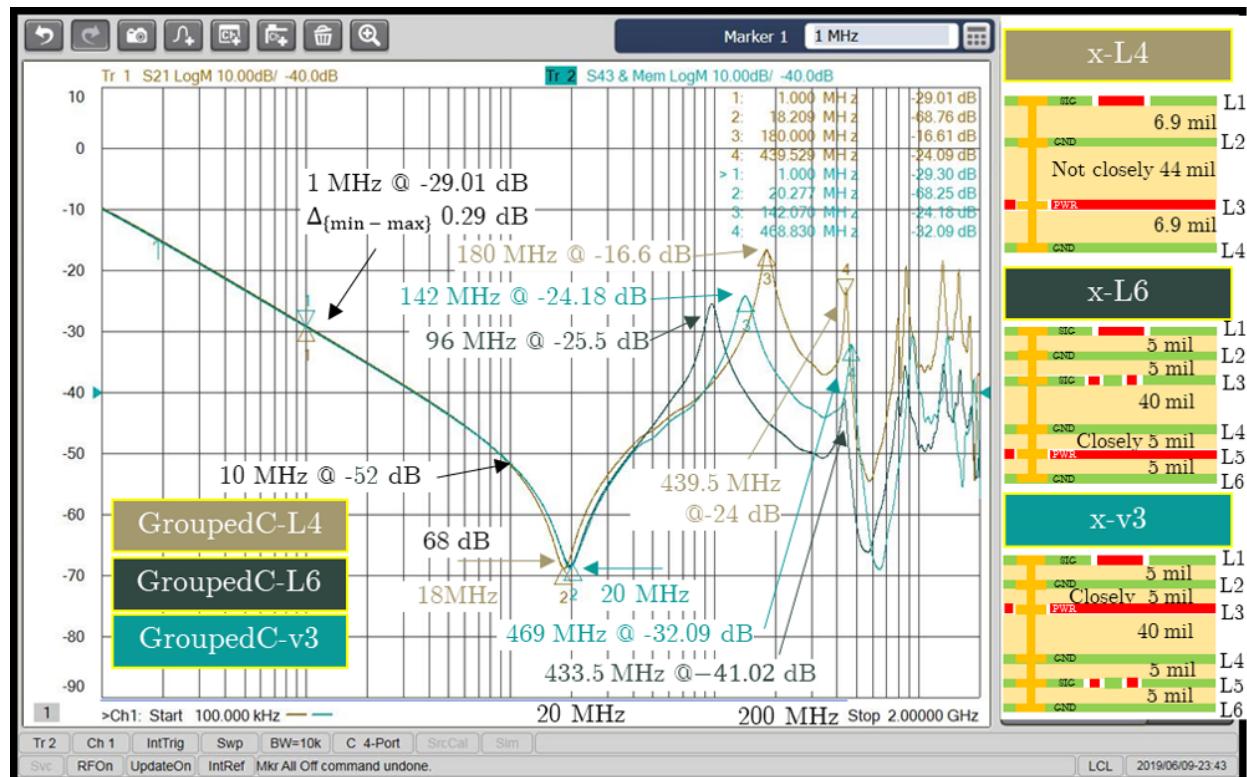


Figure 4.11: Insertion loss 4-layer, 6-layer, and 6-layer Version 3 for Grouped Capacitors.

4-Layer for No, Not Grouped, and Grouped Capacitors

Fig. 4.12 shows the measured insertion loss for a 4-layer stack-up. Three boards were measured, s_{21} (brown) shows the insertion loss of the board with no capacitors mounted. S_{43} memory trace (aquamarine) shows the insertion loss of the board with not grouped ca-

pacitors mounted. S_{43} (cyan) shows the impedance of the board with grouped capacitors mounted. The stack-up is shown on the right side.

At a frequency of 1 MHz, the insertion loss of all three stack-ups is similar at -29.01 dB. The slope is -20 dB. The first resonant frequency occurs between 18 MHz and 20 MHz. The first anti-resonance occurs at a frequency of 180 MHz for grouped capacitors with a magnitude of -16.63 dB. The not grouped capacitors have an anti-resonant frequency at 185 MHz at -16.7 dB. The no capacitors case has at a frequency of 339 MHz the first resonance with magnitude -36 dB.

The second anti-resonance occurs at a frequency of 442 MHz for grouped capacitors with a magnitude of -23.28 dB. The not grouped capacitors have an anti-resonant frequency at 442 MHz at -23.28 dB. The no capacitor case has an anti-resonance at a frequency of 439 MHz with magnitude -21.37 dB. Beyond this point, all three cases show similar performance, if good or bad, is depending on the frequency.

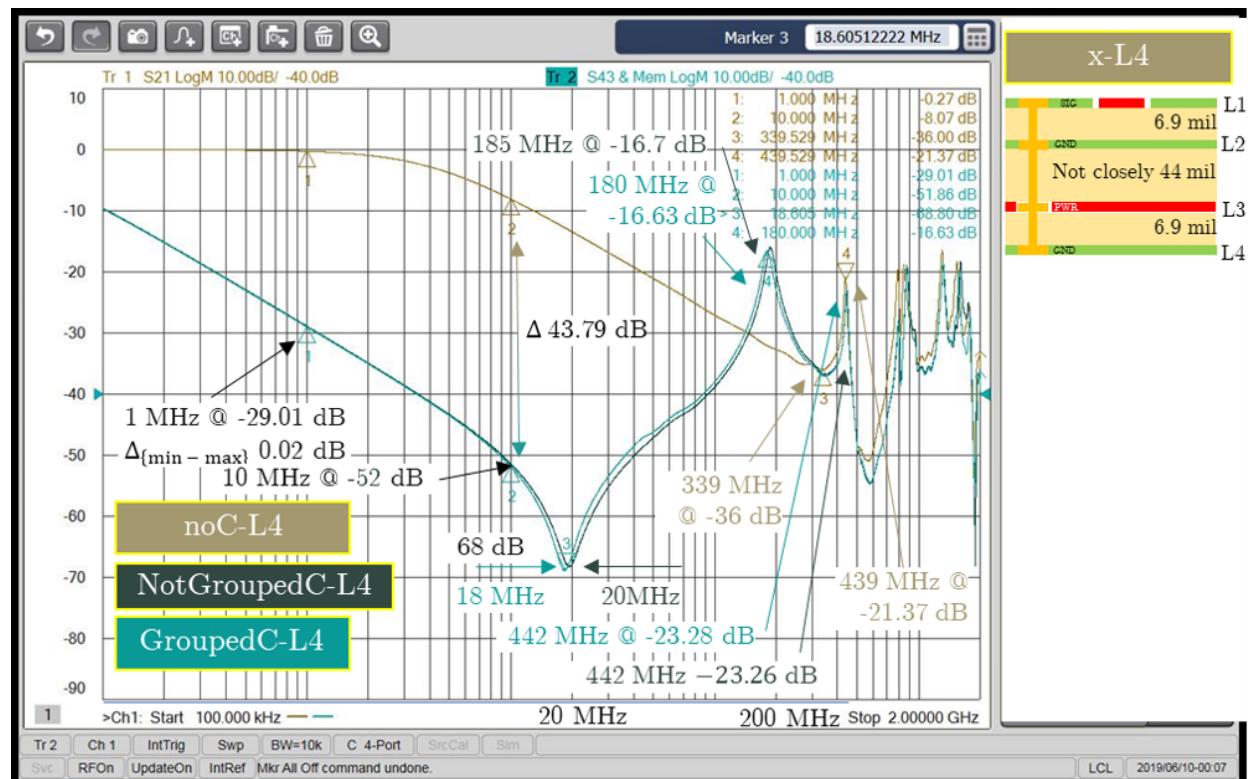


Figure 4.12: Insertion loss 4-layer for No, Not Grouped, and Grouped Capacitors.

6-Layer for No, Not Grouped, and Grouped Capacitors

Fig. 4.13 shows the measured insertion loss for a 6-layer stack-up. Three boards were measured, s_{21} (brown) shows the insertion loss of the board with no capacitors mounted. S_{43} memory trace (aquamarine) shows the insertion loss of the board with not grouped capacitors mounted. S_{43} (cyan) shows the impedance of the board with grouped capacitors mounted. The stack-up is shown on the right side.

At a frequency of 1 MHz, the insertion loss of all three stack-ups is similar at -29.01 dB. The slope is -20 dB. The first resonant frequency occurs between 19 MHz and 20 MHz. The first anti-resonance occurs at a frequency of 97 MHz for grouped capacitors with a magnitude of -25.5 dB. The not grouped capacitors have an anti-resonant frequency at 97 MHz at -25.49 dB. The no capacitors case has at a frequency of 339 MHz the first resonance with magnitude -49.7 dB.

The second anti-resonance occurs at a frequency of 433 MHz for grouped capacitors with a magnitude of -40.99 dB. The not grouped capacitors have an anti-resonant frequency at 437 MHz at -40.93 dB. The no capacitor case has an anti-resonance at a frequency of 439 MHz with magnitude -40.70 dB. Beyond this point, all three cases show similar performance, if good or bad, is depending on the frequency.

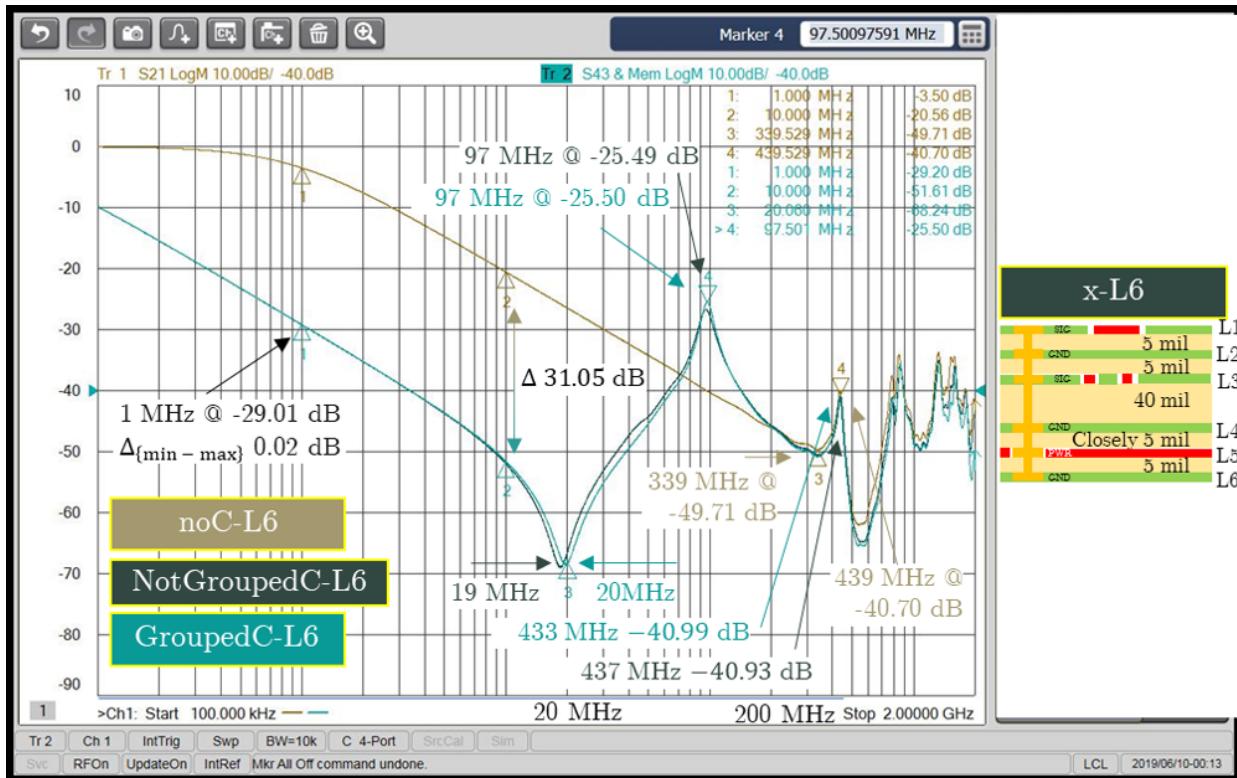


Figure 4.13: Insertion loss 6-layer for No, Not Grouped, and Grouped Capacitors.

6-Layer Version 3 for No, Not Grouped, and Grouped Capacitors

Fig. 4.14 shows the measured insertion loss for a 6-layer version 3 stack-up. Three boards were measured, s_{21} (brown) shows the insertion loss of the board with no capacitors mounted. S_{43} memory trace (aquamarine) shows the insertion loss of the board with not grouped capacitors mounted. S_{43} (cyan) shows the impedance of the board with grouped capacitors mounted. The stack-up is shown on the right side.

At a frequency of 1 MHz, the insertion loss of all three stack-ups is similar at -29.37 dB. The slope is -20 dB. The first resonant frequency occurs between 19 MHz and 20 MHz. The first anti-resonance occurs at a frequency of 131 MHz for not grouped capacitors with a magnitude of -21.53 dB. The grouped capacitors have an anti-resonant frequency at 142 MHz at -24.18 dB. The no capacitors case has at a frequency of 339 MHz the first resonance with magnitude -44.02 dB.

The second anti-resonance occurs at a frequency of 465 MHz for not grouped capacitors with a magnitude of 31.14 dB. The grouped capacitors have an anti-resonant frequency at 469 MHz at -32.08 dB. The no capacitor case has an anti-resonance at a frequency of 469 MHz with magnitude -31.28 dB. Beyond this point, all three cases show similar performance, if good or bad, is depending on the frequency.

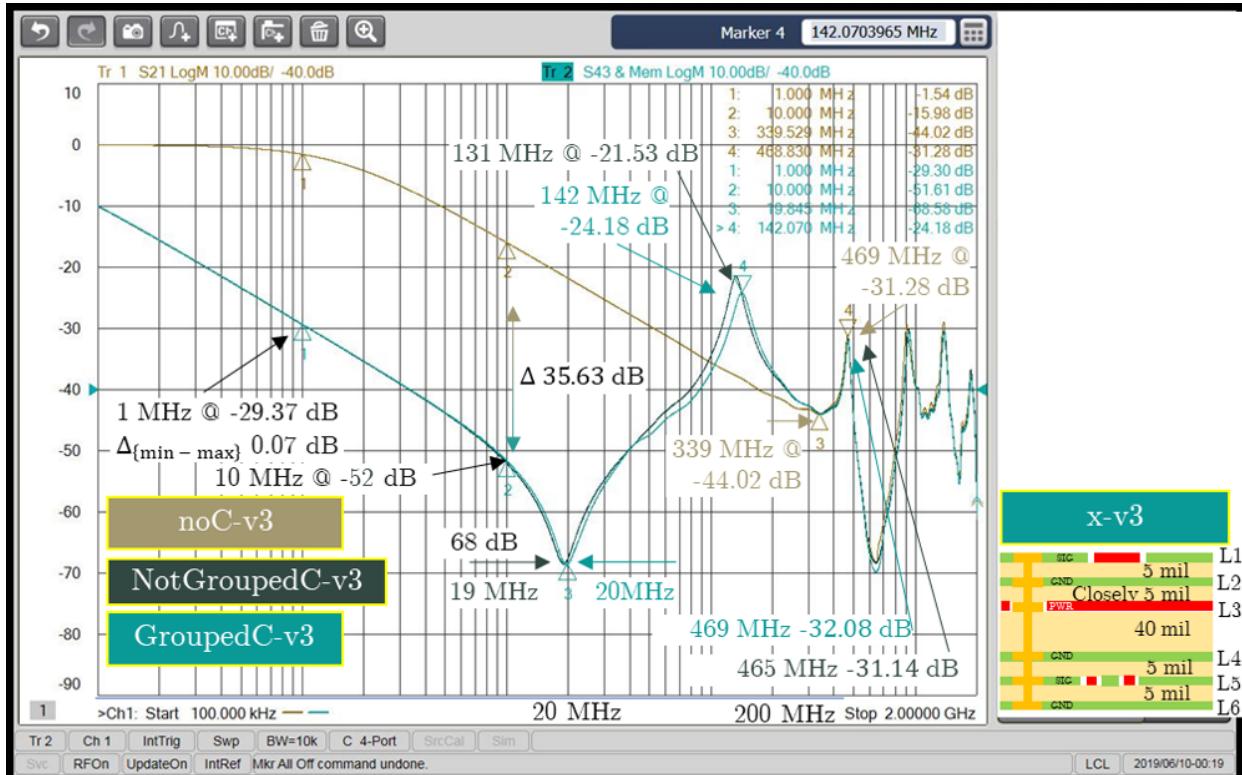


Figure 4.14: Insertion loss 6-Layer version 3 for No, Not Grouped, and Grouped Capacitors.

4.2 Embedded Capacitance of a PCB Transient Response

This section presents and discusses the results gathered with an active differential probe and oscilloscope.

4.2.1 Measurement Setup

Fig. 4.15 shows the measurement setup built to perform active differential probe measurements with an oscilloscope. The used differential probe is from Tektronix P6247 Differential Probe 1 GHz. In between the probe and oscilloscope, the Tektronix TPA-BNC TEKPROBE BNC Adapter 42 Vpk Max is used to connect the probe to the oscilloscope as shown in Fig. 4.16. To ensure probe contact and to have similar test results that can be compared to each other the PCB is assembled with a 2.54 mm 2 pin header. The pin header is soldered once on a center pad of connector J1 and once on the bottom right ground pad of connector J1, as shown in Fig. 4.17. The boards measured are shown in Fig. 4.18. To simulate load condition a load board was attached to connector P1, as shown in Fig. 4.19. Tab. 3.3 shows the used capacitors and in which case what capacitor pair was equipped.

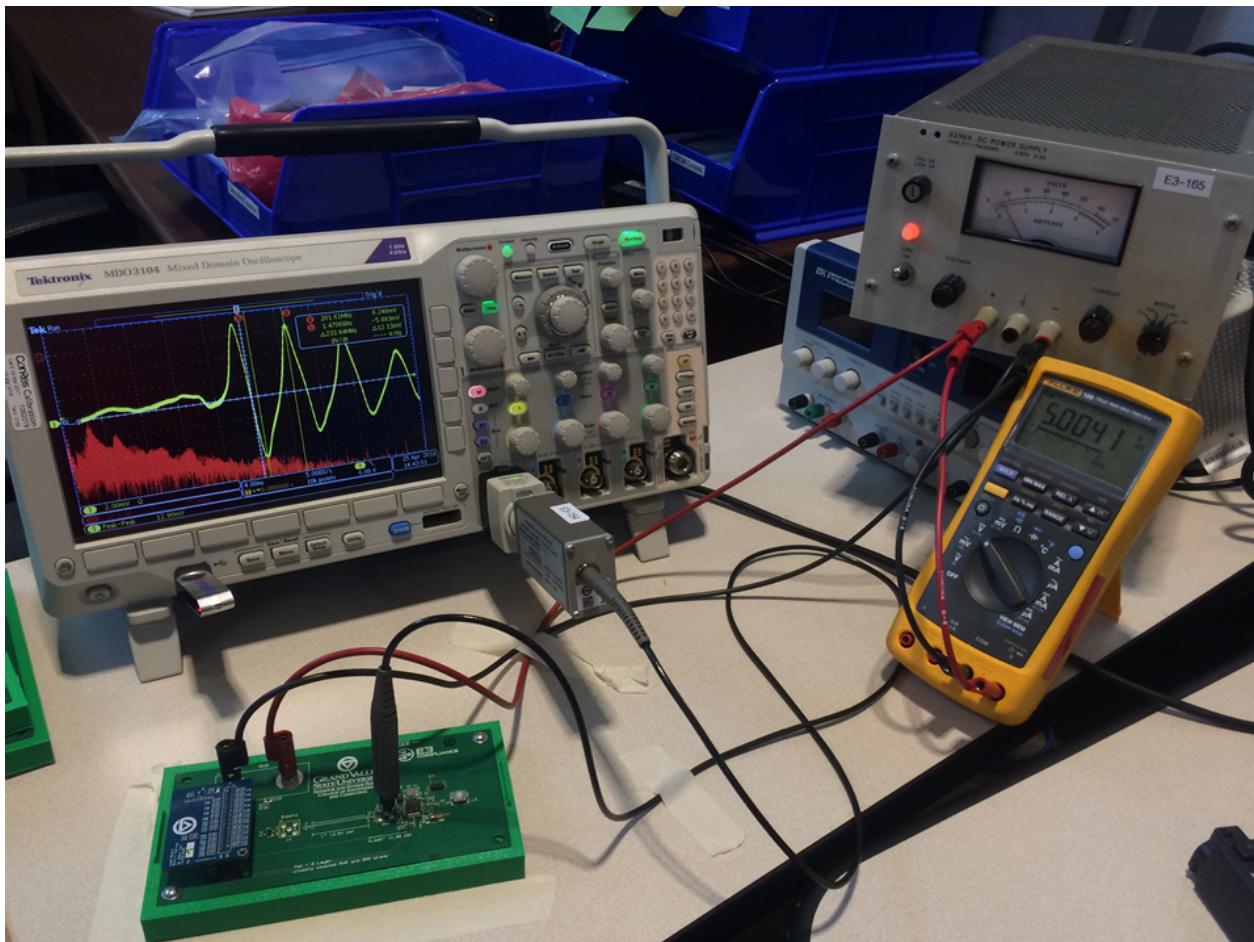


Figure 4.15: Measurement setup used to investigate the embedded capacitance and there effect in time domain.



Figure 4.16: Differential probe setting used to perform measurements.

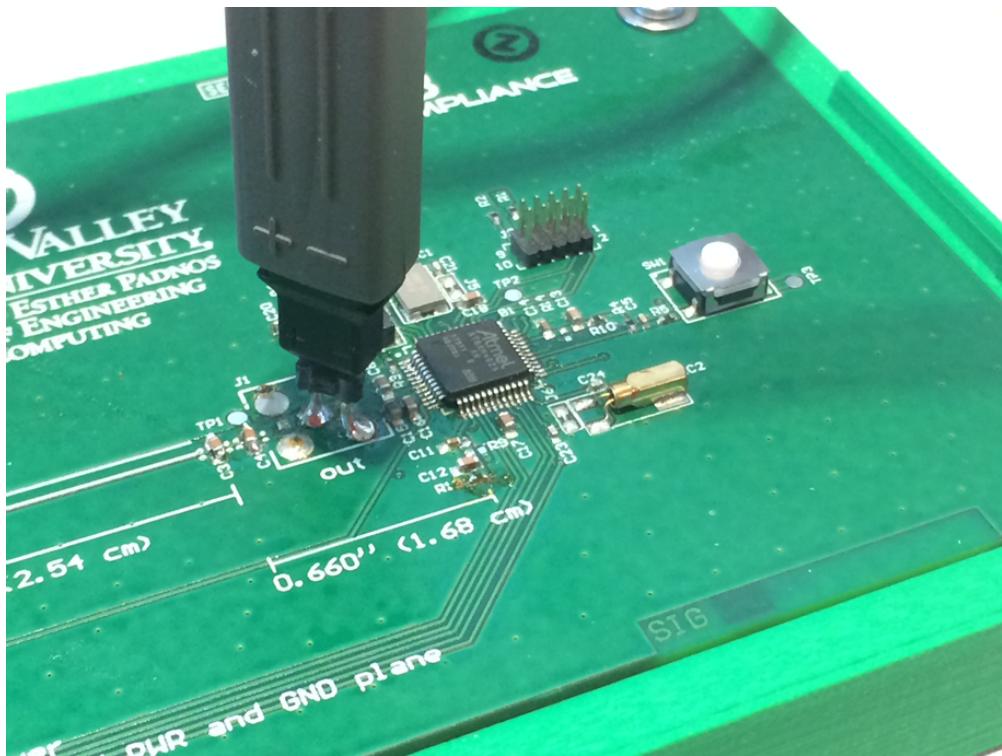


Figure 4.17: Differential probe connected to EUT with an soldered header 2.54 mm pitch on connector pad J1.



Figure 4.18: Assembled PCB used to investigate the embedded capacitance and there effect in time domain.

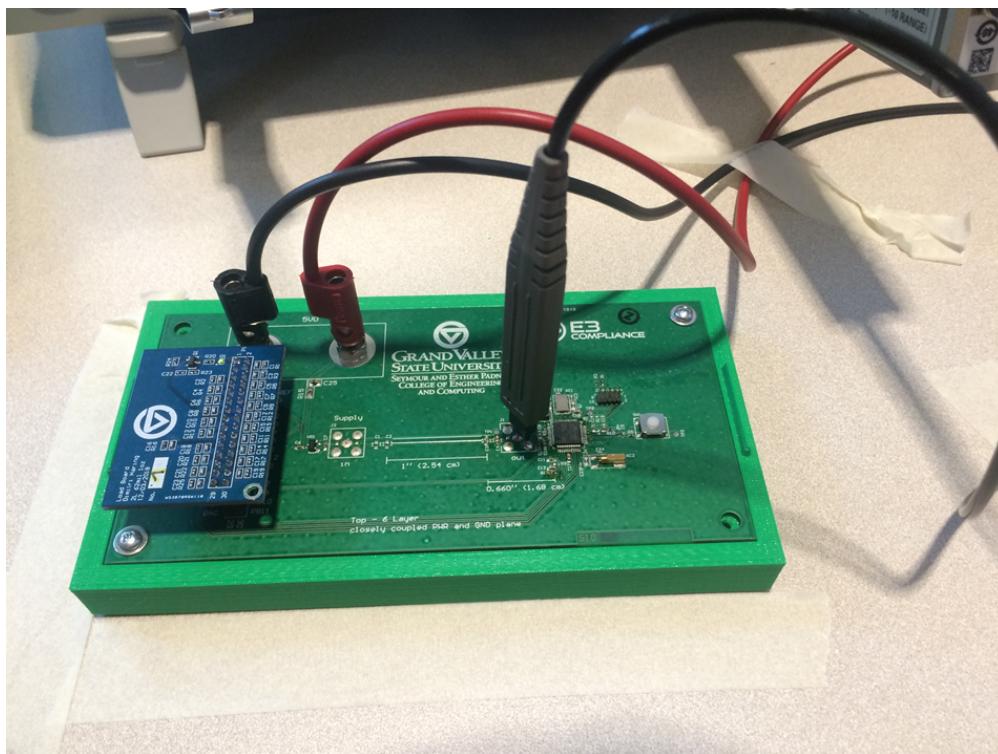


Figure 4.19: Load board attached to DUT on connector P1.

4.2.2 4-Layer Not Grouped Capacitors

Fig. 4.20 shows the measured transient response of the 4-layer stack-up with not grouped capacitors. The blue graph shows the measured voltage averaged with 512 points. The peak-to-peak voltage at cursor position has the magnitude of 21.28 mV. The measured frequency is 675.86 MHz.

The red graph shows the Fast Fourier Transform (FFT) of channel one with a Hanning window, the vertical scale is in dBV. Keep in mind that the average function will act as low pass filter. However, the frequencies of interest are in the higher frequency band. The highest peak of the FFT occurs with -66 dB at 319 MHz. A second peak above 100 dB occurs with -86 dB at 922 MHz.

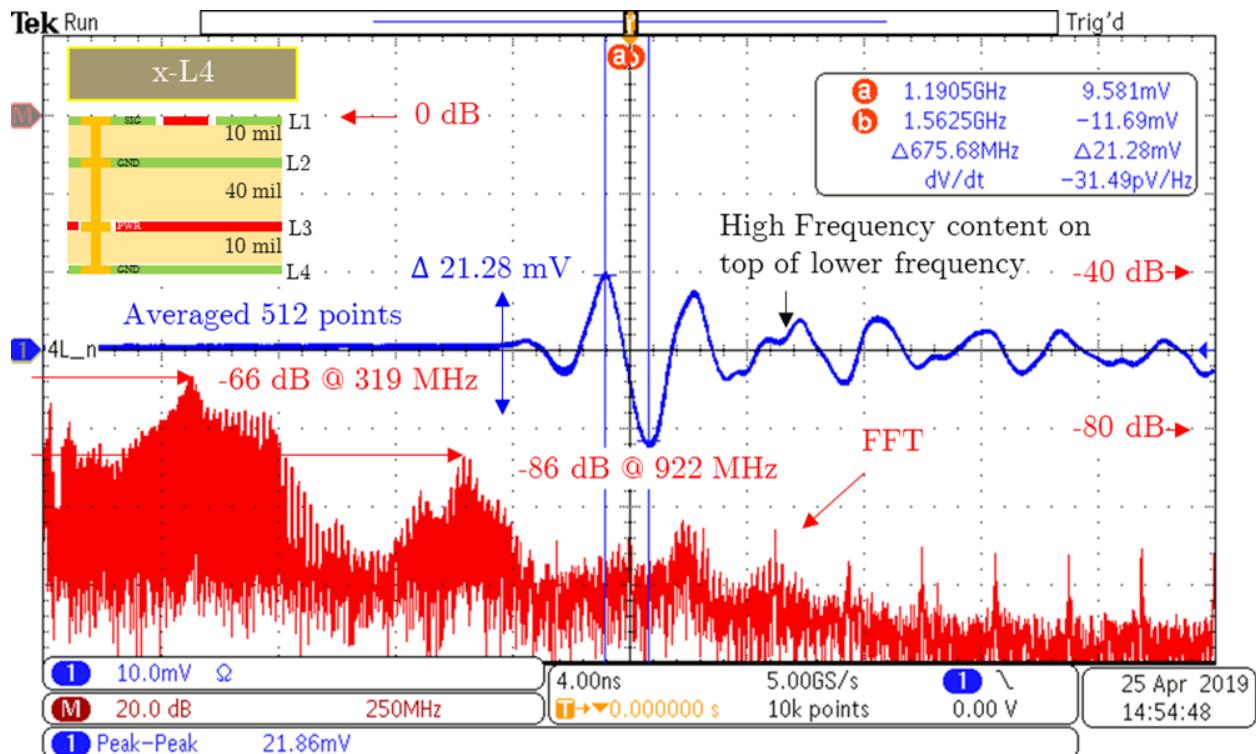


Figure 4.20: 4-layer not grouped caps measured with diff. probe and two capacitors.

4.2.3 4-Layer Grouped Capacitors

Fig. 4.21 shows the measured transient response of the 4-layer stack-up with grouped capacitors. The blue graph shows the measured voltage averaged with 512 points. The peak-to-peak voltage at cursor position has the magnitude of 16.35 mV. The measured frequency is 714.29 MHz.

The red graph shows the FFT of channel one with a Hanning window the vertical scale is in dBV. Keep in mind that the average function will act as low pass filter. However, the frequencies of interest are in the higher frequency band. The highest peak of the FFT occurs with -70 dB at 319 MHz. A second peak above 100 dB occurs with -90 dB at 922 MHz.

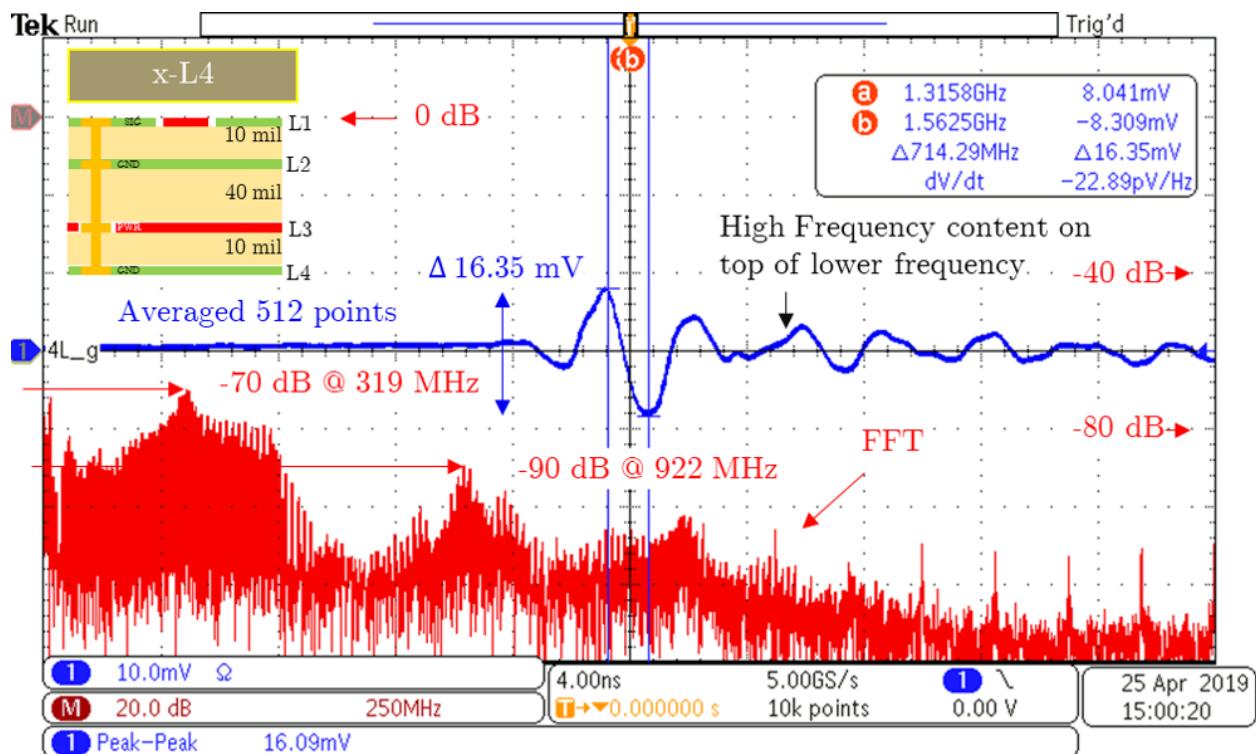


Figure 4.21: 4-layer grouped caps measured with diff. probe and two capacitors populated.

4.2.4 6-Layer Not Grouped Capacitors

Fig. 4.22 shows the measured transient response of the 6-layer stack-up with not grouped capacitors. The blue graph shows the measured voltage averaged with 512 points. The peak-to-peak voltage at cursor position has the magnitude of 15.9 mV. The measured frequency is 416.67 MHz.

The red graph shows the FFT of channel one with a Hanning window the vertical scale is in dBV. Keep in mind that the average function will act as low pass filter. However, the frequencies of interest are in the higher frequency band. The highest peak of the FFT occurs with -56 dB at 156 MHz. The second peak occurs with -83 dB at 442 MHz. A third peak above 100 dB occurs with -96 dB at 800 MHz. Additional inductance associated with longer traces gives raise to this behavior seen of the ringing before the trigger.

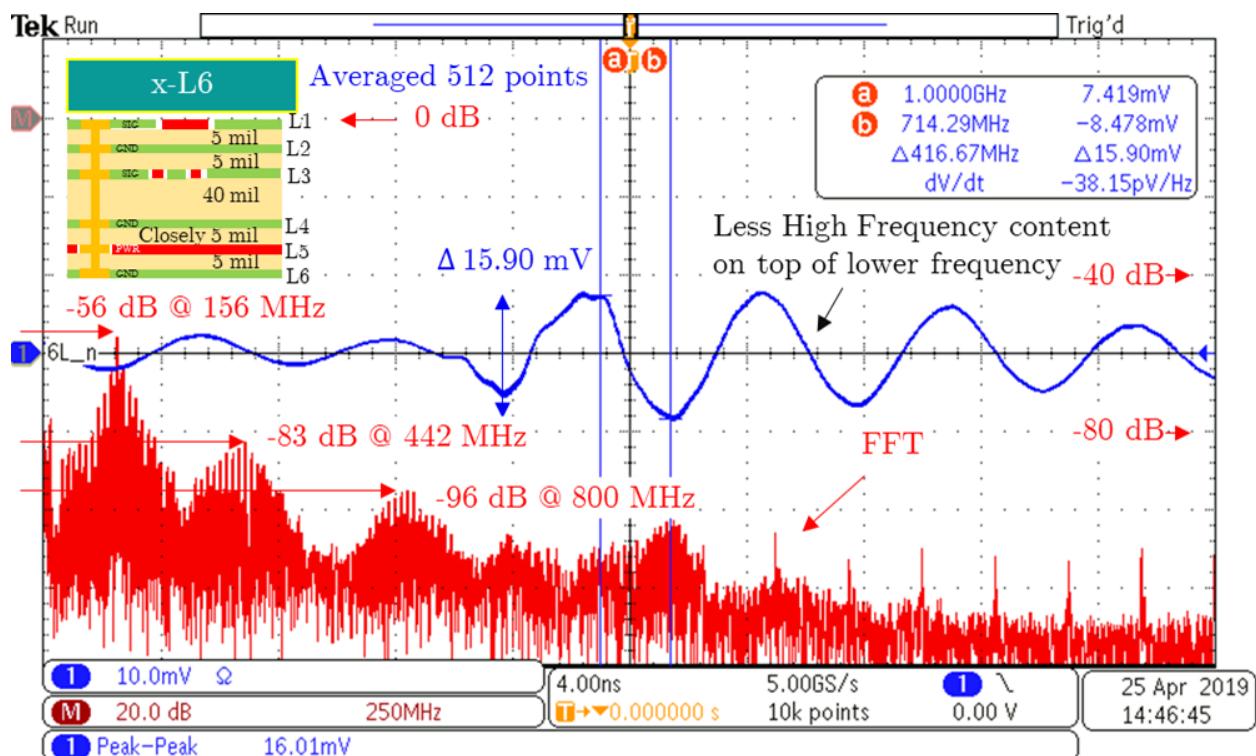


Figure 4.22: 6-layer not grouped caps measured with diff. probe and two capacitors.

4.2.5 6-Layer Grouped Capacitors

Fig. 4.22 shows the measured transient response of the 6-layer stack-up with grouped capacitors. The blue graph shows the measured voltage averaged with 512 points. The peak-to-peak voltage at cursor position has the magnitude of 12.99 mV. The measured frequency is 657.89 MHz, as shown in Fig. 4.24.

The red graph shows the FFT of channel one with a Hanning window the vertical scale is in dBV. Keep in mind that the average function will act as low pass filter. However, the frequencies of interest are in the higher frequency band. The highest peak of the FFT occurs with -60 dB at 161 MHz. The second peak occurs with -82 dB at 451 MHz. A third peak around 100 dB occurs with -102 dB at 774 MHz.

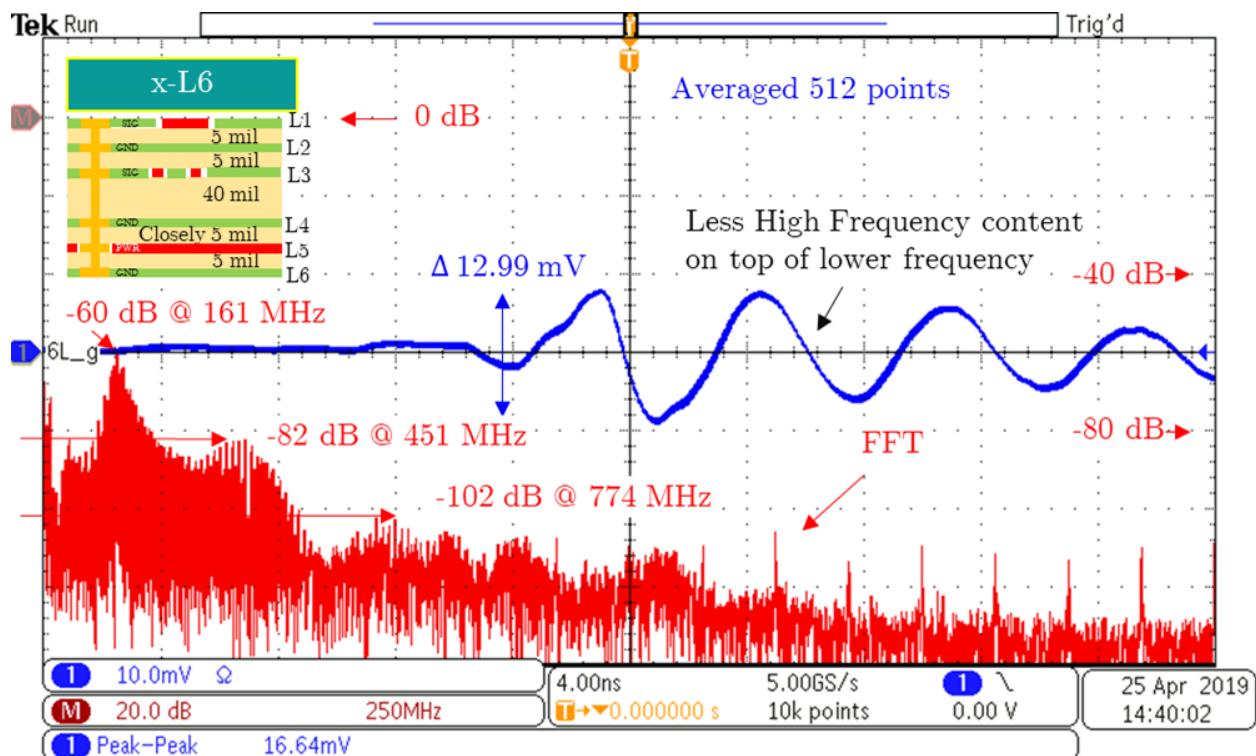


Figure 4.23: 6-layer grouped caps measured with diff. probe and two capacitors populated.

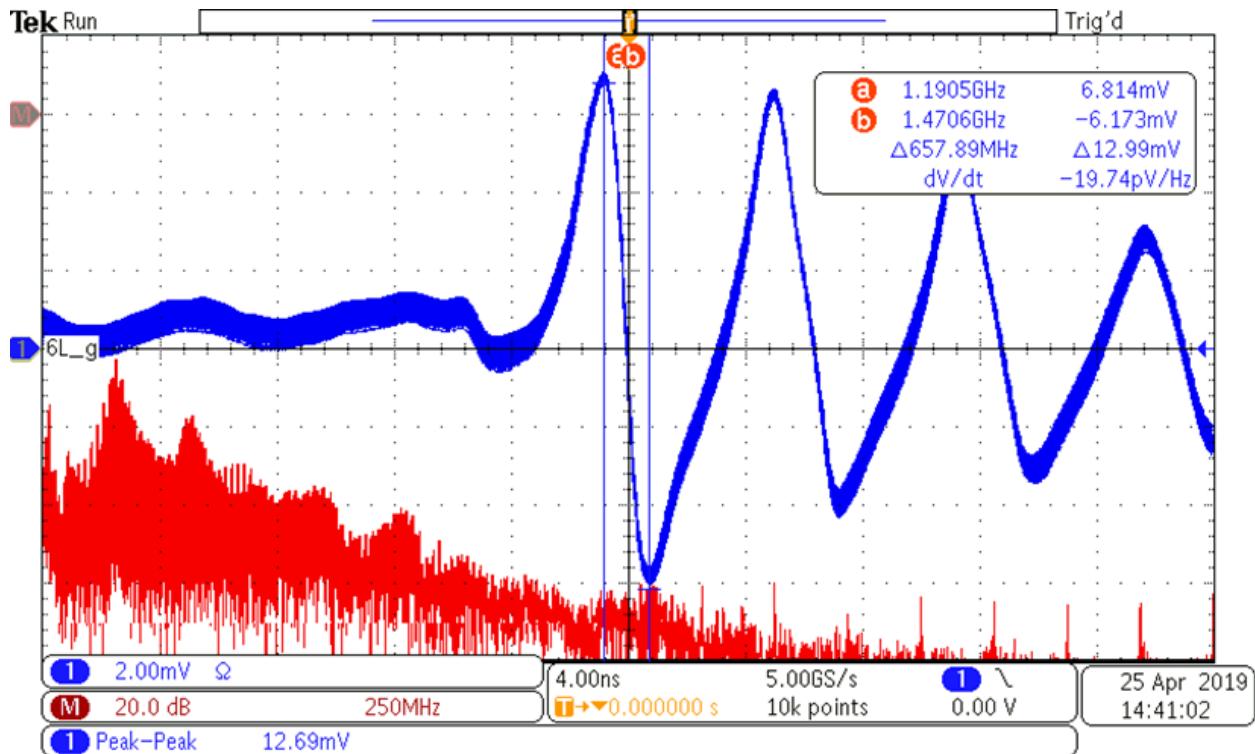


Figure 4.24: 6-layer grouped caps measured with diff. probe and two capacitors populated, 2 mV horizontal division.

4.3 EMC Filters - Source and Load Impedance

This section provides the results and discussion of EMC filter ideal simulated and measured EMC filter with VNA as presented in Section 3.2.

4.3.1 Measurement Setup

The measurement setup is illustrated in Fig. 4.25. The PCB was equipped with C 10 nF, L 4.7 uH, and 91K resistors. The topologies used were CL - R and LC - R. The VNA used is a KEYSIGHT ENA Network Analyzer E5080A 9 kHz - 9 GHz. Attached to the ports is an N-Type male to SMA female connector followed with a 4 foot M17/60-RG142 SMA male to SMA male cable. The VNA was parameterized according to settings in Tab. 4.1. Further images of measurement setup can be found in Appendix B.2.

Table 4.1: VNA settings used for EMC filter measurements.

Parameter	Setting
Frequency range	100 kHz - 1 GHz
Power	15 dBm
IF Bandwidth	1 kHz
Number of points	10001
Calibration	Full 4 port
Calibration Kit	NA717-Kit[SMA]
Calibration File	4pcal.csa

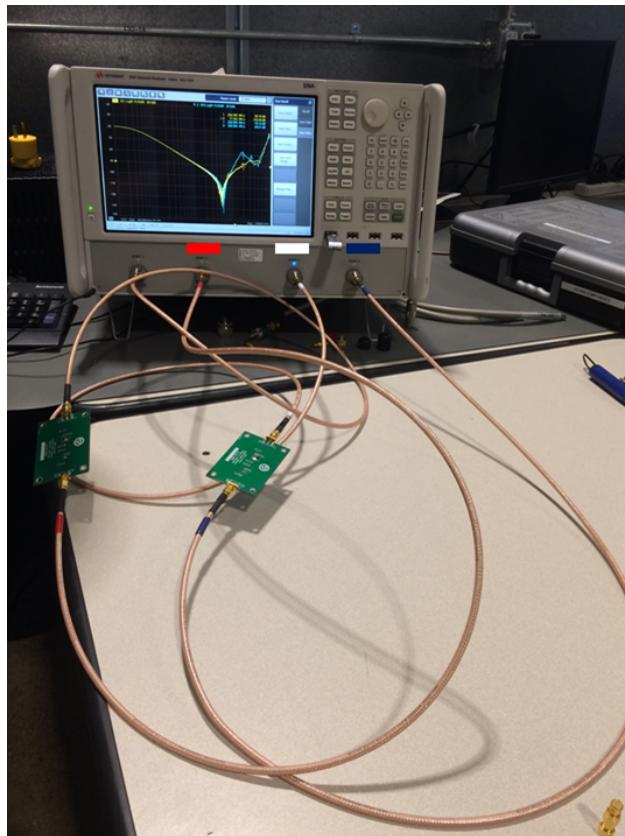


Figure 4.25: EMC filter VNA measurement setup.

The manufactured PCB accommodating these structures is shown in Fig. 4.26.

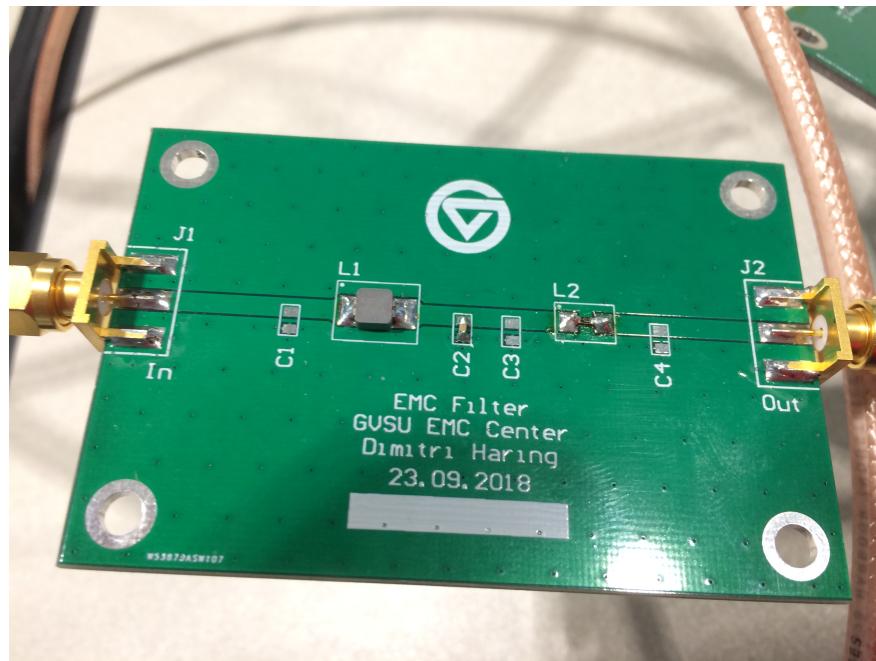


Figure 4.26: EMC Filter LC structure with C on the high impedance side. The filter is connected to VNA port 1 on connector J1 and port 2 on connector J2.

4.3.2 Measurement logMag s21 - LC - 1 k Ω , s43 - CL - 1 k Ω 100 kHz - 1 GHz

In Section 3.2.1, two different LC filter structure were discussed. The impedance of these structures were measured with VNA and shown in Fig. 4.27. To the right, the schematics and component values are shown. The compared structures are LC - R 1 k Ω (brown) versus CL - R 1 k Ω (aquamarine). Points were the magnitude and frequencies are similar are marked blue.

The curves start at an offset of -21.3 dB. At 1 MHz both graphs have a magnitude of -30 dB. At 10 MHz the CL-R structure has a magnitude of -49 dB. At 10 MHz the LC-R structure has a magnitude of -65.7 dB. The slope per decade in the frequency range of 1 MHz to 10 MHz is -19 dB for the CL-R structure, and -35.7 dB for the LC-R structure. By subtracting the slope of CL-R from the slope LC-R, the deviation at 10 MHz is 16.7 dB. The first resonance occurs at 30 MHz with -115 dB for the LC-R structure and -84.9 dB for the CL-R structure. A second resonance occurs at 60 MHz with -95.5 dB for the LC-R structure and -83.0 dB for the CL-R structure. At 122 MHz the CL-R structure has

a magnitude of -65.9 dB. At 122 MHz the LC-R structure has a magnitude of -74.5 dB. In a frequency range of 100 kHz to 1 MHz the CL-R structure outperforms the LC-R structure. In a frequency range of 1 MHz to 1 GHz the LC-R structure outperforms the CL-R structure.

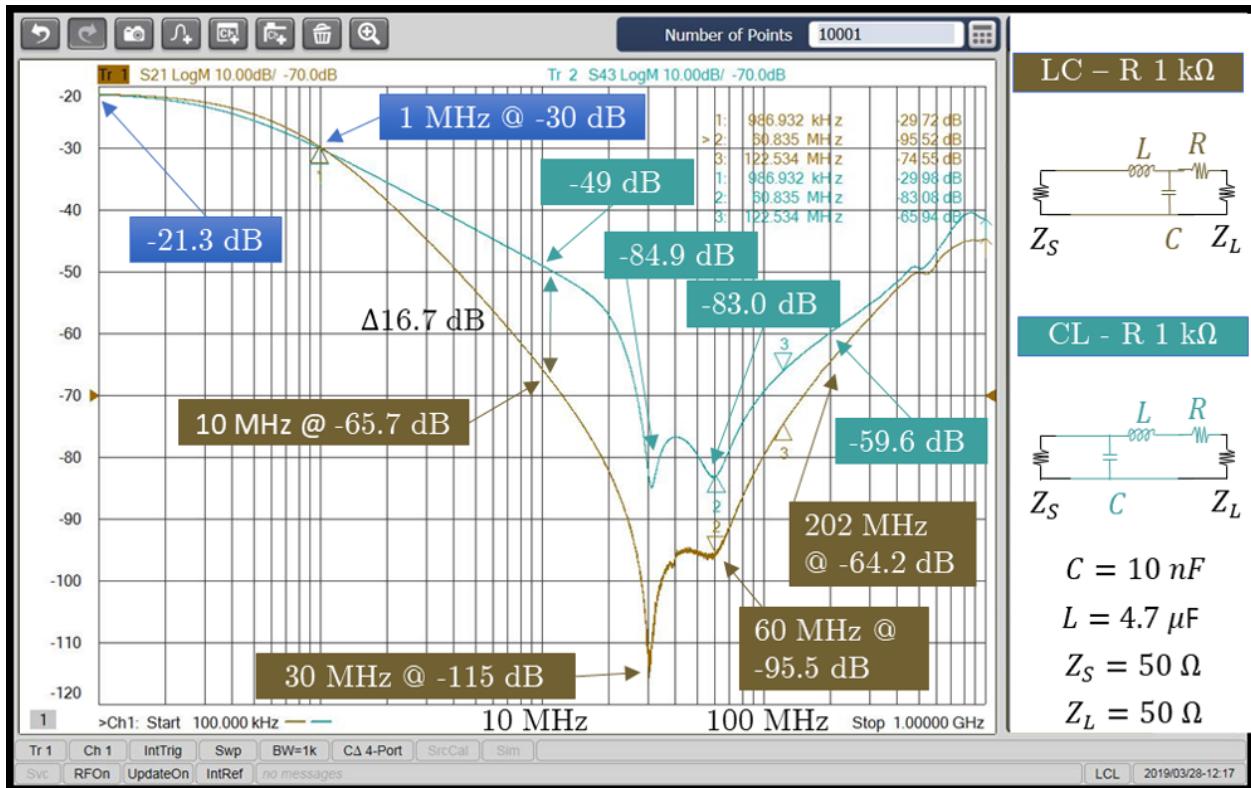


Figure 4.27: EMC Filter Measurement s_{21} R $1 \text{ k}\Omega$ - Cl vs. s_{43} CL - R $1 \text{ k}\Omega$.

4.3.3 Measurement logMag s_{21} -LC R $10 \text{ k}\Omega$ s_{43} -CL R $10 \text{ k}\Omega$ 100 kHz - 1 GHz

In Section 3.2.1, two different LC filter structures were discussed. The impedance of these structures were measured with VNA and shown in Fig. 4.28. To the right, the schematics and component values are shown. The compared structures are LC - R $10 \text{ k}\Omega$ (brown) versus CL - R $10 \text{ k}\Omega$ (aquamarine). Points where the magnitude and frequencies are similar are marked blue.

The curves start at an offset of -41 dB. At 1 MHz both graphs have a magnitude of -50 dB. At 10 MHz both graphs have a magnitude of -69.2 dB. The slope per decade in the

frequency range of 1 MHz to 10 MHz is -19.2 dB for both graphs. The first resonance occurs at 60 MHz with -101 dB for the LC-R structure and -96.2 dB for the CL-R structure. At 202 MHz the CL-R structure has a magnitude of -69 dB and hits an anti-resonance. At 202 MHz the LC-R structure has a magnitude of -82.2 dB. At 392 MHz the CL-R structure has a magnitude of -78.1 dB and hits second resonance. In a frequency range of 100 kHz to 20 MHz, both structures perform similarly. In a frequency range of 20 MHz to 1 GHz the LC-R structure outperforms the CL-R structure.

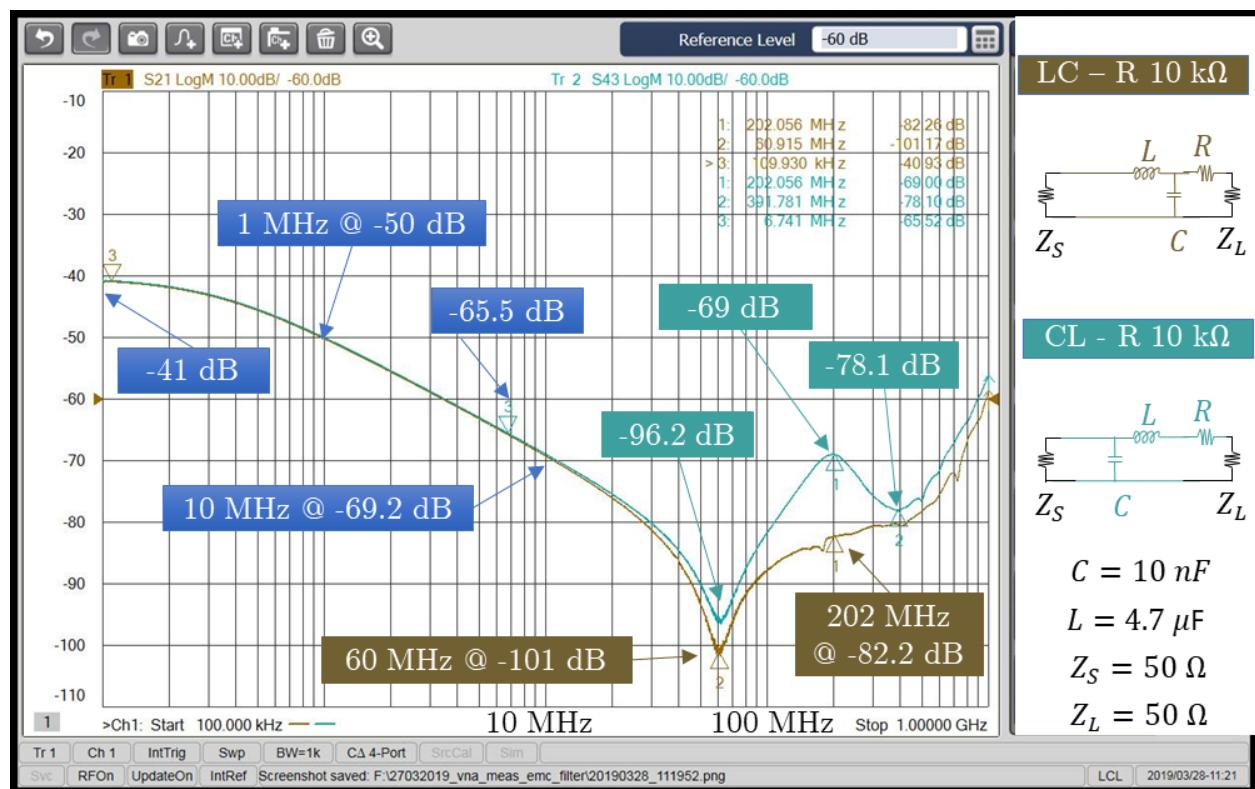


Figure 4.28: EMC filter measurement s_{21} $R 10 \text{ k}\Omega$ - Cl vs. s_{43} CL - $R 10 \text{ k}\Omega$.

4.3.4 Measurement logMag s_{21} -CL $R 91 \text{ k}\Omega$ vs s_{43} -CL $R 91 \text{ k}\Omega$ 100 kHz - 1 GHz

In Section 3.2.1, two different LC filter structures were discussed. The impedance of these structures were measured with VNA and shown in Fig. 4.29. To the right, the schematics and component values are shown. The compared structures are LC - R 91 kΩ (brown) versus CL - R 91 kΩ (aquamarine). Points where the magnitude and frequencies are similar

are marked blue.

The curves start at an offset of -60 dB. At 1 MHz both graphs have a magnitude of -69 dB. At 10 MHz both graphs have a magnitude of -87.8 dB. The slope per decade in the frequency range of 1 MHz to 10 MHz is -18.8 dB for both graphs. The first resonance occurs at 53 MHz with -123.6 dB for the LC-R structure and -109.7 dB for the CL-R structure. At 202 MHz the CL-R structure has a magnitude of -78 dB and hits an anti-resonance. At 202 MHz the LC-R structure has a magnitude of -87.69 dB. At 326 MHz the CL-R structure has a magnitude of -84.3 dB. An additional resonance can be seen for the CL-R structure at a frequency of 488 MHz with a magnitude of -90 dB. In a frequency range of 100 kHz to 25 MHz, both structures perform similarly. In a frequency range of 25 MHz to 60 MHz the LC-R structure outperforms the CL-R structure. In a frequency range of 60 MHz to 77 MHz, both structures perform similarly. In a frequency range of 77 MHz to 326 MHz the LC-R structure outperforms the CL-R structure. Beyond 326 MHz depending on resonance or not one outperforms another.

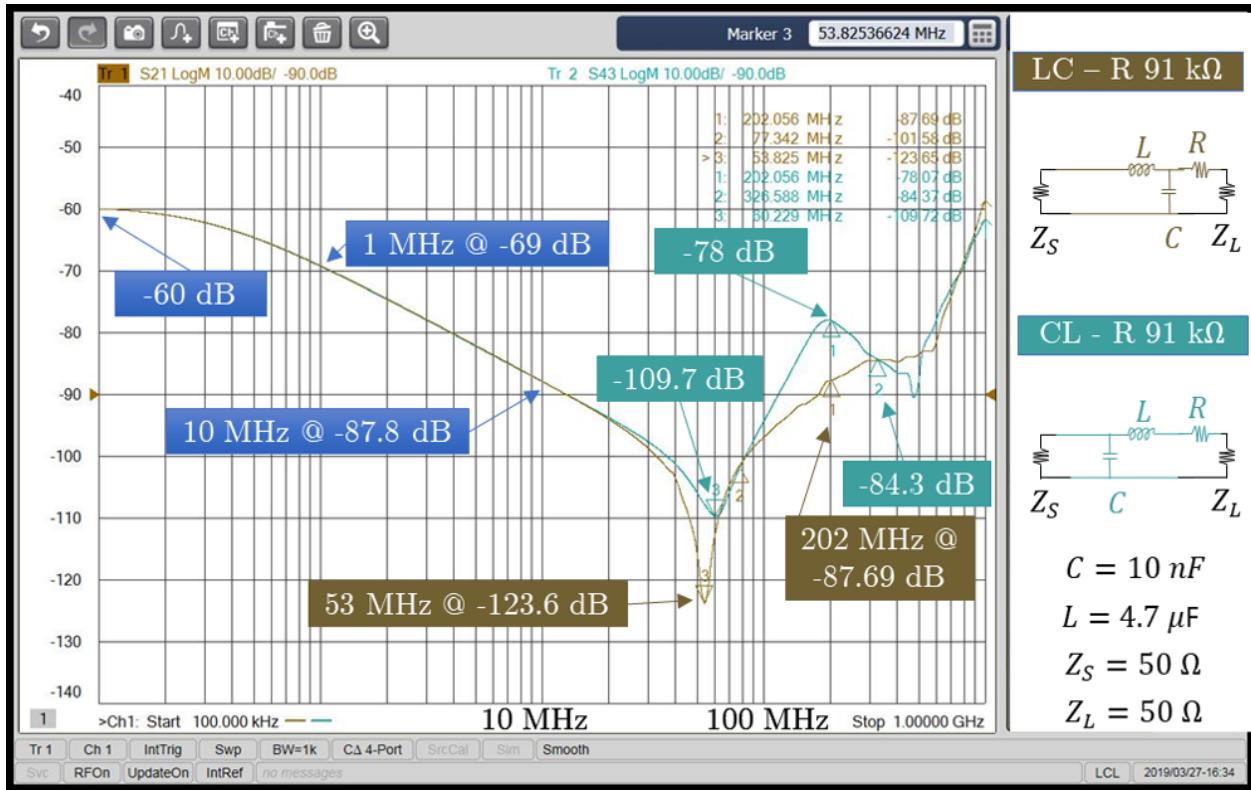
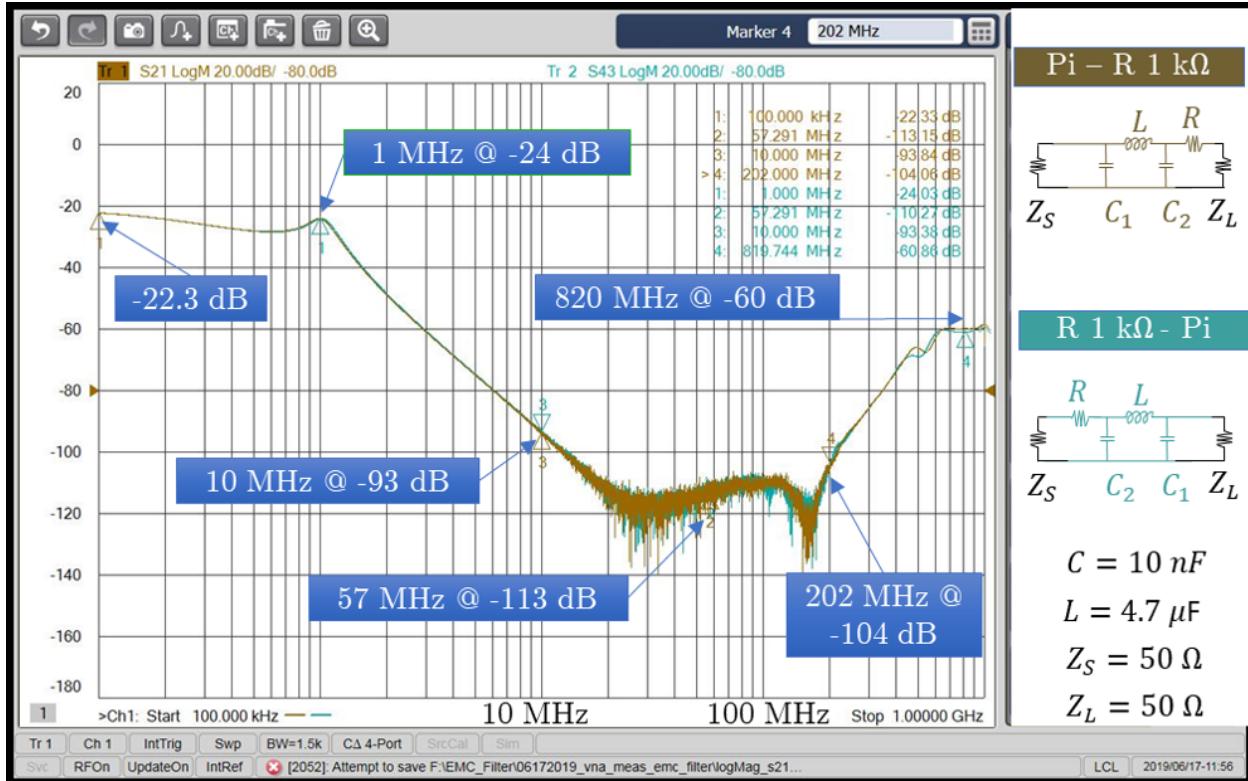


Figure 4.29: EMC filter measurement s_{21} R 91 kΩ - Cl vs. s_{43} CL - R 91 kΩ.

4.3.5 Measurement logMag s_{21} - π - R 1 kΩ vs. s_{43} - R 1 kΩ - π 100 kHz - 1 GHz

In Section 3.2.1, two different π filter structures were discussed. The impedance of these structures were measured with VNA and shown in Fig. 4.30. To the right, the schematics and component values are shown. The compared structures are π - R 1 kΩ (brown) versus R 1 kΩ - π (aquamarine). Points where the magnitude and frequencies are similar are marked blue.

The curves start at an offset of -22.3 dB. At 1 MHz both graphs have a magnitude of -24 dB which is an anti-resonance. At 10 MHz both graphs have a magnitude of -93 dB. The slope per decade in the frequency range of 1 MHz to 10 MHz is -69 dB for both graphs. The first resonance occurs for both graphs at around 57 MHz with -113 dB. At 202 MHz both graphs have a magnitude of -104 dB. At 820 MHz both graphs have a magnitude of -60 dB. Both graphs perform similar.

Figure 4.30: EMC Filter Measurement s_{21} π - R $1\text{ k}\Omega$ vs. s_{43} R $1\text{ k}\Omega$ - π .

4.3.6 Measurement logMag s_{21} - T - $1\text{ k}\Omega$, s_{43} - $1\text{ k}\Omega$ - T 100 kHz - 1 GHz

In Section 3.2.1, two different T filter structures were discussed. The impedance of these structures were measured with VNA and shown in Fig. 4.31. To the right, the schematics and component values are shown. The compared structures are T - R $1\text{ k}\Omega$ (brown) versus R $91\text{ k}\Omega$ - T (aquamarine). Points where the magnitude and frequencies are similar are marked blue.

The curves start at an offset of -21.4 dB. At 1 MHz both graphs have a magnitude of -30 dB. At 7.3 MHz both graphs have an anti-resonance of a magnitude of -59.2 dB. At 10 MHz both graphs have a magnitude of -65.5 dB. The first resonance occurs at 30 MHz with -107.4 dB for both graphs. A second resonance occurs at 57 MHz with -100 dB for both graphs. At 202 MHz both structures have a magnitude of -67.3 dB. At 404 MHz to 428 MHz the T structures start to deviate from each other slightly. At 428 MHz the R -

T structure has a magnitude of -53.8 dB. In a frequency range of 100 kHz to 428 MHz, both structures perform similarly. Beyond 428 MHz T - R structure outperforms the R - T structure mainly.

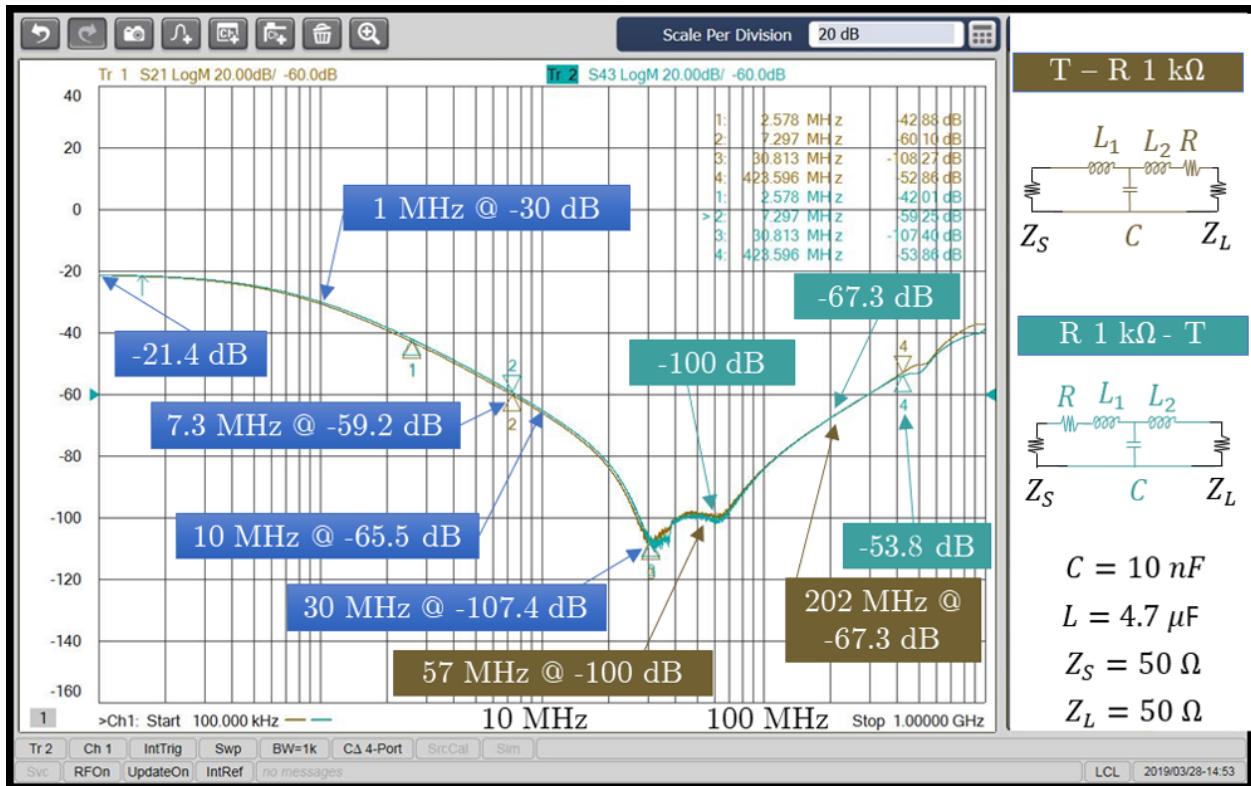


Figure 4.31: EMC filter measurement s_{21} T -R $1 \text{ k}\Omega$ vs. s_{43} R $1 \text{ k}\Omega$ - T.

4.3.7 Measurement logMag s_{21} - T - $1 \text{ k}\Omega$, s_{43} - $1 \text{ k}\Omega$ - CL 100 kHz - 1 GHz

In Section 3.2.1, the T filter structure, and LC Filter structure were discussed. The impedance of these structures were measured with VNA and shown in Fig. 4.32. To the right, the schematics and component values are shown. The compared structures are T - R $1 \text{ k}\Omega$ (brown) versus CL - R $1 \text{ k}\Omega$ (aquamarine). Points where the magnitude and frequencies are similar are marked blue.

The curves start at an offset of -21.4 dB. At 1 MHz both graphs have a magnitude of -30.5 dB. At 10 MHz the CL-R structure has a magnitude of -49 dB. At 10 MHz the T-R structure has a magnitude of -66 dB. The slope per decade in the frequency range of 1 MHz to

10 MHz is -18.5 dB for the CL-R structure, and -35.5 dB for the T - R structure. By subtracting slope CL-R of slope T-R, the deviation at 10 MHz is 17 dB. The first resonance for both structures occurs at 30.8 MHz with -107.4 dB for the T - R structure, and the magnitude for the CL - R structure is -84.7 dB. A second resonance for both structures occurs at 57 MHz with -99.7 dB for the T - R structure, and the magnitude for the CL - R structure is -82.8 dB. At 202 MHz the CL-R structure has a magnitude of -59.4 dB. At 202 MHz the T-R structure has a magnitude of -67.3 dB.

In a frequency range of 100 kHz to 1 MHz, both structures perform similarly. In a frequency range of 1 MHz to 700 MHz, the T - R structure outperforms the CL - R structure. In a frequency range of 700 MHz to 800 MHz Both structures perform the same. Beyond 800 MHz CL - R structure outperforms the T - R structure.

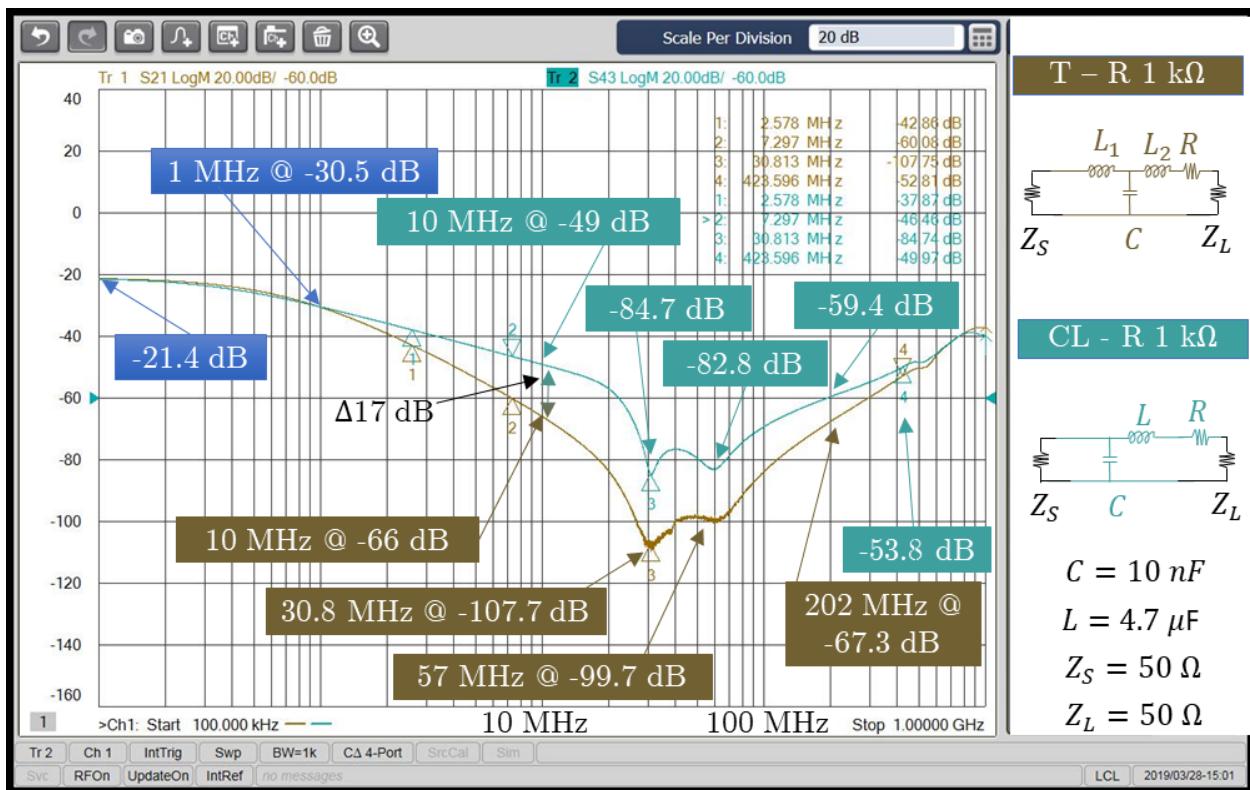


Figure 4.32: EMC filter measurement s_{21} T - R $1 \text{ k}\Omega$ vs. s_{43} CL - R $1 \text{ k}\Omega$.

4.4 SMPS EMI Suppression Techniques

The results regarding the measurements conducted with the Switched Mode Power Supply (SMPS) are presented in this section. First, time variant measurements are presented, which were used to design the snubber. Second, measurements are represented as discussed in the EMC Test plan in Section 3.3.4.

4.4.1 Snubber Transient Response

Two boards were used to perform the following shown measurements. Both boards were equally equipped and assembled at the same time.

The procedure requires to measure the high frequency ringing content which is part of the switching process of the bottom FET. Fig. 4.33 shows the measured transient response with an oscilloscope, MDO 3104. The light blue graph shows the transient response during switching. The dark blue graph shows the transient response during switching with an 100 pF capacitor added. The frequency of the high frequency ringing, marked with green arrow, is measured with the cursors for the case no C added. The frequency measured is f_r equal 892.9 MHz.

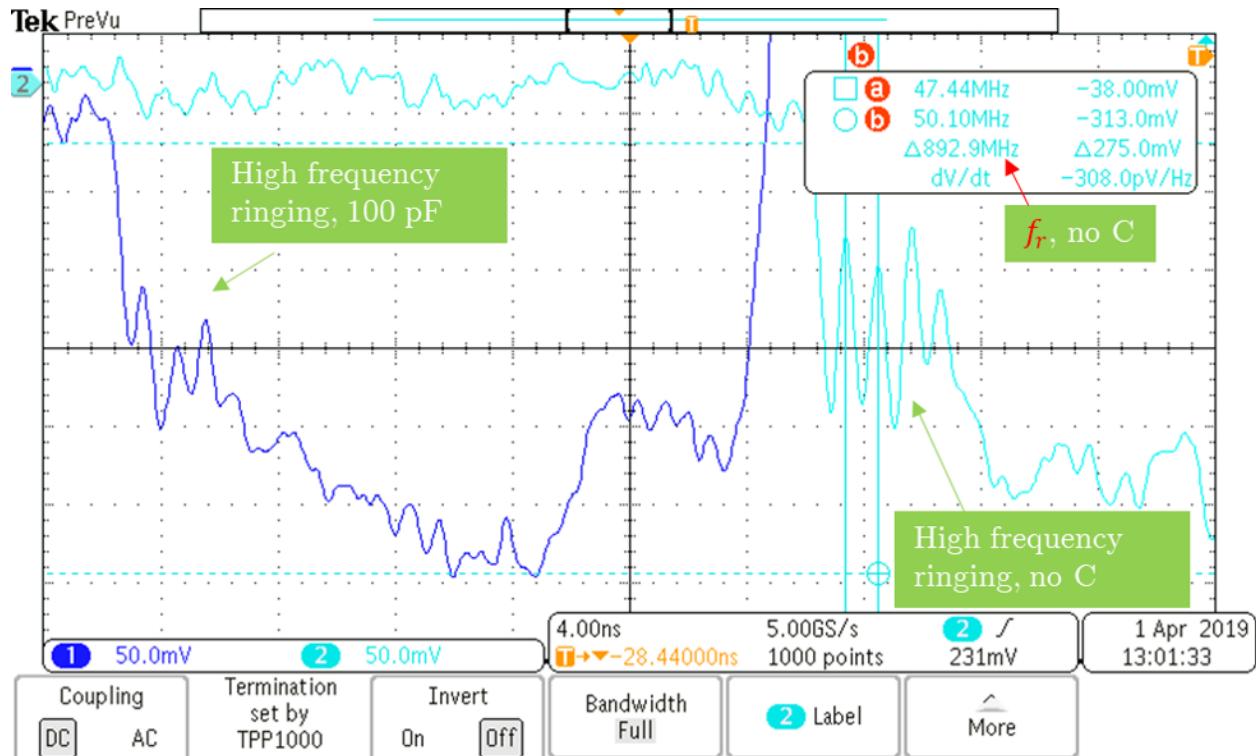


Figure 4.33: Transient response of a switch cycle of bottom FET.

To calculate the parasitic capacitance of the FET, the ringing frequency of the transient response is measured with a 100 pF capacitor added in parallel to the FET. Fig. 4.34 shows the transient response with 100 pF added. The dark blue line shows the response with a ringing frequency of f_r equal 833.3 MHz

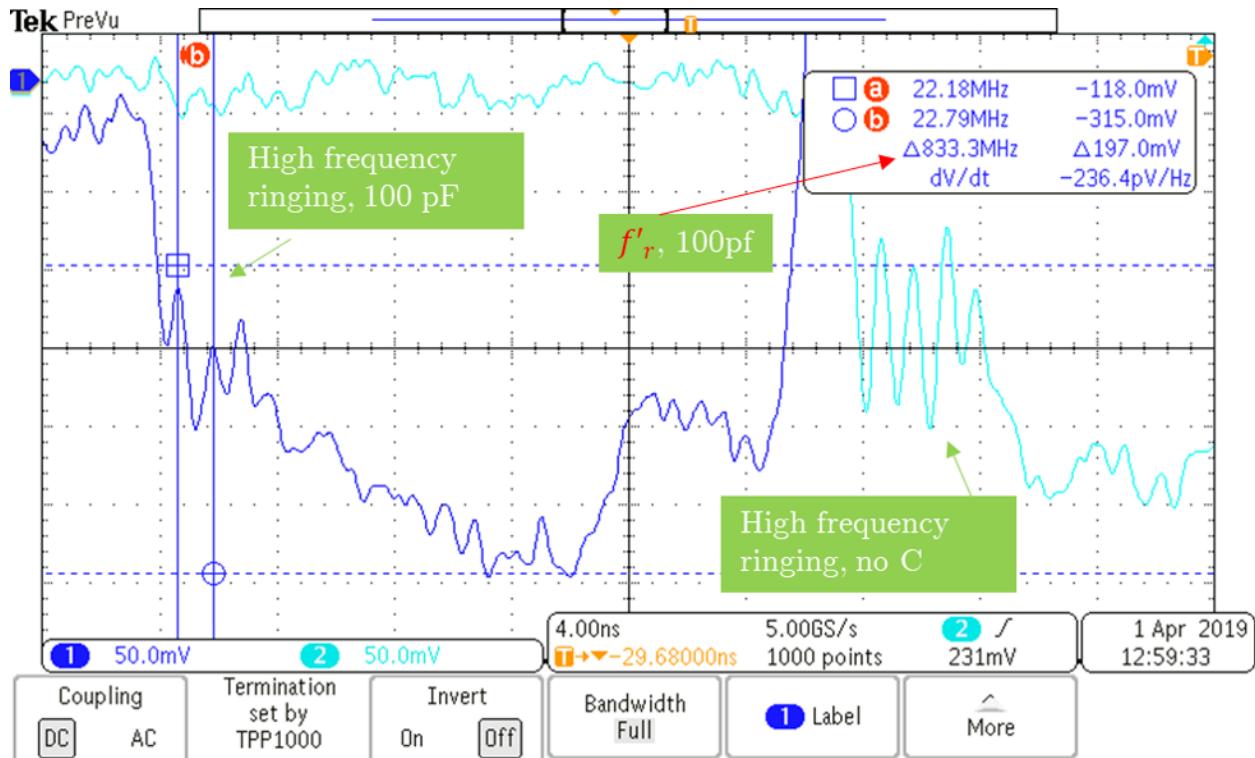


Figure 4.34: Transient response of a switch cycle of bottom FET with 100 pF capacitor added in parallel to drain and gate.

By using Eq. 3.2 the parasitic capacitance is calculated shown in Eq. 4.1 and results in 675.7 pF.

$$C_{ADD} = 100\text{pF}, C_{\sum \text{parasitics}} = \frac{C_{ADD}}{\left(\frac{f_r}{f_r}\right)^2 - 1} = \frac{100\text{pF}}{\left(\frac{892.9\text{MHz}}{833.3\text{MHz}}\right)^2 - 1} = \frac{100 * 10^{-12}}{0.148} = 675.7\text{pF} \quad (4.1)$$

Based on the parasitic capacitance the parasitic inductance can be calculated according to formula 3.3. The parasitic inductance is calculated in Eq. 4.1 and results in 47 pH.

$$L_{\sum \text{parasitics}} = \frac{1}{(C_{\sum \text{parasitics}})(2\pi f_r)^2} = \frac{1}{(675.7\text{pF})(2\pi 892.9\text{MHz})^2} = 47\text{pH} \quad (4.2)$$

Based on the parasitic inductance the estimated snubber capacitor minimum value can be calculated according to formula 3.4. The estimated snubber capacitor minimum value is calculated in Eq. 4.3 and results in 2048 pF.

$$C_{snubber\ minimum} = \frac{3}{(L_{\sum parasitics})(2\pi f_r)^2} = \frac{3}{(47pH)(2\pi 892.9mHz)^2} \quad (4.3)$$

Based on the parasitic capacitance and parasitic inductance the resistor needed can be calculated according to formula 3.5. The resistor value is calculated in Eq. 4.4 and results in 1.1884Ω .

$$R = \sqrt{\frac{L_{\sum parasitics}}{\left(\frac{C_{\sum parasitics}}{3}\right)}} = \sqrt{\frac{47pH}{\left(\frac{675.7pF}{3}\right)}} = 1.1884\Omega \quad (4.4)$$

To simplify calculations, a small MATLAB script was written, see Appendix C.1.

To evaluate the effect of the designed snubber, the snubber is placed on the board and measurements before placement and after placement are performed. The measurement without the snubber is shown in Fig. 4.35 where the high frequency content has an magnitude of 111 mV, as marked in red.

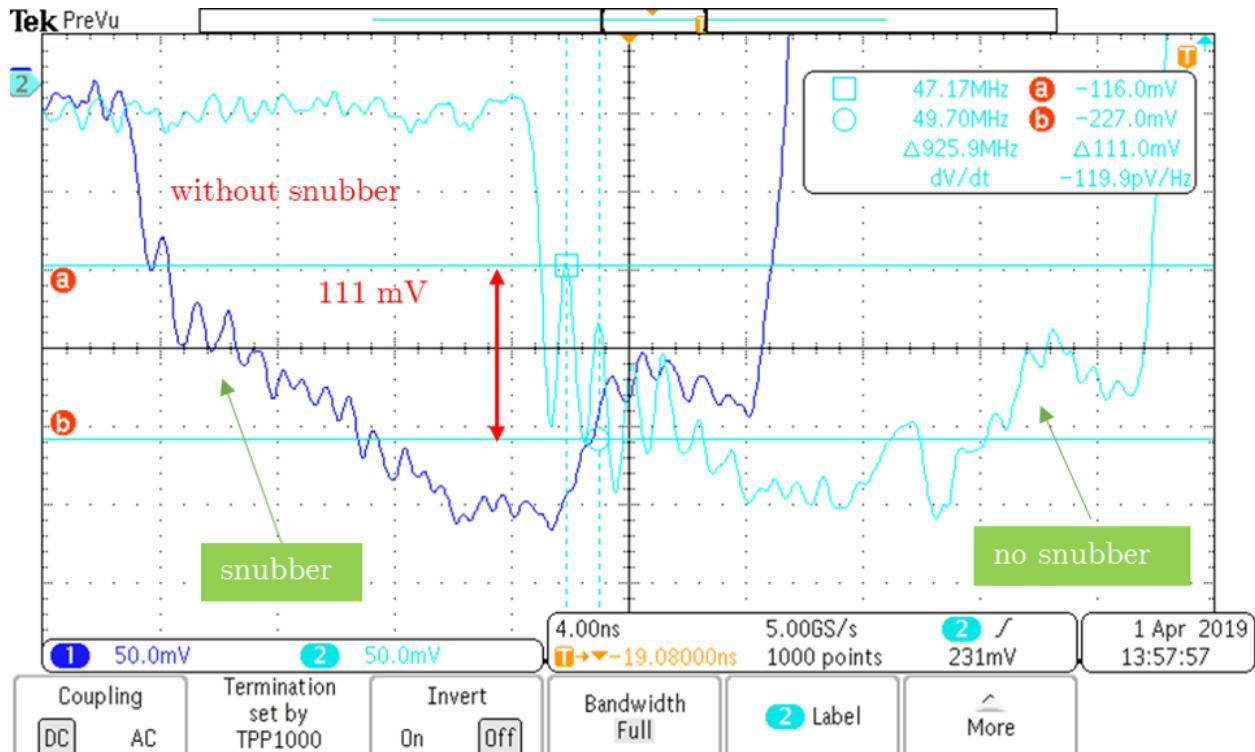


Figure 4.35: SMPS v2 transient response no snubber added.

The measured transient response with an equipped snubber is shown in Fig. 4.36. The measured magnitude of high frequency ringing has significantly decreased in amplitude to a value of 70 mV, marked in red.

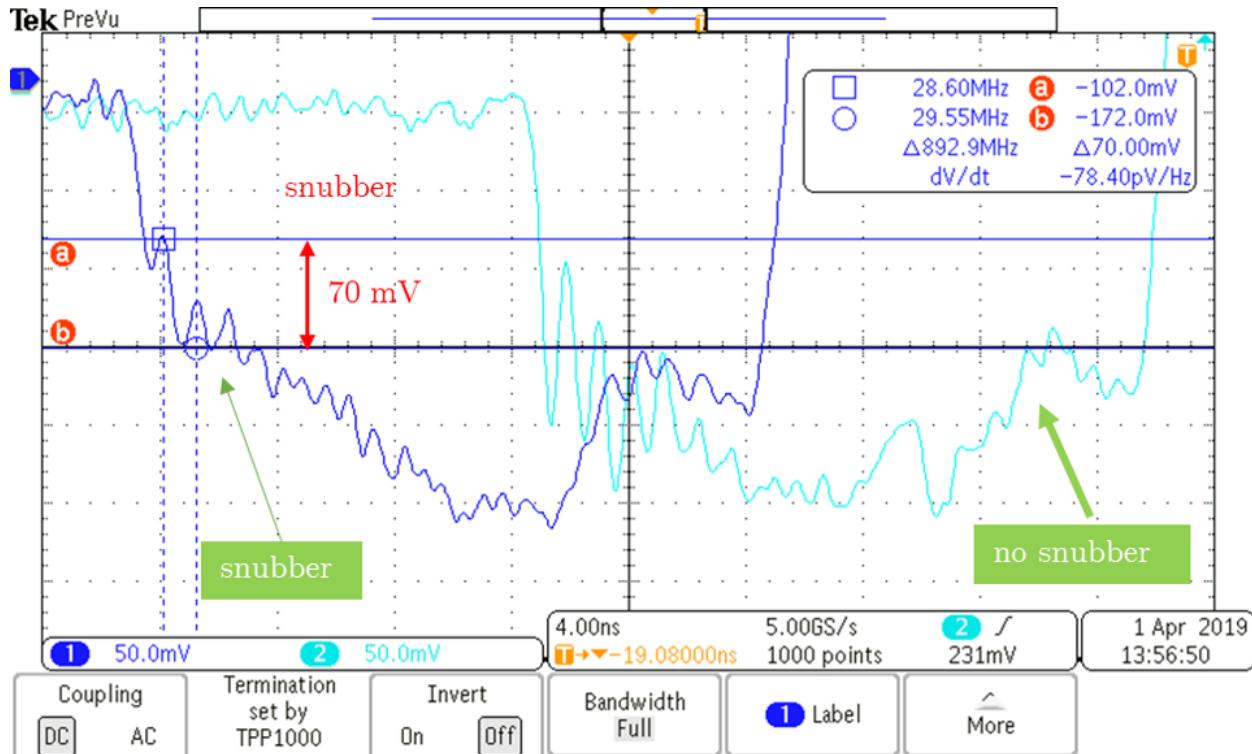


Figure 4.36: SMPS v2 transient response with snubber added.

4.4.2 Measured SMPSv3 Conducted Emissions Voltage Method

To evaluate the different suppression techniques for a Switched Mode Power Supply (SMPS) buck converter the measurement setup is shown in the Section 4.4.2 followed by the measurement results.

Measurement setup

The measurement setup was built as discussed in Section 3.3.4. The devices used for the tests are a Duracell Battery HP24DP 12V, Line Impedance Stabilization Network LI-325 5 μ H, R&S ESCI7 EMI Test Receiver, and DUT. Fig. 4.37 shows the side view of the measurement setup where the conducted metal sheet is connected to the chamber wall. The

12 V battery's negative pole is connected to the metal sheet and therefore grounded. LISN are connected to the metal sheet. Two LISN are used, one for the plus and one for negative pole. The cables and DUT are spaced 5 cm in height from the conductive metal sheet.

Battery line - Fig. 4.38a shows the top view for the battery line setup. The cables are routed over foam, 5 cm in height, and taped to the foam to prevent movement. The cables used are 30 cm long, the minimum length defined in CISPR 25 in Section 6 is 20 cm [29]. The RF cable is connected to the battery LISN and ends at the EMI receiver.

Ground line - Fig. 4.38b shows the top view for the ground measurements. The setup is basically equal to the battery line ones except that the RF cable is connected to the ground LISN while the battery LISN port is terminated with 50Ω load.

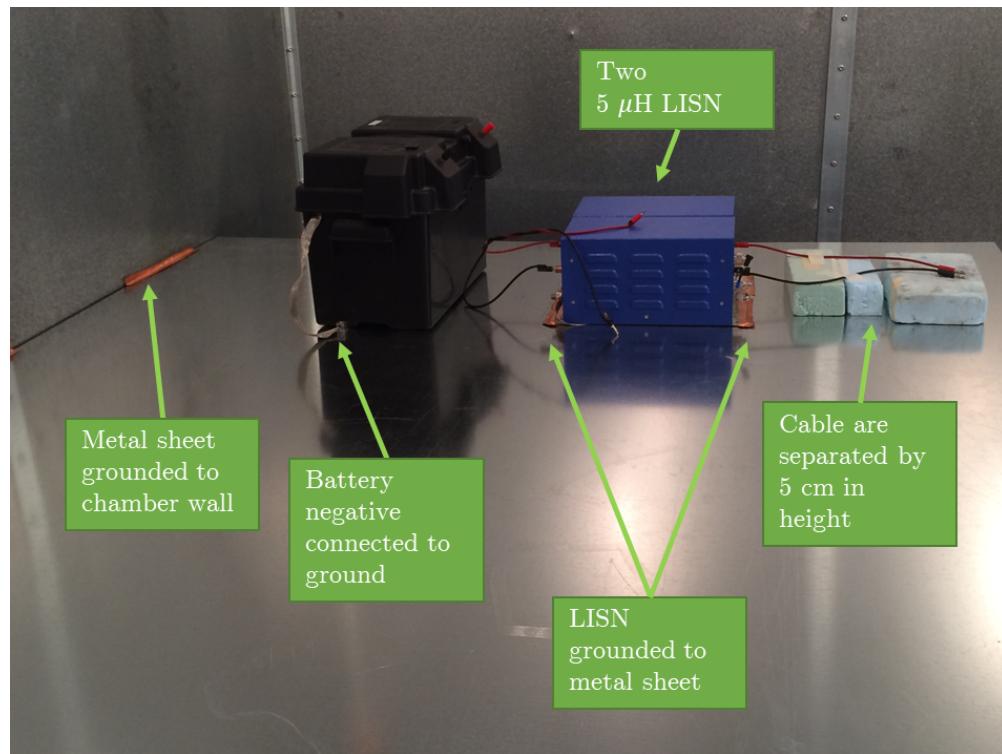


Figure 4.37: Conducted emission voltage method measurement setup side view.

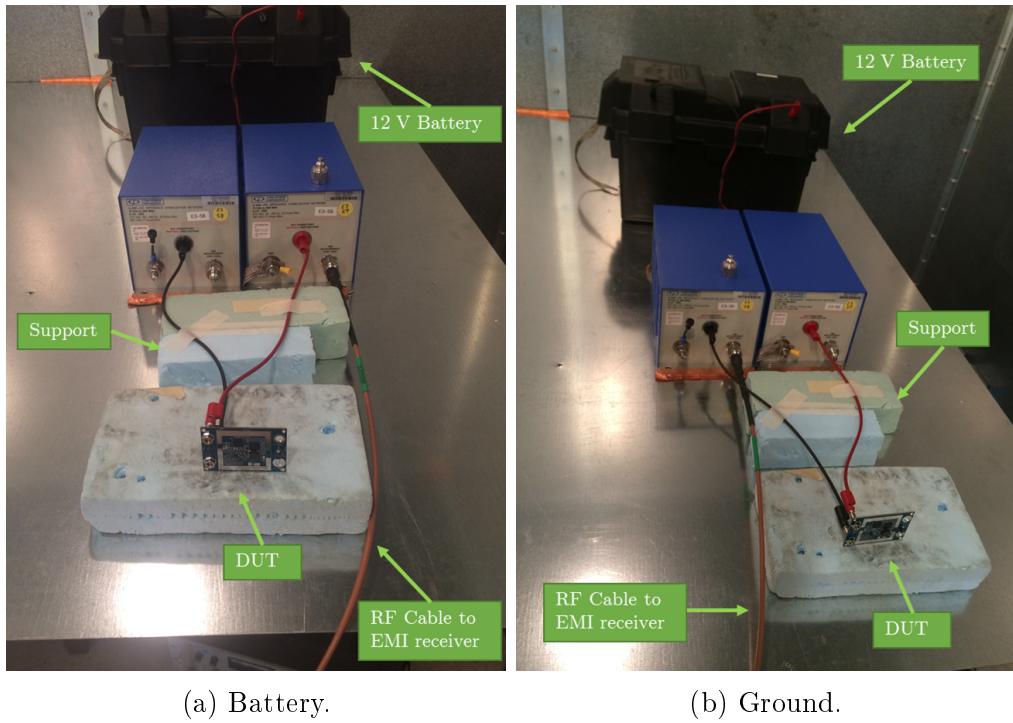


Figure 4.38: Conducted emission voltage method measurement setup top view.

Further pictures of the test setup are shown in Appendix C.4. Measured were two boards, board 3, and board 4. Board 3 is equipped with an Common Mode Choke (CMC). Board 4 has no additional parts other than the functional ones equipped. Fig. 4.39 shows board 4 with highlighted footprints where adjustments will be made as CMC L2 for board 3, snubber circuit C12 and R13, filter R1, R2, C3, C4, and C5, load 20, and shield.

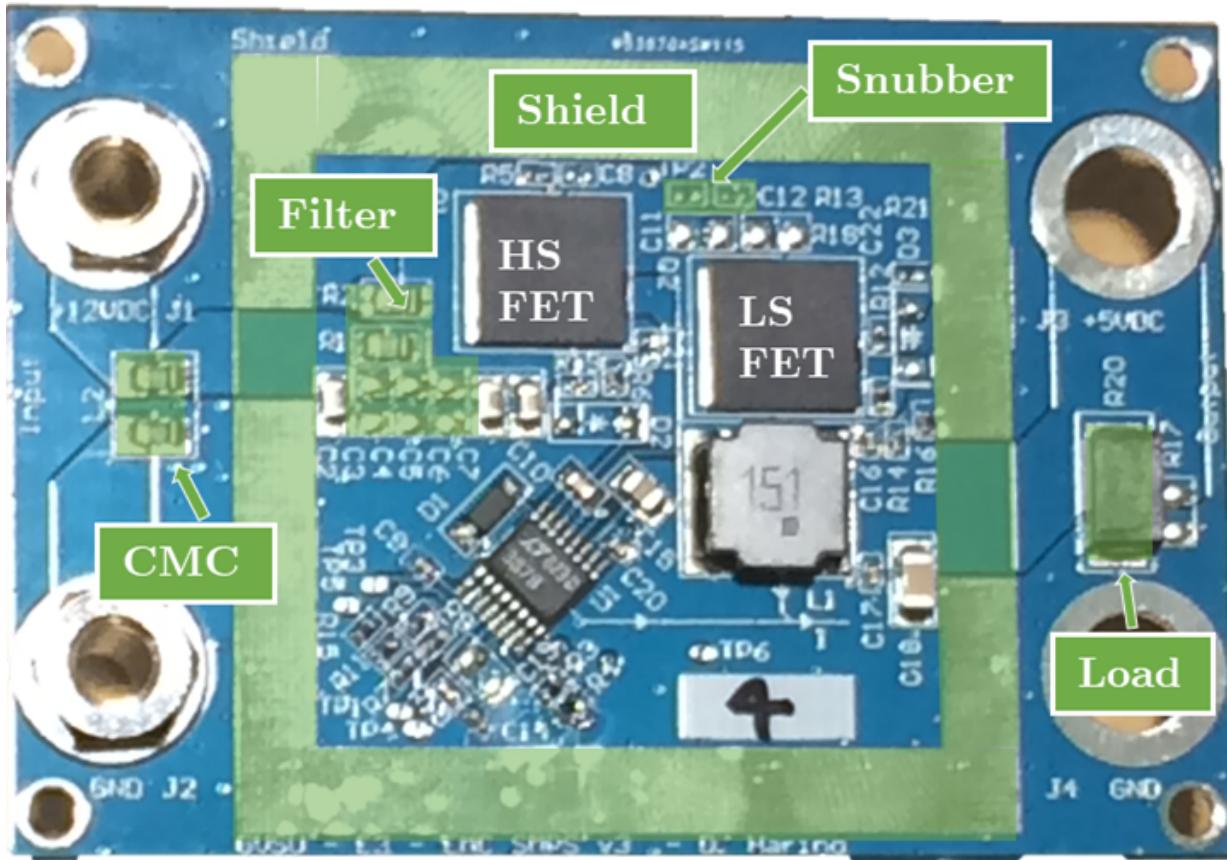


Figure 4.39: SMPS v3 board number 4 with highlighted footprints that illustrate the places where the board will be modified during measurement.

4.4.3 Measurement Results of Conducted Emissions Voltage Method SMPSv3

The results of the measured Conducted Emissions (CE) Voltage Method (V) are presented in this section. First, the ambient emissions are shown followed by the results an baseline, added snubber, filter, and shield.

Ambient

It is important to measure first the ambient environment of the chamber with power supply used to power the DUT so that eventual leakage or noise generated by any source can be detected and not mistakenly interpreted as an failure of the device. Fig. 4.40 shows the ambient emissions measured with the device under test not powered for battery line and

ground line. The ambient emissions are shown in all further plots. The graph can also be used to determine if your device is still working in case there is no other indicator.

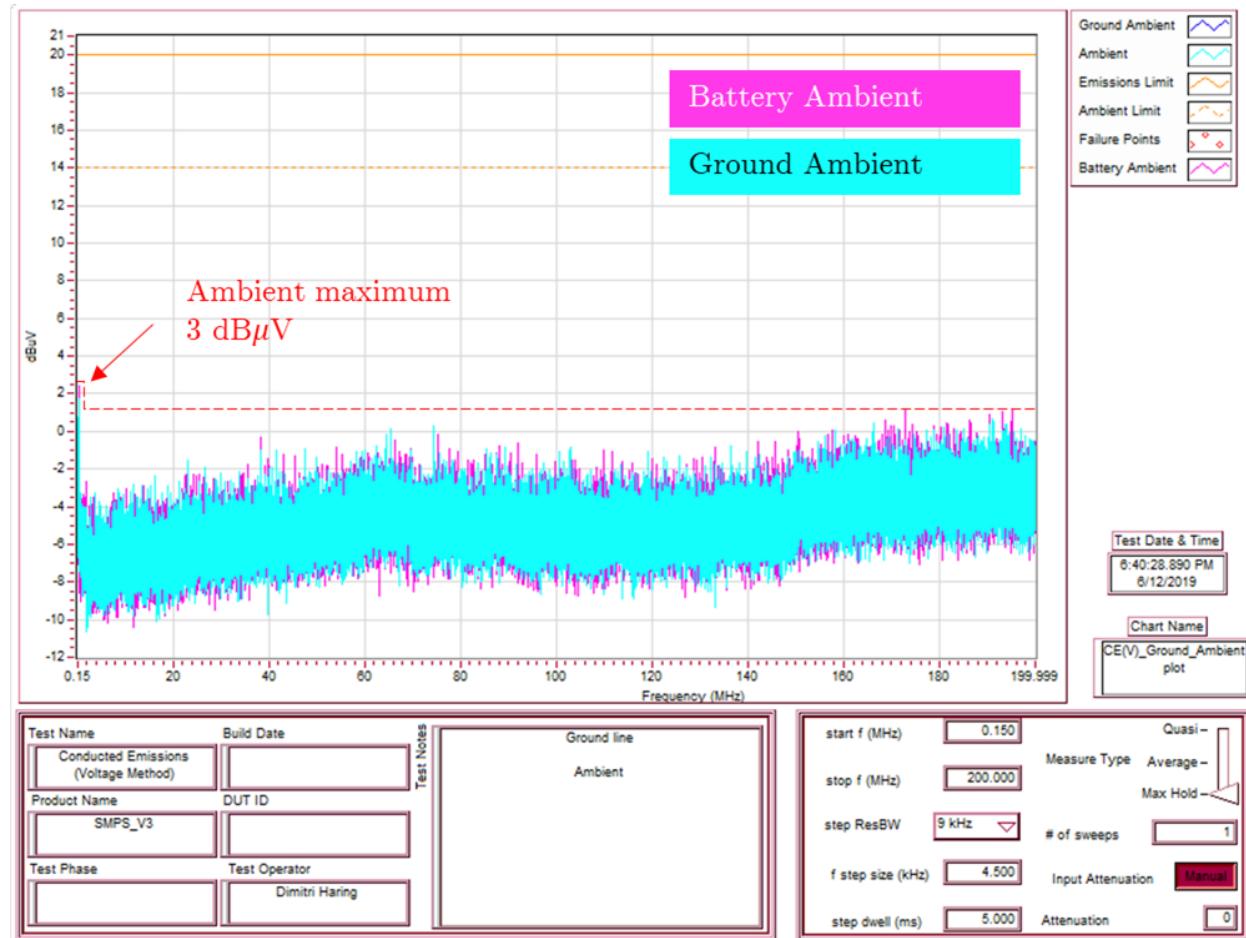


Figure 4.40: Conducted Emission (V) Ambient Battery and Ground.

Snubber vs. Baseline

Fig. 4.41 shows the battery line measurements of the baseline (orange) with no protective measurements versus the board with snubber equipped (blue). The ambient noise floor for the battery line is shown in light blue. The snubber values are 2200 pF for capacitance and 1 Ω for the resistor. The fundamental switching frequency at 415 kHz is unchanged. The 5th harmonic is increased by around +2 dB with snubber equipped. In a frequency range from 4 MHz to 10 MHz, the two graphs are slightly shifted in frequency by around 200 kHz. However, the magnitudes are much alike, and no remarkable change, which is

not related to the frequency shift can be seen. The orange baseline performs better for lower frequencies between the harmonics by around -11 dB marked with orange arrows in the 0.15 MHz to 10 MHz zoomed in scale. In a frequency range from 20 MHz up to 150 MHz the PCB with snubber shows increased performance by around -2 dB better than the PCB without the snubber. The equipped snubber causes a +2 dB spike at a frequency of around 142.3 MHz.

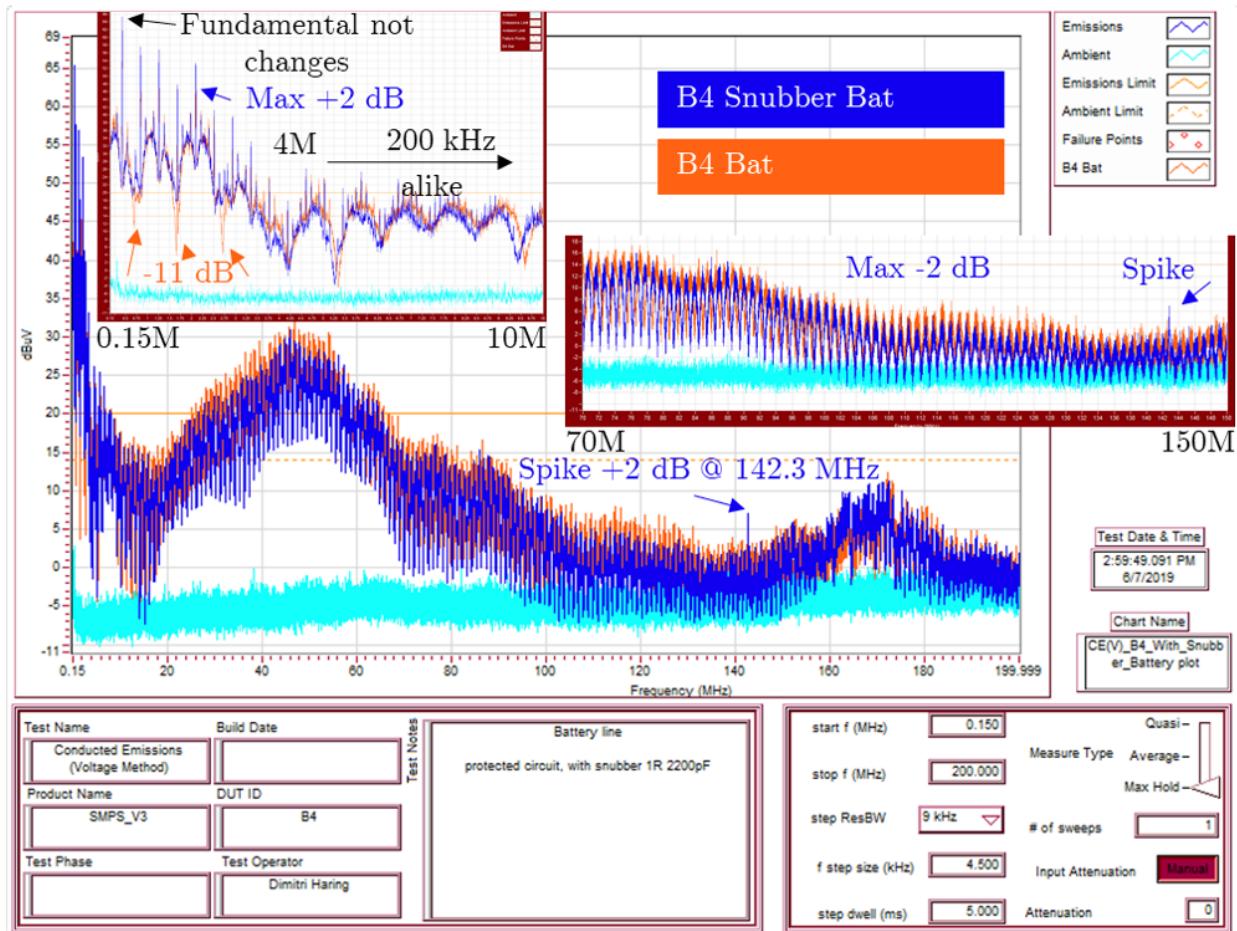


Figure 4.41: Conducted Emission (V) B4 battery line, baseline vs. snubber.

Filter 1st Order C

Fig. 4.42 shows the battery line measurements of the snubber equipped PCB (orange) versus the board with snubber equipped and a 1st order low pass filter (blue). The ambient noise floor for the battery line is shown in light blue. The snubber values are 2200 pF for

capacitance and $1\ \Omega$ for the resistor. The filter structure is C and the value populated is 6.4 nF . The fundamental switching frequency at 415 kHz is unchanged. The improvement in the frequency range of 0.15 MHz to 10 MHz is at maximum - 2 dB marked with blue arrows in the zoomed in range. In a frequency range from 4 MHz to 10 MHz , the two graphs are slightly shifted in frequency but compared to previous measurements the shift decreased significantly and can only be verified on the upper end at around 9.5 MHz . Besides the mentioned changes, the magnitudes are much alike, and no remarkable change, which is not related to the frequency shift can be seen. The orange graph, snubber without filter, performs better for lower frequencies between the harmonics by around -2 dB , marked with orange arrows in the 0.15 MHz to 5 MHz , and -1 dB in a range of 4 MHz up to 8 MHz , in the zoomed in scale. In a frequency range from 40 MHz up to 70 MHz the PCB with snubber shows increased performance by around $+2\text{ dB}$ better on the lower end and $+4\text{ dB}$ at the upper and in maximum than the PCB with snubber and filter. The equipped snubber caused spike of $+2\text{ dB}$ at a frequency of around 142.3 MHz has vanished. In a frequency range of 70 MHz up to 134 MHz the equipped capacitor decreased the magnitude by -8 dB .

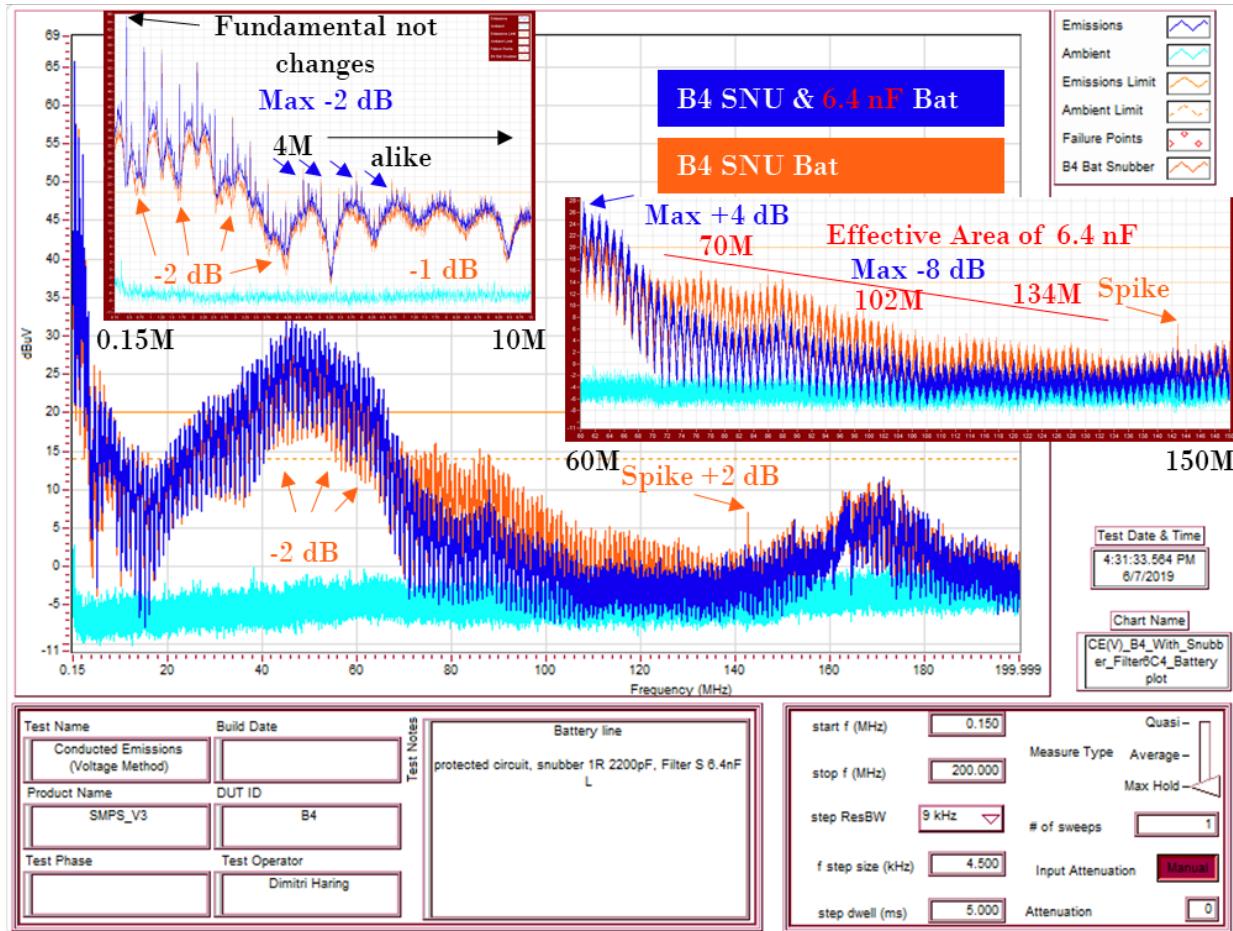


Figure 4.42: Conducted Emission (V) B4 battery line, snubber vs. snubber & filter 1st order - C - 6.4 nF.

Filter 2nd Order CL

Fig. 4.43 shows the battery line measurements of snubber and a 1st order low pass filter equipped PCB (orange) versus the board with snubber and 2nd order low pass filter (blue) equipped. The ambient noise floor for the battery line is shown in light blue. The snubber values are 2200 pF for capacitance and 1 Ω for the resistor. The filter structure 1st order is C and the value populated is 6.4 nF. The filter structure 2nd order is CL and the values populated are 6.4 nF, and 22 μH. The fundamental switching frequency at 415 kHz is attenuated by 36 dB. The 2nd harmonic is attenuated by 44 dB. The 3rd harmonic is attenuated by 38 dB. The 5th harmonic is attenuated by 50 dB. The 4th, 6th, 7th, and 8th

harmonic is significantly attenuated as well. In a frequency range from 4 MHz to 10 MHz, the frequency is shifted, which cases at some frequencies an improvement of up to 8 dB. In a frequency range of 10 MHz to 110 MHz the improvement is up to a maximum of 22 dB. In a frequency range of 110 MHz up to 160 MHz the magnitudes are alike. In a frequency range of 160 MHz to 200 mHz a slight improvement of a maximum of 2 dB can be seen. Furthermore, the spike seen at a frequency of 142 MHz without filter caused by adding a snubber is still suppressed.

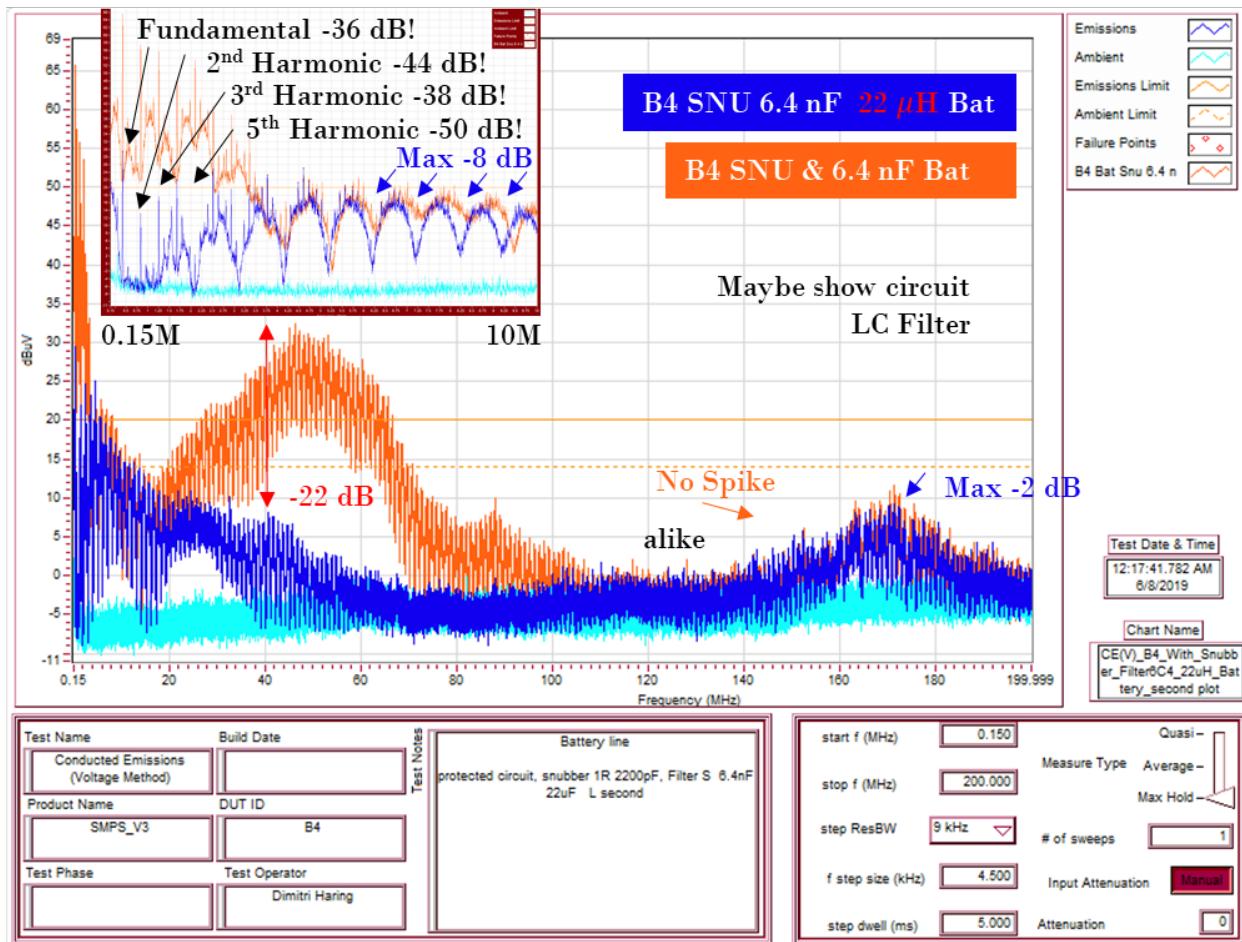
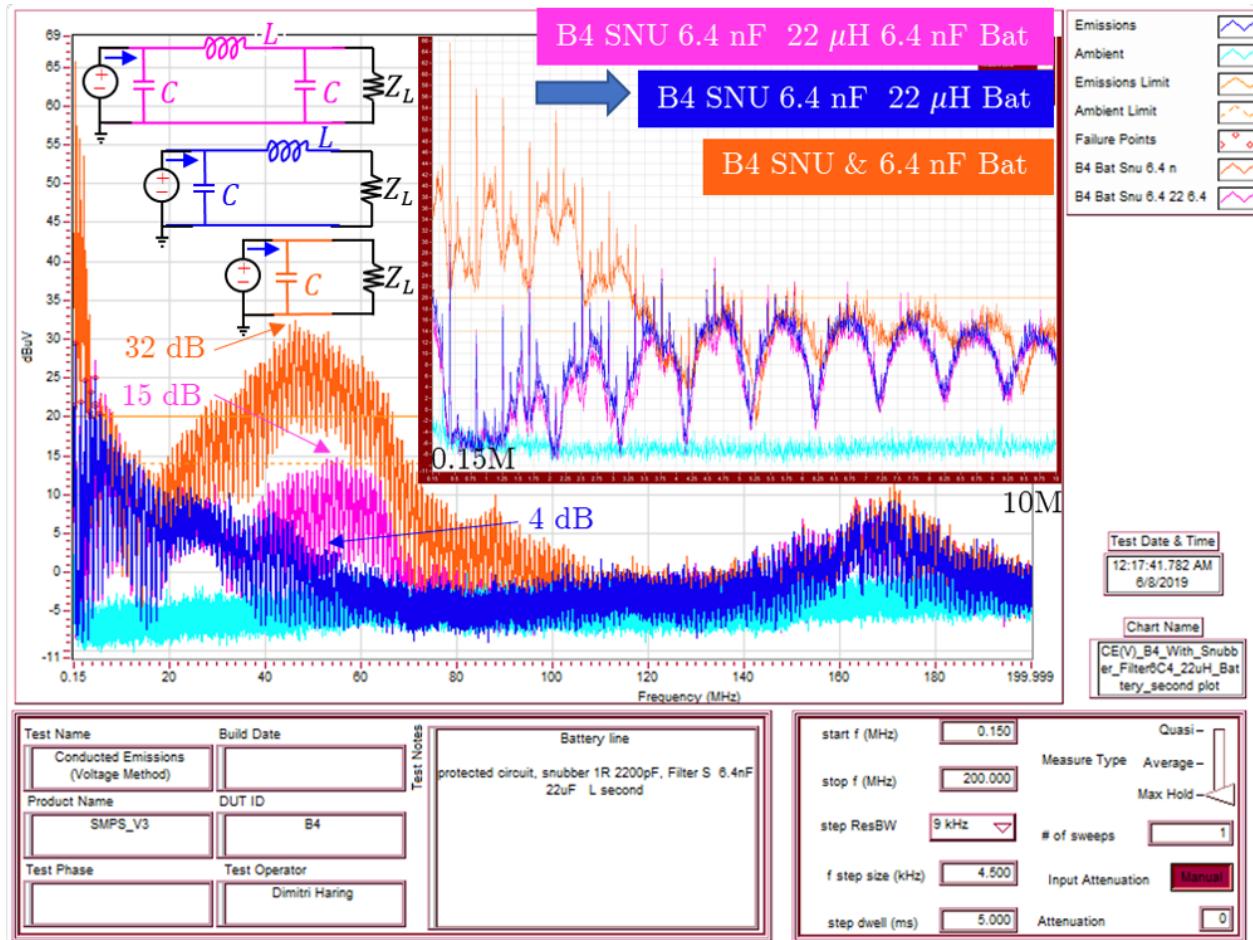


Figure 4.43: Conducted Emission (V) B4 battery line, snubber & filter 1st order - C - 6.4 nF vs. snubber & filter 2nd order - CL - 6.4 nF 22 μ H.

Filter Compression 1st to 3rd Order

Fig. 4.44 shows the battery line measurements of snubber and three different filter structures in comparison. The first structure is C with a 1st order low pass filter (orange) equipped PCB versus the board with 2nd order low pass filter (blue) and the board with 3rd order low pass filter (magenta) equipped. The ambient noise floor for the battery line is shown in light blue. The snubber values are 2200 pF for capacitance and 1 Ω for the resistor. The filter structure 1st order is C and the value populated is 6.4 nF. The filter structure 2nd order is CL and the values populated are 6.4 nF, and 22 μH. To the upper left the three filter structures with corresponding source and load are shown. In a frequency range of 0.15 MHz to 10 MHz it can be seen that the 2nd and 3rd order filter structures show similar behavior magnitude and frequency vise.

A remarkable change can be seen in the comparison between the 2nd and 3rd order filter structures where it was originally assumed that the 3rd order filter structure will outperform the 2nd order structure in a frequency range of 40 MHz to 60 MHz, the CL filter outperforms the PI filter by about 11 dB. The 1st order filter is at the same frequency range up to 32 dB. All three filters are measured with snubber.

Figure 4.44: Conducted Emission (V) B4 battery line, filter compression 1st to 3rd order.

Filter Comparison Target Frequency Fundamental

This measurement will deviate from the purposed test plan in Section 3.3.4. As the previous measurements show by looking at the resonant frequency of single components, specific target frequencies can be selected and suppressed. This works to the extent until frequency shifts in higher harmonics occur, which will invert previous suppression effects in different frequency ranges. The so far tested and purposed filter mainly suppressed the higher frequency spectrum but the fundamental is still strong. The following modifications were specifically done to target the fundamental frequency. Appendix E.3 shows a table where capacitors from the same series are listed with their impedance curve and self resonant frequency. Out of the table it can be seen that high capacitance is needed to suppress

the fundamental therefore $10 \mu\text{F}$ capacitors were used to enhance filter structures. Fig. 4.45 shows the fundamental of three filter structures in a frequency range of 0.15 MHz up to 0.5 MHz. Compared is the previous used CL filter against enhanced higher order filter structures with $10 \mu\text{F}$ capacitance added or exchanged.

The filter structure 2nd order is CL and the values populated are 6.4 nF , and $22 \mu\text{H}$ (blue). The filter structure 4th order is CCLC and the values populated are $10 \mu\text{F}$, 6.4 nF , $22 \mu\text{H}$, and $10 \mu\text{F}$ (orange). The filter structure 3rd order is CLC and the values populated are $10 \mu\text{F}$, $22 \mu\text{H}$, and $10 \mu\text{F}$ (magenta).

By exchanging the 6.4 nF capacitors to $10 \mu\text{F}$ capacitors in the π filter structure the fundamental is suppressed by 9 dB. Unfortunately, this gain comes with a trade off at frequency range around 45 MHz where the filter suppresses less by around 5 dB.

By trying fixing the lost range around 45 MHz a capacitor of 6.4 nF was added which caused the loss of 3 dB suppression of the fundamental and the issue at 45 MHz was not resolved at all.

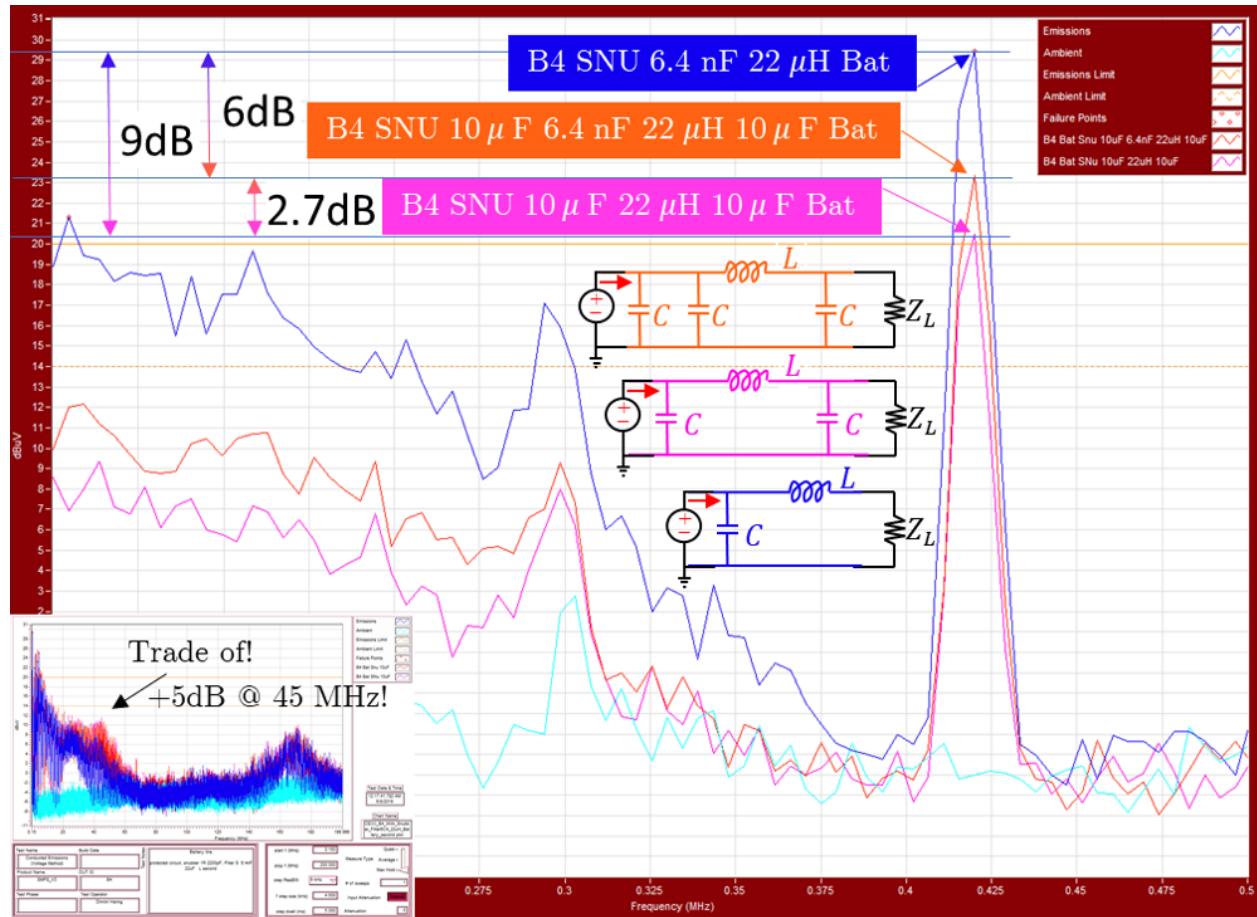


Figure 4.45: Conducted Emission (V) B4 battery line, filter compression with target frequency fundamental.

Shield

Realigning to the test plan, a shield was added. The shield was mounted with clamps, which were soldered at four places down to the ground plane. The clamps allow for the removal or exchange of the shield for test purpose.

Fig. 4.46 shows the measured board with the CL filter with 6.4 nF and $22 \mu\text{H}$ added (magenta) and the board with CL filter and a shield with no ventilation holes added (blue). The fundamentals in both cases have a similar magnitude. In a frequency range of 2 MHz up to 200 MHz the measured interference is down to the ambient floor. Fig. 4.47 shows the mounted shield with no ventilation holes on board 4 attached over cables to the LISN for the ground line measurement.

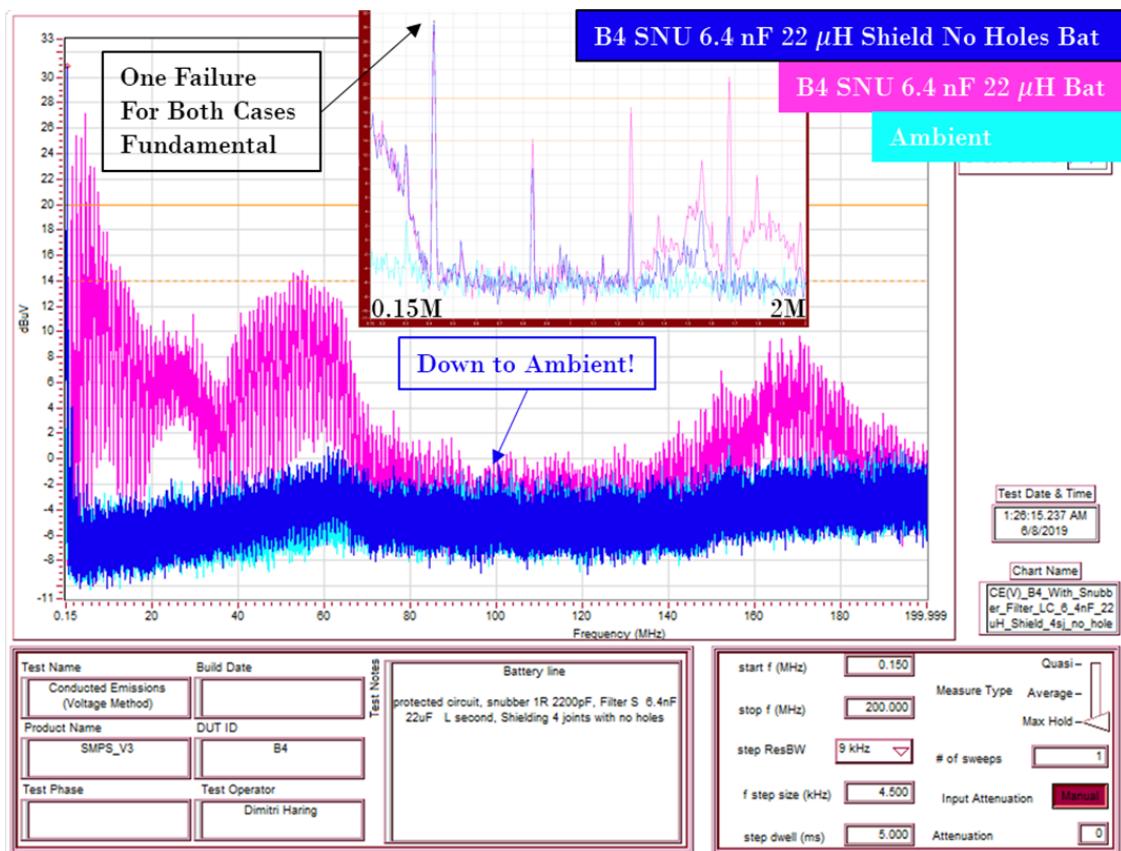


Figure 4.46: Conducted Emission (V) B4 battery line, comparison between board with no shield and with shield.

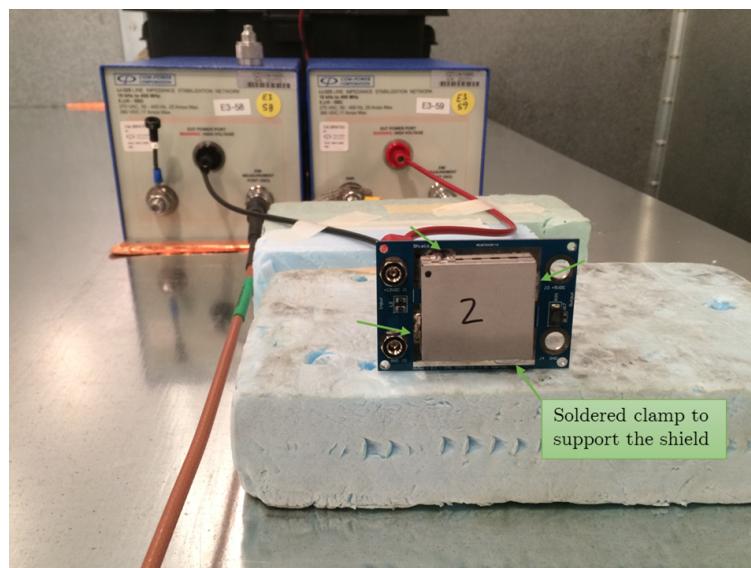


Figure 4.47: Image of the board with mounted shield with no ventilation holes.

4.4.4 Before and After

To show the overall change made between two different filter structures, both filter structures were improved by adding all the previous discussed modifications. The CL (blue) and the enhanced CCLC (green) structures were plotted along side the plot without protection (red). The red graph shows board four measured without protective measures or called the baseline. The blue graph shows the complete equipped board with an CL filter element with values of 6.4 nF and $22 \mu\text{H}$. The green graph shows the measured board with the enhanced filters structure with two $10 \mu\text{F}$ capacitors added. The green one is mainly there to show that often trade offs have to be made in terms of suppression and frequency range. Fig. 4.48 shows that the maximum over all attenuation of the fundamental is 42 dB with snubber, the enhanced filter structure, and shield with holes added. However, it comes with the trade off and loss of 16 dB in suppression in between a frequency range of 40 MHz to 60 MHz. By comparing the second case where the board was equipped with a filter of CL structure the fundamental is suppressed by 35 dB. The difference in terms of fundamental suppression is 7 dB between the two options. And it comes with an trade off of 16 dB at another frequency range.

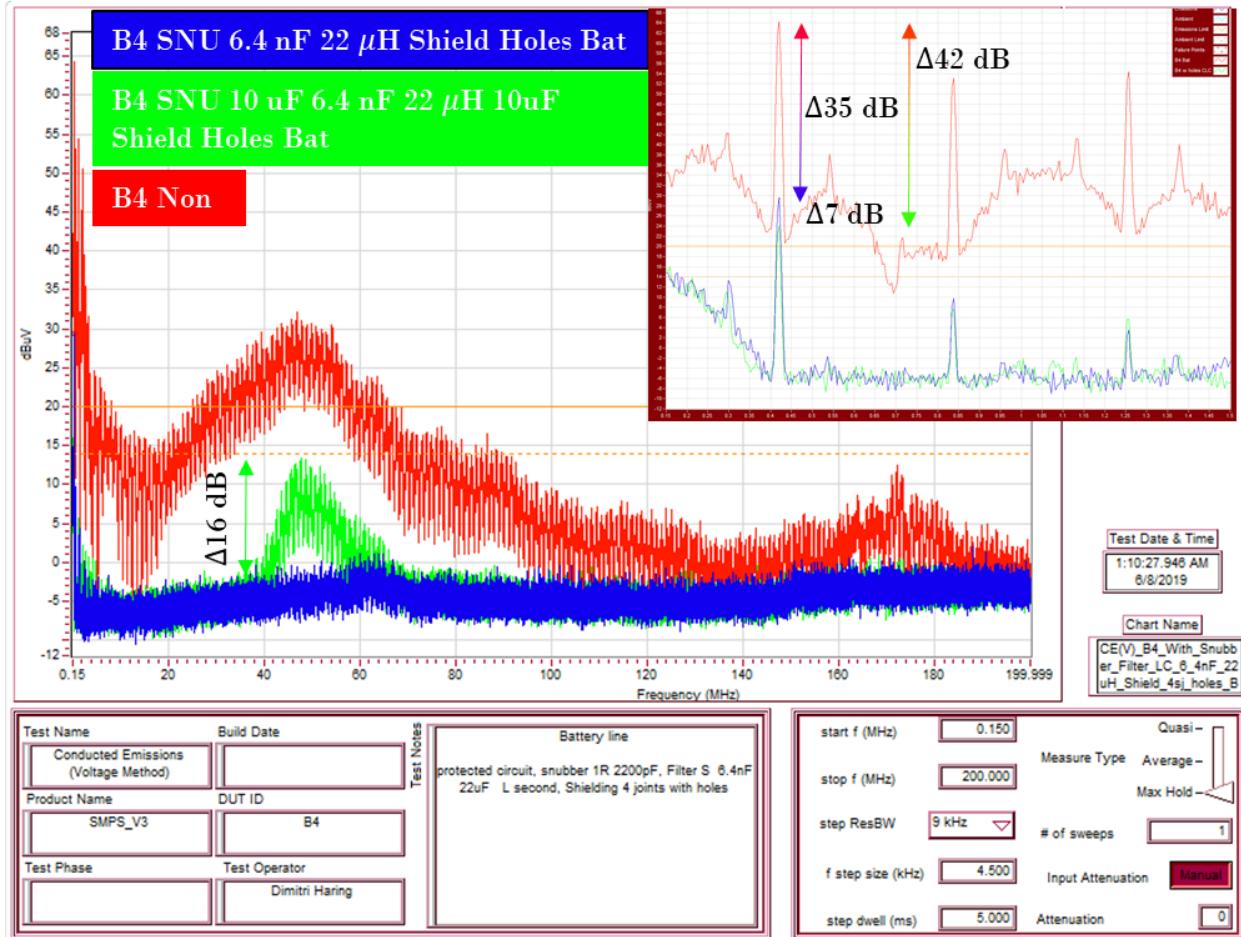


Figure 4.48: Conducted Emission (V) B4 battery line, comparison with no measures vs. board with CL filter and shield vs. board with enhanced filter and shield.

4.4.5 Further Measurements not Presented

More measurements were conducted but not presented. All measurements shown were also performed with ground line. All measurements presented in addition performed with a second PCB which had a CMC mounted. In comparison between battery and ground line the same effects could be observed at similar frequencies. The effect might have slightly differed in magnitude. No comparison should be made between ground and battery line. In terms of CMC, measurements showed only slight differences between the addition of a common mode choke and not having one populated. However, overall the CMC did not perform as well as without CMC, in magnitude this is about 2 to 4 dB in certain fre-

quency ranges, shown in Fig. 4.49. The main difference is around 90 MHz to 130 MHz where the board with CMC shows an increased magnitude of around +4 dB. On the contrary the board without CMC shows a 4 dB increase of emissions in a frequency range of 160 MHz to 180 MHz.

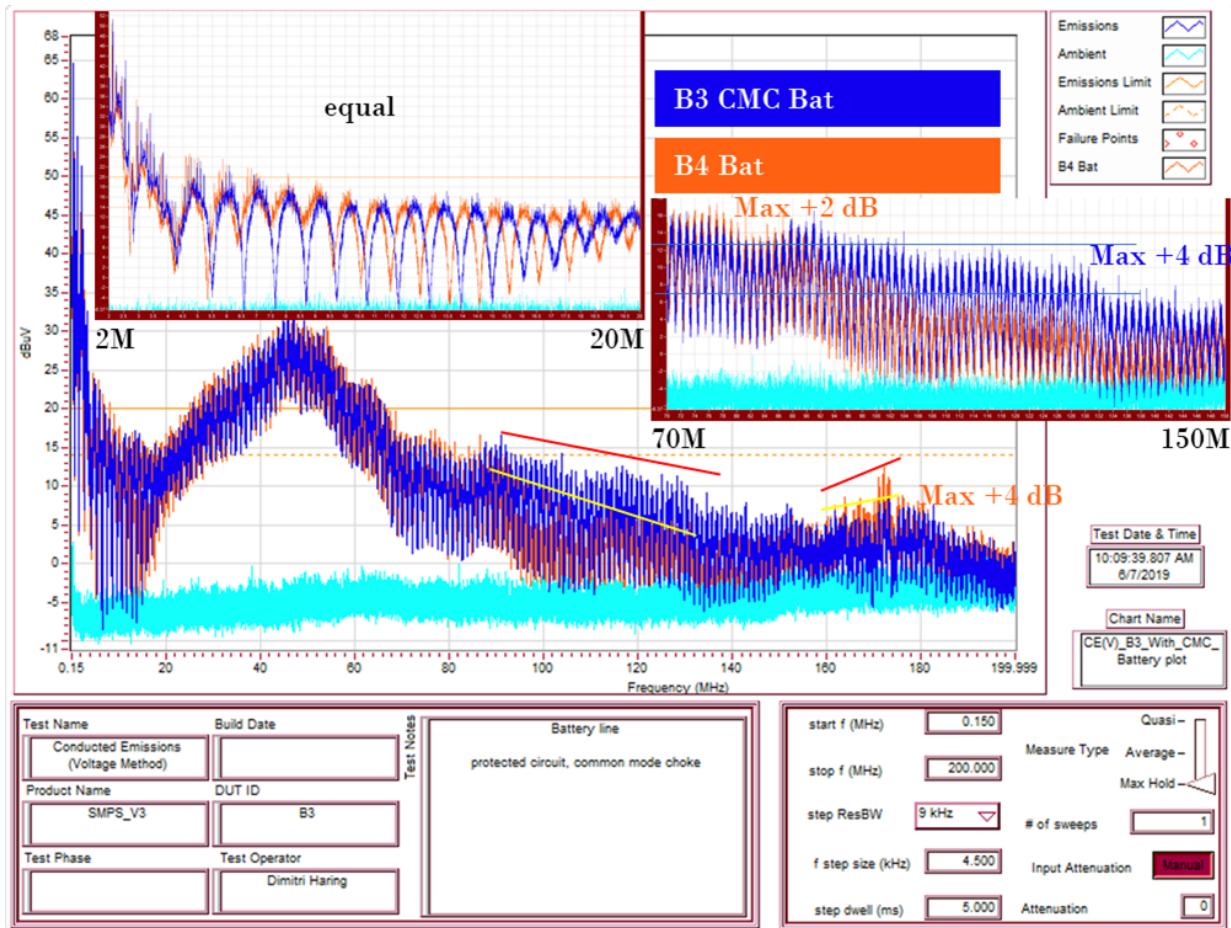


Figure 4.49: Conducted Emission (V) B4 battery line baseline vs. B3 battery with CMC baseline.

Here only the Conducted Emmissions (CE) Voltage Method (V) is measured and presented. In reality there would also be measurements with current method, this method allows the differentiation of Differential Mode (DM) and Common Mode (CM) current. In addition, Radiated Emmissions (RE) tests would be performed. The measurements presented here took over two shifts where one shift is defined as 8 hours in time. Current method and RE requires a different setup where the wire harness is laid out in the length

and type as expected to be used in the system or product.

Chapter - 5 VHF Auto Tuner Applied EMC in Design

5.1 Introduction

To demonstrate the importance of the evaluated topics an example application of a VHF auto tuner is presented. The VHF auto tuner was developed up to a running functional prototype, but many EMC concepts haven't been implemented yet. The hardware design of the tuner was done in three months. To establish defined tests which are reproducible a good understanding of the PCBs circuitry is necessary. Therefore, the different design aspects regarding hardware are discussed and explained step by step. The goal is to use the previous gained knowledge to use as countermeasures or to improve existing well established measurements which aid the Electromagnetic Interference (EMI) suppression and hence increase the RF immunity performance. For future EMC tests, it is important to make a list that contains all test cases which shall be tested. As aid to come up with a list the sections of the RTCA/DO-160G can be used as reference [30]. Based on this list an analysis of eventual failures and their countermeasures is conducted.

5.2 System Design

Auto tuners secure a reasonable power transfer from a radio to an antenna system. To allow a radio to operate on different frequencies, a fixed matching circuit might not be enough to ensure a broad band match. This leads to multiple possible variations on how to solve the issue. One, design a hardware circuit that will match in any case. This sounds great but it is hard to realize. Second, build a system that measures the Standing Wave Ratio (SWR) and use an algorithm to minimize the SWR. Fig. 5.1, shows the system overview of a radio and an antenna with an auto tuner in between.

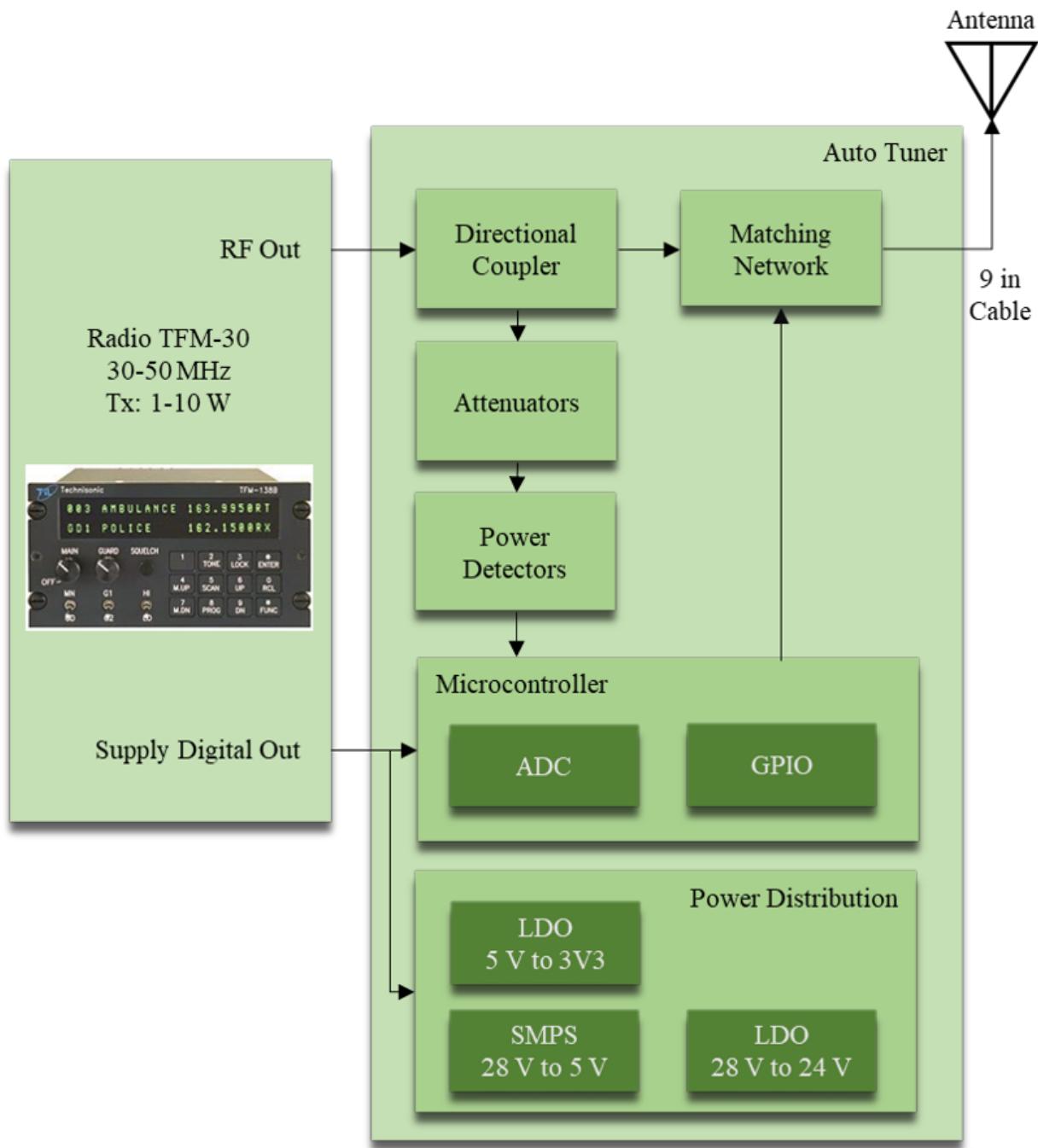


Figure 5.1: VHF auto tuner block diagram.

5.3 EMC Aspects of Design

Each of the following sections will discuss applied EMC techniques on the case of the VHF auto tuner. The discussed techniques are based on the gathered information of the previous chapters and thoughts made based on the existing standards.

5.3.1 Embedded Capacitance

Following recommendations for the VHF auto tuner design based on the previous work done are stated with respect to the embedded capacitance of a PCB. Fig. 5.2 shows the VHF auto tuner board with suggested measures to improve Electromagnetic Compatibility (EMC). The labels are described from right side top clockwise. A solid ground plane on layer two is required and is used in the design. The used stack-up is a 4-layer, which was chosen at the time because thought to functionality did not suggest that a higher order stack-up would provide benefits. However, as seen in the measured results of Section 4.1, an increased layer stack provides increased impedance stability. This can be evaluated on the prototype, whereas example simple conducted measurements can be made to see if the desired specifications can be met. The ground island that is built by the capacitors could be avoided by turning the capacitors into the opposite direction so that supply voltage (V_{DD}) and analog supply voltage (V_{DDA}) are parallel routed to each other, if possible. The power (PWR) routing should be performed in a layer, not in a plane, with empty spots and outer edges filled with ground (GND). Closely couple and power planes are recommended; however, in a 4-layer design not realistic to achieve. It might be desirable to place an additional footprint form trace to the ground, which allows to electrically terminate a long trace, in this case, digital. However, keep in mind that not high capacitance can be added; signal integrity and functionality has still to be provided. Most likely, the gate capacitance does the job already, which is usually somewhere around nano to picofarad. The PCB is essentially a waveguide and should be treated as such. Via stitching

is used to build a fence around the board and to improve impedance stability in-between ground planes. Remember, by parallel resistors; the resistance is smaller or equal, then the smallest resistor of the circuit. It is not directly embedded capacitance but kind of related to it. Place, decoupling capacitors close to the V_{DD} pin of the μ C, IC. As shown by the measured transient response in Section 4.2, grouped or not grouped decoupling capacitors make a difference. The fundamental goal is to achieve a stable supply voltage by decoupling the voltage from the current. Measurements showed that the used SMPS needs more capacitance to provide stable results, it is advisable in a prototype stage to provide a sufficient number of footprints to account for enough decoupling, bulk, filtering, and EMI suppression capacitors (1st order filter to target single frequency not covered or not suppressed enough by EMC/EMI filter or CMC). The switched mode power supply has two voltage inputs on each side, both sides need a decoupling capacitor. To protect the input for unwanted transient, an RF short is placed in the form of a small capacitor for each input line. To enhance further protection, a simple voltage divider with high resistance is used to adjust to level shift the input voltage and provide current limitation.

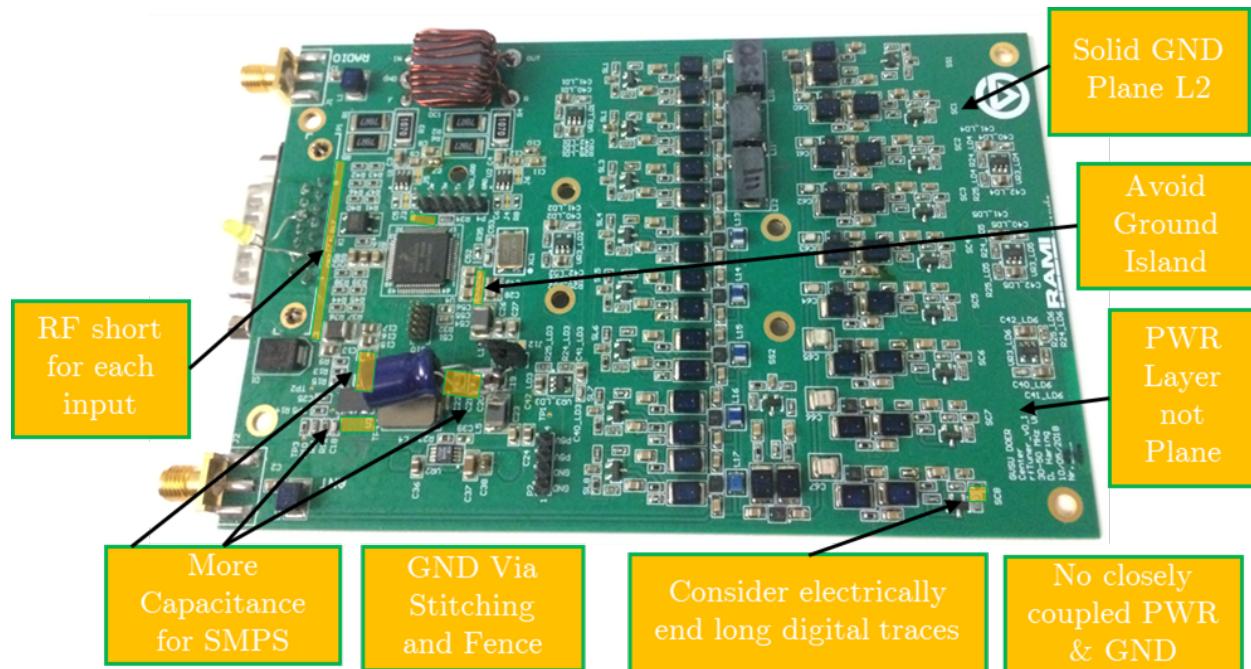


Figure 5.2: Embedded capacitance consideration applied on the VHF auto tuner design.

5.3.2 EMC / EMI Filter

Following recommendations for the VHF auto tuner design based on the previous work done are stated with respect to EMC / EMI filter. Fig. 5.3 shows the VHF auto tuner board with suggested measures to improve Electromagnetic Compatibility (EMC). The labels are described from right side top clockwise. An EMI filter with π structure is used for the analog supply voltage (V_{DDA}). The filter is designed for wide band frequency suppression with two different capacitor values on each side of the ferrite bead. The capacitor values are $0.1 \mu\text{F}$, and $1 \mu\text{F}$. The ferrite bead provides 100Ω impedance at 100 MHz. The output of the SMPS is equipped with an EMI filter with π structure. The filter is designed for wide band frequency suppression with two different capacitor values on each side of the ferrite bead. The capacitor values are $0.1 \mu\text{F}$, and $1 \mu\text{F}$. The ferrite bead provides 100Ω impedance at 100 MHz. Recommended is to place on the input of the LDO an EMC filter with π structure. The filter is designed for lower band frequency suppression with one capacitor value on each side of the ferrite bead. The capacitor value is $4.7 \mu\text{F}$. The ferrite bead provides 100Ω impedance at 100 MHz. This might not be needed, but providing footprints may prevent an expensive redesign. The input of the SMPS is equipped with an EMC filter with π structure. The filter is designed for lower band frequency suppression with one capacitor value on each side of the ferrite bead. The capacitor value is $4.7 \mu\text{F}$. The ferrite bead provides 100Ω impedance at 100 MHz.

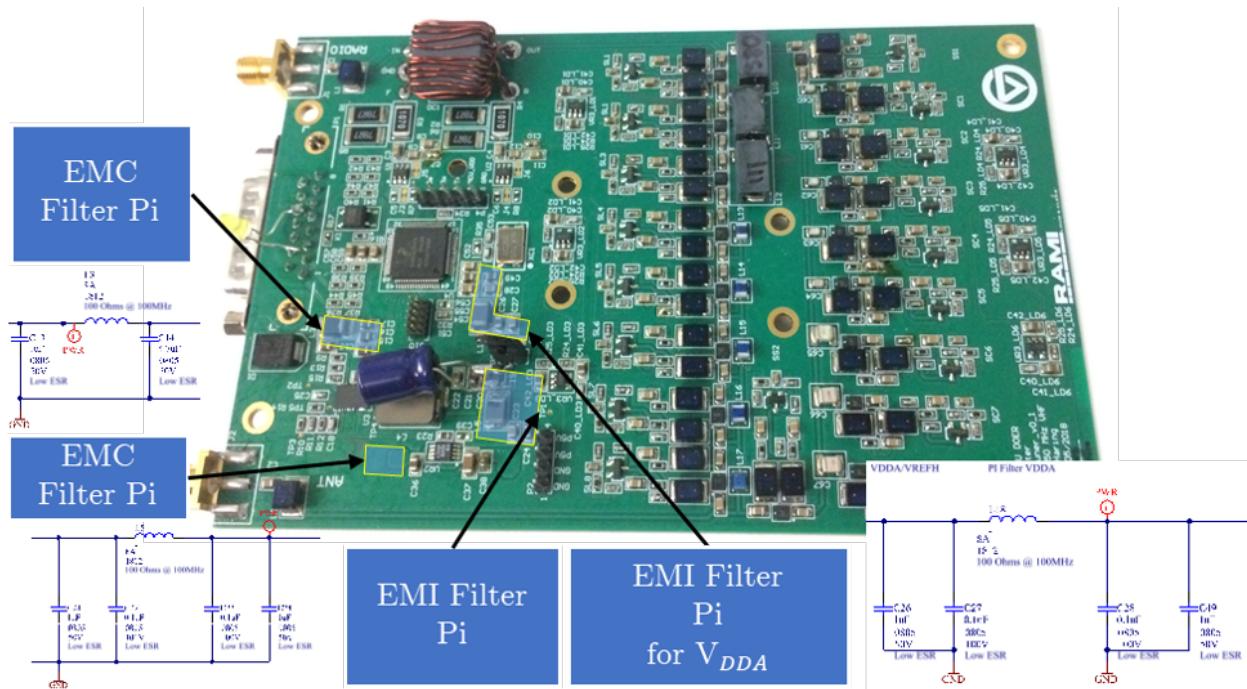


Figure 5.3: EMC / EMI filter consideration applied on the VHF auto tuner design.

5.3.3 SMPS EMI Suppression Techniques

Following recommendations for the VHF auto tuner design based on the previous work done are stated with respect to SMPS EMI suppression techniques. Fig. 5.4 shows the VHF auto tuner board with suggested measures to improve Electromagnetic Compatibility (EMC). The labels are described from right side top clockwise. To optimize the rise time, a gate series resistor should be placed. This might not be applicable because it will increase the time to switch states of the FET. For the LDO bulk capacitors should be used as input and output. It is never wrong to place a footprint for a small capacitor to the ground which would provide an RF return path for high-frequency signal content in case the trace length is substantial. This is usually also provided by using closely coupled ground and power planes with wide trace width in the power layer which might make a discrete component obsolete. A snubber is used to minimize ringing of the FET. The snubber placed on the existing design was designed with LTspice simulations. Recommended is to perform the optimization according to Section 3.3.1. It is always recom-

mended to measure this kind of stuff on the workbench before entering an EMC laboratory if a high-frequency oscilloscope is available. Rf short to shorten high-frequency current path close as possible to the coil. Take attention to the coils marking, which indicates where the wiring starts of the used coil. The inner wire should be placed at the switched node side. The outer layers of the wire wrapped coil to act as additional shielding and can be reasonably assumed to suppress radiated emissions. The coil placement should also be taken with care to provide a controlled current return path. If possible, try to protect the feedback (FB) trace as good as possible. It is like an analog signal, Radio Frequency (RF) immunity wise. If the trace is long for whatever reason, think about low pass filtering or at least provide footprints for a low-pass filter. In Fig. 5.4 the SMPS Quad Flat No-leads (QFN) 32-pin package with integrated FET is shown. The used SMPS from Texas Instruments Incorporated (TI) is optimized for low noise performance. Notice, the flat package size and small in width and length. The maximum current is 8 A. the small package size provides short current return paths which allow minimizing parasitic. The minimal height is favorable for two reasons, once for vibrations, and not acting as an antenna or stub. In terms of soldering it is desirable to read the following application note "AN1902 Assembly guidelines for QFN (quad flat no-lead) and SON (small outline no-lead)" from NXP [31]. Keep in mind that a bad solder joint will increase impedance significantly and should be avoided by all means. A Common Mode Choke (CMC) is recommended at the main supply path. The common mode choke will electrically isolate the device from other subsystems by providing a high impedance for occurring common mode current as learned in Section 2.1. Keep in mind that a high impedance also will reflect RF content and provide a high SWR. The reason I mention that is that the traces or better regions/polygons (terminology of Altium Designer) is acting as a dipole antenna, which will cause radiated emissions, shown in Fig. 5.5. The recommendation is to bury them if the current used allows it in terms of thermal and impedance issues. Reverse bias protection will avoid damage in case reverse polarity is applied to the voltage supply pins. All inputs are electrically

terminated with an RF short shunt capacitor. The capacitors should be as close as possibly placed to the input pin. It will help to short any high-frequency transients, such as Electrostatic Discharge (ESD).

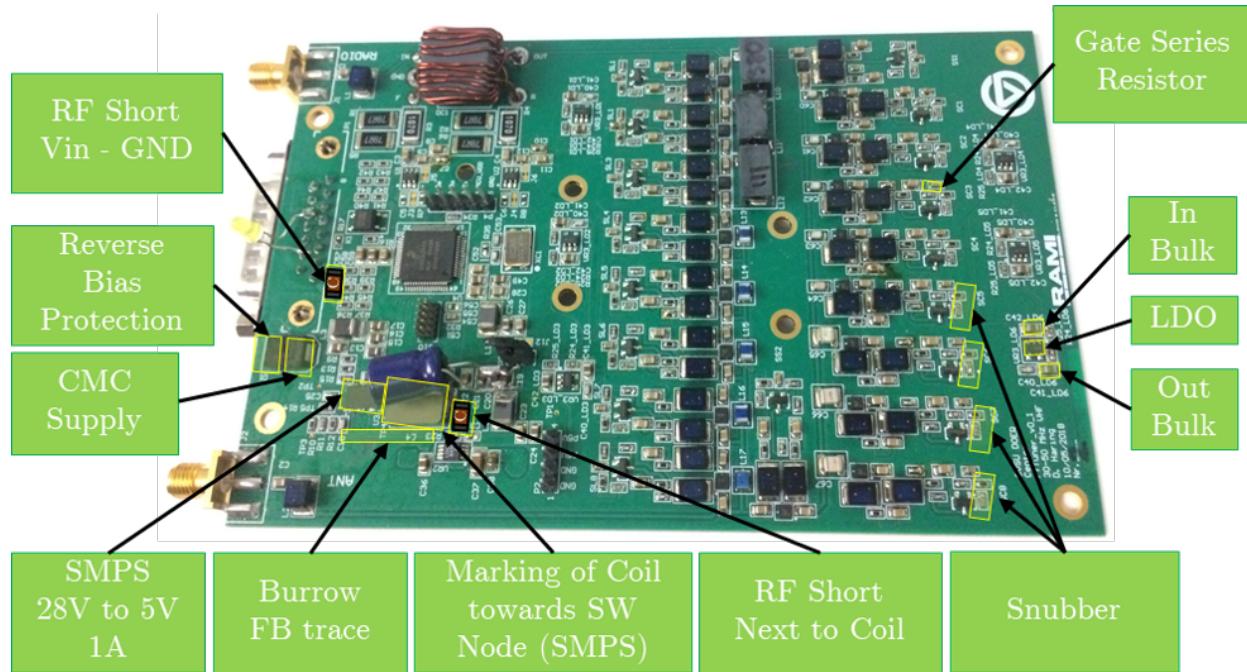


Figure 5.4: SMPS EMI suppression consideration applied on the VHF auto tuner design.

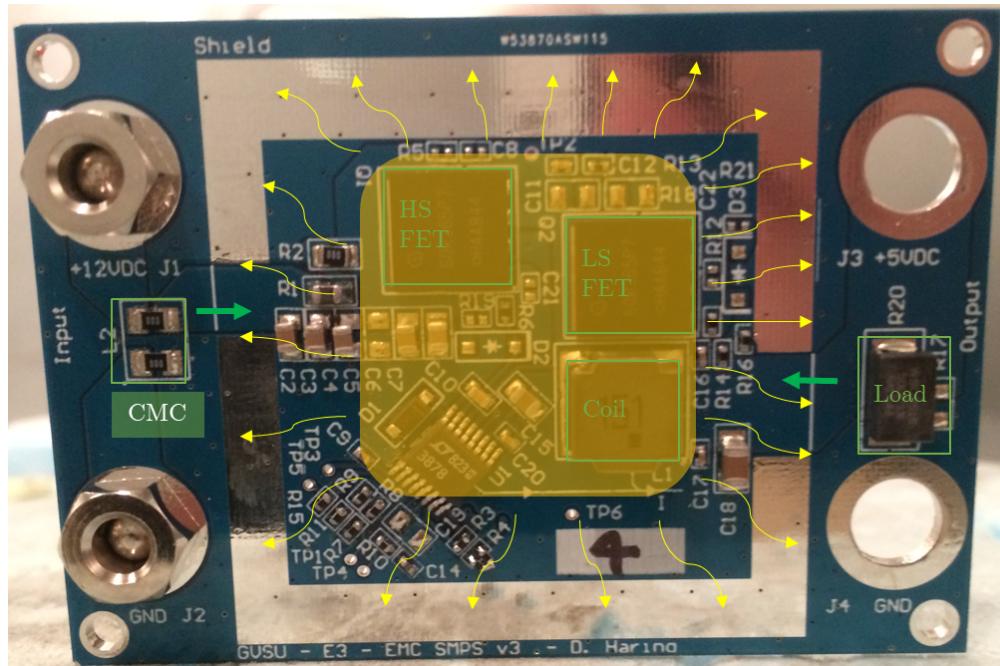


Figure 5.5: SMPS EMI suppression consideration applied on the VHF auto tuner design, CMC high impedance.

5.3.4 Ratio of EMC Related to Functional Components

By superposition of the different cases presented previously it becomes quite obvious that an increased number of components is used to suppress EMI or decoupling alternating current (AC) from DC voltage. The BOM was used to get a rough estimate of the prototype's components which can be related to EMC. It shows that approximately half of the components are somewhat related to enhance EMC. In addition, further components will be added to the design for extra EMC enhancements.

Chapter - 6 Discussions & Conclusion

6.1 Embedded Capacitance of a PCB

This section discusses the results gathered with measurements to embedded capacitance of the presented PCB. The results of the input impedance measurements are discussed. The results of the insertion loss measurements are discussed. Further differentiated discussion and thoughts are presented.

6.1.1 Input Impedance

Comparison between the Three Different Layer Stacks Results with Regards to Input Impedance

The measured results of the input impedance s_{11} shows that by comparison of all three stack-ups that the 6-layer board with closely spaced power and ground plane, and a far spaced power plane outperforms the 4-layer and the 6-layer version 3. The 6-layer stack outperforms the 6-layer version 3 stack slightly. However, the biggest difference can be seen between the 6-layer stacks (not defined version) and the 4-layer stack which shows that if increased noise reduction is required a six layer design should be favored. Tab. 6.1 to Tab. 6.3 summarizes the most important measurement results.

Comparison between Not Grouped and Grouped Results with Regards to Input Impedance

The Section 4.1.2 presents the results for the not grouped case, while Section 4.1.2 presents the results for the grouped case of all three layer stack-ups. The main difference can be seen in impedance magnitude at the first and second anti- resonant frequency where the grouped case outperforms the not grouped case. This can be explained by the placement of the capacitors if the measurement would have been performed at connector J2 the result would be vise versa. The measurements for J2 have been performed but are not shown in

the thesis.

The shift of frequency between the grouped and not grouped capacitors can be explained by examining the plot of the three layer stack-ups and no capacitors placed, presented in Section 4.1. The first resonant frequency is shifted by several MHz depending on the stack-up, this shift is caused by the embedded capacitance value. As for normal capacitors the lower the resonant frequency, the higher the capacitance value, shown for normal capacitors in Tab. E.1. This results in the assumption that the 6-layer board has the highest embedded capacitance for lower frequencies up to 142 MHz. Beyond this point the highest capacitance depends on the resonant frequencies occurring in the structure are either the 6-layer board or the 6-layer version 3 board.

4-Layer for No, Not Grouped, and Grouped Capacitors

Table 6.1: Comparison of embedded capacitance for 4-Layer (L4) for No, Not Grouped, and Grouped Capacitors input impedance measurements.

Stack-up	100 kHz	1 MHz	10 MHz	1 st Resonance	2 nd Resonance	2 nd Anti-Resonance
noC-L4	60.3 dB	40.49 dB	20.7 dB	-22.5 dB @ 225 MHz	6.57 dB @ 434 MHz	
notGroupedC-L4	18.9 dB	-0.93 dB	-24 dB	-36.8 dB @ 16 MHz	16.75 dB @ 188 MHz	4 dB @ 443 MHz
GroupedC-L4	18.9 dB	-1.05 dB	-24 dB	-35.4 dB @ 16 MHz	9.43 dB @ 180 MHz	4 dB @ 443 MHz

6-Layer for No, Not Grouped, and Grouped Capacitors

Table 6.2: Comparison of embedded capacitance for 6-Layer (L6) for No, Not Grouped, and Grouped Capacitors input impedance measurements.

Stack-up	100 kHz	1 MHz	10 MHz	1 st Resonance	2 nd Resonance	2 nd Anti-Resonance
noC-L6	46.9 dB	27.19 dB	7.46 dB	-25.84 dB @ 160 MHz	-4.6 dB @ 463 MHz	
notGroupedC-L6	18.5 dB	-1.3 dB	-24 dB	-35.02 dB @ 16 MHz	2.68 dB @ 97 MHz	-6 dB @ 463 MHz
GroupedC-L6	18.5 dB	-1.25 dB	-24 dB	-32.7 dB @ 18.8 MHz	0.4 dB @ 95 MHz	-6 dB @ 463 MHz

6-Layer Version 3 for No, Not Grouped, and Grouped Capacitors

Table 6.3: Comparison of embedded capacitance for 6-Layer Version 3 (v3) for No, Not Grouped, and Grouped Capacitors input impedance measurements.

Stack-up	100 kHz	1 MHz	10 MHz	1 st Resonance	2 nd Resonance	2 nd Anti-Resonance
noC-v3	57.7 dB	31.9 dB	12.11 dB	-34.4 dB @ 168 MHz	-0.33 dB @ 463 MHz	
notGroupedC-v3	18.4 dB	-1.4 dB	-23.52 dB	-41.4 dB @ 19.5 MHz	7.5 dB @ 129 MHz	-2.22 dB @ 463 MHz
GroupedC-v3	18.4 dB	-1.4 dB	-25.49 dB	-35.8 dB @ 15 MHz	2.76 dB @ 139 MHz	0.38 dB @ 463 MHz

6.1.2 Insertion Loss

The insertion loss usually shows the signal loss in communications. The insertion loss is generally defined as positive number. The reason why no positive numbers are used is that the VNA presents the transmission coefficient s_{21} parameter and presents it in algorithmic scale without taking the absolute value. Therefore, the lower the value the lower is the impedance. Hubing et al. [9] presents the analytical form which relates the transmission coefficient, the characteristic impedance and the board impedance to each other. Furthermore he states that the measured and calculated impedance based on the measured s_{11} is less accurate than the one measured with s_{21} . This assumes that port two is terminated with 50Ω . The main part of the boards impedance is mainly reactive, therefore s_{11} of a 50Ω will show a flat line, as shown in Fig. 6.1. However more accurate measurements with s_{11} can be made by terminating port two with an open. Hence, the measured results of transmission coefficient (insertion loss) presented in Section 4.1.3 and the measurements presented as input impedance in Section 4.1.2, cannot be directly correlated.

The gathered results are summarized in Tab. 6.4 to Tab. 6.9. The insertion loss measurements present a good resolution compared to the input impedance measurements especially at the higher frequency range. The term impedance stability, used for input impedance, cannot be confirmed here and should not be used. It is favorable to lead the discussion in terms of high or low impedance. The measurement with insertion loss shows the same trend as the measurements presented with input impedance. In general it can be stated that the 6-layer version 3 board with not-far spaced power plane outperforms the 4-layer board. The 6-layer board with far spaced power plane outperforms the 6-layer version 3 board with not-far spaced power plane. On all three boards grouped capacitors outperform not grouped capacitors. A board with capacitors equipped presents itself with lower impedance in the frequency range where the capacitors self-resonant frequency is compared to boards with no capacitors placed.

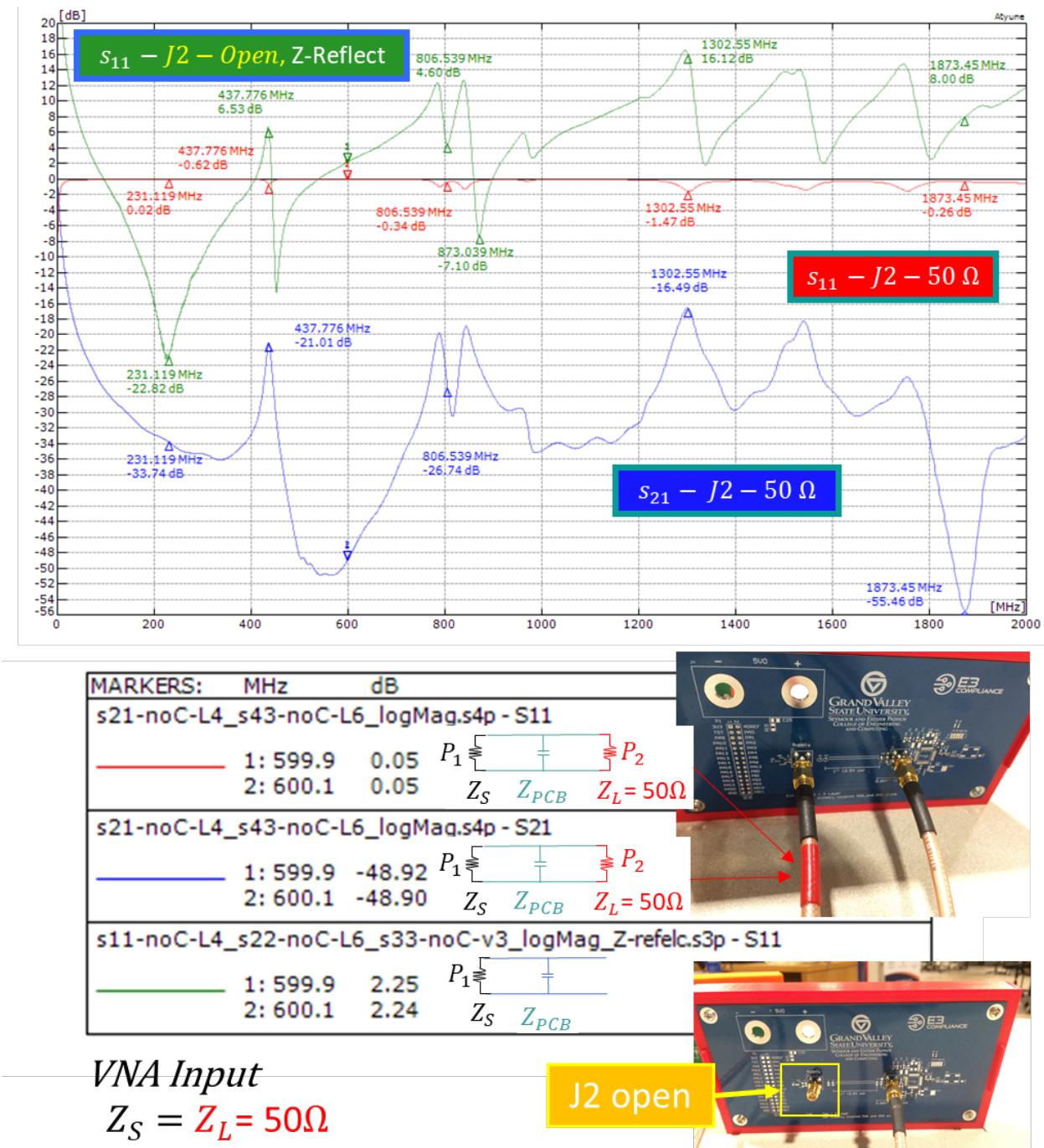


Figure 6.1: Comparison of measured results under different load conditions.

4-Layer, 6-Layer, and 6-Layer Version 3 for No Capacitors

Table 6.4: Comparison of embedded capacitance for 4-Layer, 6-Layer, and 6-Layer Version 3 for No Capacitors insertion loss measurements.

Stack-up	100 kHz	1 MHz	10 MHz	1 st Resonance	2 nd Resonance	Misc
noC-L4	0 dB	-0.27 dB	-8.07 dB	-36 dB @ 339 MHz	-21.37 dB @ 439 MHz	-55 dB @ 1873 MHz
noC-L6	0 dB	-3.5 dB	-20.54 dB	-49.61 dB @ 344 MHz	-40.06 dB @ 433 MHz	
noC-v3	0 dB	-1.54 dB	-15.98 dB	-43.93 dB @ 347 MHz	-31.29 dB @ 468 MHz	

4-Layer, 6-Layer, and 6-Layer Version 3 for Not Grouped Capacitors

Table 6.5: Comparison of embedded capacitance for 4-Layer, 6-Layer, and 6-Layer Version 3 for Not Grouped Capacitors insertion loss measurements.

Stack-up	100 kHz	1 MHz	10 MHz	1 st Resonance	2 nd Resonance	2 nd Anti-Resonance
notGroupedC-L4	-10 dB	-29.22 dB	-52 dB	-68 dB @ 18 MHz	-16.3 dB @ 189 MHz	-22.8 dB @ 444 MHz
notGroupedC-L6	-10 dB	-29.22 dB	-52 dB	-68 dB @ 18 MHz	-26.71 dB @ 96 MHz	-40.03 dB @ 437 MHz
notGroupedC-v3	-10 dB	-29.22 dB	-52 dB	-68 dB @ 18 MHz	-24.18 dB @ 142 MHz	-32.82 dB @ 474 MHz

4-Layer, 6-Layer, and 6-Layer Version 3 for Grouped Capacitors

Table 6.6: Comparison of embedded capacitance for 4-Layer, 6-Layer, and 6-Layer Version 3 for Grouped Capacitors insertion loss measurements.

Stack-up	100 kHz	1 MHz	10 MHz	1 st Resonance	2 nd Resonance	2 nd Anti-Resonance
GroupedC-L4	-10 dB	-29.01 dB	-52 dB	-68.7 dB @ 18 MHz	-16.6 dB @ 180 MHz	-24 dB @ 439.5 MHz
GroupedC-L6	-10 dB	-29.01 dB	-52 dB	-68.25 dB @ 20 MHz	-25.5 dB @ 96 MHz	-41.02 dB @ 433.5 MHz
GroupedC-v3	-10 dB	-29.01 dB	-52 dB	-68.25 dB @ 20 MHz	-24.18 dB @ 142 MHz	-32.09 dB @ 469 MHz

4-Layer for No, Not Grouped, and Grouped Capacitors

Table 6.7: Comparison of embedded capacitance for 4-Layer for No, Not Grouped, and Grouped Capacitors insertion loss measurements.

Stack-up	100 kHz	1 MHz	10 MHz	1 st Resonance	2 nd Resonance	2 nd Anti-Resonance
noC-L4	-0 dB	-0.27 dB	-8.07 dB	-36 dB @ 339 MHz	-21.37 dB @ 439 MHz	
notGroupedC-L4	-10 dB	-29.01 dB	-51.86 dB	-68 dB @ 20 MHz	-16.7 dB @ 185 MHz	-23.26 dB @ 442 MHz
GroupedC-L4	-10 dB	-29.01 dB	-51.86 dB	-68 dB @ 18 MHz	-16.63 dB @ 180 MHz	-23.28 dB @ 442 MHz

6-Layer for No, Not Grouped, and Grouped Capacitors

Table 6.8: Comparison of embedded capacitance for 6-Layer for No, Not Grouped, and Grouped Capacitors insertion loss measurements.

Stack-up	100 kHz	1 MHz	10 MHz	1 st Resonance	2 nd Resonance	2 nd Anti-Resonance
noC-L6	-0 dB	-3.5 dB	-20.56 dB	-49.7 dB @ 339 MHz	-40.7 dB @ 439 MHz	
notGroupedC-L6	-10 dB	-29.01 dB	-51.61 dB	-68 dB @ 19 MHz	-25.5 dB @ 97 MHz	-40.93 dB @ 437 MHz
GroupedC-L6	-10 dB	-29.01 dB	-51.61 dB	-68 dB @ 20 MHz	-25.5 dB @ 97 MHz	-40.99 dB @ 433 MHz

6-Layer Version 3 for No, Not Grouped, and Grouped Capacitors

Table 6.9: Comparison of embedded capacitance for 6-Layer Version 3 (v3) for No, Not Grouped, and Grouped Capacitors insertion loss measurements.

Stack-up	100 kHz	1 MHz	10 MHz	1 st Resonance	2 nd Resonance	2 nd Anti-Resonance
noC-v3	-0 dB	-1.54 dB	-15.98 dB	-44.02 dB @ 339 MHz	-31.28 dB @ 469 MHz	
notGroupedC-v3	-10 dB	-29.37 dB	-51.61 dB	-68 dB @ 19 MHz	-21.53 dB @ 131 MHz	-31.14 dB @ 465 MHz
GroupedC-v3	-10 dB	-29.37 dB	-51.61 dB	-68 dB @ 20 MHz	-24.18 dB @ 142 MHz	-32.08 dB @ 469 MHz

6.1.3 Comparison of Frequencies for Input Impedance vs. Insertion loss

For practical reasons it would be handy to be able to perform measurements with s_{11} rather than s_{21} . The reasons are that it is faster to make an OSL calibration than an OSLT calibration. Space on the PCB might limited and it is not always possible to place a second SMA connector. Alternatively it could be soldered directly on the port but calibration will be time consuming. Most often the information of the poles of the system is enough to find the anti-resonant frequencies which are of interest. It is not uncommon that the issues of measurements are related to the anti-resonance frequencies. As shown previously the comparison of the magnitude between the two gathered measurements set is not a good idea. However, choosing the focus on resonance and anti resonance frequencies the two measurement sets can be compared. This is because the measured system is the same and the poles should not differ in extreme. To establish the comparison three cases were compared with No, Not Grouped, and Grouped Capacitors each for one layer stack. The gathered results are presented in Tab. 6.10 to Tab. 6.12. The comparison is performed with three chosen points of interest, namely the 1st resonance, and the following two anti-resonant frequencies. The comparison shows that the frequencies only slightly differ. The most deviation can be observed in the case of no capacitor mounted for the 1st resonant frequency, the frequency is approximately doubled. For all other cases no deviation or a deviation maximum of 20 MHz can be observed at a higher frequency of 400 MHz. This can be called alike because if a capacitor would be chosen to suppress the frequency at this point the suppressed bandwidth would be greater then 20 MHz at this frequency range.

4-Layer for No, Not Grouped, and Grouped Capacitors

Table 6.10: Comparison of embedded capacitance for 4-Layer for No, Not Grouped, and Grouped Capacitors input impedance vs. insertion loss measurements.

Stack-up	1 st Resonance	Anti-Resonance	Anti-Resonance
s11, J2-open noC-L4	225 MHz		434 MHz
s11, J2-open notGroupedC-L4	16 MHz	188 MHz	443 MHz
s11, J2-open GroupedC-L4	16 MHz	180 MHz	443 MHz
s21, J2-50 Ω noC-L4	339 MHz		439 MHz
s21, J2-50 Ω notGroupedC-L4	20 MHz	185 MHz	442 MHz
s21, J2-50 Ω GroupedC-L4	18 MHz	180 MHz	442 MHz

6-Layer for No, Not Grouped, and Grouped Capacitors

Table 6.11: Comparison of embedded capacitance for 6-Layer for No, Not Grouped, and Grouped Capacitors input impedance vs. insertion loss measurements.

Stack-up	1 st Resonance	Anti-Resonance	Anti-Resonance
s11, J2-open noC-L6	160 MHz		463 MHz
s11, J2-open notGroupedC-L6	16 MHz	97 MHz	463 MHz
s11, J2-open GroupedC-L6	18.8 MHz	95 MHz	463 MHz
s21, J2-50 Ω noC-L6	339 MHz		439 MHz
s21, J2-50 Ω notGroupedC-L6	19 MHz	97 MHz	437 MHz
s21, J2-50 Ω GroupedC-L6	20 MHz	97 MHz	433 MHz

6-Layer Version 3 for No, Not Grouped, and Grouped Capacitors

Table 6.12: Comparison of embedded capacitance for 6-Layer Version 3 (v3) for No, Not Grouped, and Grouped Capacitors input impedance vs. insertion loss measurements.

Stack-up	1 st Resonance	Anti-Resonance	Anti-Resonance
s11, J2-open noC-v3	168 MHz		463 MHz
s11, J2-open notGroupedC-v3	19.5 MHz	129 MHz	463 MHz
s11, J2-open GroupedC-v3	15 MHz	139 MHz	463 MHz
<hr/>			
s21, J2-50 Ω noC-v3	339 MHz		469 MHz
s21, J2-50 Ω notGroupedC-v3	19 MHz	131 MHz	465 MHz
s21, J2-50 Ω GroupedC-v3	20 MHz	142 MHz	469 MHz

General Observations to Initial or First Slope

Each initial or first occurring slope observed has a slope of 20 dB. This leads to the statement that a PCB itself acts as 1st order filter structure. This means if not affected by any additional components the falling and rising slope will be similar. The slope is effected by parasitic as higher the frequency.

6.1.4 Transient Response

Tab. 6.13 presents the summary of the measured results. It is shown that the 6-Layer stack-up suppresses higher frequency content better than the 4-Layer stack-up. In terms of magnitude the grouped capacitors outperform not grouped capacitors.

Table 6.13: Transient response measurement results PCB.

Test Case	Cursor		FFT		
	V _{pp} mV	Δf MHz	1 st dBV @ f _c	2 nd dBV @ f _c	3 rd dBV @ f _c
4-Layer Not Grouped	21.28	675.68	-66 dBV @ 319 MHz	-86 dBV @ 922 MHz	
4-Layer Grouped	16.35	714.29	-70 dBV @ 319 MHz	-90 dBV @ 922 MHz	
6-Layer Not Grouped	15.90	419.67	-56 dBV @ 156 MHz	-83 dBV @ 442 MHz	-69 dBV @ 800 MHz
6-Layer Grouped	12.99	657.89	-60 dBV @ 161 MHz	-82 dBV @ 451 MHz	-102 dBV @ 774 MHz

6.1.5 Why is the 6-Layer PCB Outperforming the 6-Layer Version 3

According to the theory and the thoughts around the trivial answer is that the six-layer version three board will outperform the six-layer board in terms of having a lower input impedance. This is based on the thought that the connectors are closer to the measured closely coupled power and ground planes. However, by investigating the case with no capacitors mounted on the boards, it can be seen that the main difference is in the lower frequency range up to the board's resonant frequency. Fig. 6.2 shows the two stack-ups under investigation.

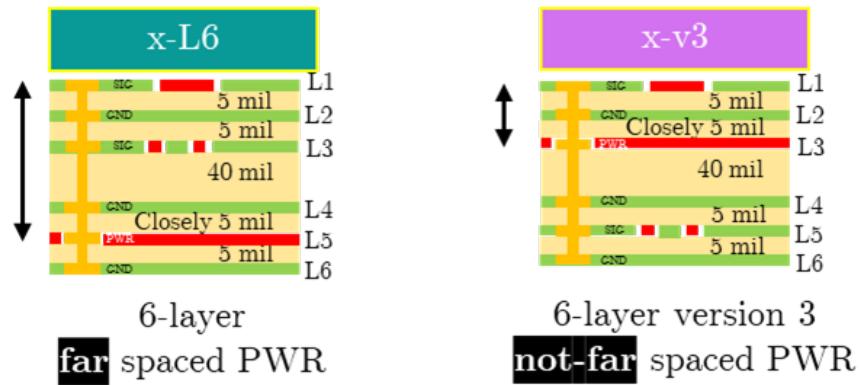


Figure 6.2: Discussed layer stacks, to the left the 6-layer with far spaced power plane, and to the right 6-layer version 3 with not far-spaced power plane.

Hypothesis 1 - The current will flow through the lowest impedance. Based on that, the lowest impedance is the parallel circuit of the four ground layers or partial layers on top of the power plan, and build the lowest impedance path up to the resonant frequency of the board. For higher frequency, as the loop area of the current flow increases, the impedance decreases. In case for higher frequencies, all ground planes regardless of their placement are utilized to some extent which stabilizes the impedance of two six-layer boards, and impedance variations diminish as the frequency increases.

Hypothesis 2 - By closer examination it can be seen that the 6-layer (L6) stack-up with the far-spaced power plane is closely coupled to the ground plane above and to the signal layer on the bottom which contains a lot of ground surface as well. The increased capacitance would lead to an decreased impedance.

Hypothesis 3 - The biggest change is the inductive region. Therefore it seems not unreasonable to argue that the length of the stubs caused by the via could result in larger impedance. Therefore, the impedance would be increased in comparison to the 6-layer version 3 stack-up.

6.1.6 The Impact on Impedance by the Capacitors

Two $0.1 \mu\text{F}$ capacitors in parallel were mounted either grouped or not grouped. The data shows that in all cases, the capacitors are the predominant figure of impedance. All three stack-ups had at 1 MHz the same impedance. However, the capacitors only influence a frequency range centered on their self-resonant frequency. The frequency range impact on the data can be defined as from 100 kHz up to 70 to 90 MHz range. The 70 to 90 MHz range results in the intercept point where the board impedance is superposed with the capacitors ESL.

6.1.7 Fundamental Objective of Decoupling

Due to the fundamentals of circuit design, most circuits are based on the assumption that in the ideal case the reference voltage is stable. This is assumed any time enough charge can be supplied to the load. Bear in mind that the impedance is highly depending on the frequency. However, the following important statement can be made which allows the understanding of a fundamental knowledge that explains many design rules around PCB.

Decoupling - Voltage is decoupled from the current. The voltage does not change, if the current changes.

It can be stated that a closely spaced design outperforms a not closely spaced design for higher frequency. Besides that, embedded capacitance is with respect to EMC most often desired. The only exception is controlled impedance where it might not be possible to improve embedded capacitance because the dielectric height is given due to the design of a RF trace.

6.2 EMC Filters - Source and Load Impedance

In this section the EMC filter simulations and measured results are discussed.

6.2.1 LC - R vs. CL - R Filter Structure

Simulations and measurements show that placing the capacitor on the high impedance side clearly improves the filter performance over a frequency range of 1 MHz up to 1 GHz. For a frequency range of 100 kHz to 1 MHz the CL - R structure with the inductor at the high impedance sides outperforms the LC - R structure slightly. This is shown for a impedance of $1 \text{ k}\Omega$ in series to the 50Ω measured port. By increasing the impedance to $10 \text{ k}\Omega$ it can be shown that the LC - R structure still outperforms the CL - R structure but in a lower frequency range of 20 MHz up to 1 GHz. Below 20 MHz, no change in performance can be reasonably seen. For a load impedance of $91 \text{ k}\Omega$ the outperformed frequency range for the LC - R structure diminishes even more as shown in Fig. 4.29.

Tab. 6.15 presents the summarized key points highlighted in the simulation of various filter structures of the previous sections. Fig. B.11 shows the Self-Resonant Frequency (SRF) of a used 10 nF capacitor is at 60 MHZ with a magnitude of -49.7 dB, measured on board. The SRF of two used 10 nF capacitor in parallel is at 61 MHZ with a magnitude of -80.2 dB, measured on board. Fig. B.10 shows the SRF of a used $4.7 \mu\text{H}$ inductor is at 31.8 MHZ with a magnitude of -40.1 dB, measured on board. The SRF of two used $4.7 \mu\text{H}$ inductor in series is at 32.7 MHZ with a magnitude of -59.8 dB, measured on board.

Table 6.15: Comparison of LC filter structure with source-load impedance of $1 \text{ k}\Omega$, $10 \text{ k}\Omega$, and $91 \text{ k}\Omega$.

Filter	100 kHz	1 MHz	10 MHz	1 st Resonance	2 nd Resonance	202 MHz
LC - R $1 \text{ k}\Omega$ sim	-21.2 dB	-30.8 dB	-65.8 dB			
CL - R $1 \text{ k}\Omega$ sim	-21.2 dB	-30.8 dB	-50.7 dB			
LC - R $1 \text{ k}\Omega$	-21.3 dB	-30 dB	-65.8 dB	-115 dB @ 30 MHz	-95.5 dB 60 MHz	-64.2 dB

Continuation of Table 6.15						
Filter	100 kHz	1 MHz	10 MHz	1 st Resonance	2 nd Resonance	202 MHz
CL - R 1 kΩ	-21.3 dB	-30 dB	-49 dB	-84.9 dB @ 30 MHz	-83 dB @ 60 MHz	-59.6 dB
LC - R 10 kΩ sim	-40.5 dB	-50.4 dB	-85.5 dB			
CL - R 10 kΩ sim	-40.5 dB	-50.4 dB	-70 dB			
LC - R 10 kΩ	-40.1 dB	-50 dB	-69.2 dB	-101 dB @ 60 MHz		-82.2 dB
CL - R 10 kΩ	-40.1 dB	-50 dB	-69.2 dB	-96.2 dB @ 60 MHz		-69 dB
LC - R 91 kΩ sim	-59.5 dB	-69.6 dB	-104.6 dB			
CL - R 91 kΩ sim	-59.5 dB	-69.6 dB	-89.1 dB			
LC - R 91 kΩ	-60 dB	-69 dB	-87.8 dB	-123.6 dB @ 53 MHz		-87.69 dB
CL - R 91 kΩ	-60 dB	-69 dB	-87.8 dB	-109.7 dB @ 53 MHz		-78 dB

6.2.2 π - R 1 kΩ vs. π - R 1 k Ω Filter Structure

Tab. 6.16 shows the key points of the simulated and measured results. It can be seen that in a frequency range from 100 kHz to 10 MHz simulated and measured results act with no deviation. The simulated result converge close upon resonant frequency of the circuit from where on the non-linear behavior of the components take over. At 1 MHz a difference of 0.3 dB from simulation to measurements is shown, which is an anti-resonance too.

At a frequency of 10 MHz the simulated board has -95.64 dB and the measured has a magnitude of -93 dB which results in a difference of 2.64 dB. It can be seen that above the resonant frequency of the circuit which is at 57 MHz the filter decreases in performance and looks more like a band-stop filter. The inductance of the traces, components, and the coil limit the lower boundary condition of the impedance. The SRF of the coil was measured at 31.8 MHz. The SRF of two 10 nF capacitors in parallel is at 61 MHz.

Table 6.16: Comparison of π filter structure with source-load impedance of $1 \text{ k}\Omega$.

Filter	100 kHz	1 MHz	1 st Anti-Resonance	10 MHz	1 st Resonance	202 MHz
π - R $1 \text{ k}\Omega$ sim	-22 dB	-20.5 dB	-20.5 dB @ 1 MHz	-95.64 dB		
R $1 \text{ k}\Omega$ - π sim	-22 dB	-20.5 dB	-20.5 dB @ 1 MHz	-95.64 dB		
π - R $1 \text{ k}\Omega$	-22.3 dB	-24 dB	-24 dB @ 1 MHz	-93 dB	-113 dB @ 57 MHz	-104 dB
R $1 \text{ k}\Omega$ - π	-22.3 dB	-24 dB	-24 dB @ 1 MHz	-93 dB	-113 dB @ 57 MHz	-104 dB

6.2.3 T - R $1 \text{ k}\Omega$ vs. R $1 \text{ k}\Omega$ - T Filter Structure

Tab. 6.17 shows the key points of the simulated and measured results. It can be seen that in a frequency range from 100 kHz to 10 MHz simulated and measured results act with no deviation. The simulated result converge close upon resonant frequency of the circuit from where on the non-linear behavior of the components take over. It is interesting to see that there are two resonant frequencies: one at 30 MHz and one at 57 MHz. The measured resonant frequency of a single coil mounted on the board shows a resonance at 25 MHz. It seems not unreasonable that this might be related to each other.

Table 6.17: Comparison of T filter structure with source-load impedance of $1 \text{ k}\Omega$.

Filter	100 kHz	1 MHz	10 MHz	1 st Reso-nance	2 nd Reso-nance	202 MHz
T - R $1 \text{ k}\Omega$ sim	-21 dB	-30.7 dB	-66.2 dB			
R $1 \text{ k}\Omega$ - T sim	-21 dB	-30.7 dB	-66.2 dB			
T - R $1 \text{ k}\Omega$	-21.4 dB	-30 dB	-65.5 dB	-107.4 dB @ 30 MHz	-100 dB @ 57 MHz	-67.3 dB
R $1 \text{ k}\Omega$ - T	-21.4 dB	-30 dB	-66.5 dB	-107.4 dB @ 30 MHz	-100 dB @ 57 MHz	-67.3 dB

6.2.4 T - R $1 \text{ k}\Omega$ vs. CL - R $1 \text{ k}\Omega$ Filter Structure

Tab. 6.18 shows the key points of the simulated and measured results. It can be seen that in a frequency range from 100 kHz to 1 MHz simulated and measured results act with no deviation. The rest of the frequencies are discussed at some point in this document. Interesting is that the measured results show that T - R and CL - R have the same resonant frequencies. The T structure shows at the first resonant frequency of 30.8 MHz an improved performance of 23 dB. At the second resonant frequency the T structure shows a performance improvement of 16.9 dB. At a frequency of 202 MHz the improvement is 7.9 dB.

Table 6.18: Comparison of T filter structure versus CL - R structure with load impedance of $1 \text{ k}\Omega$.

Filter	100 kHz	1 MHz	10 MHz	1 st Reso-nance	2 nd Reso-nance	202 MHz
T - R $1 \text{ k}\Omega$ sim	-21 dB	-30.7 dB	-66.2 dB			

Continuation of Table 6.18						
Filter	100 kHz	1 MHz	10 MHz	1 st Resonance	2 nd Resonance	202 MHz
CL - R 1 kΩ sim	-21.2 dB	-30.8 dB	-50.7 dB			
T - R 1 kΩ	-21.4 dB	-30.5 dB	-66 dB	-107.7 dB @ 30.8 MHz	-99.7 dB @ 57 MHz	-67.3 dB
CL - R 1 kΩ	-21.4 dB	-30.5 dB	-49 dB	-84.7 dB @ 30.8 MHz	-82.8 dB @ 57 MHz	-59.4 dB

6.2.5 Simulation vs. Measurement

The previous comparisons between simulated results and measured results show that the simulated models match well for the lower frequency range up to 10 MHz. Beyond this point the most comparable result is shown by the T filter. The π filter showed results that are basically identical to the simulations. The T filter outperforms the Pi filter around 1 MHz because of the anti resonance of the Pi filter by around 10 dB. The Pi filter outperforms the T filter at the resonant frequency significantly. Both Filters have a resonance at 57 MHz. The T filter has a second resonance at 30 MHz. The T filter therefore shows a improved bandwidth compared to the Pi filter.

The second resonant frequency for the T filter can be explained by examining the measurement of a L and two Ls in series shown in Appendix Fig. B.10. At the resonant frequency of the inductors, the two inductors outperforms the performance of one inductor by 20 dB. Thanks to the simplicity of the boards and the tested structures it can be reasonably assumed that the influence on the π filter is mainly capacitive. The influence on the T filter is inductive. The LC filter comparison shows clearly that the influence of high impedance site matters and should not be neglected in design considerations and component placement. No statements should be made in terms of absolute magnitude of perfor-

mance due to the fact that the measurements have multiple error sources. However, these errors do not conflict radically with the comparison of equally performed measurements which makes the measurements and drawn statements valid.

6.2.6 Reality Check

This discussion is very hypothetical. Keep in mind that to build an LC or CL filter is difficult. On a PCB most of the time multiple capacitors are placed for various reasons. Fig. 6.3 shows blue marked capacitors of the SMPS. From left to right there is an RF short which is a relatively small capacitor, as example 470 pF. After the CMC there are large bulk capacitors to provide enough charges in a medium time which helps voltage stability a lot. The bulk capacitors can be up to 100 μ F in size. Finally, the EMC filter is placed with whatever structure the product designer finds appropriate. The component size is usually based on the target frequencies. However, here in the SMPS there where 10 μ F capacitors and 22 μ H used. Finally, the decoupling capacitors are placed close to the V_{DD} pin or pins of the IC. Decoupling caps are commonly used in a range of 10 μ F down to 10 nF. Common values are 0.1 μ F and multiples may be used. It is clear that an LC or CL structure still makes sense because all these components cover different target frequencies. The capacitors also serve different purposes and have a designated prime function which affects the surrounding areas as well. The components that are not placed at the footprint will act also in slight time variance to each other. For all these reasons, even if it seems unlikely, the components can be designed for a specific target and will show more or less influence there. As the measurements showed with the SMPS, not every additional component is an actual improvement due to changing harmonics and shift of resonant frequencies favorable or unfavorable outcomes can be produced. So far mainly interference from inside the product was discussed. Keep in mind that filters work both ways. Furthermore the impedance provided by an LISN is not the same over the entire frequency range, it is frequency dependent and most likely not exactly the same as the product will be used in the

field.



Figure 6.3: Reality check for EMC filters with SMPS.

6.2.7 How to simply design an EMC/EMI Filter?

Make an estimate about the target frequency or frequency range or better measure it.

Therefore, think what might generate the interference that you try to counteract. Simulate a π filter in LTSpice with the estimated source and load conditions that are to be expected approximately. It helps to start with 50Ω because that is what is used in the VNA to perform insertion loss measurements. Use the insertion loss in simulations to compare the performance of different filter structures or values. As shown in the results the lower

frequency part is basically the same as in the simulation. Estimate the filter's resonant frequency. Use the manufacturer's resonant frequency data to do so. As seen, the resonance of two components does not change in great order so it can be neglected. The difference of the SRF between manufacturer data and measurement is only 3 to 4 MHz. The rising slope after the resonant frequency can be assumed to have the same slope as the falling slope simulated in software. Beyond a certain frequency it will not matter because as seen in the measurements of embedded capacitance in Section 4.1 the impedance of the board will be the predominant component for a higher frequency range. Verification is important, perform measurements. Optimize to your needs, shift component values and see if improvement occurs. Take a capacitor out and make an LC out of it to see how it reacts in your real design. Fig. 6.4 shows the worked out process in colored steps. Fig. 6.5 shows the defined target frequency range of 0.15 MHz to 120 MHz. The main target was to suppress the fundamental.

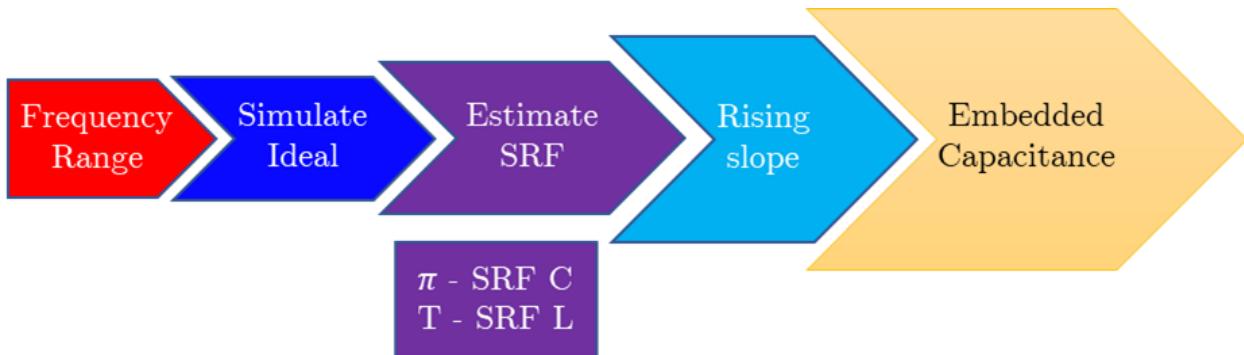


Figure 6.4: Novel EMC filter design approach based on simple geometric structures presented in colored steps.

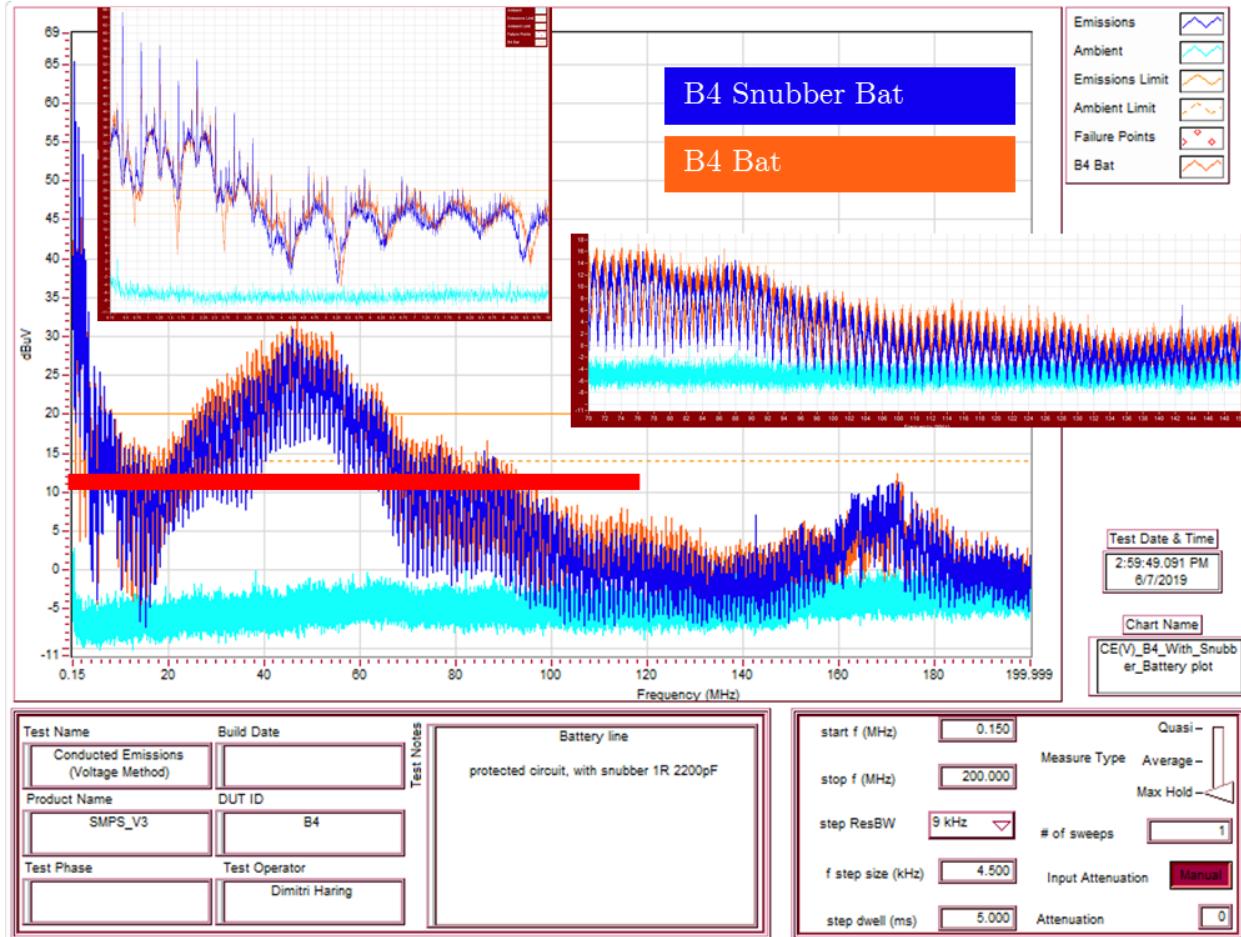


Figure 6.5: Novel EMC filter design approach step one target frequency.

Fig. 6.6 shows the circuit to the bottom left. The dark blue line shows the simulated ideal case. The resonant frequency is defined by the π filter based on the used capacitors SRF. The SRF is 2 MHz. It can be seen that the expected anti-resonance is occurring at 20 kHz. Based on the falling slope to the right of the anti-resonance is used to construct a triangle which will show an estimate on the rising slope occurring after the resonant frequency. The yellow line shows from where on that it can be assumed that the embedded capacitance of the board takes over. The embedded capacitance can be assumed according to the performed measurements being around 400 MHz.

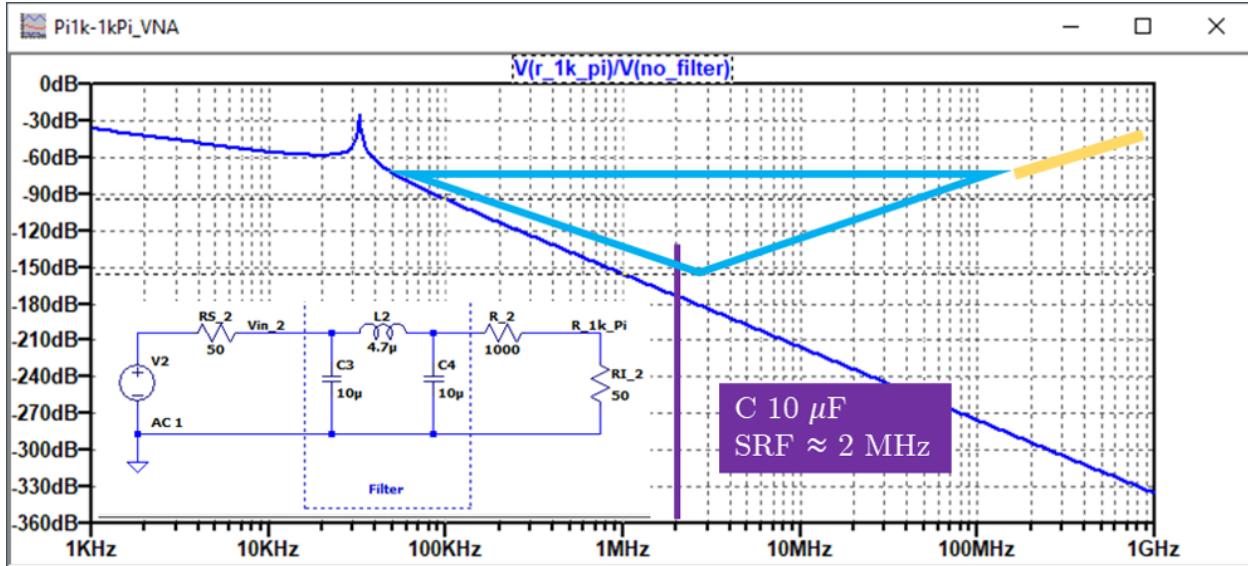


Figure 6.6: Novel EMC filter design approach step two to four.

6.2.8 What to Do if the Simple Strategy Fails

There are three options to process further. One, trial and error, which is an empirical approach based on observations by changing values slightly and measuring after each change. This can work but might not be a good idea to use booked chamber time if it is not fully needed. This can also be used to figure out if there is a better solution than the one already found. Two, spiral, the spiral approach leads to a path of simulation and measurement each time after measurements have been performed, you take the results and feed them back in a simulation model. This is the preferred approach for expensive or life depending designs because variations can be easily modeled with Monte Carlo which increases on the long run reliability. This can be done in software packages like CST, HFSS, or similar. However, there are costly but very insightful for complex structures or where designs get to boundary limitations. Three, find a guru, hopefully a solution can be found. This can also be used for beginners who do not know where to start so they see what he does and learn first.

6.2.9 What is the Difference Between an EMC and an EMI Filter?

The EMC filter is used to make device or subsystem compatible electromagnetic energy wise. The EMC filter is usually placed by a devices input supply. The EMC filter has to work therefore both ways. An EMI filter is used to suppress interference in general or partial interference. The construction is mainly the same but the usage differs. In general EMC counter measure are named by what they try to achieve.

6.3 SMPS EMI Suppression Techniques

The manufactured PCB passed the test requirements set by the customer. By placing an excess of footprints, the design changes can be made with equipping components instead of redesigning the PCB. A variate of extra measures to pass EMC testing is added as common mode choke, input filtering, snubber circuit, boot circuit, gate resistors, uninterrupted ground plane, and shielding. Overall the PCB design will provide a good base for the switched mode power supply and reduce unwanted emissions to the lowest possible minimum.

6.3.1 Snubber

The snubber measurement of the transient response presented in Section 4.4.1 show that the high frequency ringing caused due the switch of an FET is significantly suppressed by the use of the snubber. Furthermore, the purposed method of designing a snubber, by Adamczyk and Spence [19], is sound. The high frequency ringing seen in time domain could be reduced by 63.6 %. Interesting is that the ringing frequency does not change with the applied snubber compared to the stage where the 100 pF capacitor was added.

6.3.2 Filter

The nature of the EMC filtering is that the impedance is not fixed and a wide range of frequencies with different impedance can occur. The described nature makes defined characteristics complex and the achieved design can most commonly not be achieved without performing measurements. Keep in mind that very low voltages of μ V matter in this case. The following discusses the results measured in Section 4.4.3.

1st Order Filter 6.4 nF Capacitor added on C3 - The added capacitor lowered the impedance around a frequency of 80 MHz. This resulted in a suppression of interference of around 6 dB as discovered in the measured results 4.4.3.

2nd Order Filter CL 6.4 nF Capacitor added on C3, and 22 μ -H inductor added on R1 - The inductor added on R1 brought a massive performance increase for medium and high frequencies, However the performance increase on the fundamental was not outstanding, but noticeable. This was expected due to the low capacitor values.

3rd Order Filter CLC 6.4 nF Capacitor added on C3, and 22 μ -H inductor added on R1, 6.4 nF Capacitor added on C4 - This filter structure showed that an additional small capacitor added decreases performance.

6.3.3 Shielding

The shield's original purpose is to serve as reflective boundary between the environment and SMPS. As measurements showed, see 4.4.3, it also acts as an additional return current path. The shield's reflective nature will also prevent coupling from the circuit to external cables. However the shield should not be initially used as suppression technique for conducted emissions. Cost-wise it is not desirable to pay for something that is eventually not needed.

6.3.4 Coil Orientation

According to Hegarty et al. [32] the dot or dash on a wire wrap coil represents the starting point of the winding. Most coils warped for the desired current rating and inductance used for SMPS start the winding of the inside of the coil and end at the outside. This means that the starting point should be close to the switched node site. The highest ripple will be at the beginning of coil, hence the outer winding with lower ripple will act as a shield and enhance EMI suppression.

6.3.5 Load and Current

As shown in measurements where the load was changed from $50\ \Omega$ to $20\ \Omega$ the EMI issue worsened. In a real life set up a load between 2.5 to $0.5\ \Omega$ sounds most realistic. This was not originally considered in the design therefore the components and footprints used for filtering are dimensioned too small with respect to load current.

6.3.6 Via Stitching around FET

Due to high frequency content generated by switching of a FET it should be considered like an RF trace and it should be guarded or shielded with via stitching which was not considered in the deign.

6.3.7 Discussion on the use of the Top Layer

The reason for that is simple, high current requires cooling. Now there is also the possibility to make the top layer a solid ground and layer two is solid ground too and put all the routing into the layer three which for sure will shield more then routing Vin and Vout on the top layer if currents are not too large, then this is a possibility. This may need a 6 -layer stack so that there is layer 5 that can be used in addition to layer three for digital signal routing. Layer 4 and layer six would be ground in that case. The feedback trace

should always be buried if possible.

6.3.8 Solid Ground Plane Under Top Layer

The solid ground plane gives a reference plane to all signals on the board. The ground plane gives a direct current return path. This is important to realize in terms of via placement, avoid building slots.

6.3.9 Power and Ground Via Next to Capacitors

The ground via should be as close as possible to the capacitor pads. Ground and power via should be close together as possible to minimize current loops. In all the design guide and lectures a solid ground plane is always used, unfortunately in real life most likely the ground side will have thermal reliefs to enhance reliable production. Use multiple vias at least two on each pad and more for larger package size.

6.3.10 Via Stitching around FET, Vin, and Vout

The stitching around a FET can be looked at like an RF shielding along a controlled impedance RF trace. The stitching aids either way protecting FET to be perceptible to other noise sources and suppresses radiated noise caused by the FET. Vin and Vout can be stitched with via, think of it as a dipole antenna which radiates. By a buck converter directly on the input of Vin a capacitor high frequency short should be placed which terminates the supply line. This can be a 10 nF capacitor also the arranging from multiple capacitors can be done which will suppress a band.

6.3.11 Overview of EMI Suppression for SMPS

Fig. 6.7 shows an overview of protective measurements categorized in CM, DM, and Radiated Immunity (RI) with respect to effectiveness and frequency dependency. The chart was established based on the gathered knowledge acquired through literature review, and

discussed results of the master thesis. Two aspects where not measured in the chart one of the series gate resistor and the boot circuit. Those were based out of the authors thought process. The shielding the chart refers to is actually designed to shield the circuit against external radiation. However, as measurements showed it helps also for EMI suppression of internal sources for medium and higher frequencies. This chart might not present a full picture on what is out there but it represents the most common measures. The chart can also be used as a checklist for product design engineers which allows to go through the different cases and place according to it footprints for components or adjust the layer stack-up.

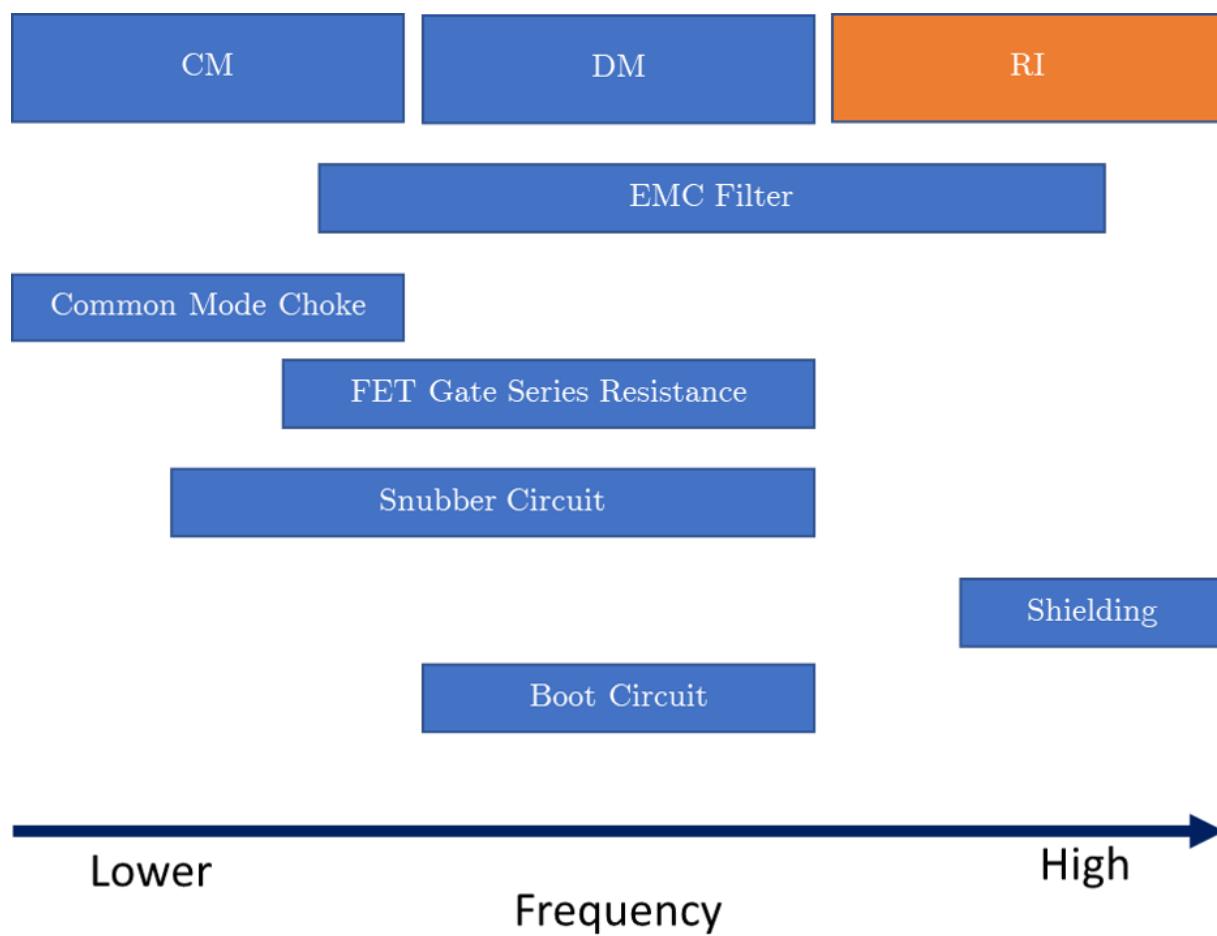


Figure 6.7: SMPS counter measurements.

6.3.12 Overview of Hardware Design Related EMI Suppression for SMPS

Fig. 6.8 shows an overview of PCB design knowledge - techniques - or things to think about it. The categories are ordered from top to down by their significance and left to right in terms of frequency. The three top categories are stated but hard to actually reference in terms of how much it helps because it depends on too many factors. However, it still helps the user to think about it, which simplifies decision making at the end.



Figure 6.8: SMPS PCB Design.

6.4 VHF Auto Tuner Applied EMC in Design

The VHF auto tuner study from Chapter 5, discusses the results previous to the chapter. It shows that each evaluated topic is used in a real world design and should be understood by product designers so that they are properly implemented. In a designs early stage, room should be left to apply common measures as CMC, snubber, EMC/EMI filter, and capacitors. If pre-compliance testing is performed, try to emulate the actual conditions as close as possible, especially current strength and load conditions. The case shows how many components are not directly related to a functionality. About half of the used components are used to suppress issues caused by the function of components.

6.5 Conclusion

The presented material integrates from the evaluations of PCB designs, simulation, and measurements. The evaluated topics are each connected by the desire to enhance Electromagnetic Compatibility (EMC). The thesis started with the embedded capacitance of a PCB which is fundamental to understand. The topic grants insight into the elementary study of capacitance, inductance, and impedance. The literature review is given credit by showing that most of the findings correspond to it. However, the case of the 6-layer board with far spaced power plane from the top signal layer outperforming the not-far spaced case is an exceptional case which leads to further research. The case could not be fully explained within the performed evaluation. Additionally, it could be shown that a 6-layer stack-up is mainly superior to a 4-layer stack-up. Grouped capacitors should be preferred, but by utilizing embedded capacitance with respect to high-frequency range, the capacitors can be placed not grouped. The EMC filter evaluation showed that the gathered knowledge of the literature review holds firm. In case of a high impedance side, the capacitor should be placed closer to it and the inductor away. Furthermore, it could be shown

that a third order filter π or T outperforms mainly a 2nd order filter structure. The π filter structure has a wider bandwidth than the T structure but comes with the trade-off of an anti-resonance whereas the T filter has no anti-resonance. Also, it can be stated that it is hard to effectively build a 1st order filter in reality because there are always more capacitors placed before or after the filter. Additionally, a simple EMC filter design process is proposed. The SMPS chapters showed how effectively a snubber could be designed within a well-defined procedure presented by Adamczyk and Spence. Time domain measurements showed a clear reduction of the target frequency's content. The snubber shows how well defined analysis can be used for applied design processes. The effectiveness of the snubber could be shown with conducted emissions voltage method measurements. Furthermore, design applications of filter structures could be tested and shown that the most obvious simple choice might not always present the best solution due to trade-offs. The evaluated shielding shows that it can have a high effect on noise suppression, and it is advisable to keep space for it on a design, even if not needed at the end. A design guidance for passive components is presented which relates importance, current mode, RF immunity, and frequency to established measures for EMI suppression used to enhance the EMC behavior of either a device or subsystem. A similar guide has been built for hardware design, which can be used by product designers to make design decisions. The analog RF immunity evaluation showed some interesting and unexpected results for the EMI protection of the Universal Asynchronous Receiver/Transmitter (UART) and failures of Low-Voltage Detect (LVD). In addition, different error behaviors could be represented on the UART lines depending on Amplitude Modulation (AM) or continuous waveform (CW) modulated ration patterns. However, the intended evaluation of the performance in three different trace structures could not be performed. Further evaluations with different measurement set-ups are recommended. A fully functional VHF auto tuner was designed to have a study on which the gained knowledge of the evaluated EMC on PCB can be applied. The study showed how and where the gathered knowledge and results could be used in actual

product design. Additionally, it showed how many components are only added to enhance EMC compatibility, which is approximately half of the components. As presented in the introduction, EMC has many angles it can be viewed on like a house in a sphere. Once the window of the house is closed and more capacitors are added, the issue becomes more complicated and the time it will take to make sense of its effects will greatly increase.

6.6 Areas for Future Efforts

This section will discuss or recommend further work based on questions raised during the performed evaluations.

6.6.1 Embedded Capacitance of a PCB

The boards were originally designed to test more, such as the capacitance strategies and the impact of current flow through the decoupling capacitors. The stated hypothesizes should be further investigated. To understand the impact of each component, simpler models are needed. The goal of such models would be the understanding of the predominant factors. A further area of research would be to use the approach of embedded capacitance materials to reduce the number of used capacitors. In terms of Ball Grid Array (BGA) packages where decoupling capacitors have to be placed on the bottom side of the boards. Recommended is to design a new board with embedded capacitance for evaluation. In addition a benefit-cost analysis would be performed to show the impact on different cases which allows a product designer to make educated decisions. In Section 6.1.5 three hypotheses were presented in terms of explanation why the 6-layer stack-up with far spaced power plane is outperforming the 6-layer version 3 stack-up with not-far spaced power plane. An additional 6-layer stack-up version is proposed with far spaced power plane on layer 4 instead of layer 5.

6.6.2 EMC Filters - Source and Load Impedance

Further evaluations would be interesting for designs filters with ferrite beads or as some manufacturer call it EMI beads.

6.6.3 SMPS Circuit Protection

During measurements it became clear that the load of 50Ω is too high and the current is too small, a reasonable load would be 2Ω which leads to a current of 2.5 A. This was not considered during the design stage. Therefore, it is recommended to adjust the components used to allow the test under improved test conditions with increased current. Suggested is a re-design of the existing board to accommodate higher currents. The impact of the orientation of coils was discussed but could not be proven with measurements. The existing SMPS design can be used research the impact of coil orientation for the output coil.

6.7 Reflection

This work is based on applied research. Measurements play an integral role. The work shall represent the interdisciplinary character that EMC comes with. An academic might question the methods used to come to conclusions which are mainly empirical and based on simple ideal models. The truth is, if you have the money to build it you do not have to play around with simulations. However, in the real world that is what engineers want to use to make quick design decisions in most cases. Therefore, an applied case was chosen to demonstrate the gained knowledge.

Appendix - A: Embedded Capacitance of a PCB

A.1 VNA Calibration

To ensure a proper VNA use the calibration has to be understood and validated so that the calibrated measurements expect a known value. First, the inner cylinder of a -Type female to SMA female connector was damaged, as shown in Fig. A.1.

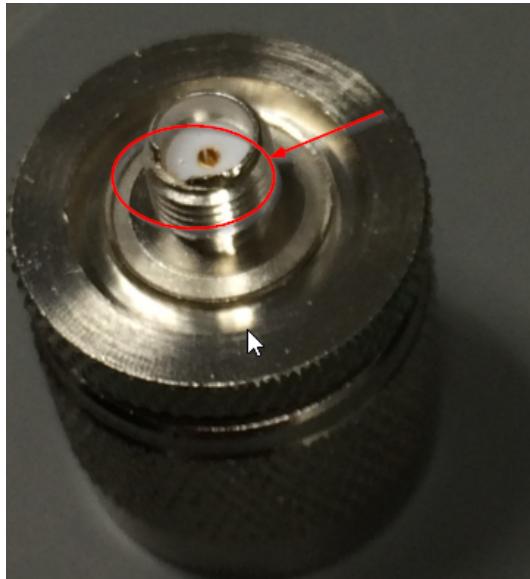


Figure A.1: Defective N-Type female to SMA female connector.



Figure A.2: Calibration kit used for VNA measurements in frequency domain.

Second, it could be determined that the use of torque is essential, otherwise inconsistent measurement will be made. Finally, a vast phase delay could be recognized after calibration, which was caused due to the small pin length of the through hole SMA connector, as shown in Fig. A.2. Equations A.1 to A.3 are used to deepen the understanding of phase delay and construction of the SMA connectors soldered on the board [33]. This showed that a port extension needs to be setup in the VNA after calibration. This was done by

using the auto port extension function with an open and short SMA connector.

$$v_p = \frac{c}{\sqrt{\epsilon_r}} \quad (\text{A.1})$$

$$\lambda = \frac{v_p}{f} = \frac{c}{\sqrt{\epsilon_r} \cdot f} \quad (\text{A.2})$$

$$\lambda_{normalized} = \frac{d}{\lambda} \quad (\text{A.3})$$

A.2 Design

This sections presents the designs of the 4-layer, 6-layer, and 6-layer version 3 PCB. The following design documents were made with Altium Designer.

A.2.1 Schematics

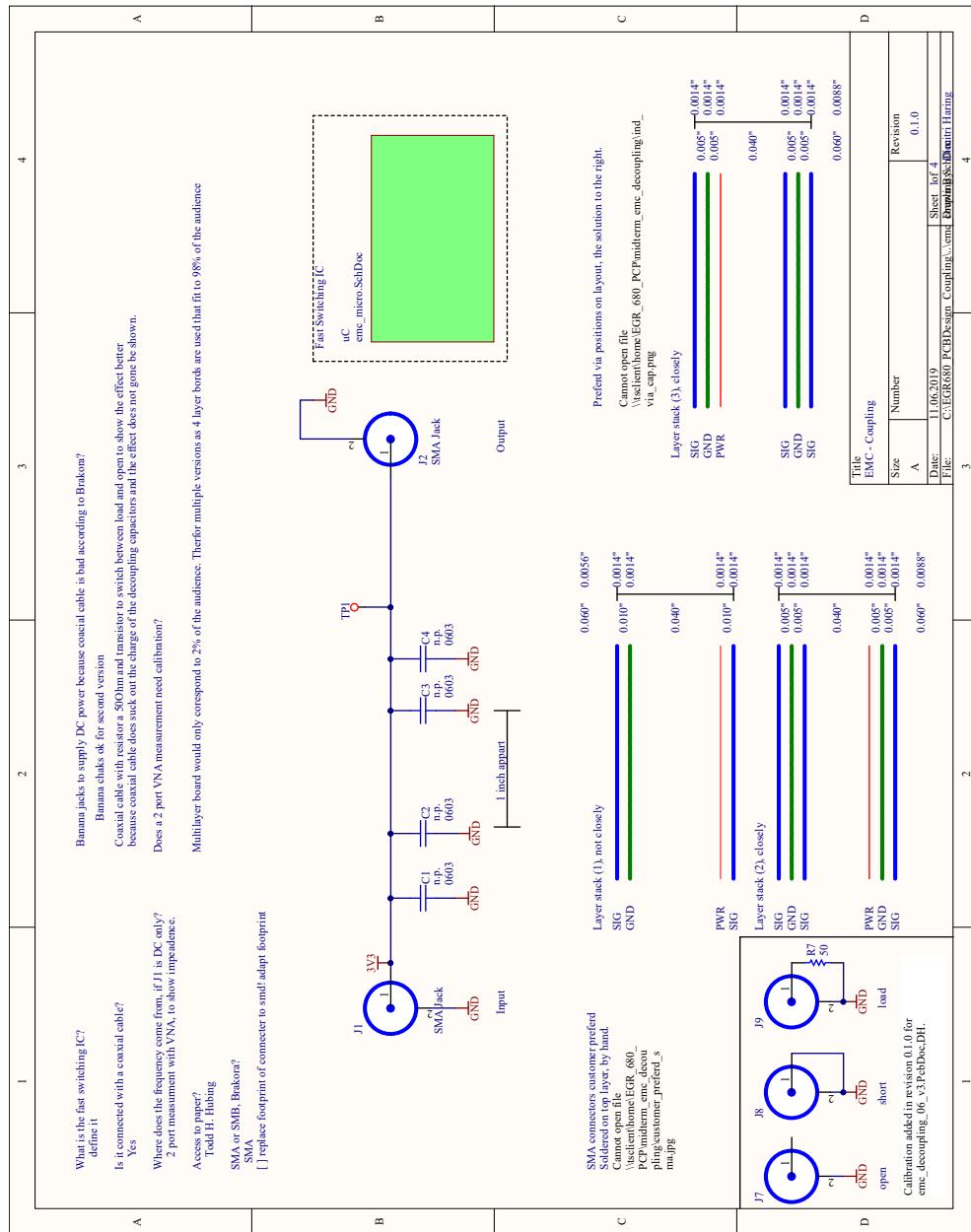
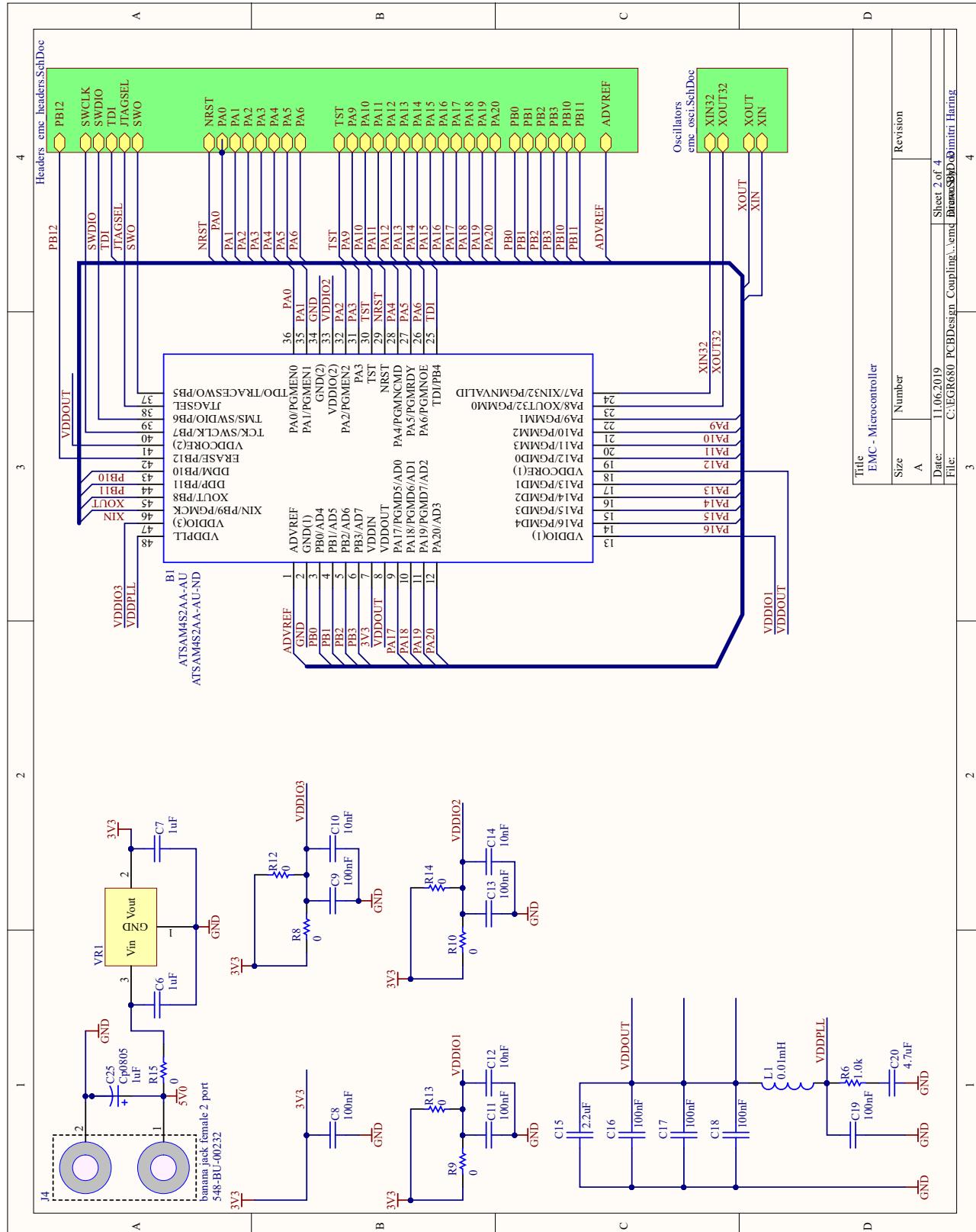


Figure A.3: Embedded capacitance schematic page 1, test trace for VNA measurements.

Figure A.4: Embedded capacitance schematic page 2, μ C.

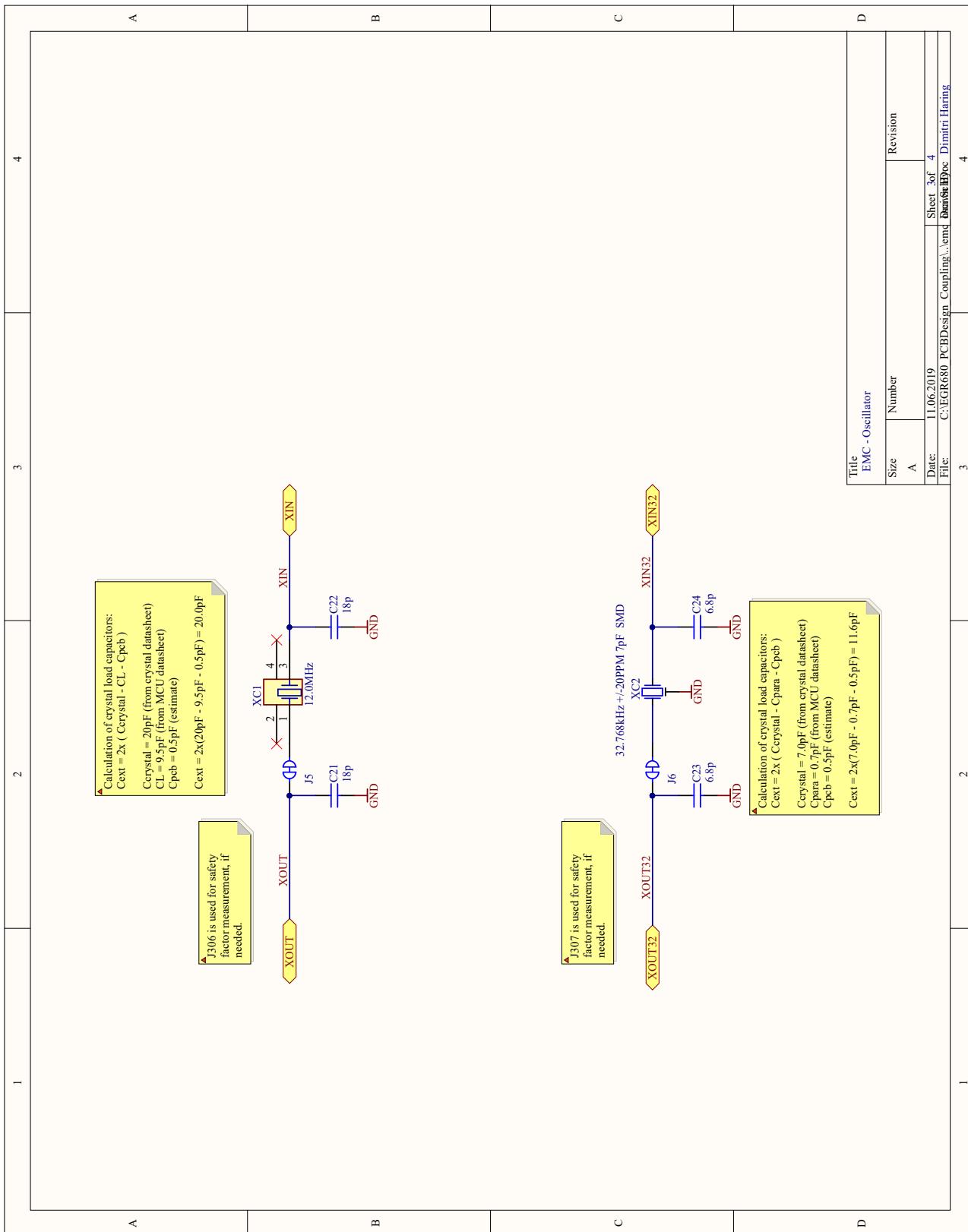


Figure A.5: Embedded capacitance schematic page 3, oscillators.

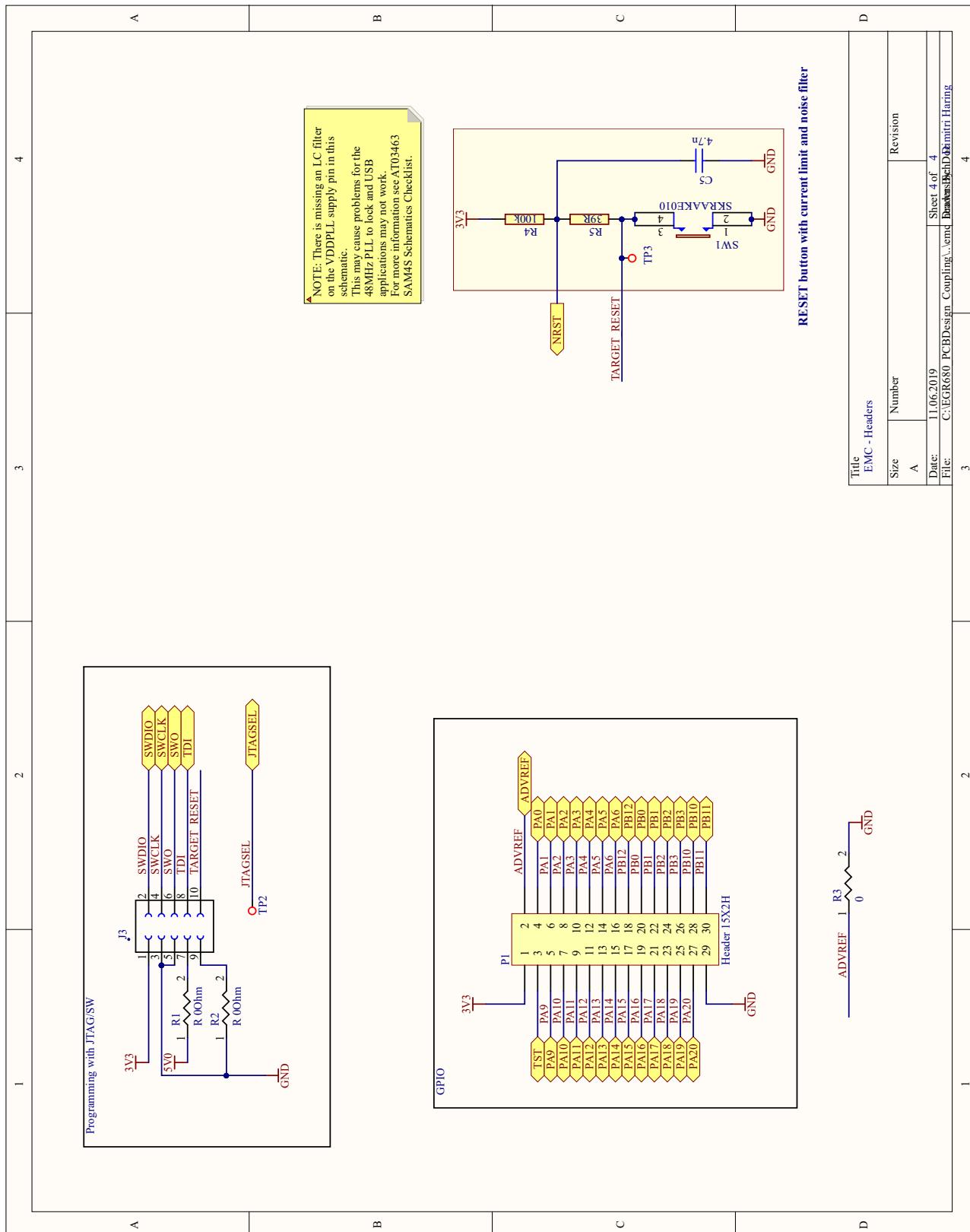


Figure A.6: Embedded capacitance schematic page 4, connectors and reset button.

A.2.2 Bill of Material

Designator	Value	Footprint	Description	Quantity
B1		QFP50P900X900X160-45N	ATMEL - ATSAM4S2AA-AU - MCU - CORTEX-M4, 128kB, 120MHz, LQFP-48	1
C1, C2, C3, C4	n.p.	0603	Standard Ceramic Capacitor 0603	4
C5	4.7n	0402	Ceramic capacitor, SMD 0402, X7R, 25V, +/-10% (de35287)	1
C6, C7	1uF	0603	Standard Ceramic Capacitor 0603	2
C8, C9, C11, C13, C16, C17, C18	100nF	0603	Standard Ceramic Capacitor 0603	8
C19		0603	Standard Ceramic Capacitor 0603	1
C10, C12, C14	10nF	0603	Standard Ceramic Capacitor 0603	3
C15	2.2uF	0603	Standard Ceramic Capacitor 0603	1
C20	4.7uF	0603	Standard Ceramic Capacitor 0603	1
C21, C22	18p	0402	Ceramic capacitor, SMD 0402, NPO, 50V, +/-5%	2
C23, C24	6.8p	0402	Ceramic capacitor, SMD 0402, NPO, 50V, +/-5%	2
C25	1uF	0805p	P0805 Polarized Chip Capacitor - Standard	1
J1, J7, J8, J9		SMA 0603 compined	Huber & Suhner 50 Ohm 18 GHz	4
J2		SMA 0603 compined v2	Huber & Suhner 50 Ohm 18 GHz	1
J3		header 5x2 1.27	CONN HEADER VERT DUAL 10POS 1.27 62201021121	1
J4		Banana hole 2 port		1
L1	0.01mH	1210RES	1210 Chip Inductor - Standard	1
P1		HDR2X15	Header, 15-Pin, Dual row, Right Angle	1
R1, R2, R3		0402 1.00 * 0.5 mm	0Ohm resistor 0402	3
R4	100k	0402	Thick film resistor, SMD 0402, 1/16W, 1%	1
R5	33R	0402	Thick film resistor, SMD 0402, 1/16W, 1%	1
R6	1.0k	0402 1.00 * 0.5 mm	0402 Chip Resistor - Standard	1
R7	50	0603RES	0603 Chip Resistor - Standard	1
R8, R9, R10, R12, R13, R14	0	0402 1.00 * 0.5 mm	0402 Chip Resistor - Standard	6
R15	0	0805RES	0805 Chip Resistor - Standard	1
SW1	SKRAAKE010	AP8-00137	6.2x6.2 mm SMD tact switch, same as A08-00911 but less force is needed	1
VR1		SOT-23 - 3		1
XC1	12.0MHz	AP7-00039	Fox FQ5032B 12.0MHz SMD crystal 738B-12	1
XC2	32.768kHz +/-20ppm	AP7-00044	32k768 crystal, +/-20ppm, CL=7pF, max ESR 60kOhm	1

Figure A.7: Embedded capacitance BOM.

A.2.3 4-Layer Design

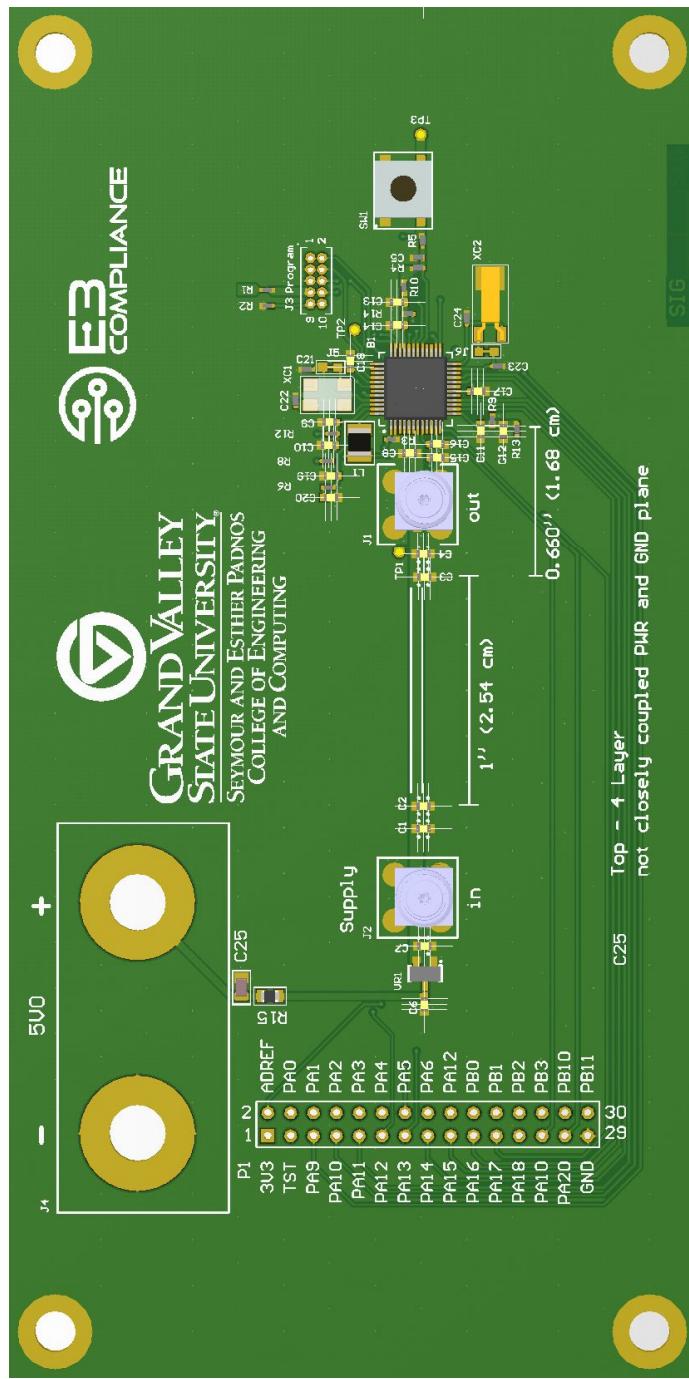


Figure A.8: Embedded capacitance 4-layer design, 3D top view.

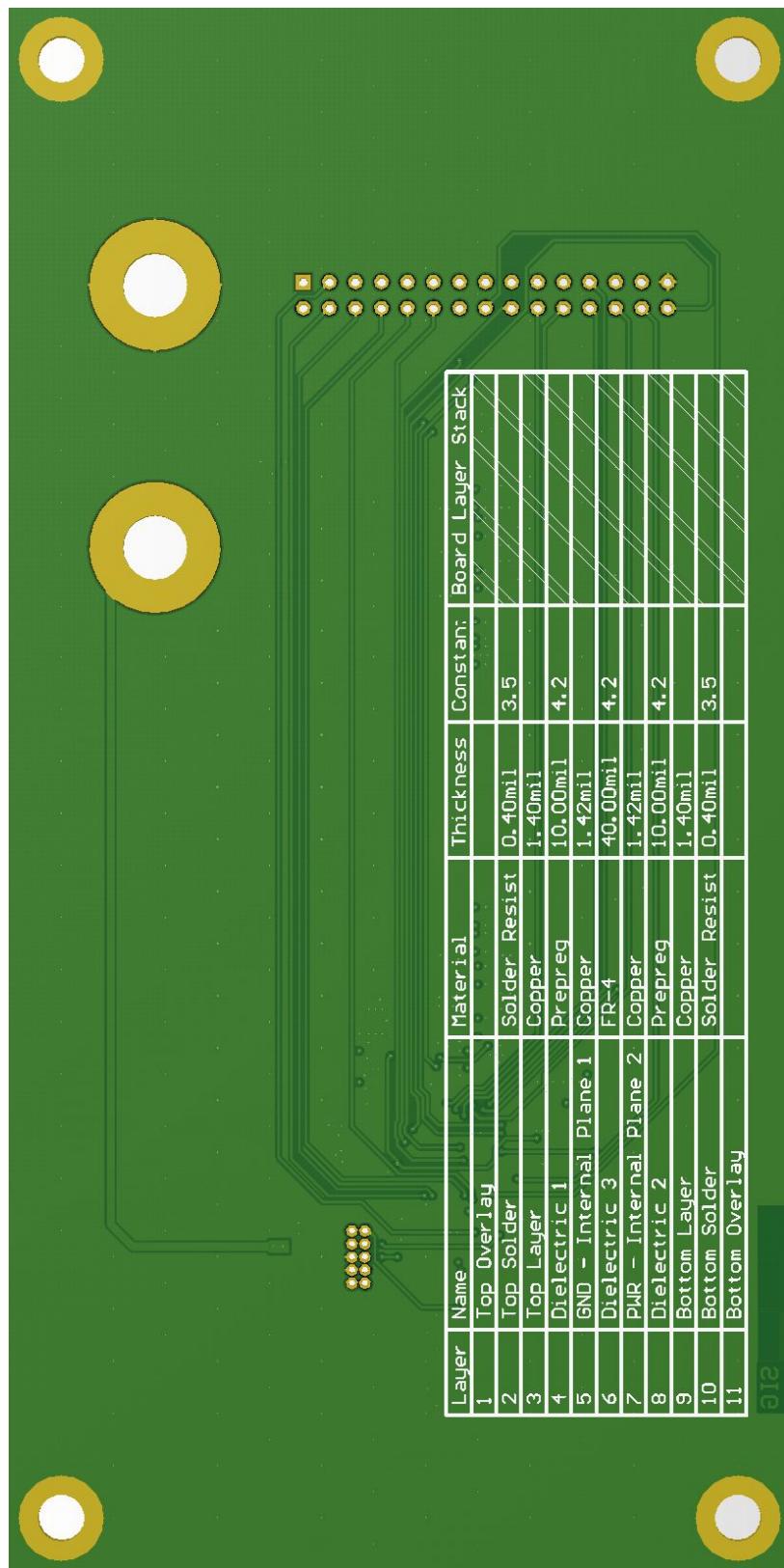


Figure A.9: Embedded capacitance 4-layer design, 3D bottom view.

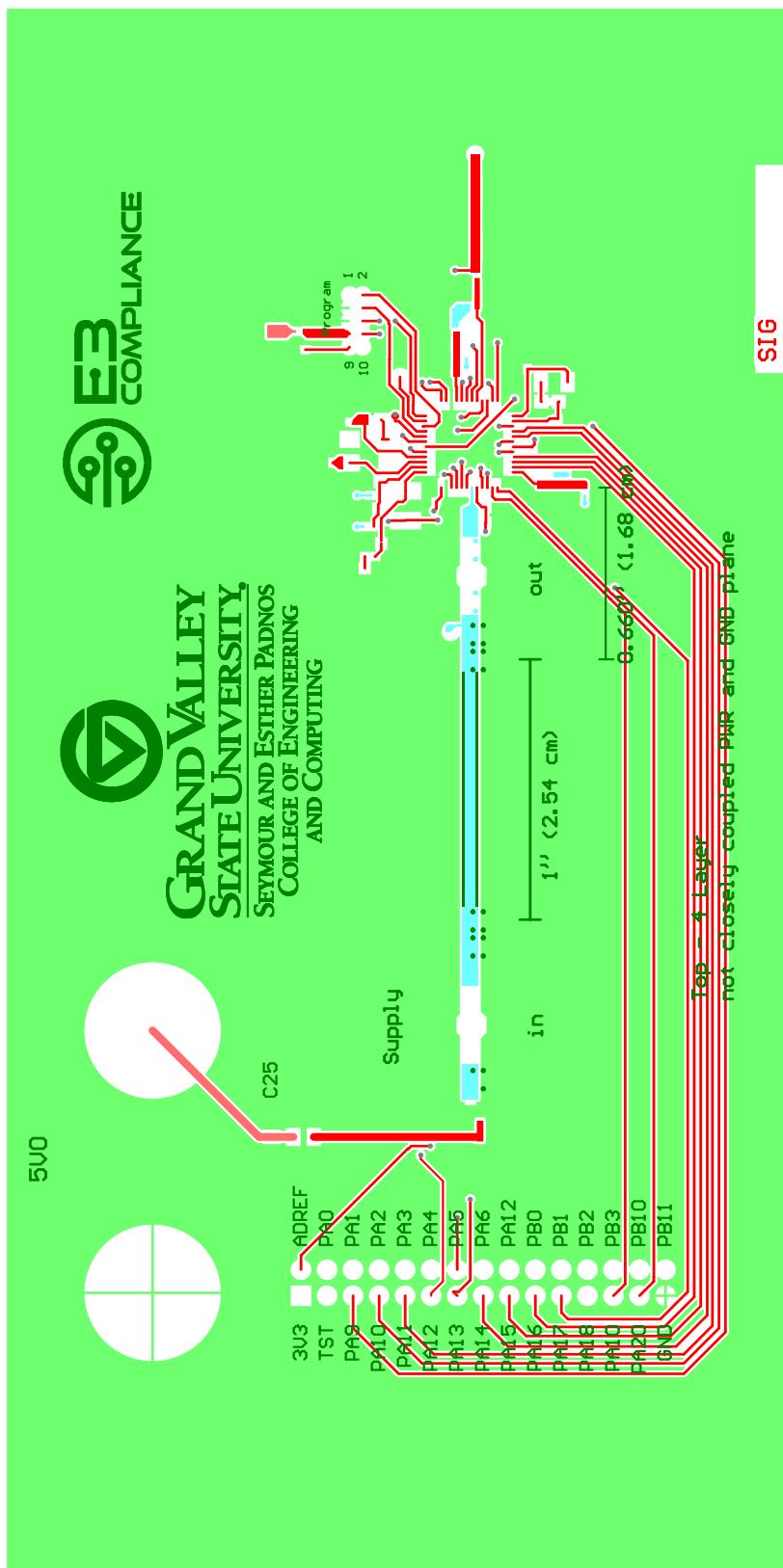


Figure A.10: Embedded capacitance 4-layer design, top layer L1.

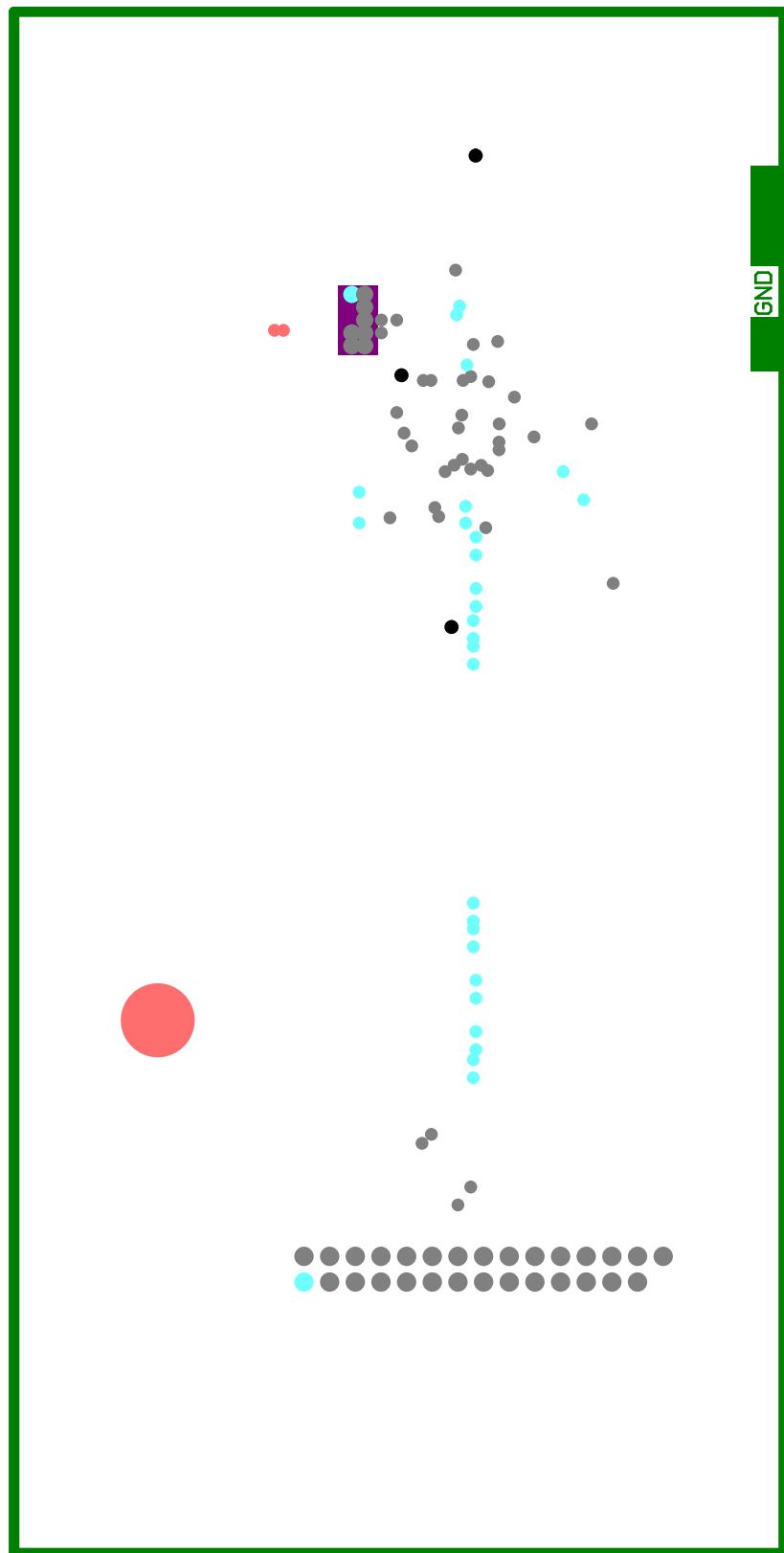


Figure A.11: Embedded capacitance 4-layer design, GND plane L2.

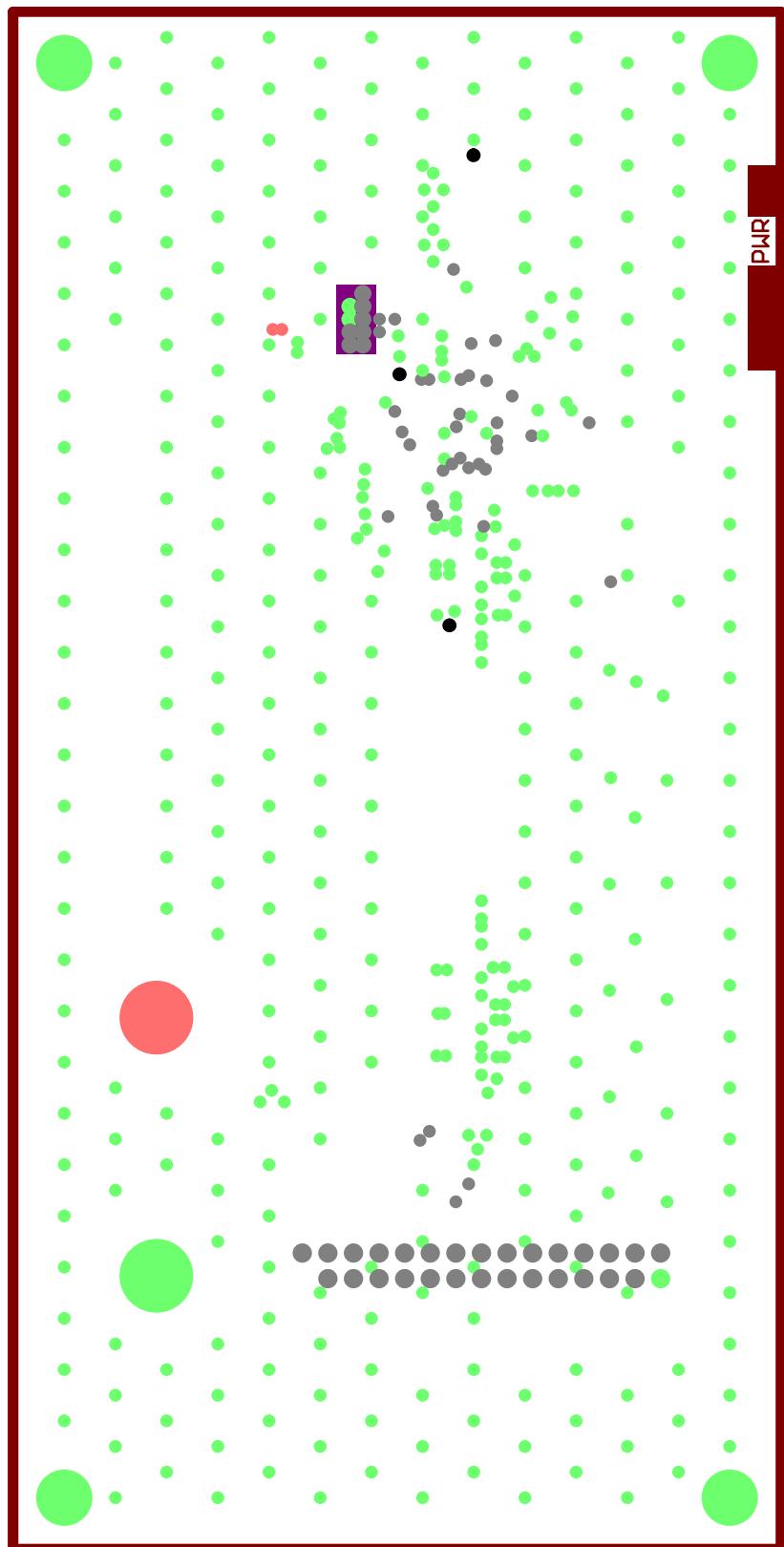


Figure A.12: Embedded capacitance 4-layer design, PWR plane L3.

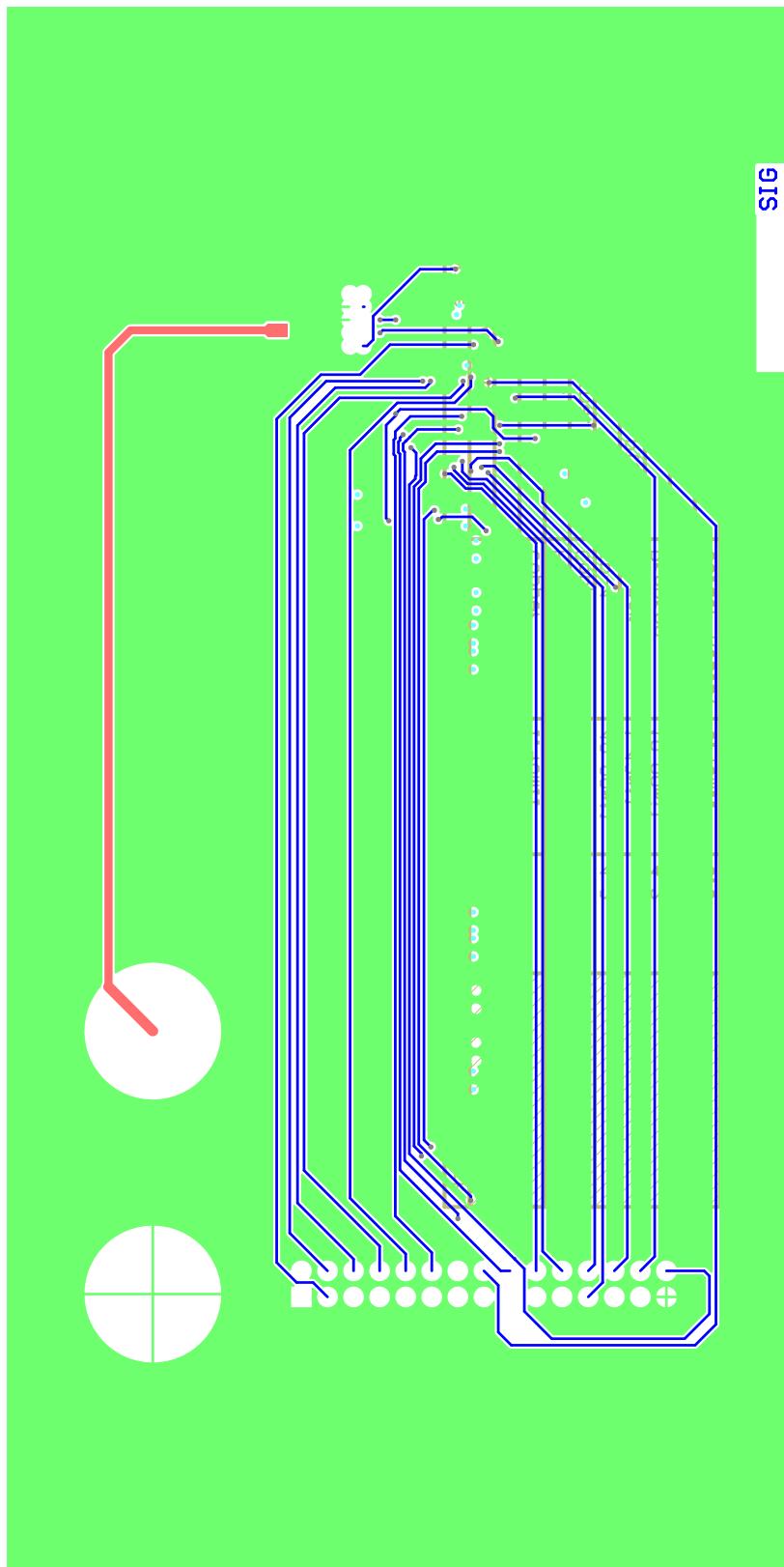


Figure A.13: Embedded capacitance 4-layer design, bottom layer L4.

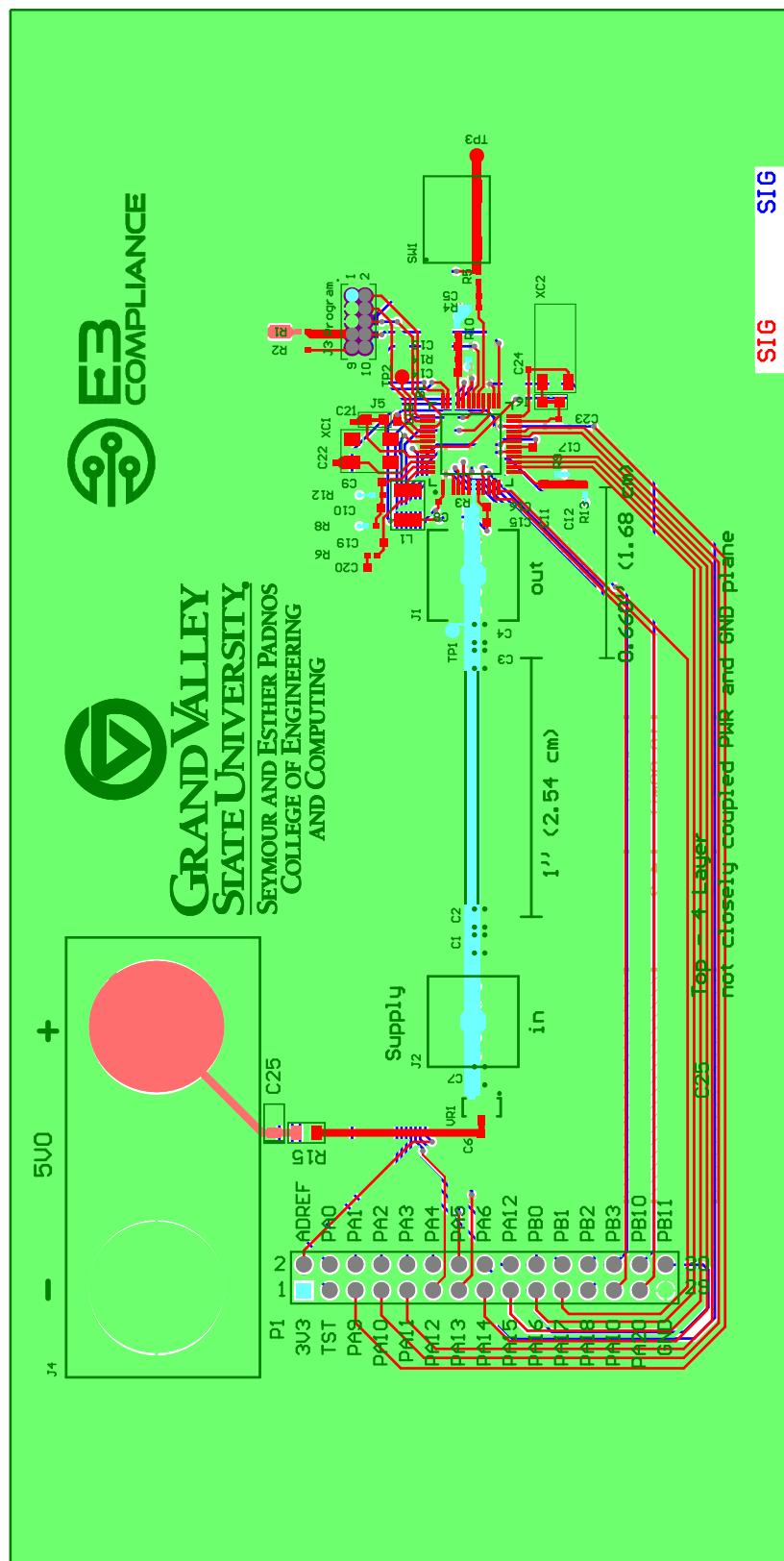


Figure A.14: Embedded capacitance 4-layer design, composite view.

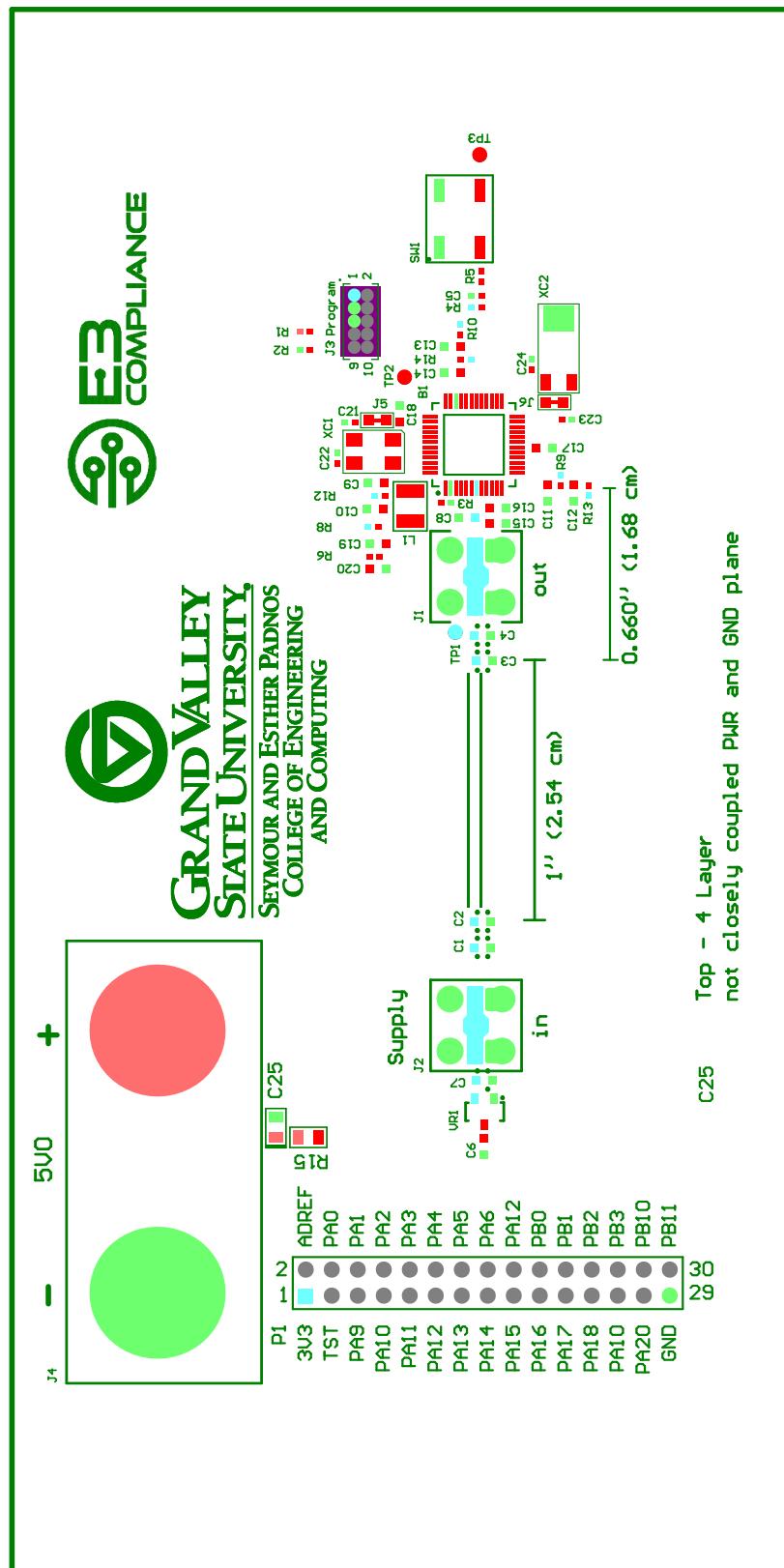


Figure A.15: Embedded capacitance 4-layer design, assembly top.

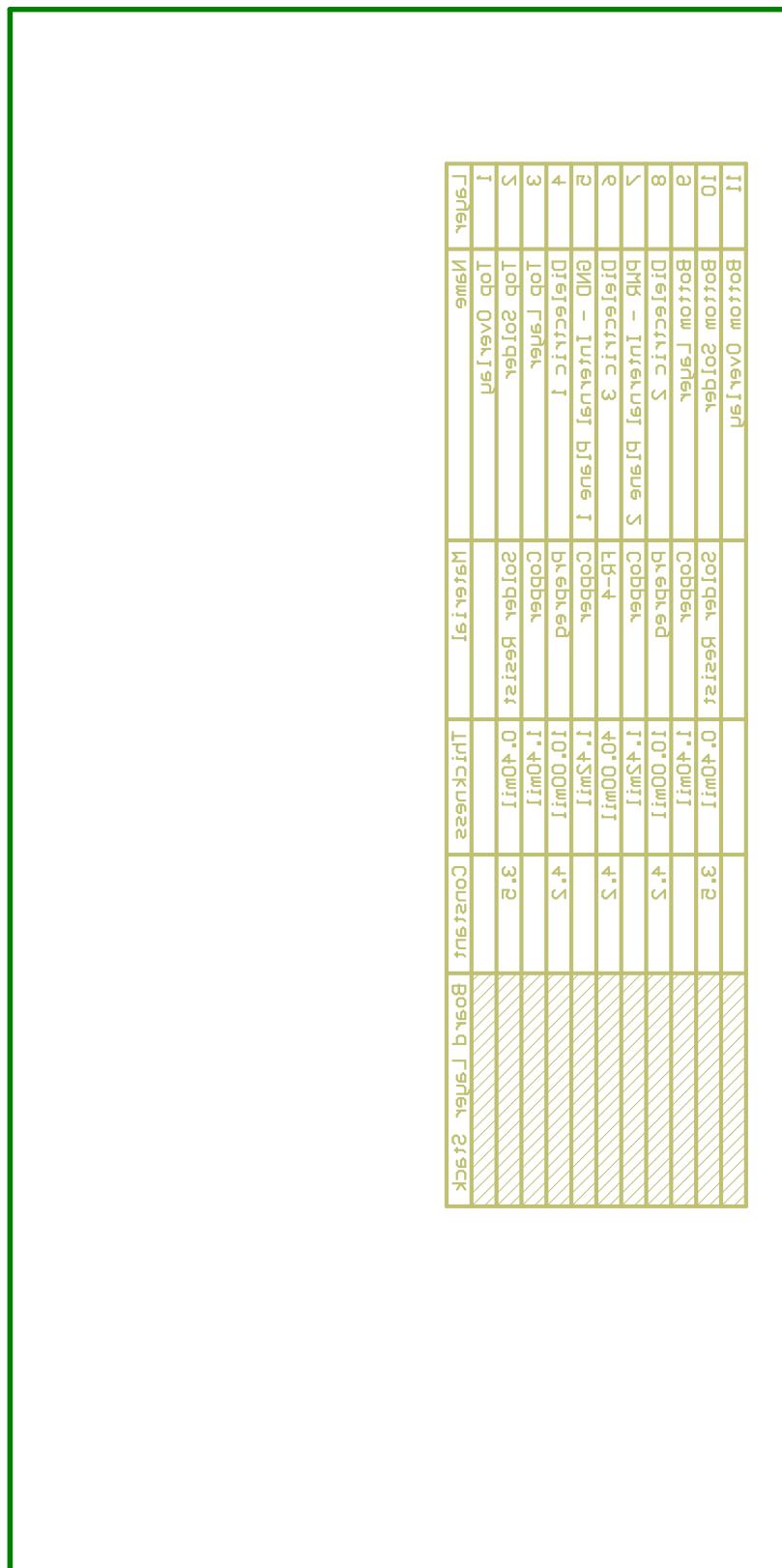


Figure A.16: Embedded capacitance 4-layer design, assembly bottom.

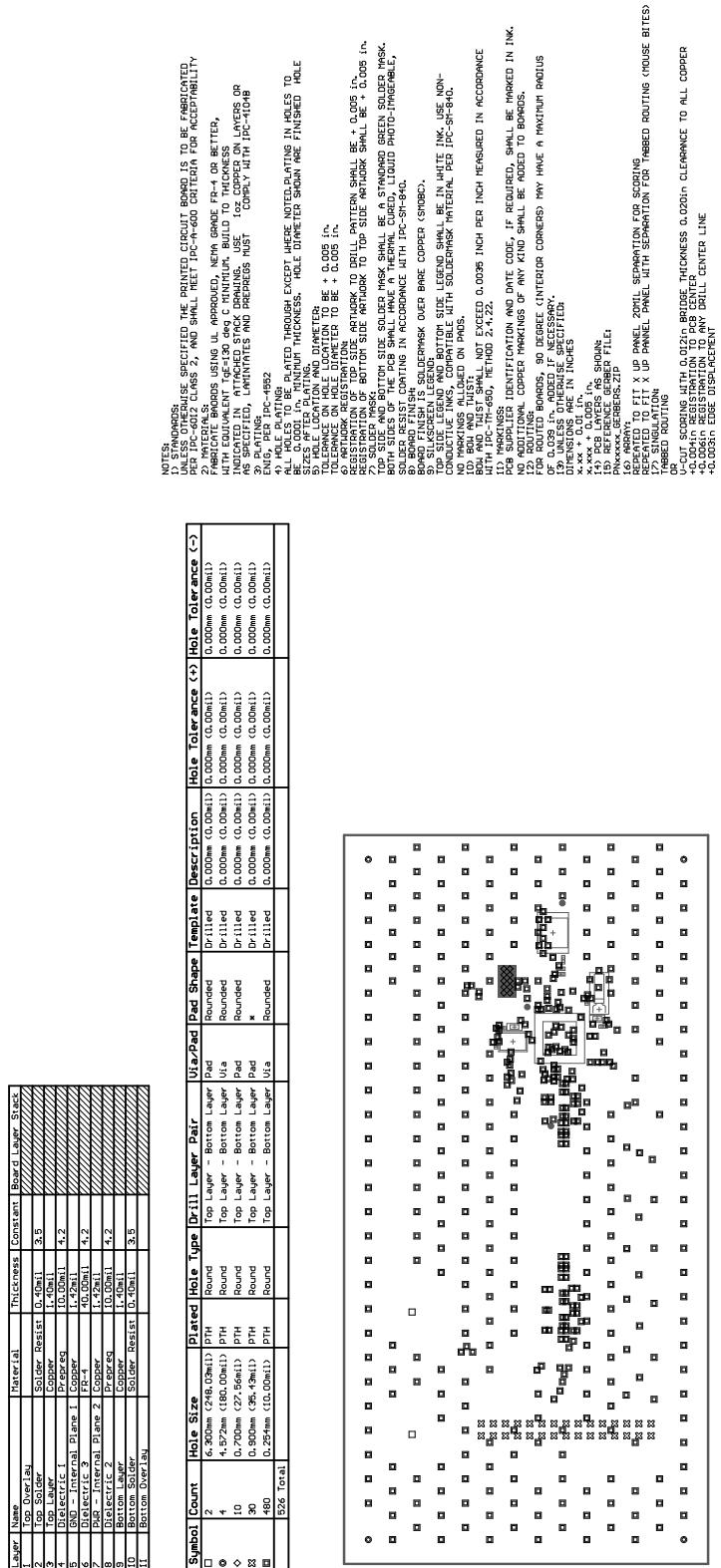


Figure A.17: Embedded capacitance 4-layer design, mechanical drawing top.

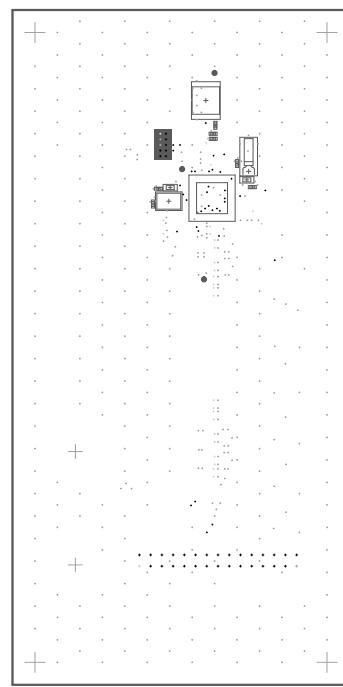


Figure A.18: Embedded capacitance 4-layer design, mechanical drawing bottom.

A.2.4 6-Layer Design

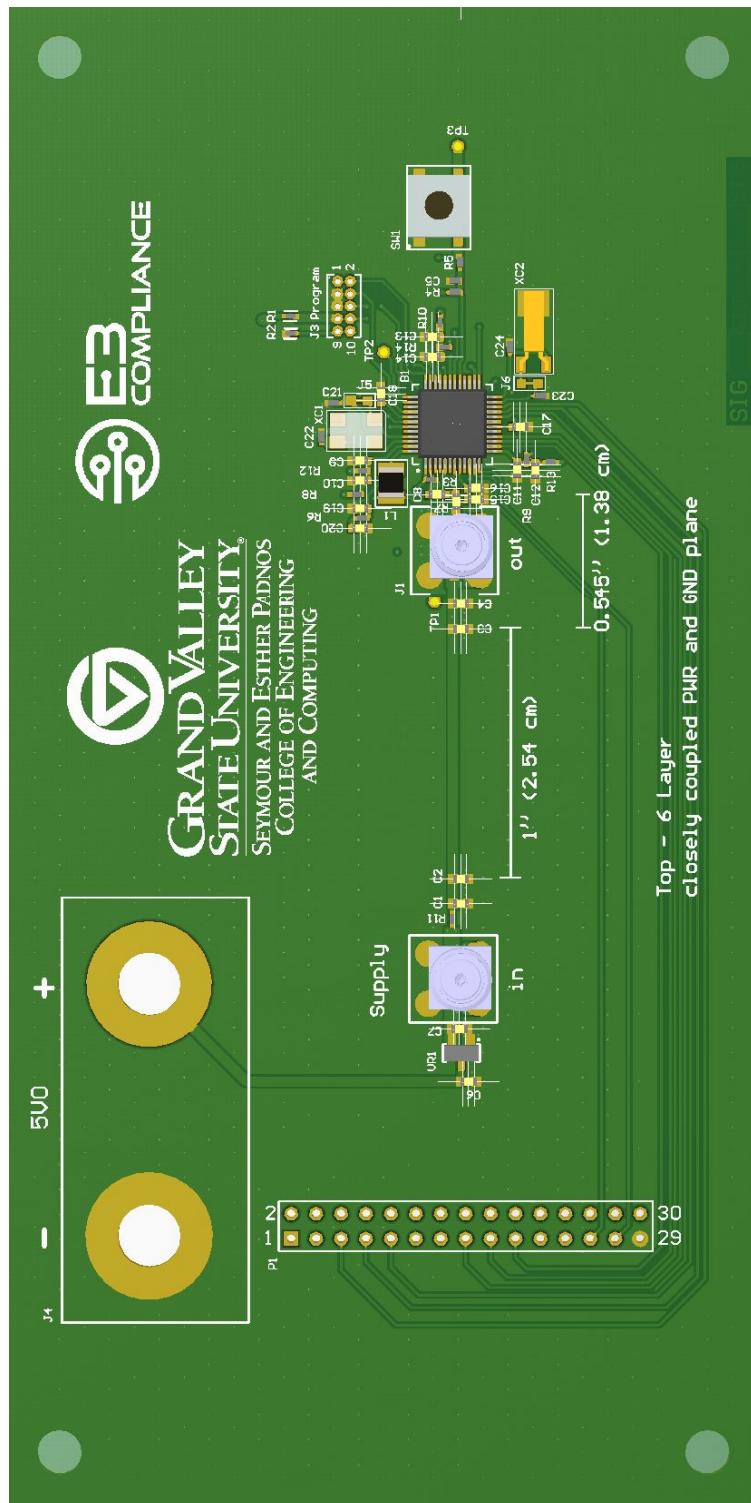


Figure A.19: Embedded capacitance 6-layer design, 3D top view.

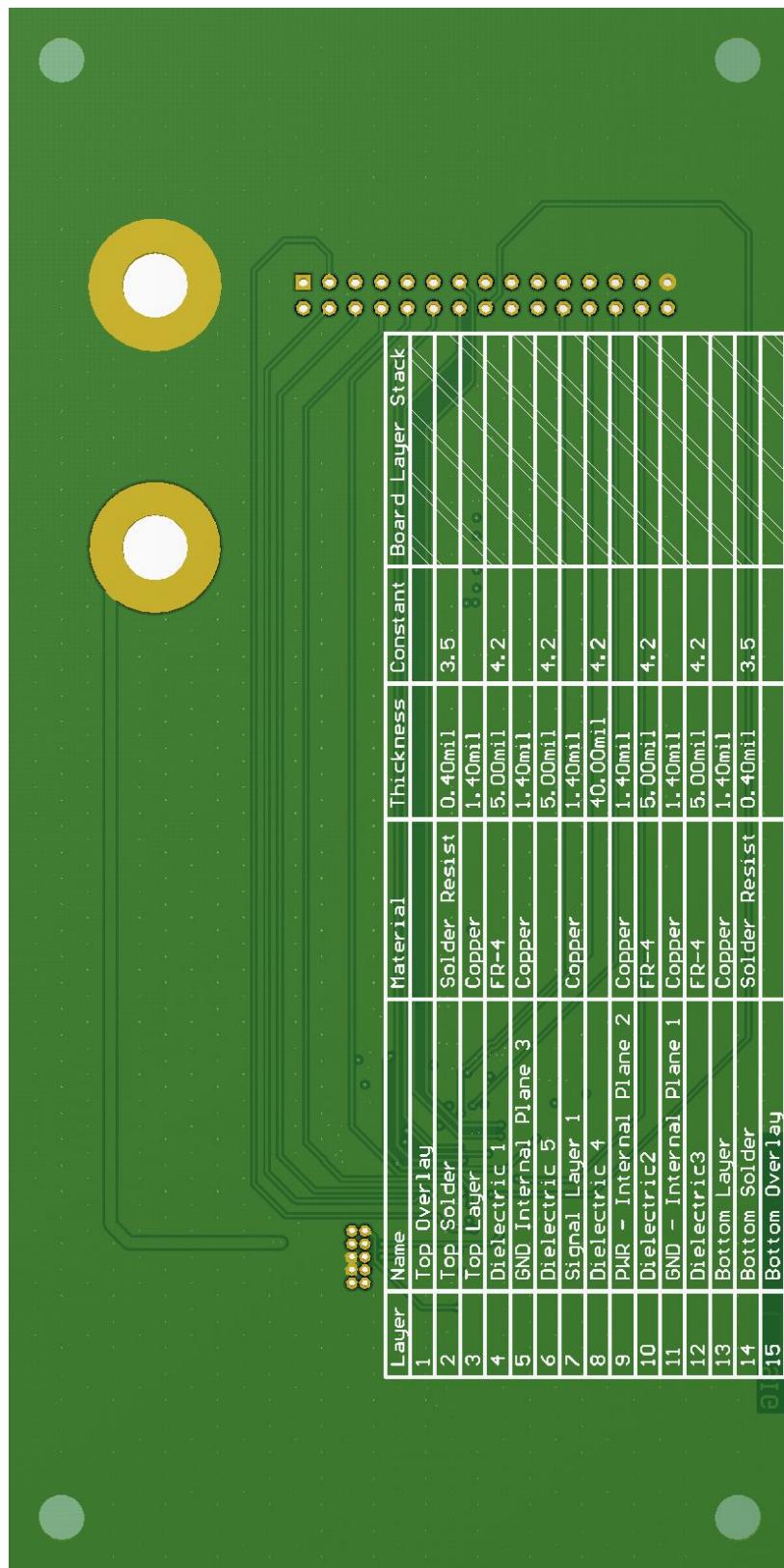


Figure A.20: Embedded capacitance 6-layer design, 3D bottom view.

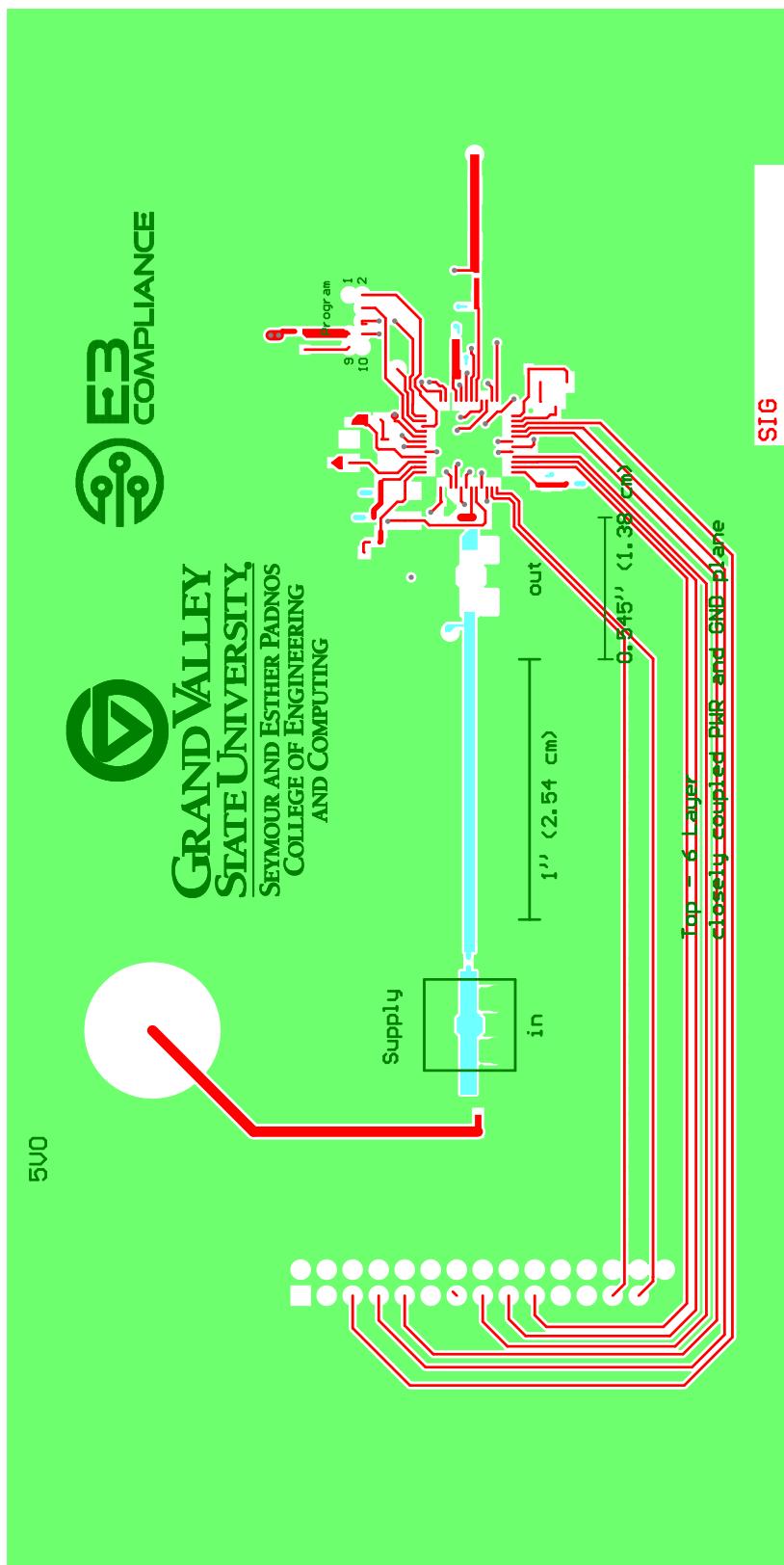


Figure A.21: Embedded capacitance 6-layer design, top layer L1.

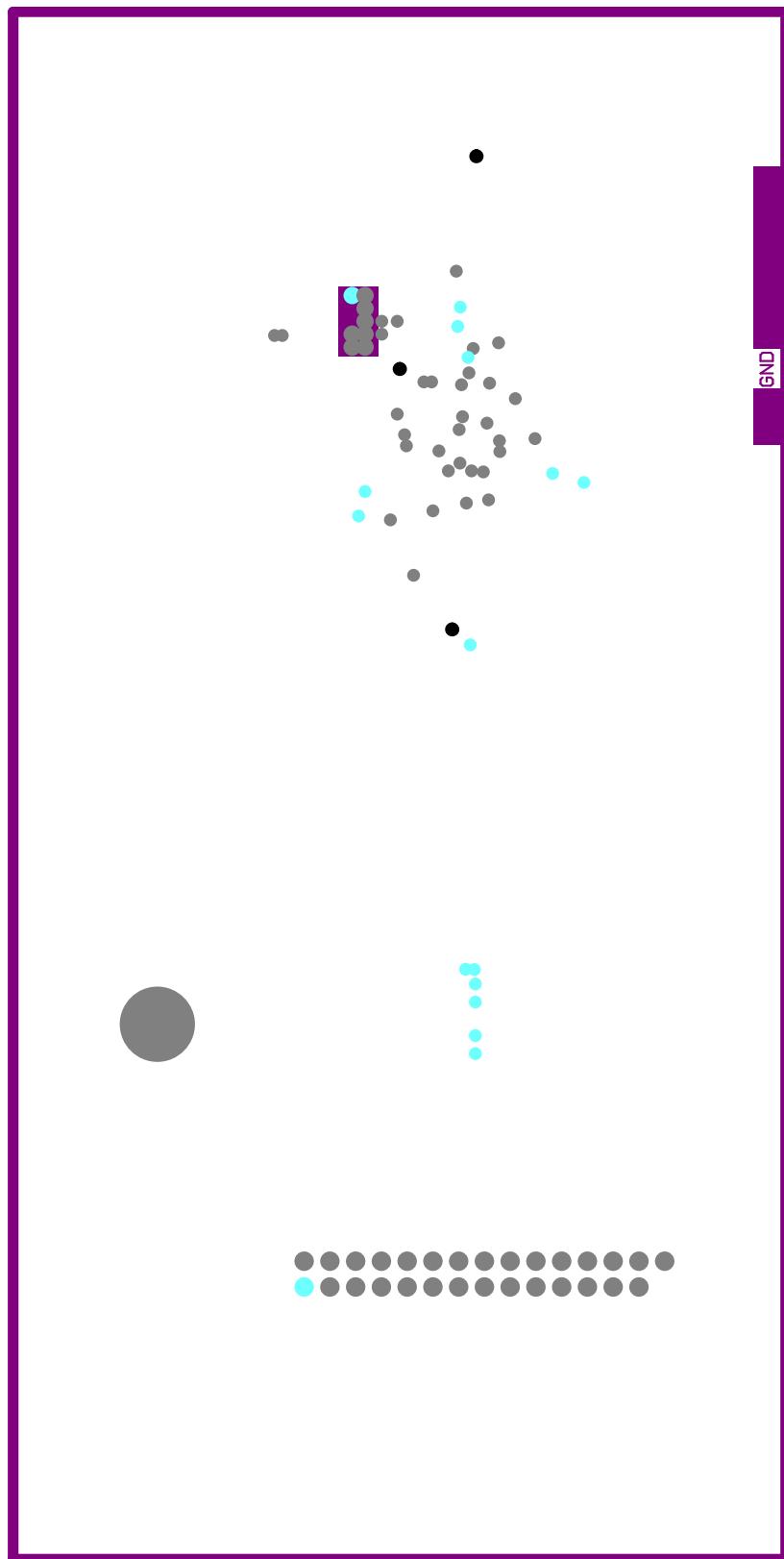


Figure A.22: Embedded capacitance 6-layer design, GND plane L2.

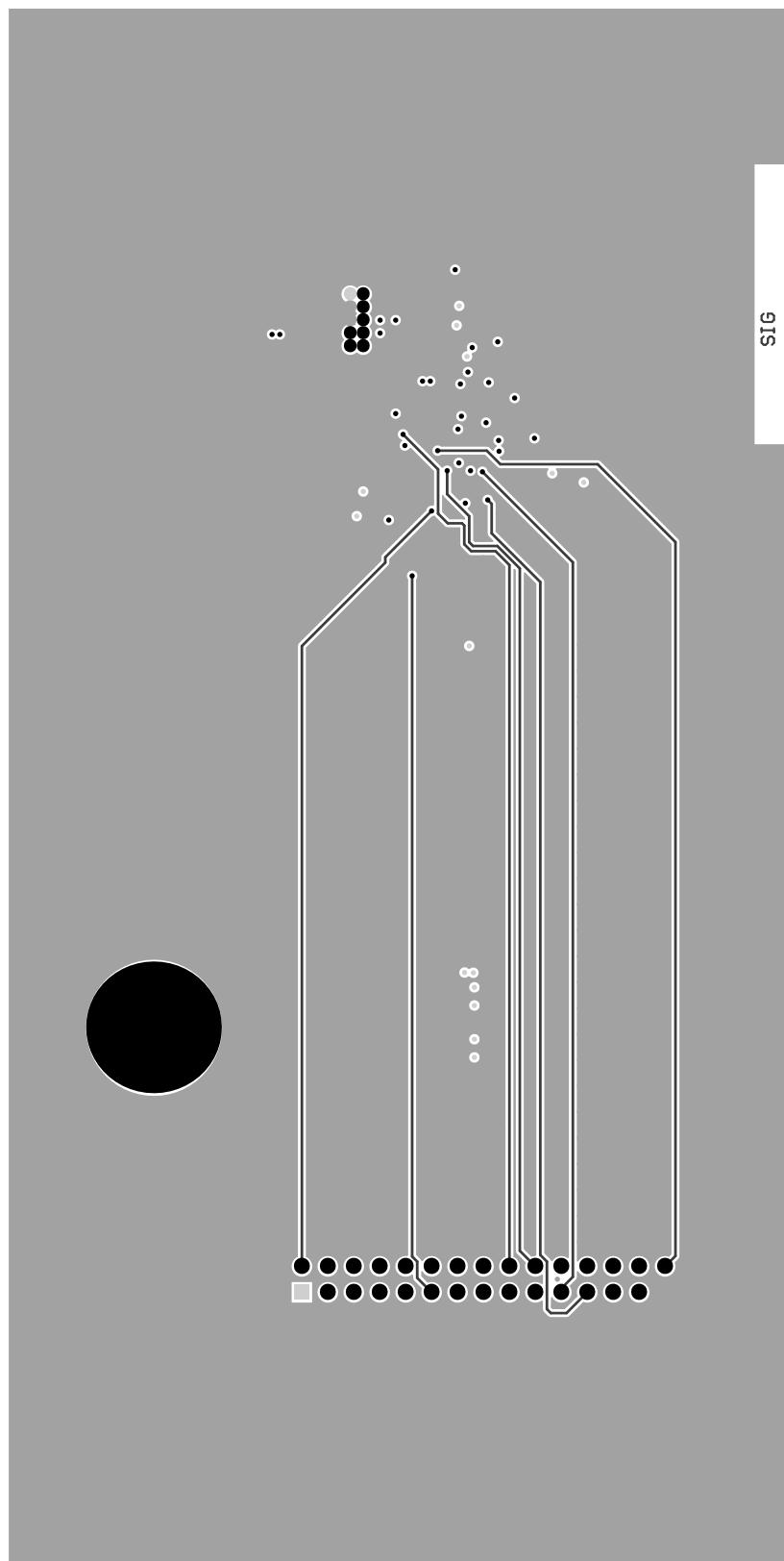


Figure A.23: Embedded capacitance 6-layer design, SIG layer L3.

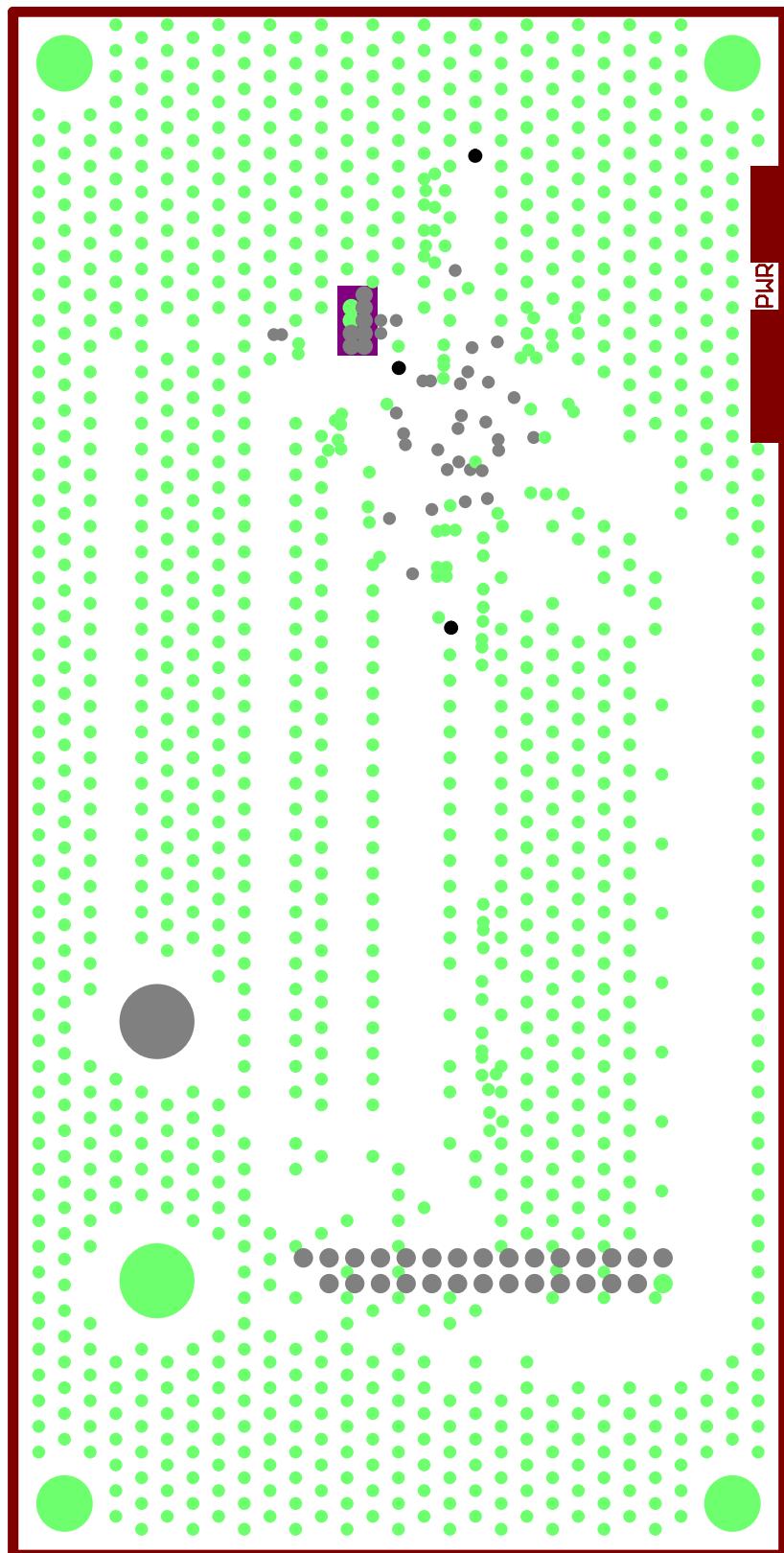


Figure A.24: Embedded capacitance 6-layer design, PWR plane L4.

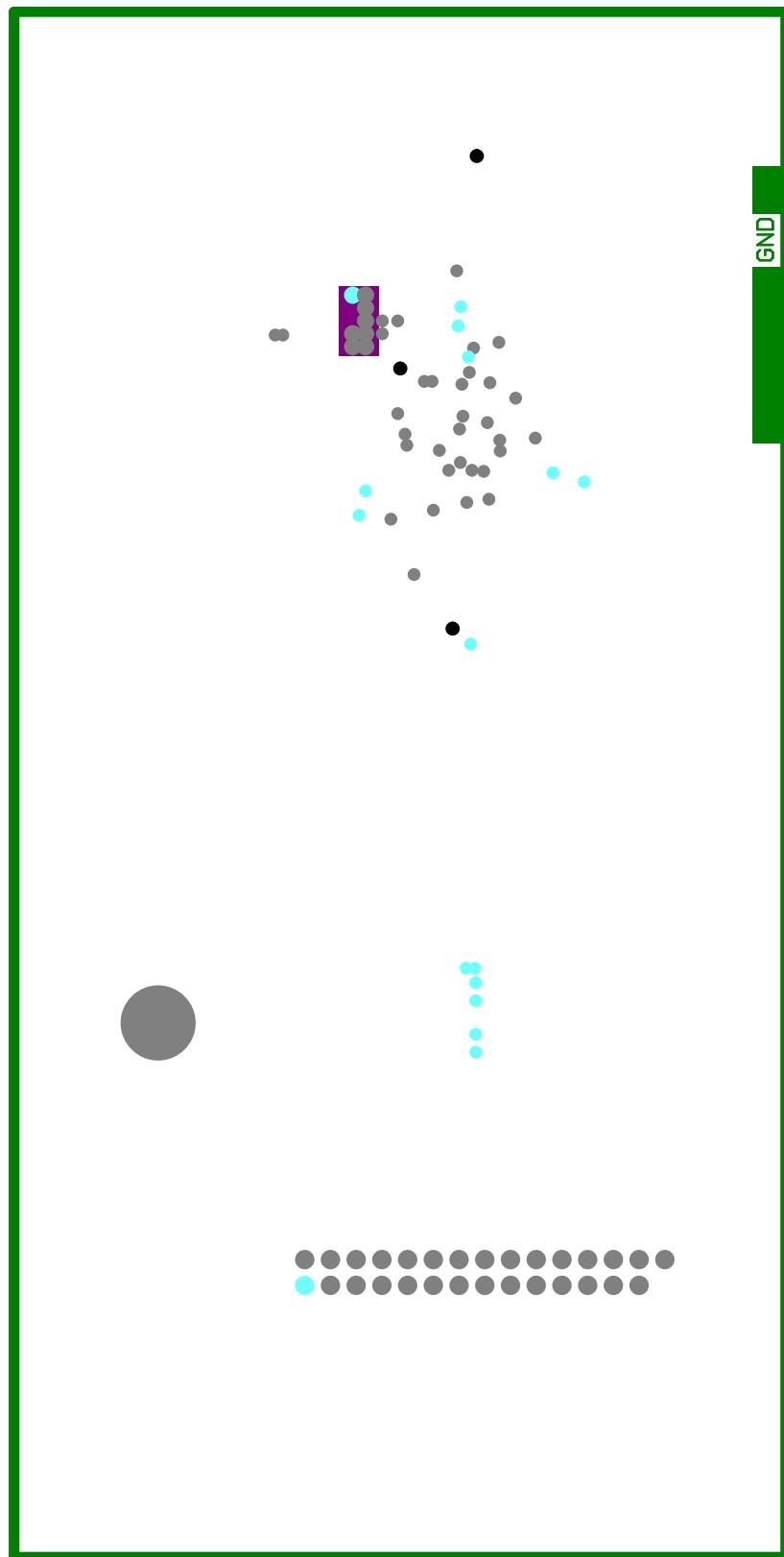


Figure A.25: Embedded capacitance 6-layer design, GND plane L5.

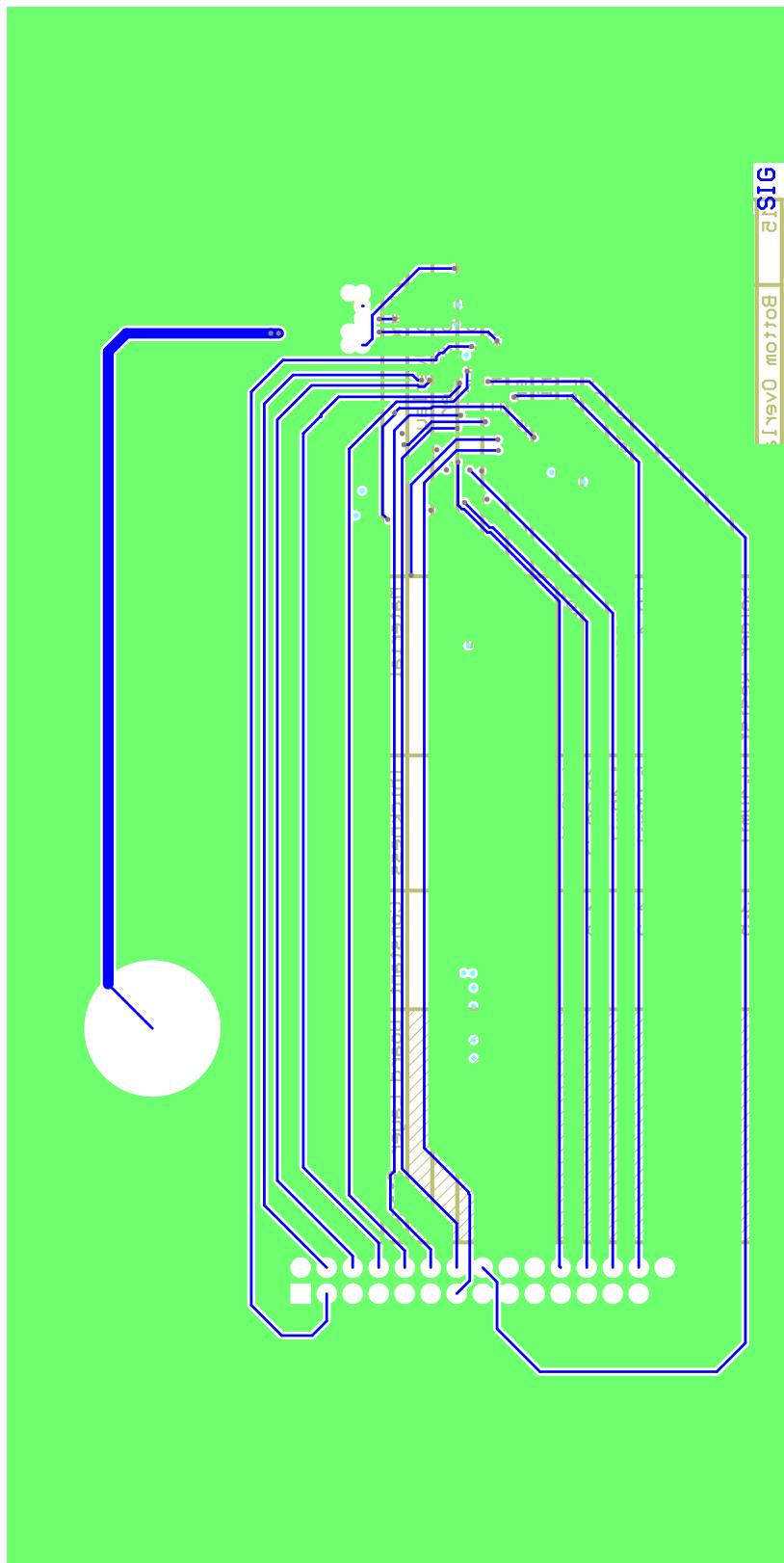


Figure A.26: Embedded capacitance 6-layer design, Bottom Layer L6.

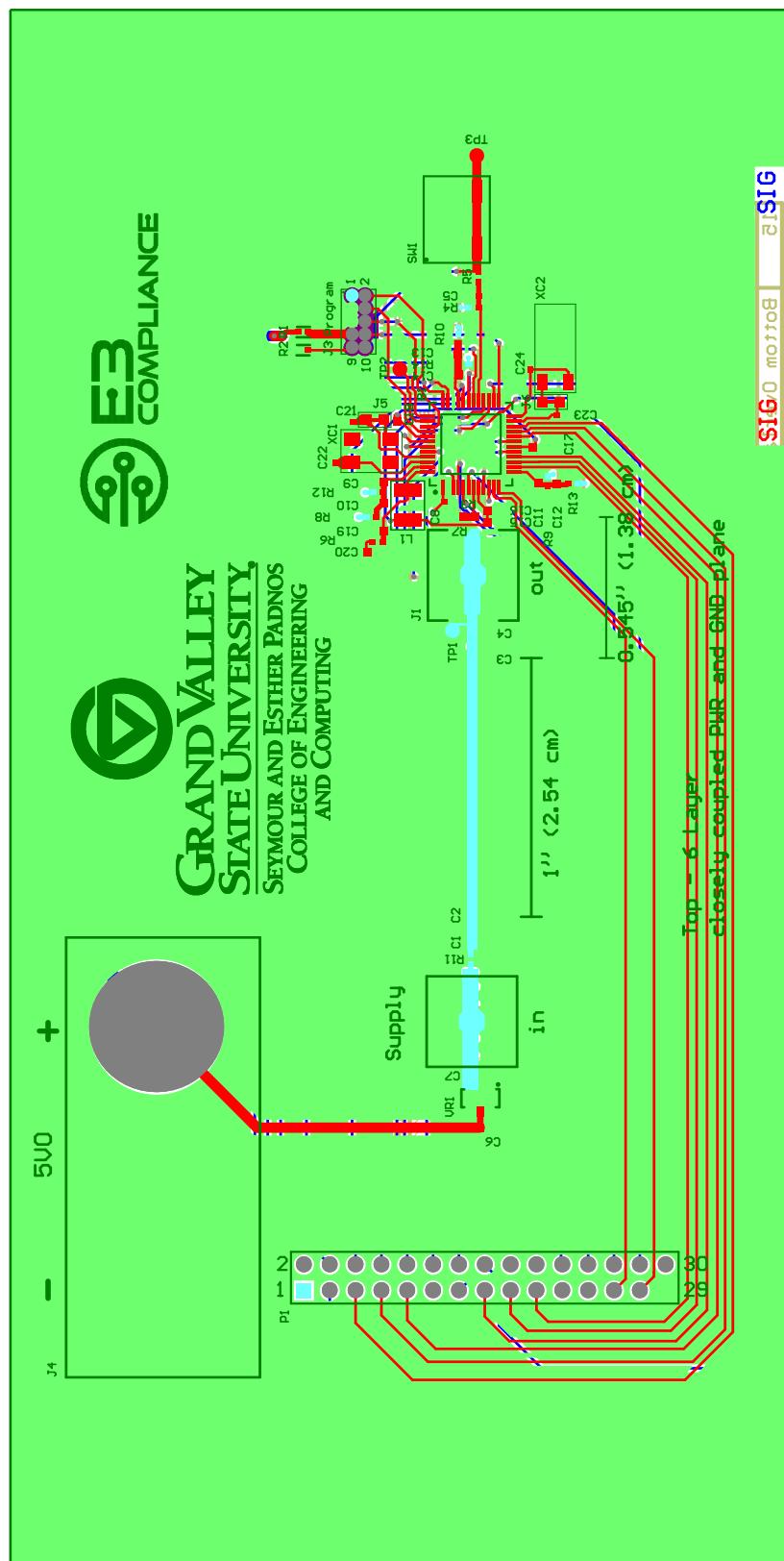


Figure A.27: Embedded capacitance 6-layer design, composite view.

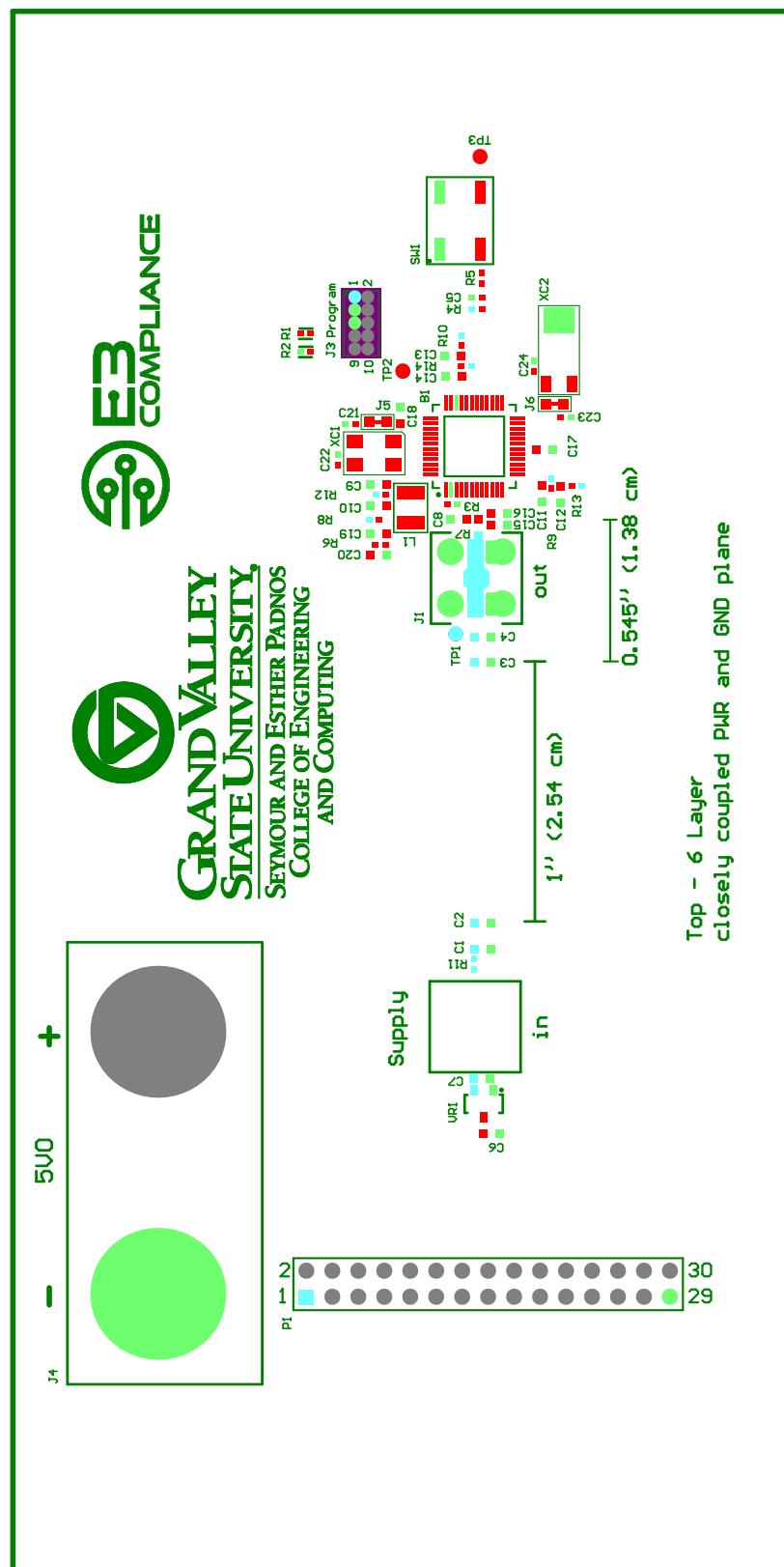


Figure A.28: Embedded capacitance 6-layer design, assembly top.

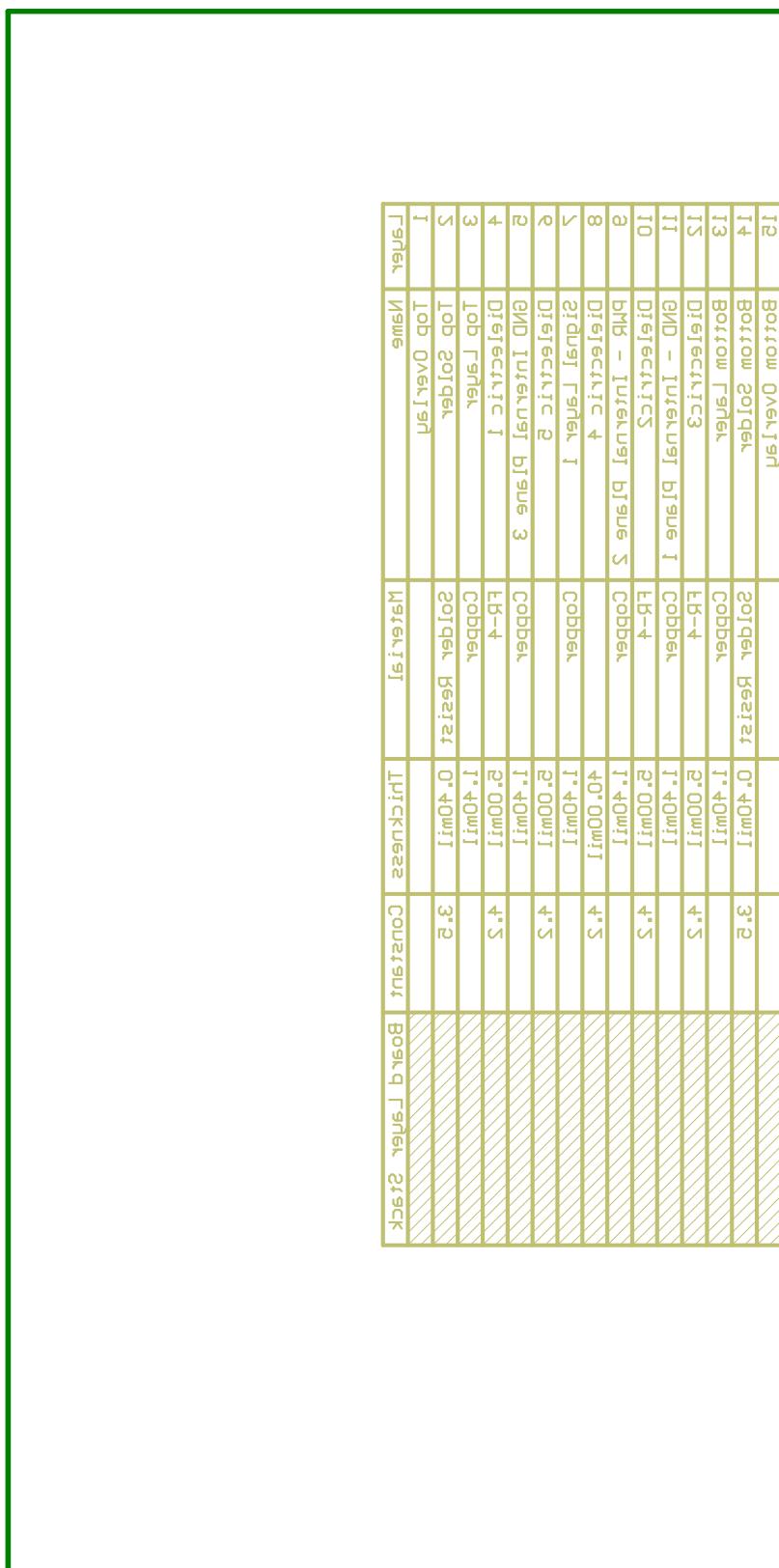


Figure A.29: Embedded capacitance 6-layer design, assembly bottom.

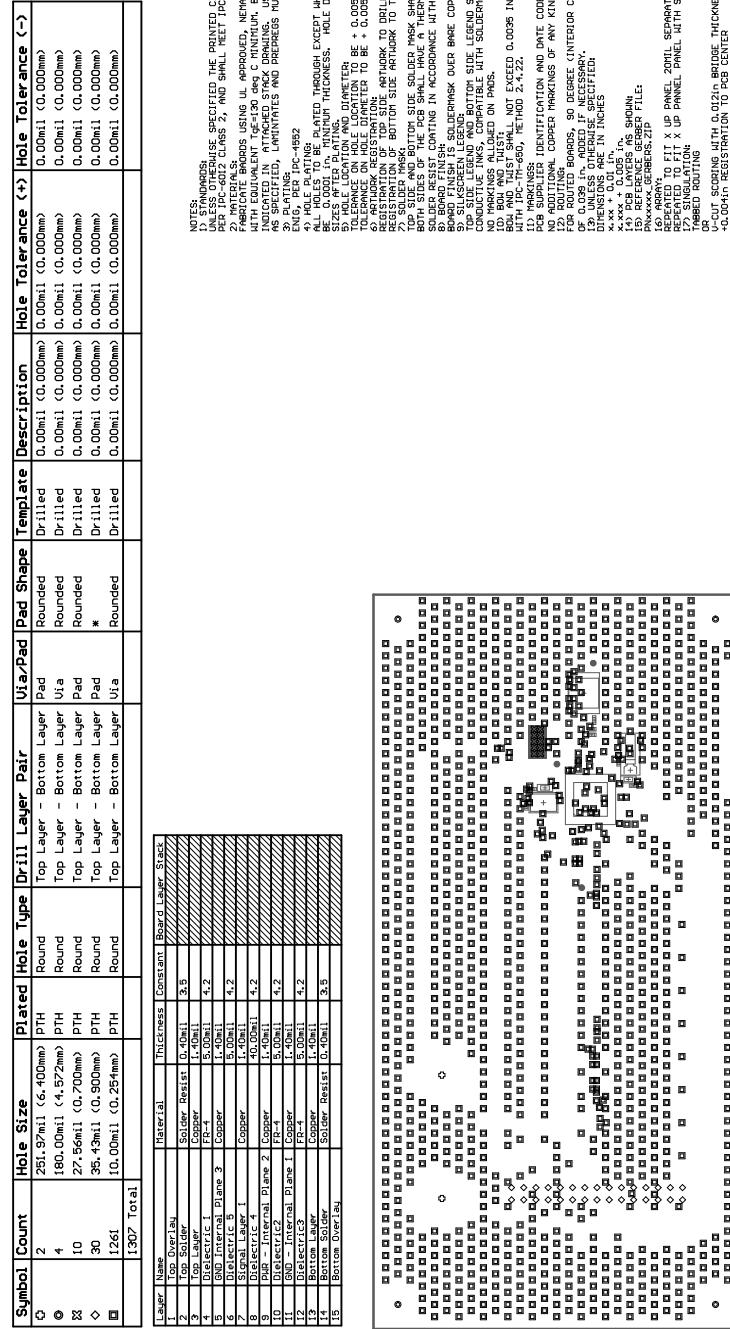


Figure A.30: Embedded capacitance 6-layer design, mechanical drawing top.

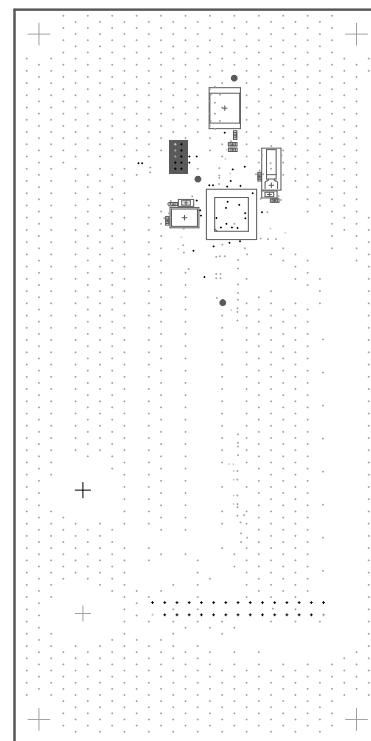


Figure A.31: Embedded capacitance 6-layer design, mechanical drawing bottom.

A.2.5 6-Layer version 3 Design

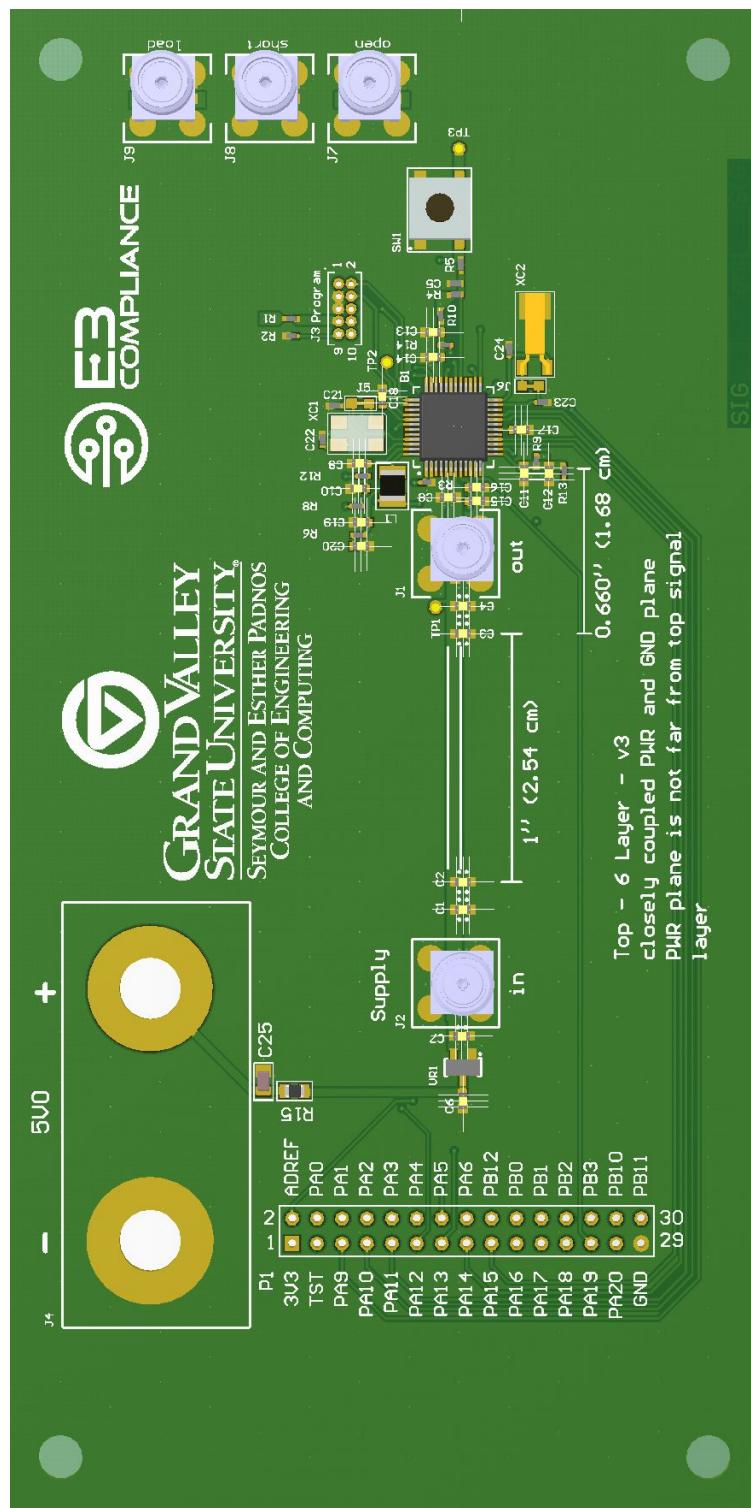


Figure A.32: Embedded capacitance 6-layer version 3 design, 3D top view.

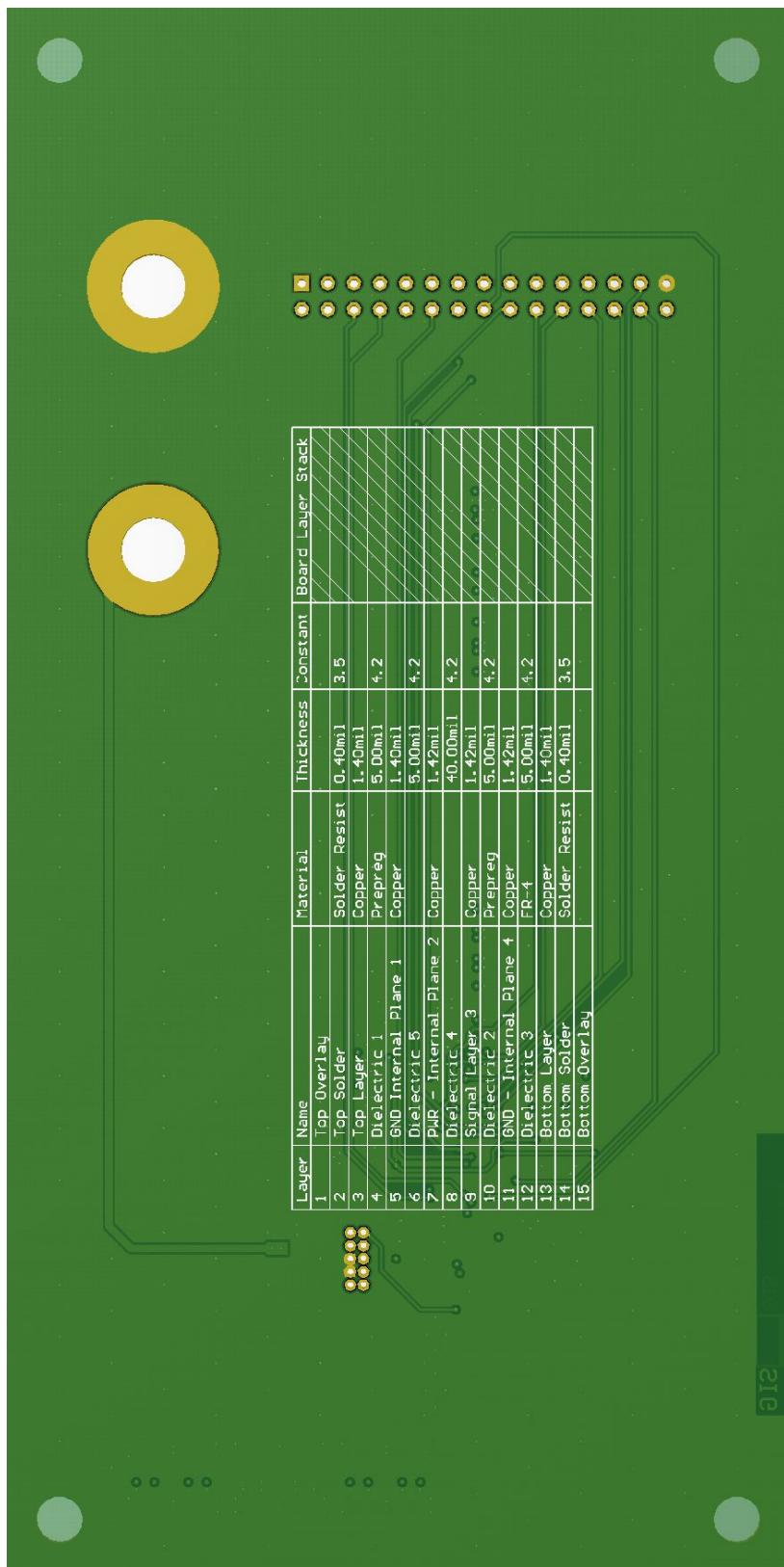


Figure A.33: Embedded capacitance 6-layer version 3 design, 3D bottom view.

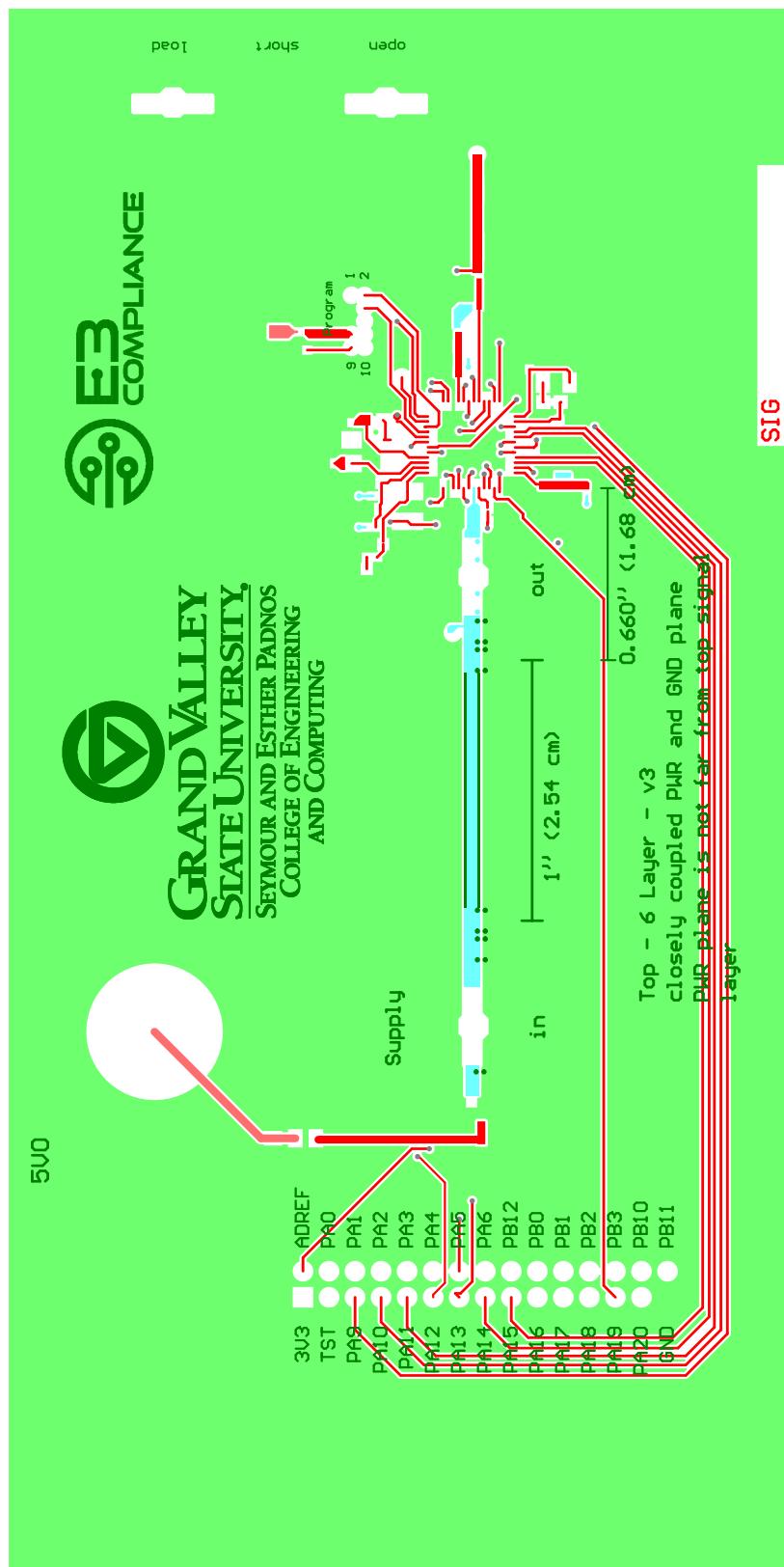


Figure A.34: Embedded capacitance 6-layer version 3 design, top layer L1.

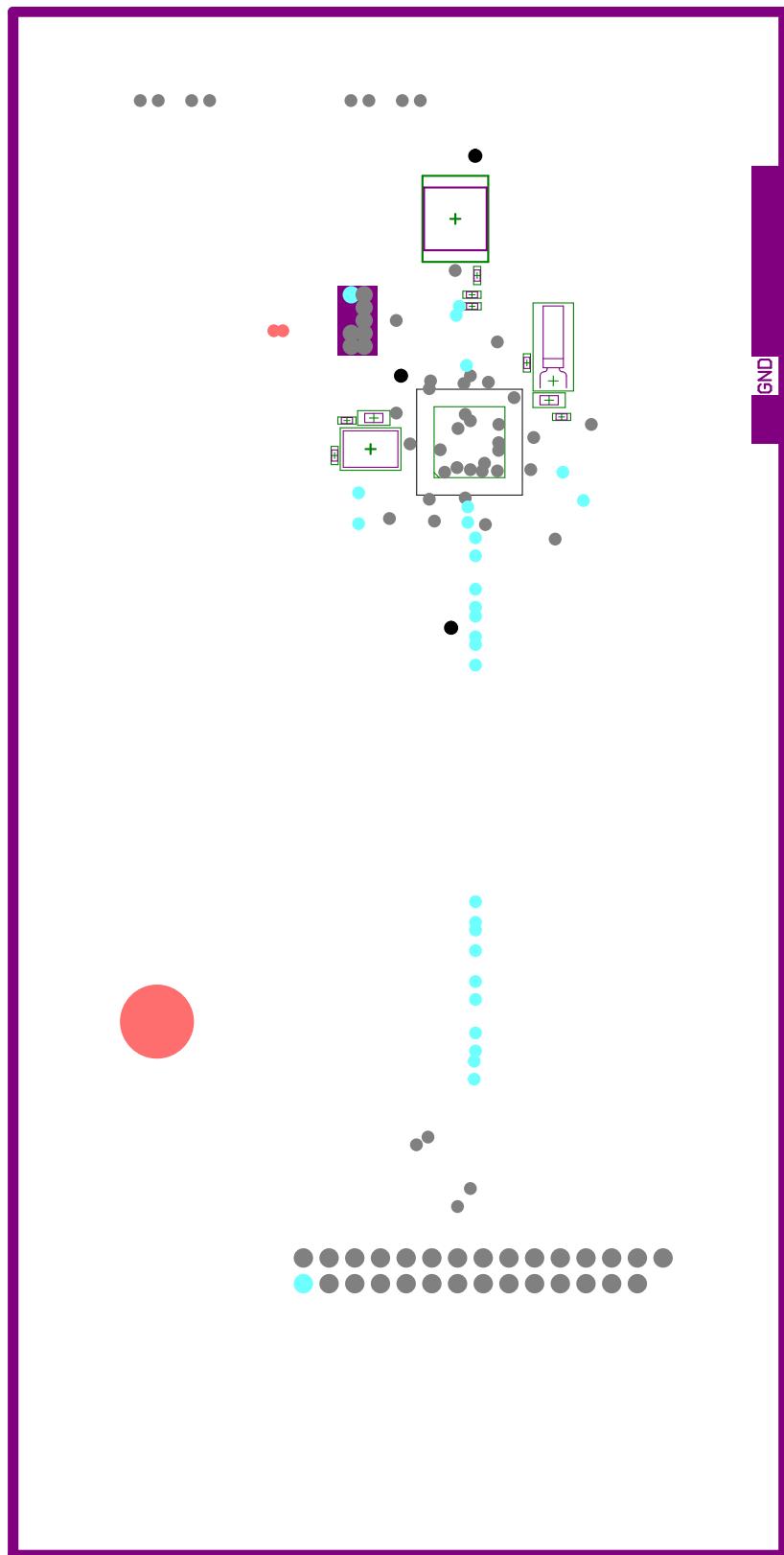


Figure A.35: Embedded capacitance 6-layer version 3 design, GND plane L2.

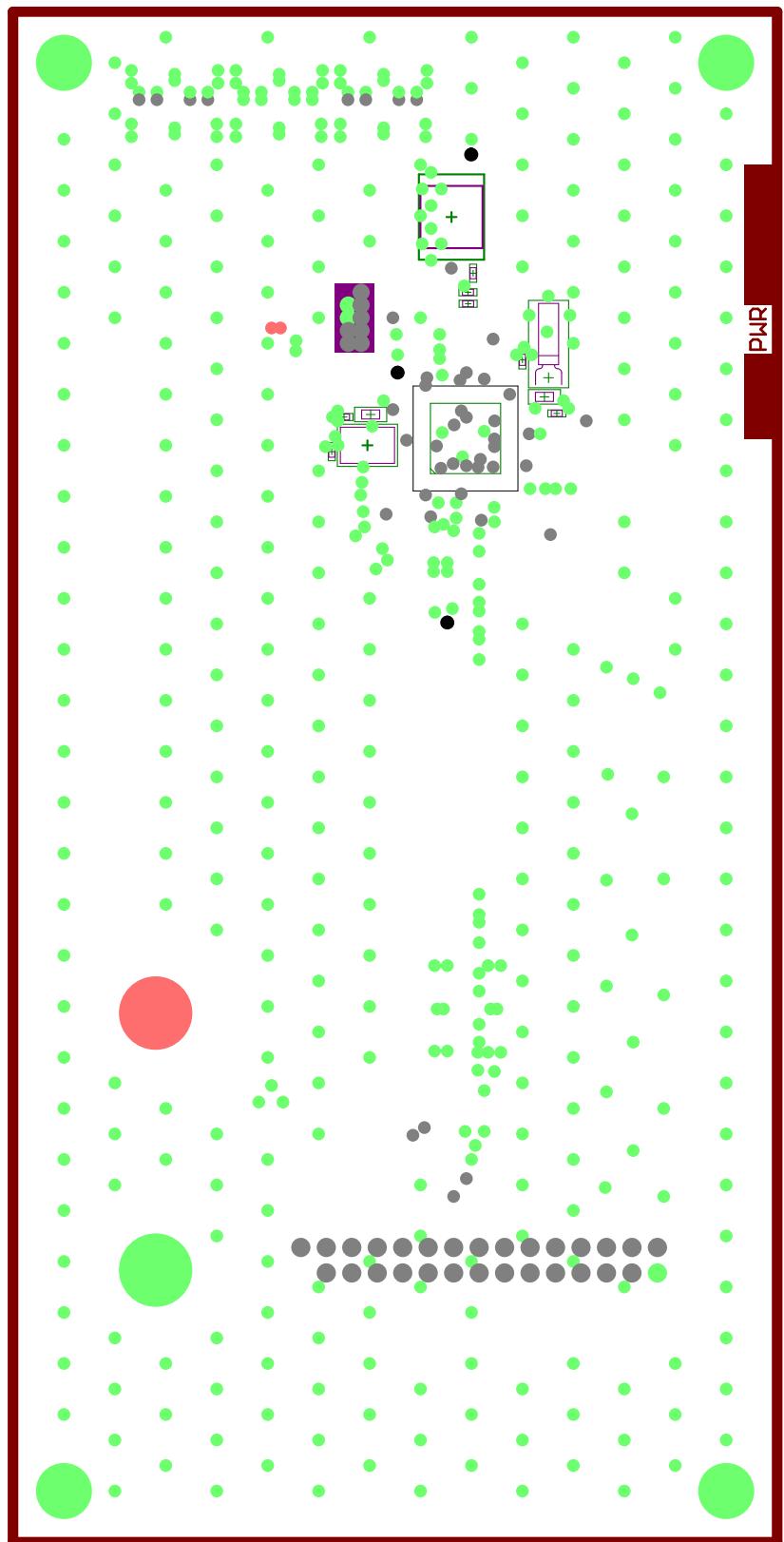


Figure A.36: Embedded capacitance 6-layer version 3 design, PWR plane L3.

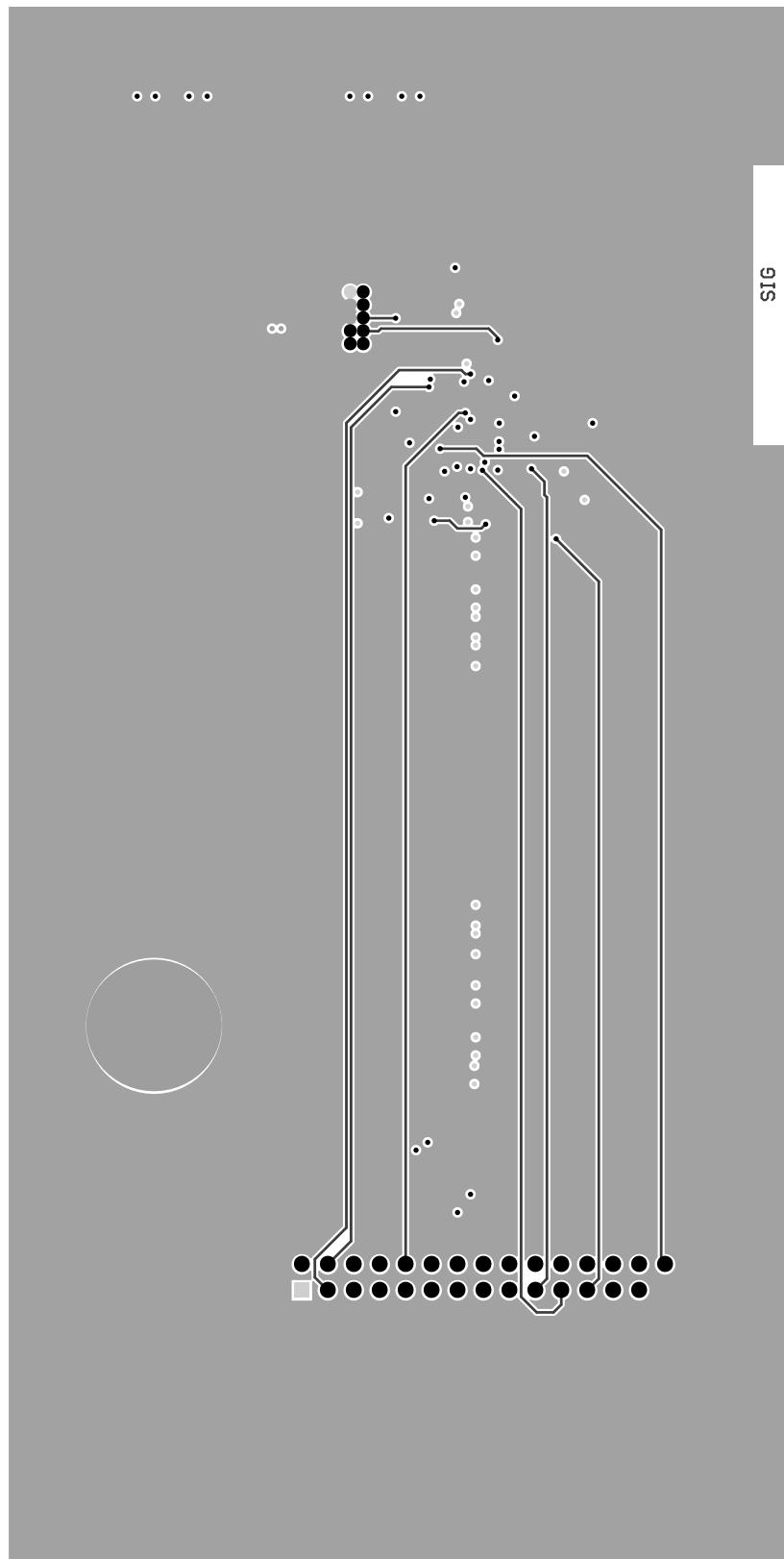


Figure A.37: Embedded capacitance 6-layer version 3 design, SIG layer L4.

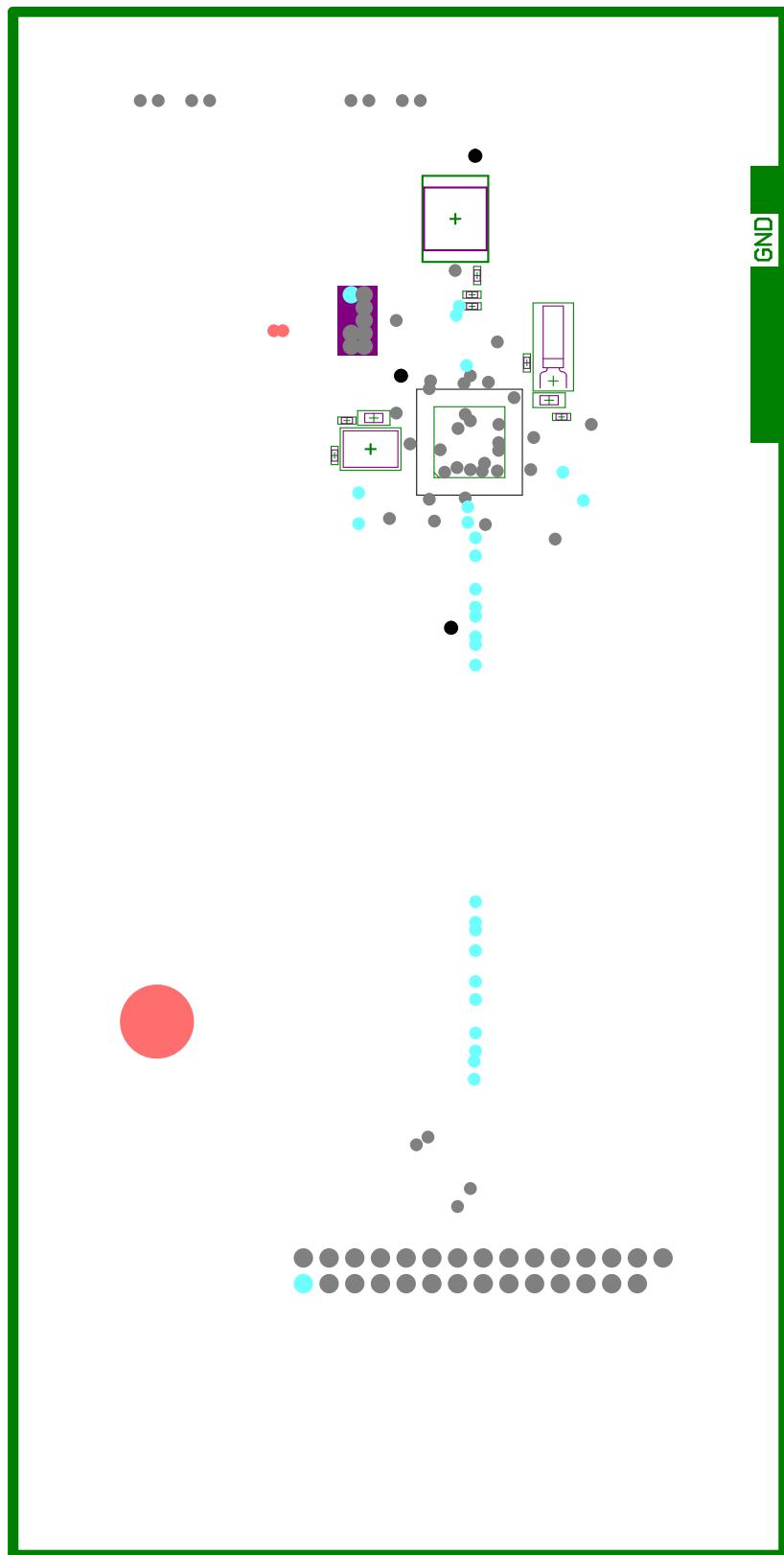


Figure A.38: Embedded capacitance 6-layer version 3 design, GND plane L5.

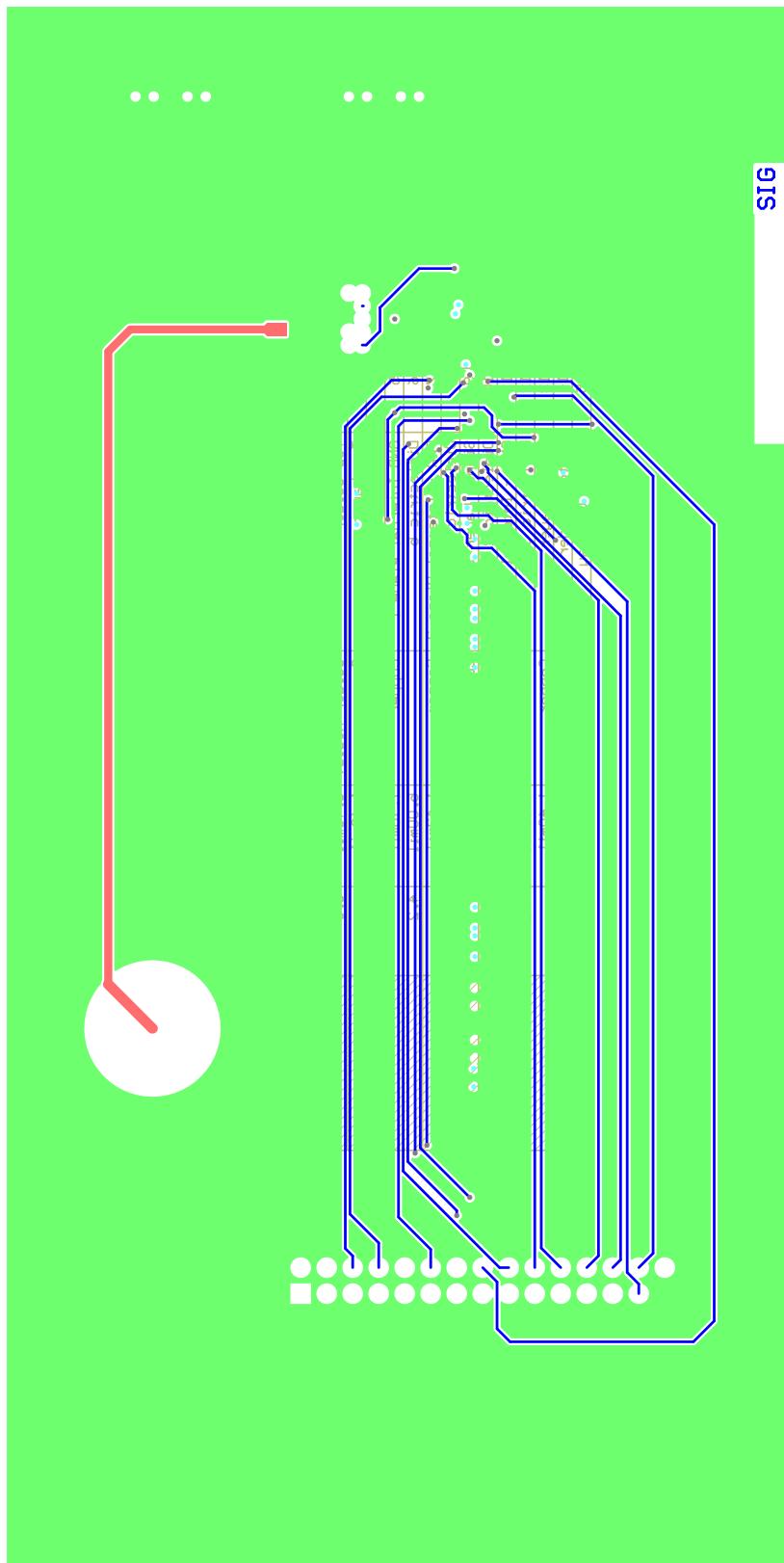


Figure A.39: Embedded capacitance 6-layer version 3 design, Bottom Layer L6.

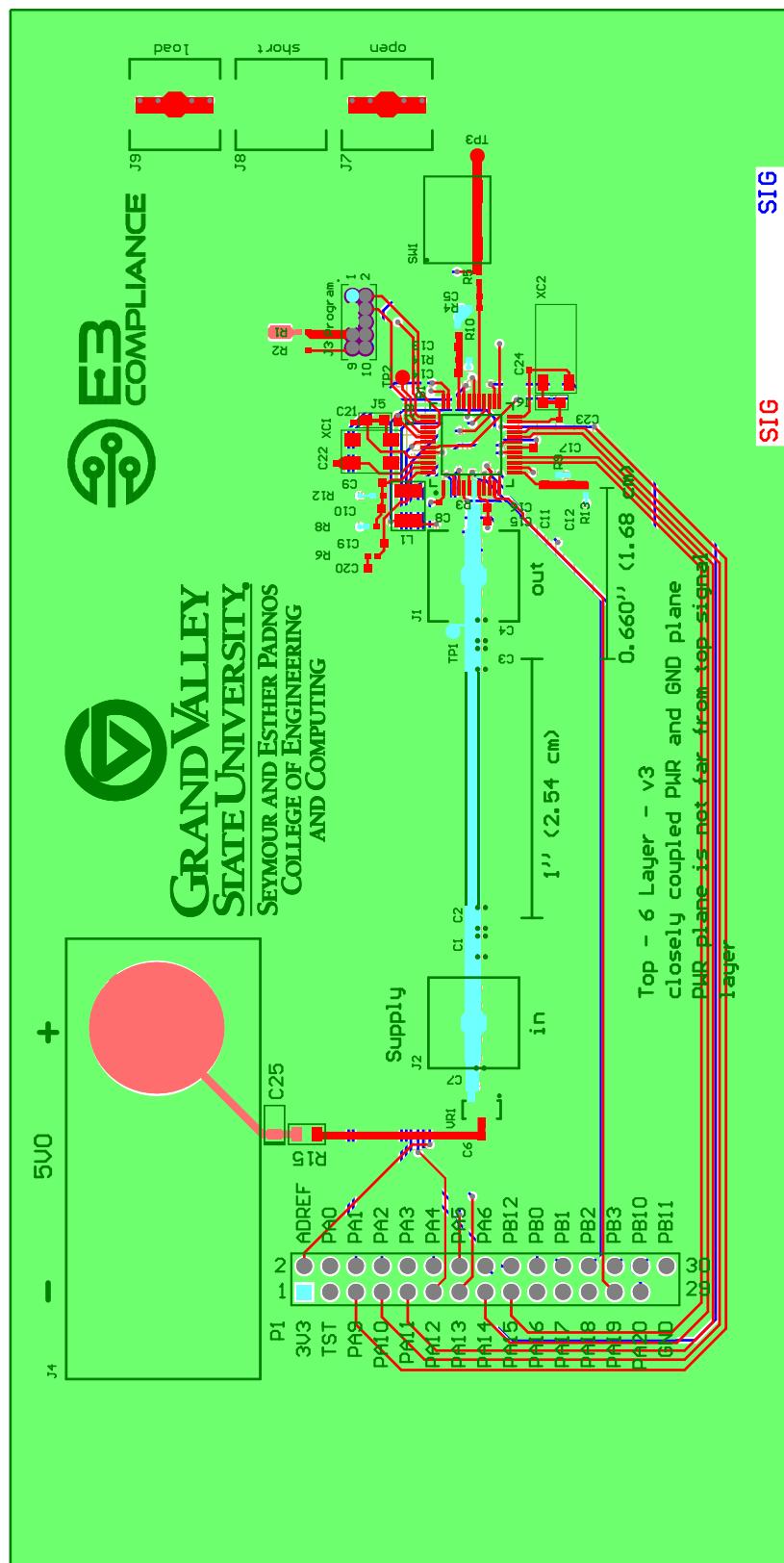


Figure A.40: Embedded capacitance 6-layer version 3 design, composite view.

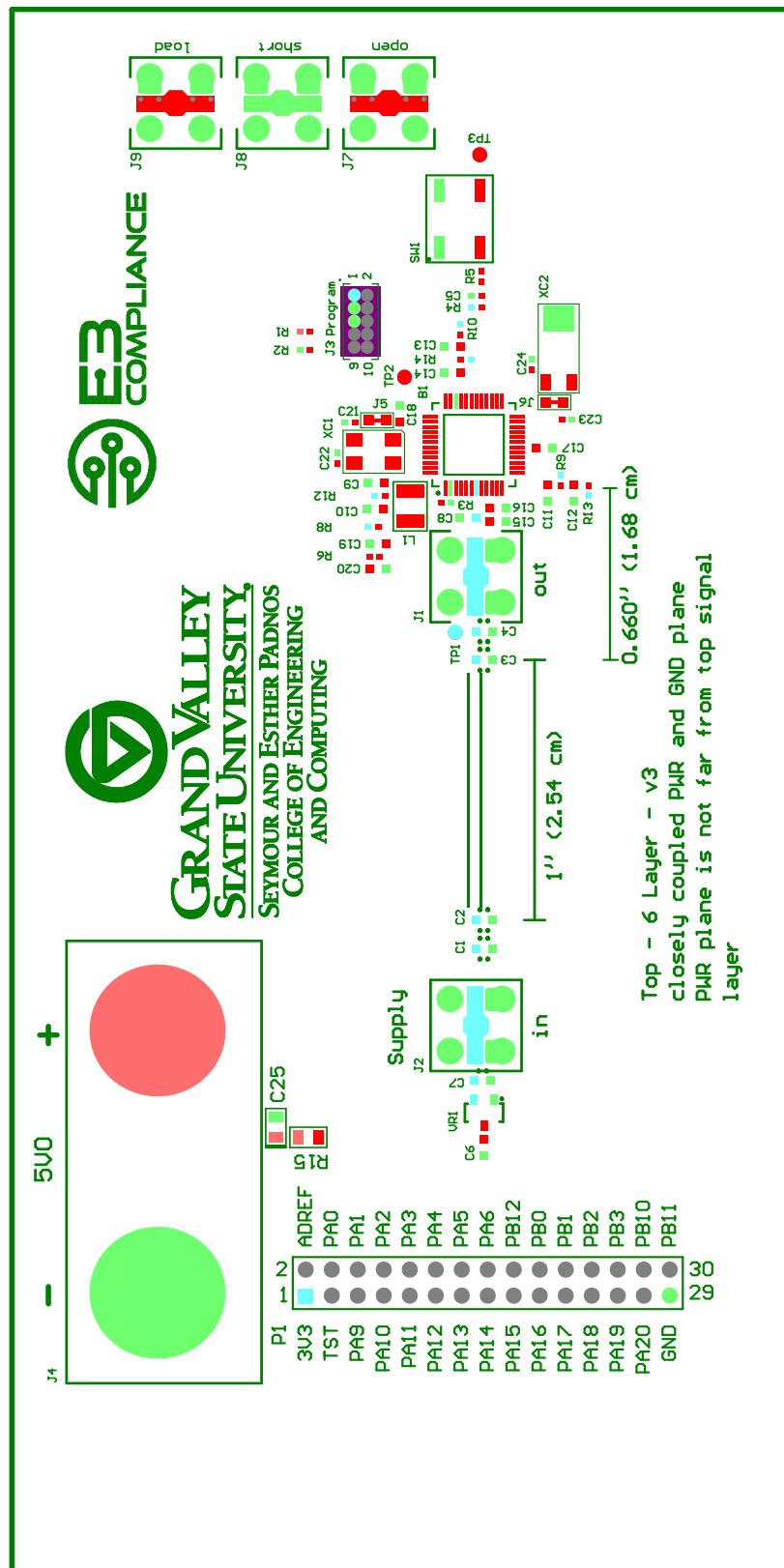


Figure A.41: Embedded capacitance 6-layer version 3 design, assembly top.

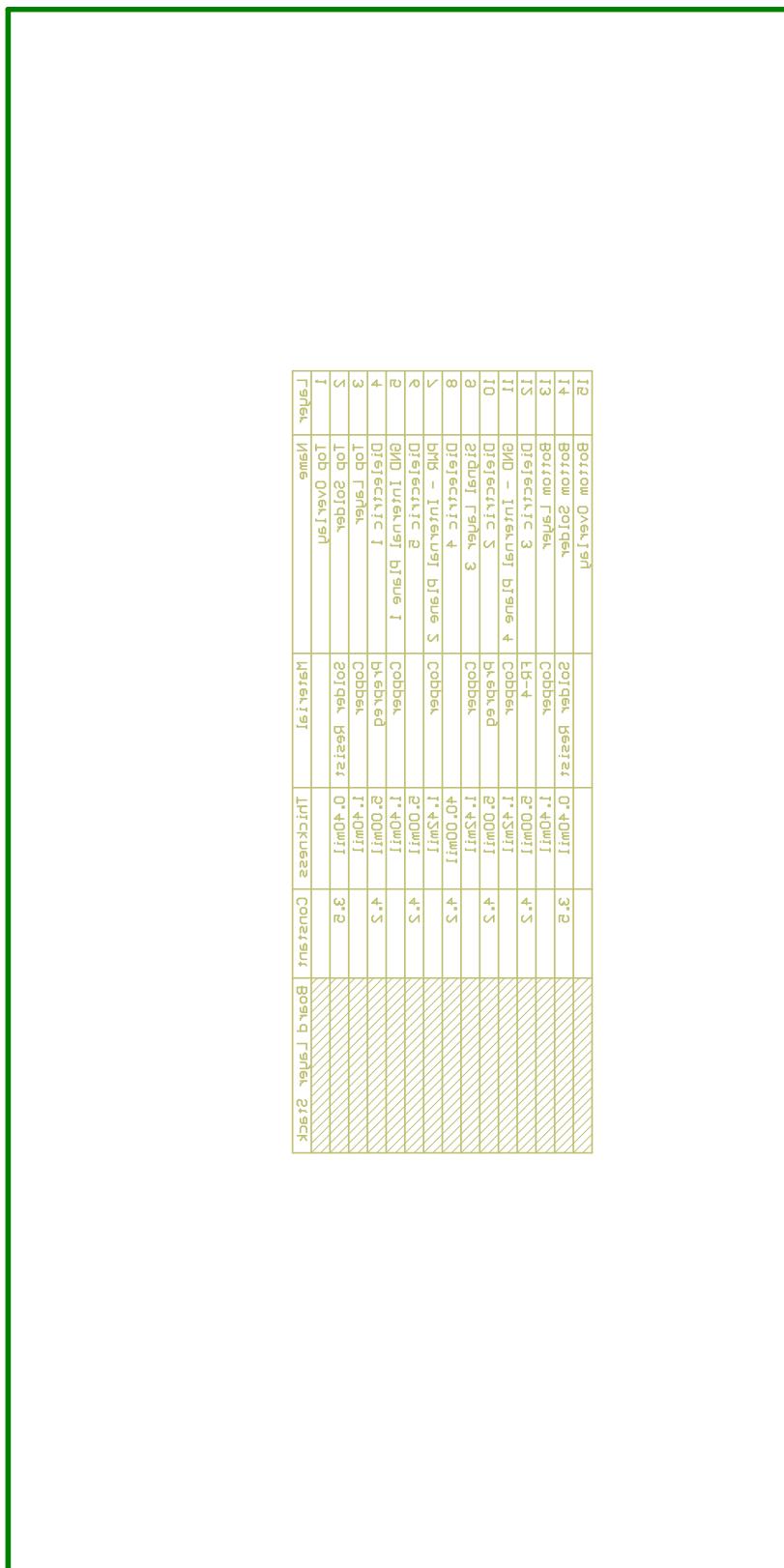


Figure A.42: Embedded capacitance 6-layer version 3 design, assembly bottom.

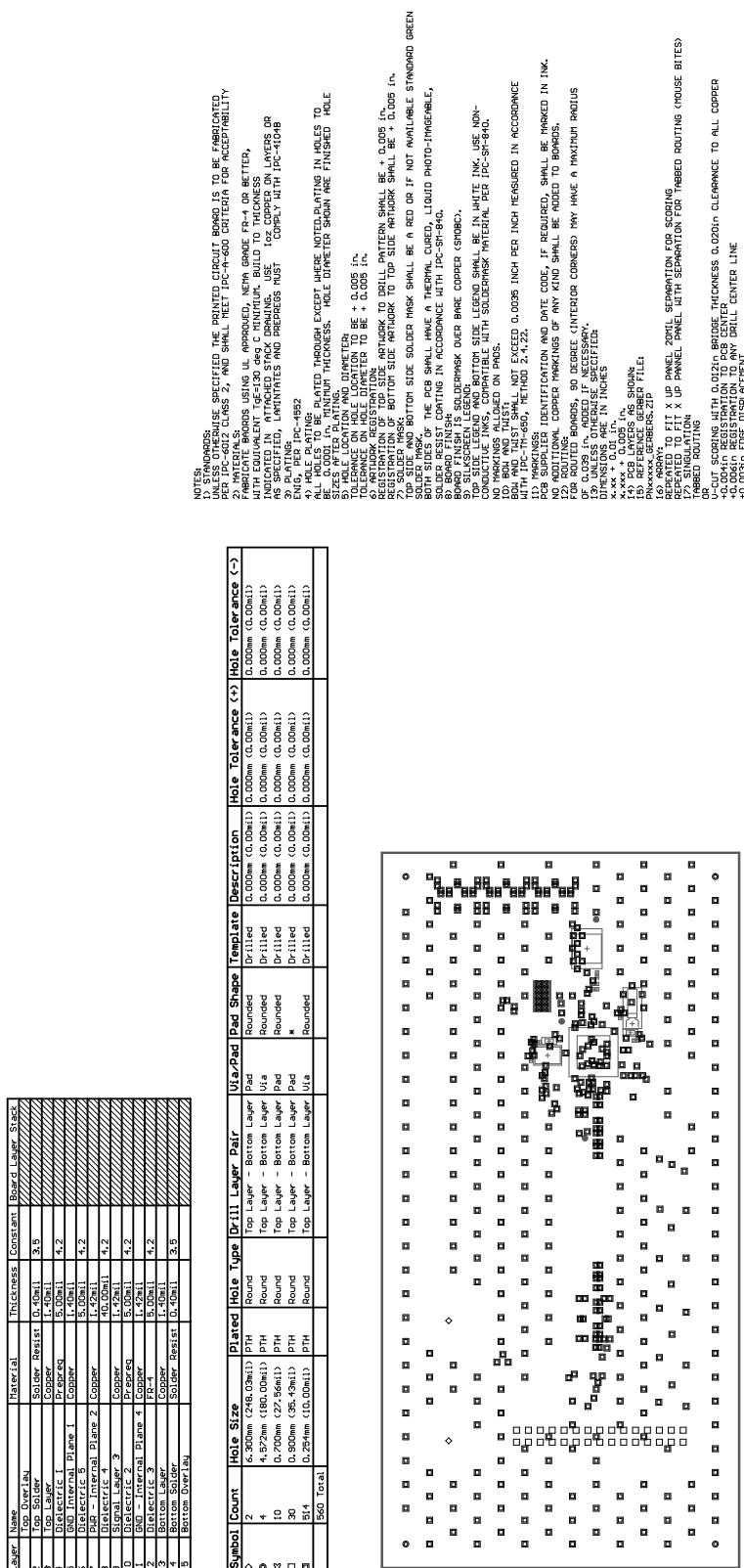


Figure A.43: Embedded capacitance 6-layer version 3 design, mechanical drawing top.

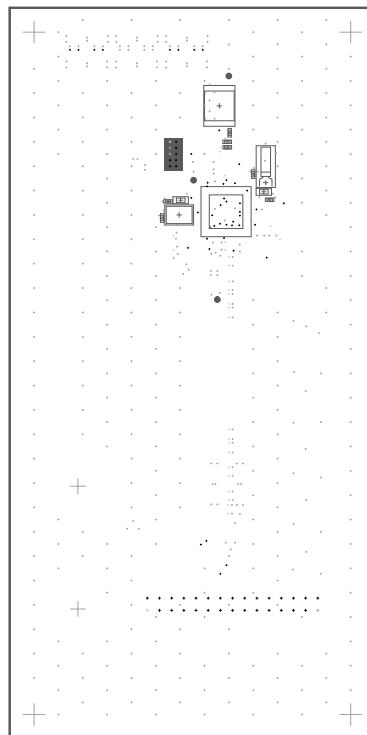


Figure A.44: Embedded capacitance 6-layer version 3 design, mechanical drawing bottom.

A.3 Design Load Board

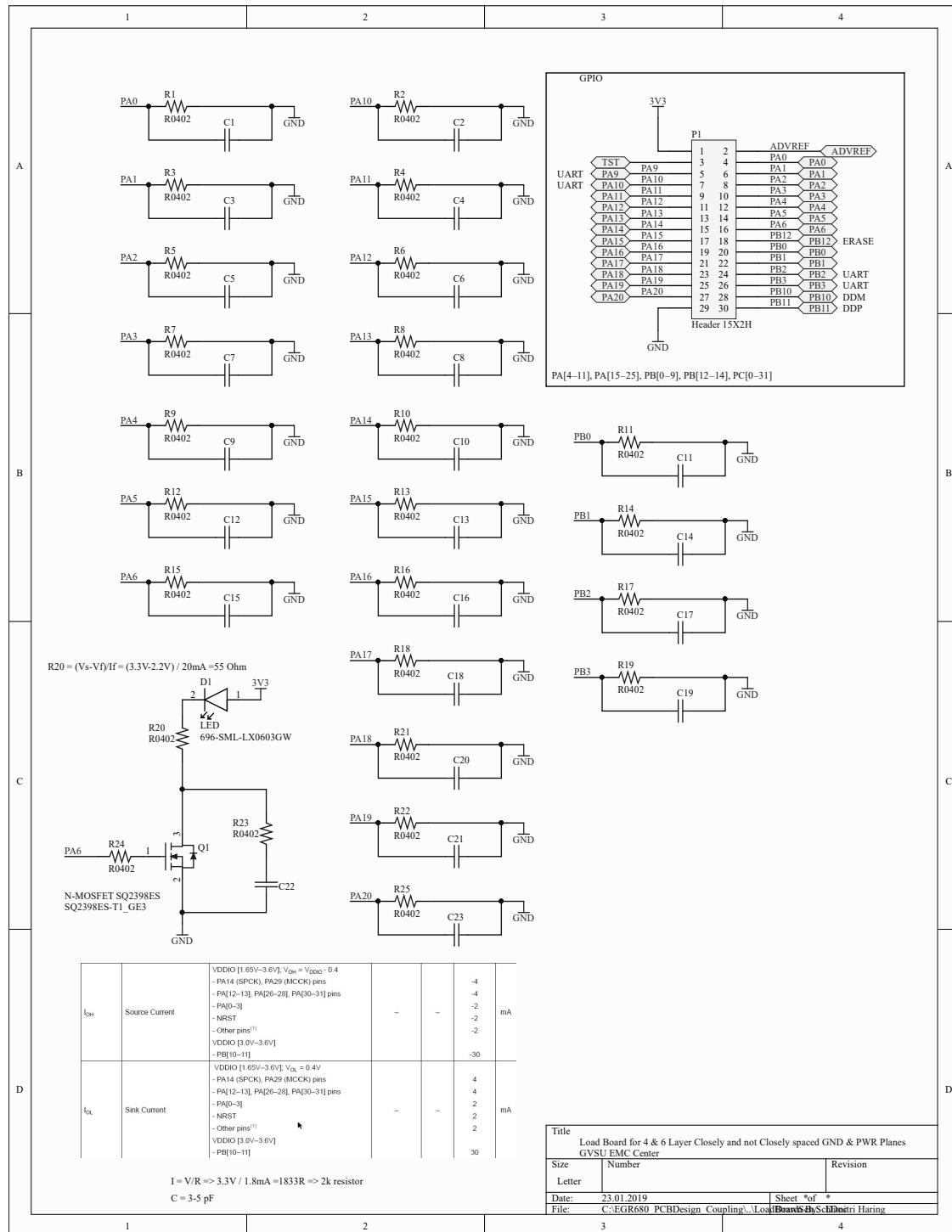


Figure A.45: Load Board Schematic.

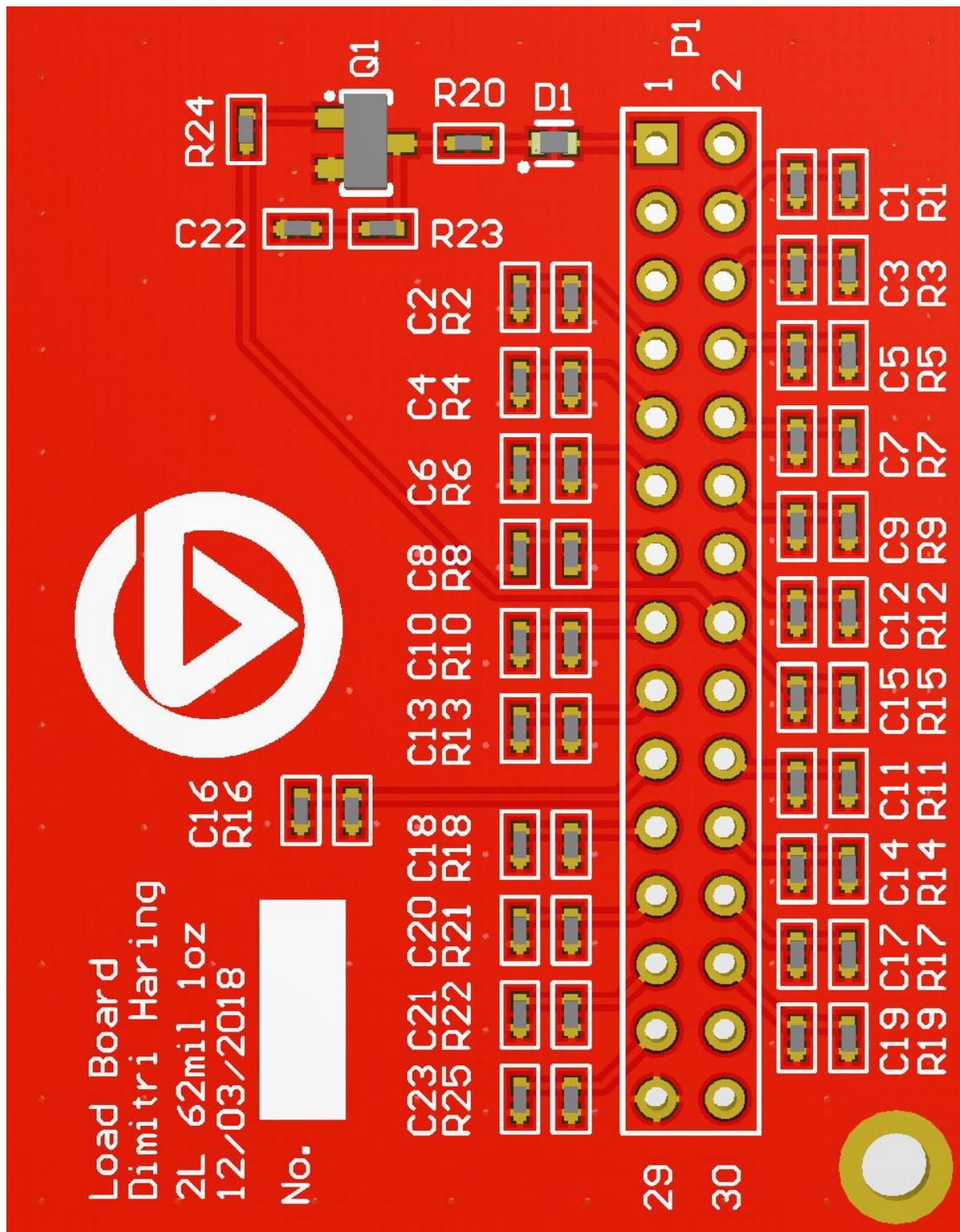


Figure A.46: Load Board 3D top view.

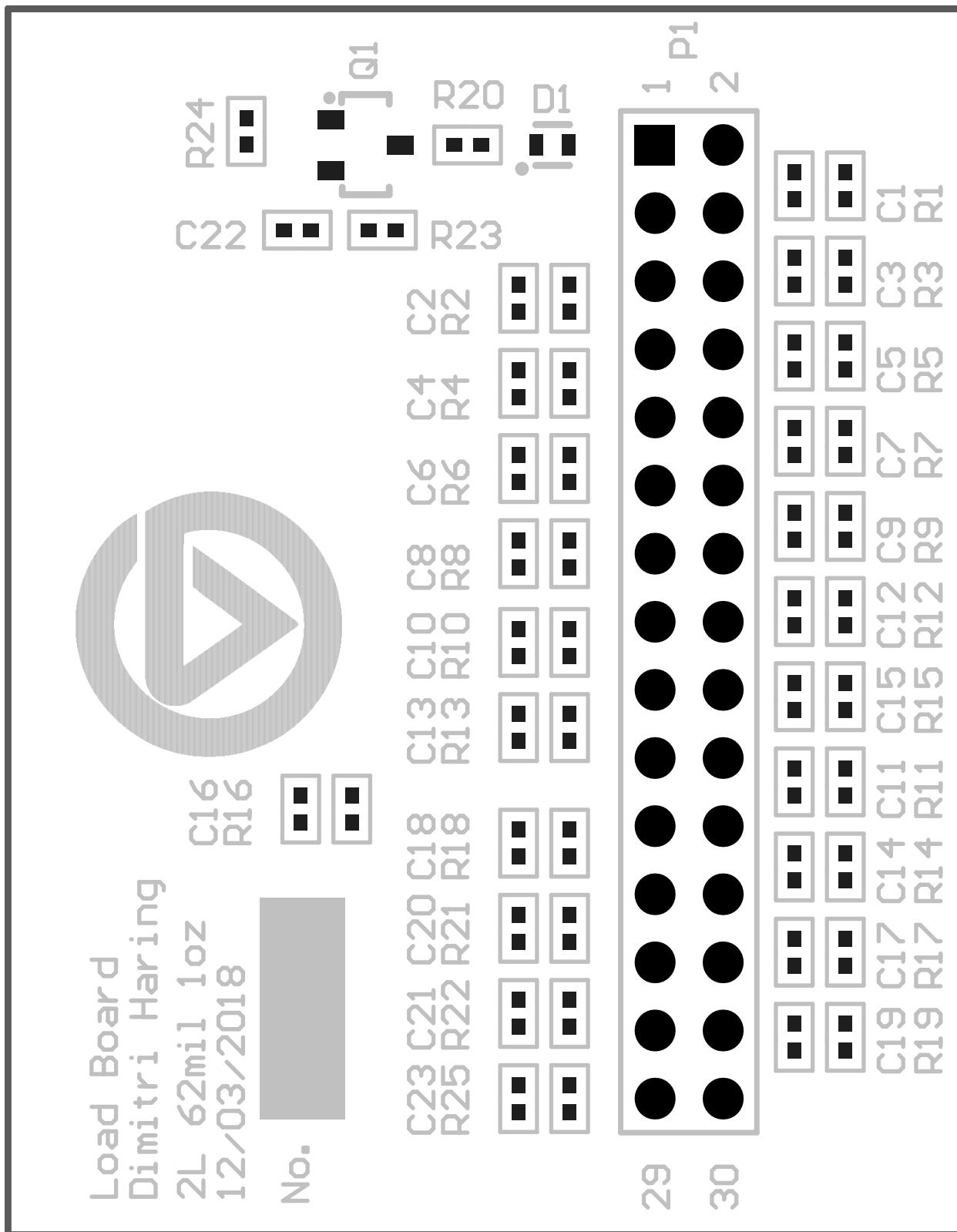


Figure A.47: Load Board assembly.

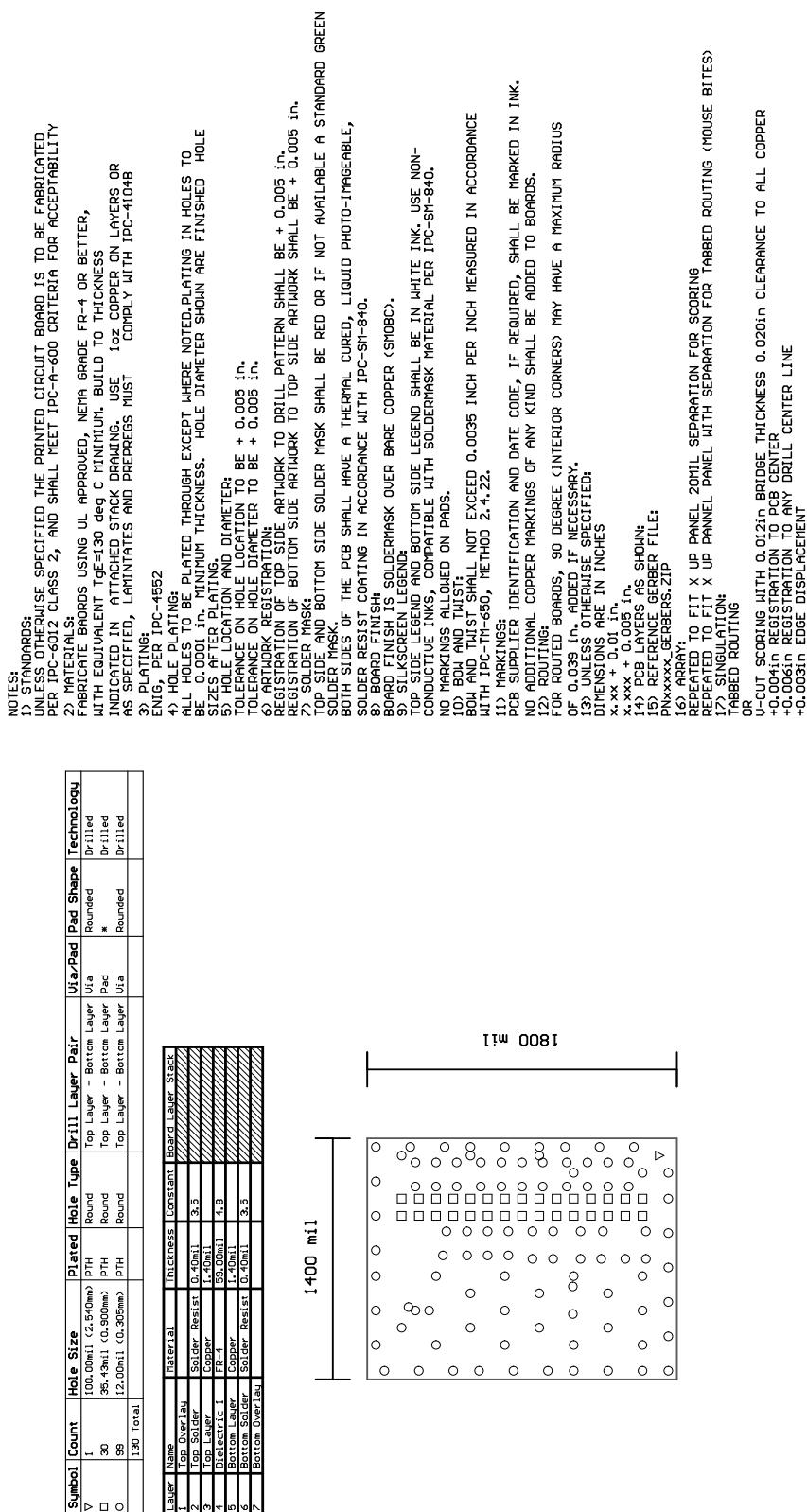


Figure A.48: Load Board mechanical drawing top.

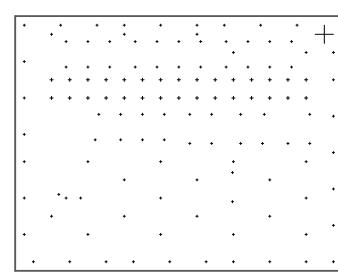


Figure A.49: Load Board mechanical drawing bottom.

Comment	Description	Designator	Footprint	Manufacturer Part Number 1	Supplier Part Number 1	Quantity	
C0402	Standard Ceramic Capacitor 0402	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23	0402 1.00 * 0.5 mm - framed				23
LED	Standard LEDs - SMD Green, 565nm 2.2V, 18mcd	D1	SMD 1.6*0.8 mm	Loading...	696-SML-LX0603GW	1	
Header 15X2H	Header, 15-Pin, Dual row, Right Angle	P1	HDR2X15			1	
N-MOSFET SQ2398ES	N-Channel 100V 1.6A (T _c) 2W (T _c) Surface Mount SOT-23-3 (TO-236)	Q1	SOT-23 - 3	Loading...	SQ2398ES-T1_GE3CT-ND	1	
R0402	Standard Ceramic Resistor 0402 1.00 * 0.5 mm - 1%	R1, R2, R3, R4, R5, R6	0402 1.00 * 0.5 mm - 1%			25	

Figure A.50: Load Board BOM.

A.4 Relationship between dB and Input Impedance

The conversion from dB to input impedance is performed with Eq. A.4. Tab. A.1 shows computed values based on Eq. A.4

$$\text{Input Impedance } \Omega = 10^{dB/20} \quad (\text{A.4})$$

Table A.1: Relationship between dB and input impedance in Ω

No.	dB	Impedance in Ω
1	60 dB	1000 Ω
2	50 dB	316.22 Ω
3	40 dB	100 Ω
4	30 dB	31.62 Ω
5	20 dB	10 Ω
6	10 dB	3.16 Ω
7	0 dB	1 Ω
8	-10 dB	0.316 Ω
9	-20 dB	0.1 Ω
10	-40 dB	0.0316 Ω
11	-60 dB	0.01 Ω
12	-70 dB	0.00316 Ω
13	-80 dB	0.001 Ω
14	-90 dB	0.000316 Ω

Appendix - B: EMC Filters - Source and Load Impedance

B.1 Design

The designs presented in this section were made with Altium Designer.

B.1.1 Schematics

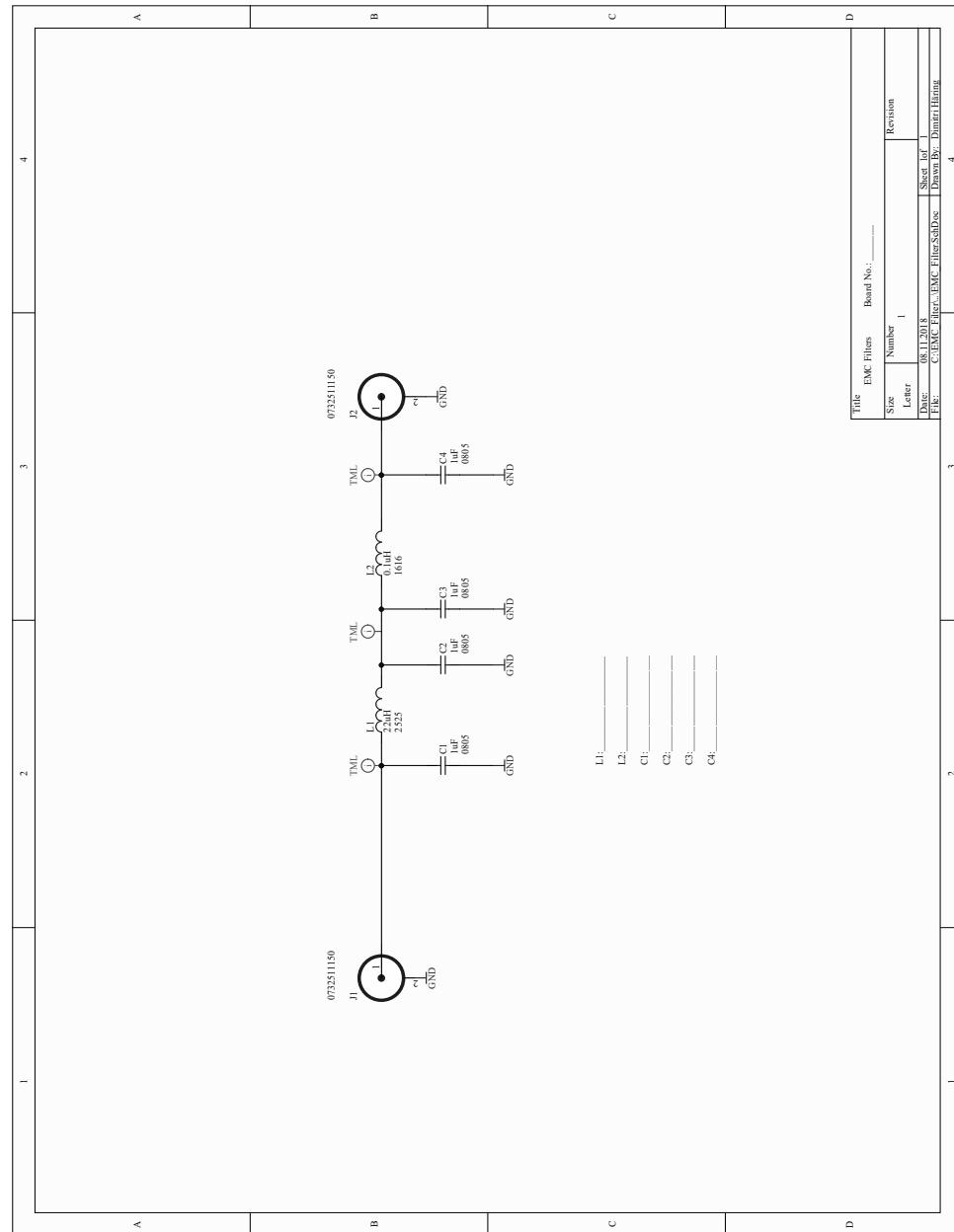


Figure B.1: EMC filter schematic.

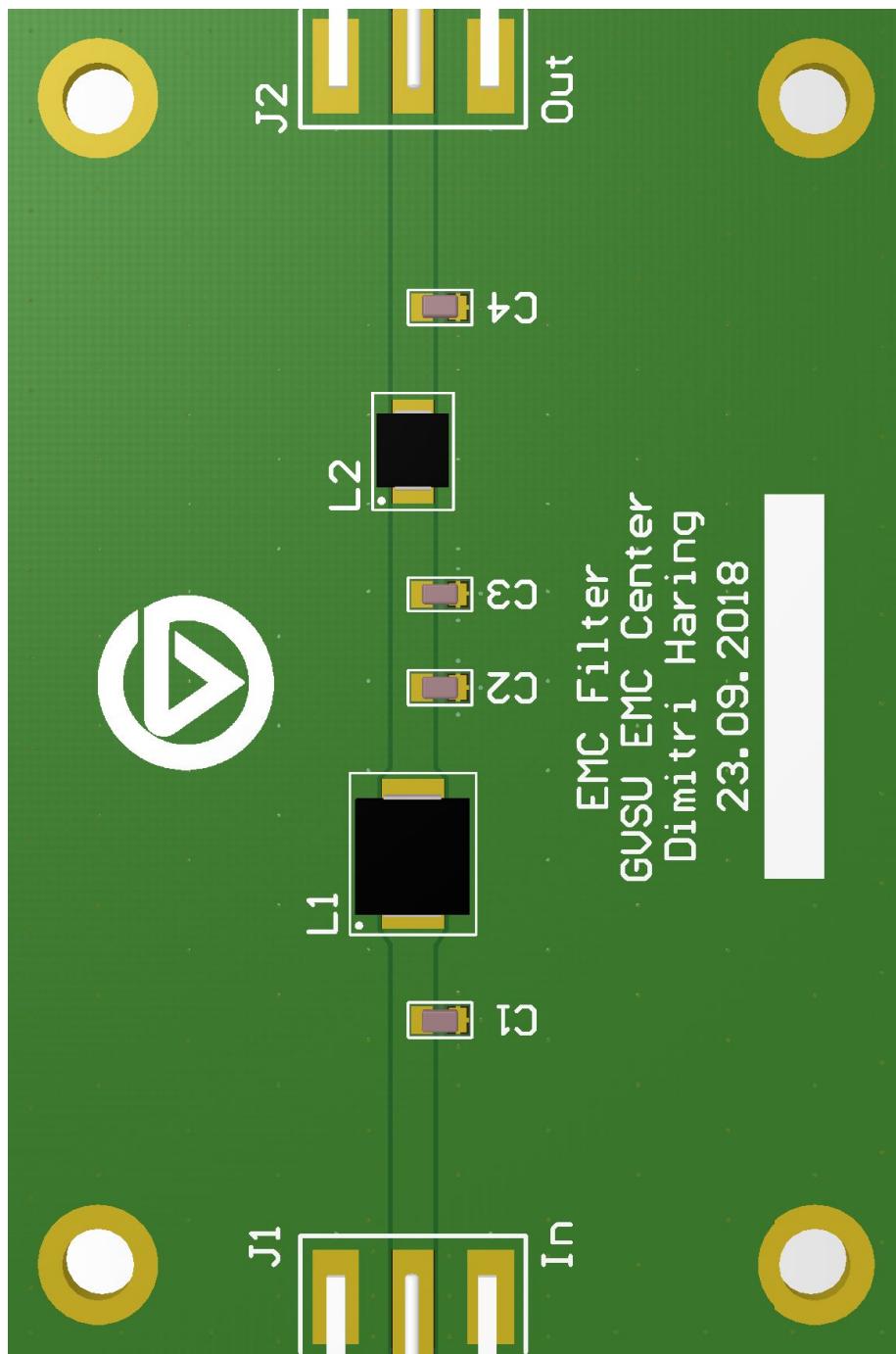
B.1.2 PCB 3D View

Figure B.2: EMC filter 3D top view.

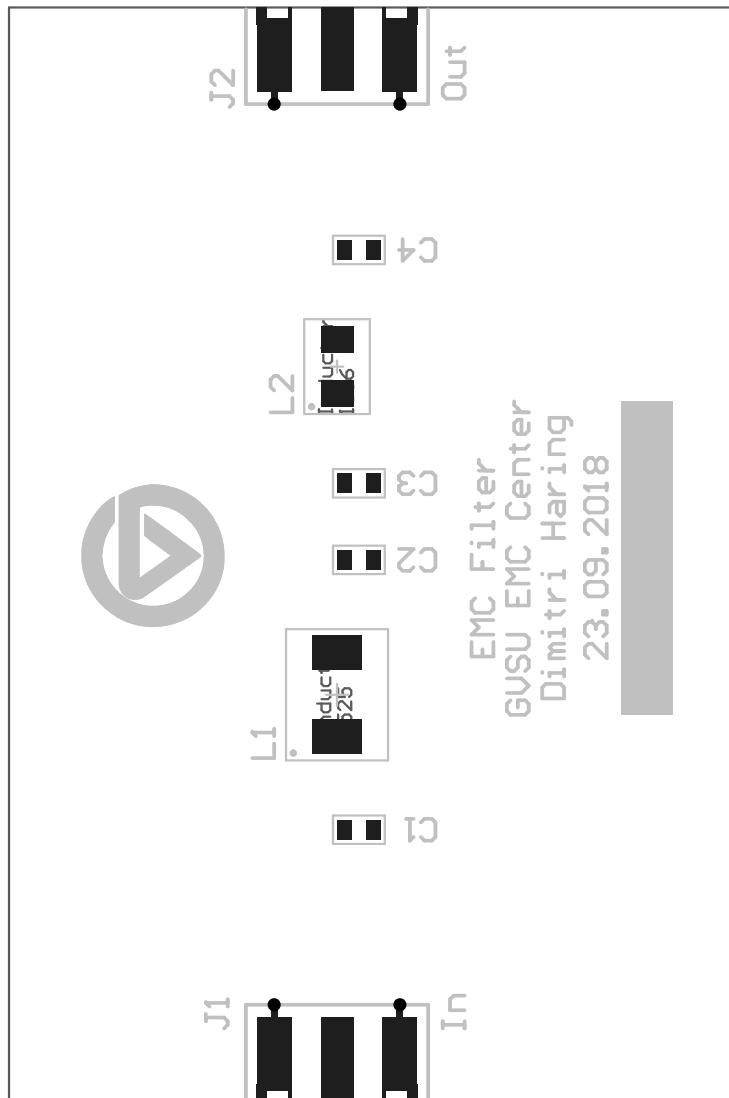
B.1.3 Assembly

Figure B.3: EMC filter assembly top view.

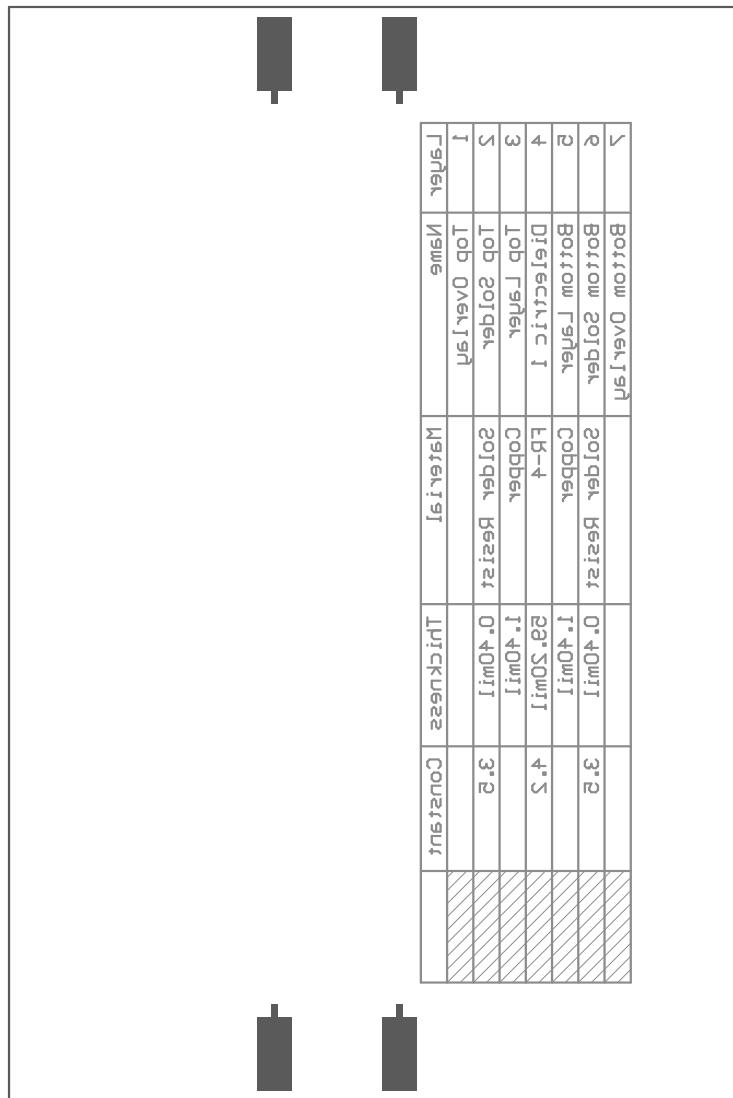


Figure B.4: EMC filter assembly bottom view.

B.1.4 Mechanical Drawing and Instructions

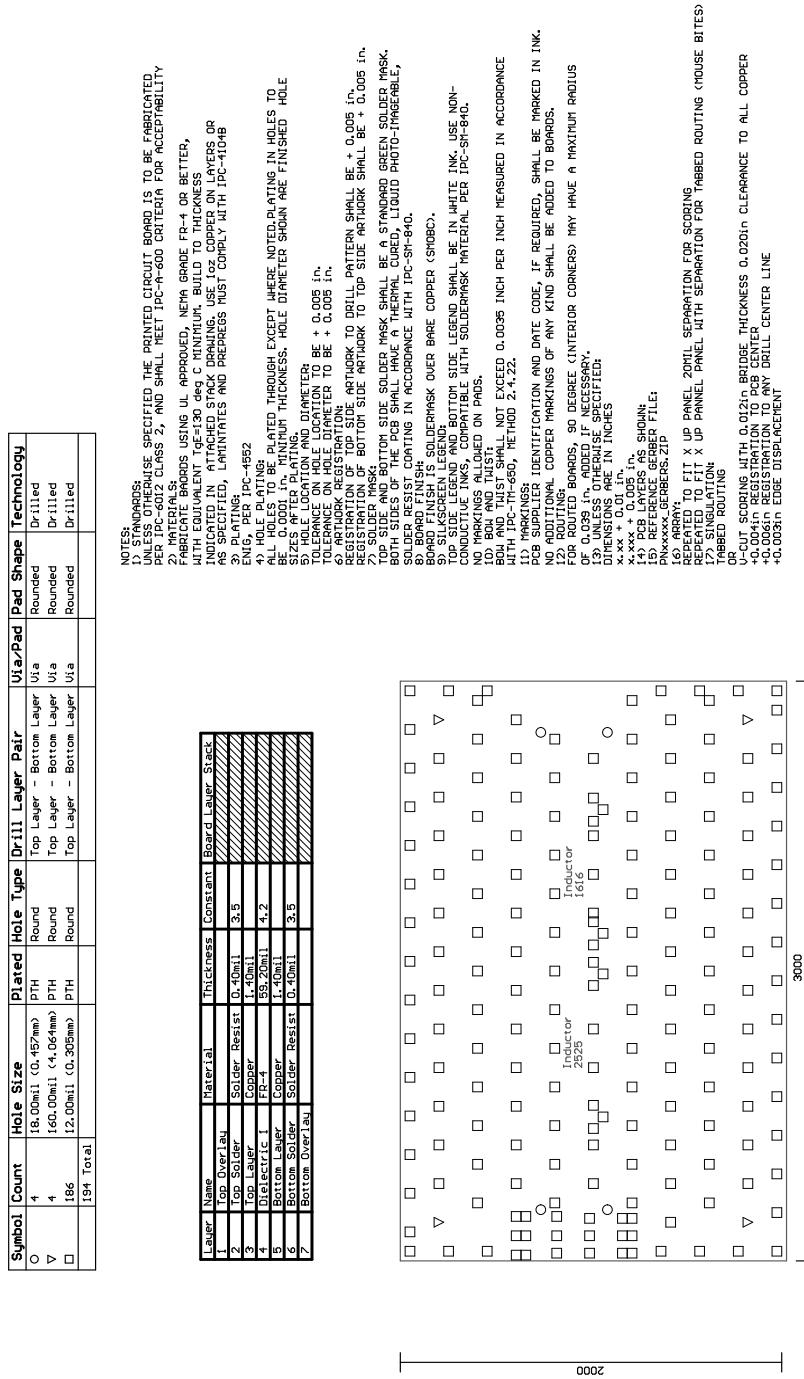


Figure B.5: EMC filter mechanical drawing and instructions.

B.2 Measurement Setup Additional Pictures

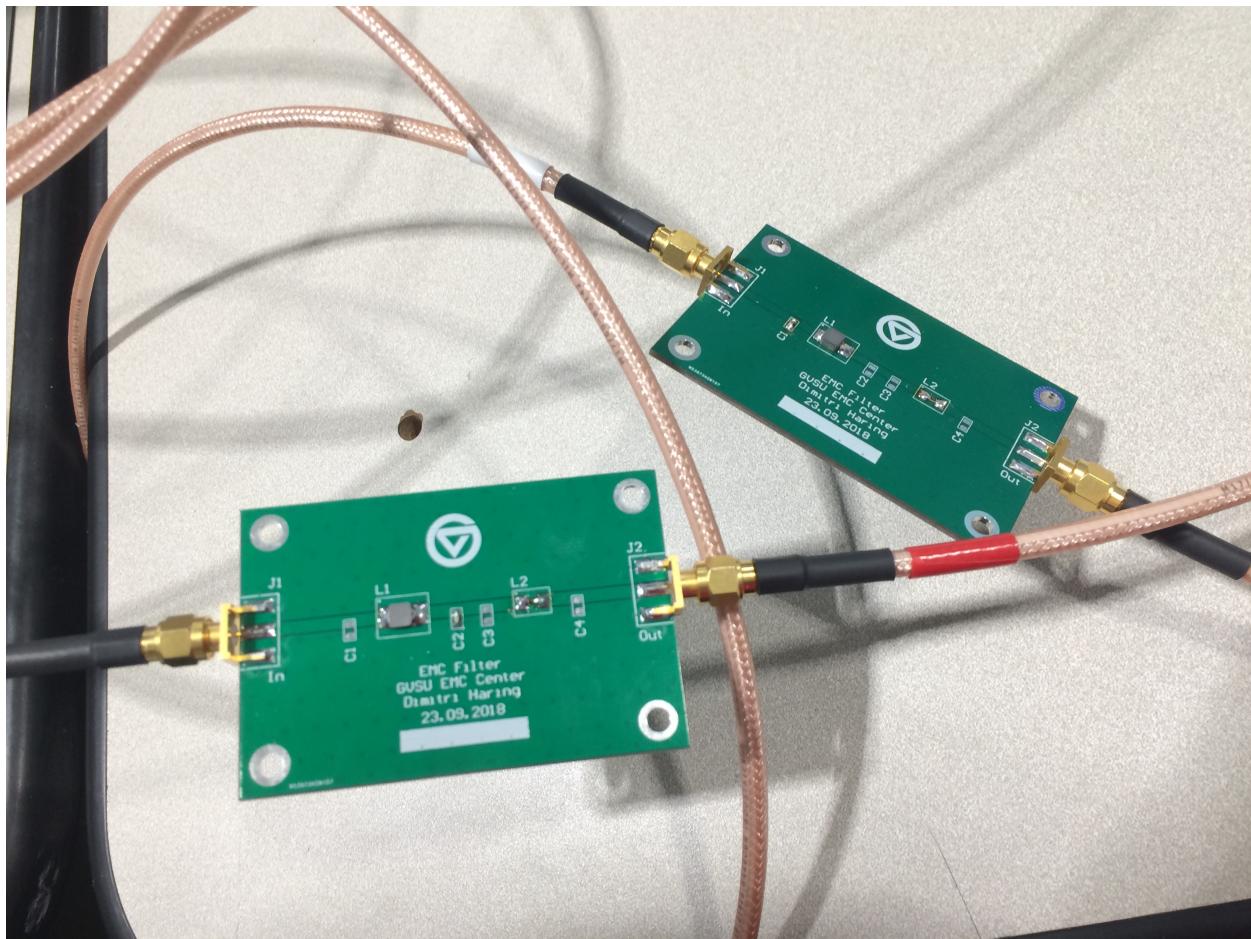


Figure B.6: Measurement setup date 03/28/2019 of a 1k CL on trace S21 and 1k LC structure on trace S43.

B.3 Additional Results

B.3.1 Measurement logMag s_{21} - π - R 1 k Ω vs. s_{43} - R 1 k Ω - π 100 kHz - 1 GHz with 0.1 μ H Inductor

In Section 3.2.1, two different π filter structure were discussed. The impedance of these structures were measured with VNA and shown in Fig. B.7. To the right, the schematics and component values are shown. The compared structures are π - R 1 k Ω (brown) versus R 91 k Ω - π (aquamarine). Points were the magnitude and frequencies are similar are marked blue.

The curves start at an offset of -22.5 dB. At 1 MHz both graphs have a magnitude of -35.7 dB. At 7.3 MHz both graphs have an anti-resonance of a magnitude of -34.4 dB. At 10 MHz both graphs have a magnitude of -53 dB. The first resonance occurs at 57 MHz with -114.2 dB for the π -R structure and -116 dB for the R- π structure. At 182 MHz a second resonant frequency is hit for the π -R structure, which cannot be as good identified in the R- π structure. At 202 MHz the π -R structure has a magnitude of -94.89 dB. At 202 MHz the R- π structure has a magnitude of -95.6 dB. An additional resonance indication can be seen for the π - R structure at a frequency of 390 MHz and for the R - π structure at 317 MHz. At 404 MHz both graphs have a magnitude of around -90 dB. In a frequency range of 100 kHz to 182 MHz, both structures perform similarly. Beyond 182 MHz depending on resonance or not one outperforms another.

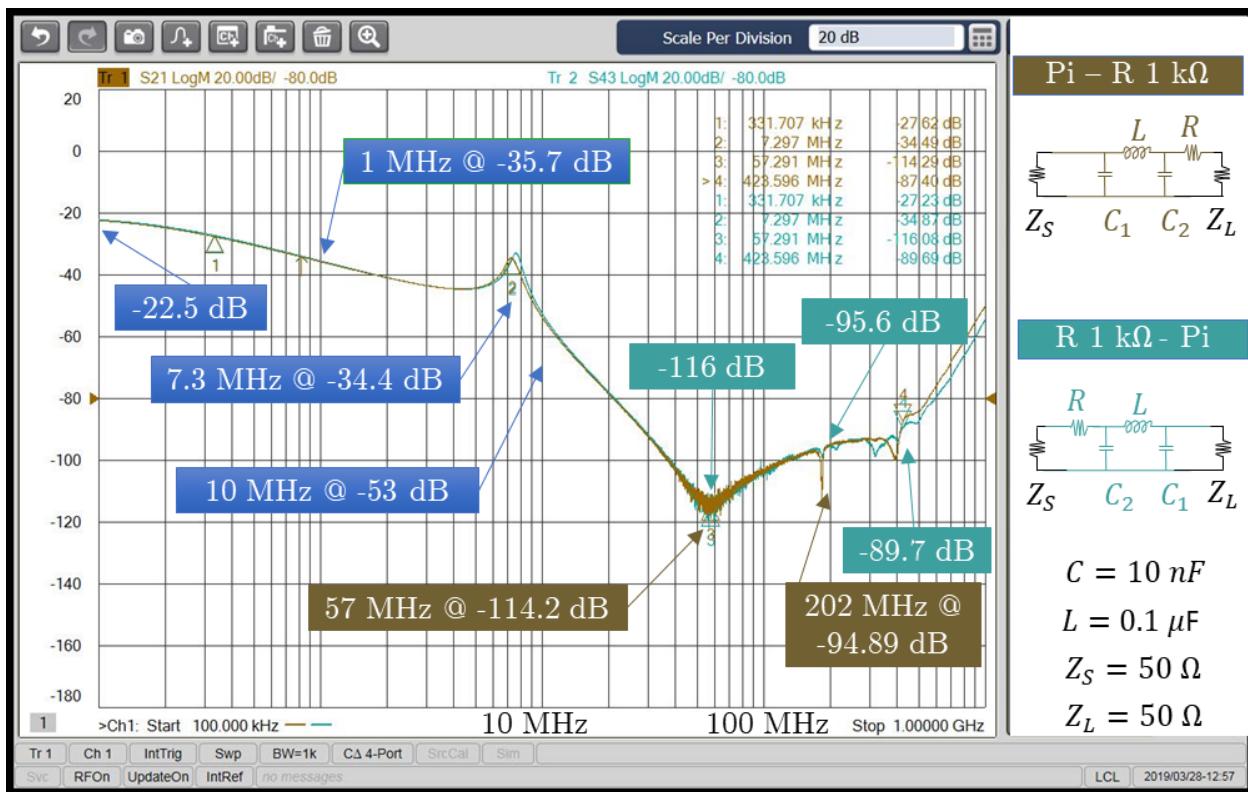


Figure B.7: EMC Filter Measurement $s_{21} \pi - R 1 \text{ k}\Omega$ vs. $s_{43} R 1 \text{ k}\Omega - \pi$ with $0.1 \mu\text{H}$ inductor.

B.3.2 Measurement logMag s₂₁ - π - R 1 k Ω with 4.7 μ H Inductor vs. s₄₃ - R 1 k Ω

- π with 4.7 μ H Inductor for 100 kHz - 1 GHz

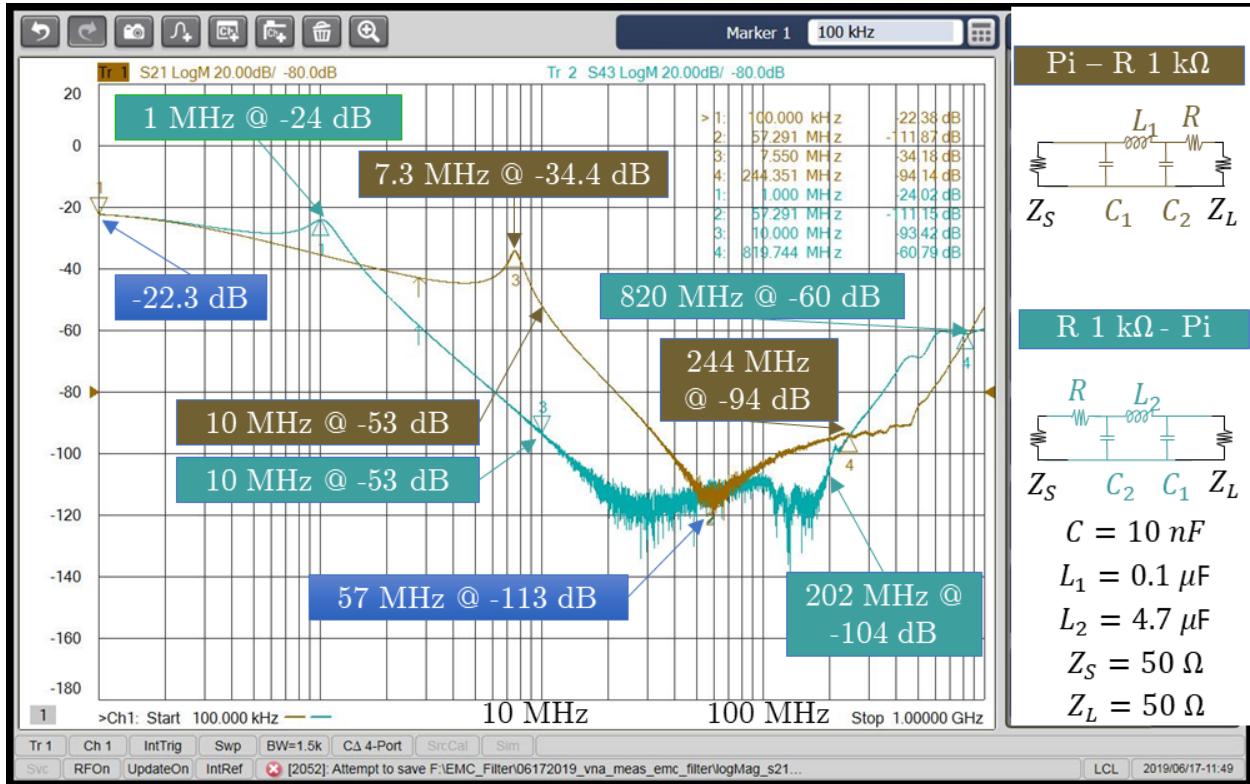


Figure B.8: EMC Filter Measurement s₂₁ π - R 1 k Ω with 0.1 μ H inductor vs. s₄₃ R 1 k Ω - π with 4.7 μ H inductor.

B.3.3 Measurement logMag s₂₁ - L with 4.7 μ H Inductor vs. s₄₃ - 0 Ω - Trace for 100 kHz - 1 GHz

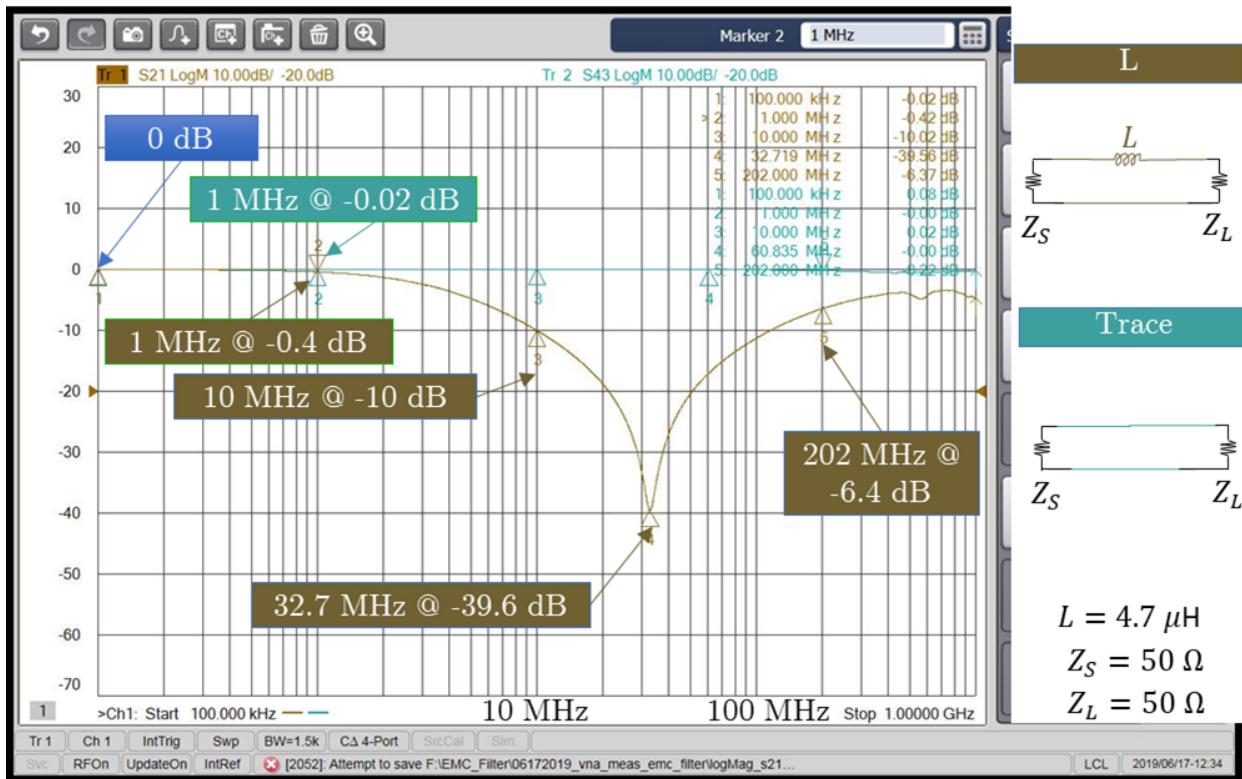


Figure B.9: EMC Filter Measurement s₂₁ L with 4.7 μ H inductor vs. s₄₃ 0 Ω - trace.

B.3.4 Measurement logMag s₂₁ - Two L with 4.7 μ H Inductor vs. s₄₃ - L with 4.7 μ H Inductor for 100 kHz - 1 GHz

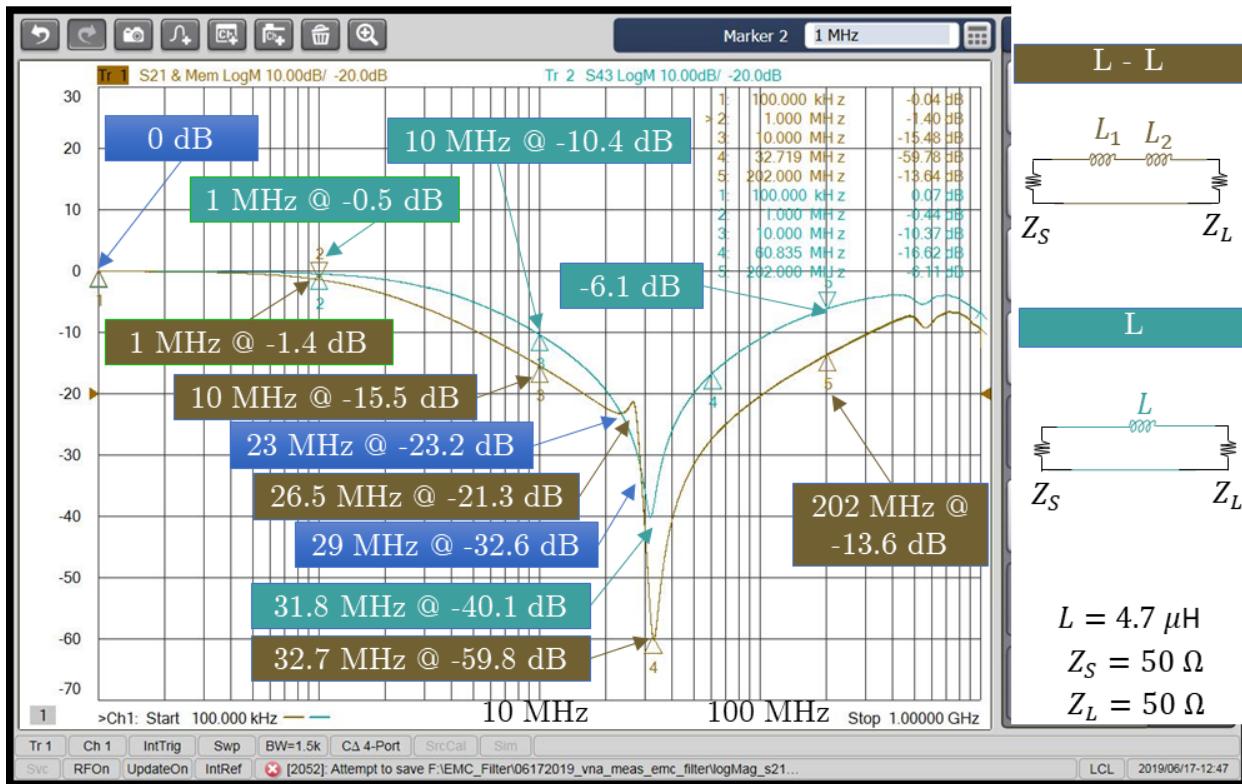


Figure B.10: EMC Filter Measurement s₂₁ two Ls with 4.7 μ H inductor vs. s₄₃ L with 4.7 μ H inductor.

B.3.5 Measurement logMag s₂₁ - Two C with 10 nF Capacitor vs. s₄₃ - C with 10 nF Capacitor for 100 kHz - 1 GHz

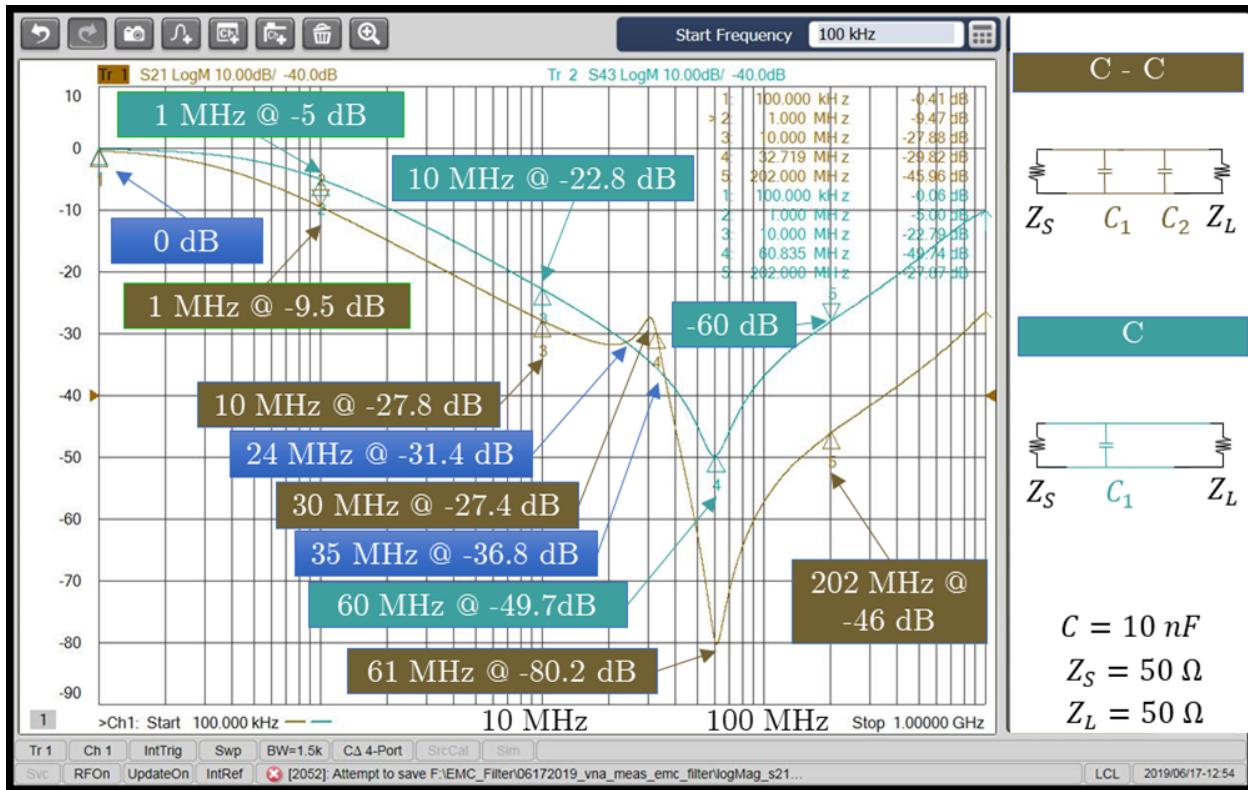


Figure B.11: EMC Filter Measurement s₂₁ two Cs with 10 nF capacitor vs. s₄₃ C with 10 nF capacitor.

Appendix - C: SMPS EMI Suppression Techniques

C.1 Design

The designs presented in this section were made with Altium Designer.

C.1.1 Schematic

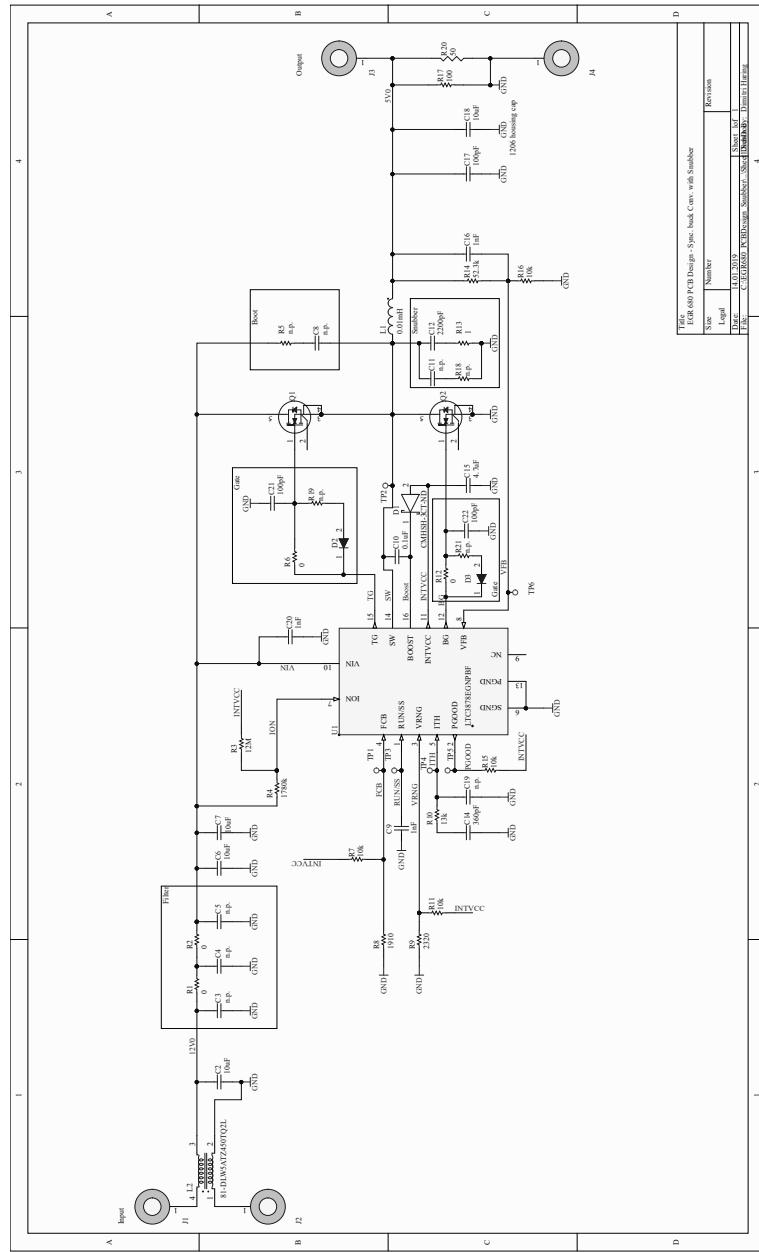


Figure C.1: Switched Mode Power Supply v2 schematic.

C.2 3D view top and bottom

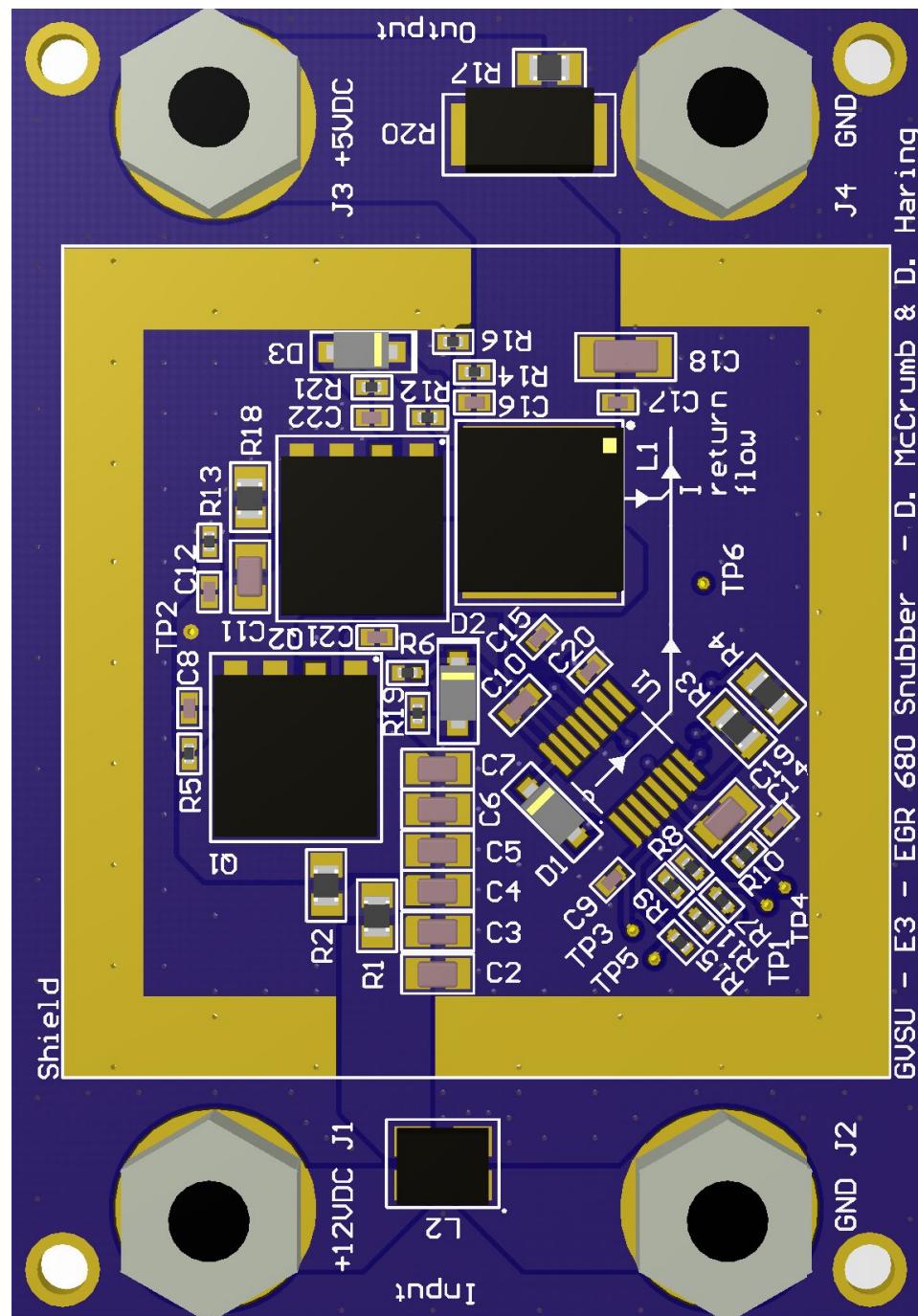


Figure C.2: Switched Mode Power Supply v2 3D view top.

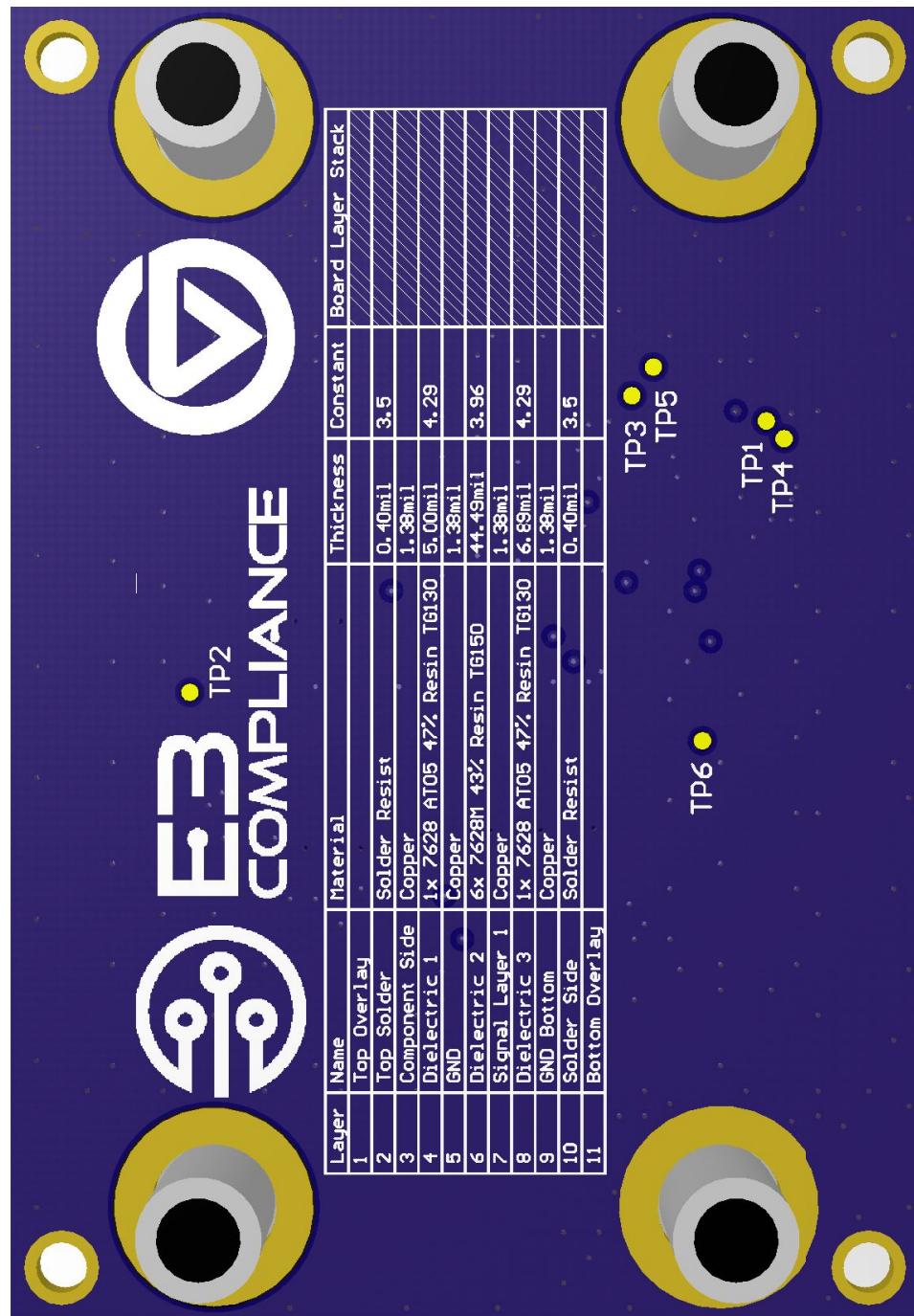


Figure C.3: Switched Mode Power Supply v2 3D view bottom.

C.2.1 Assembly

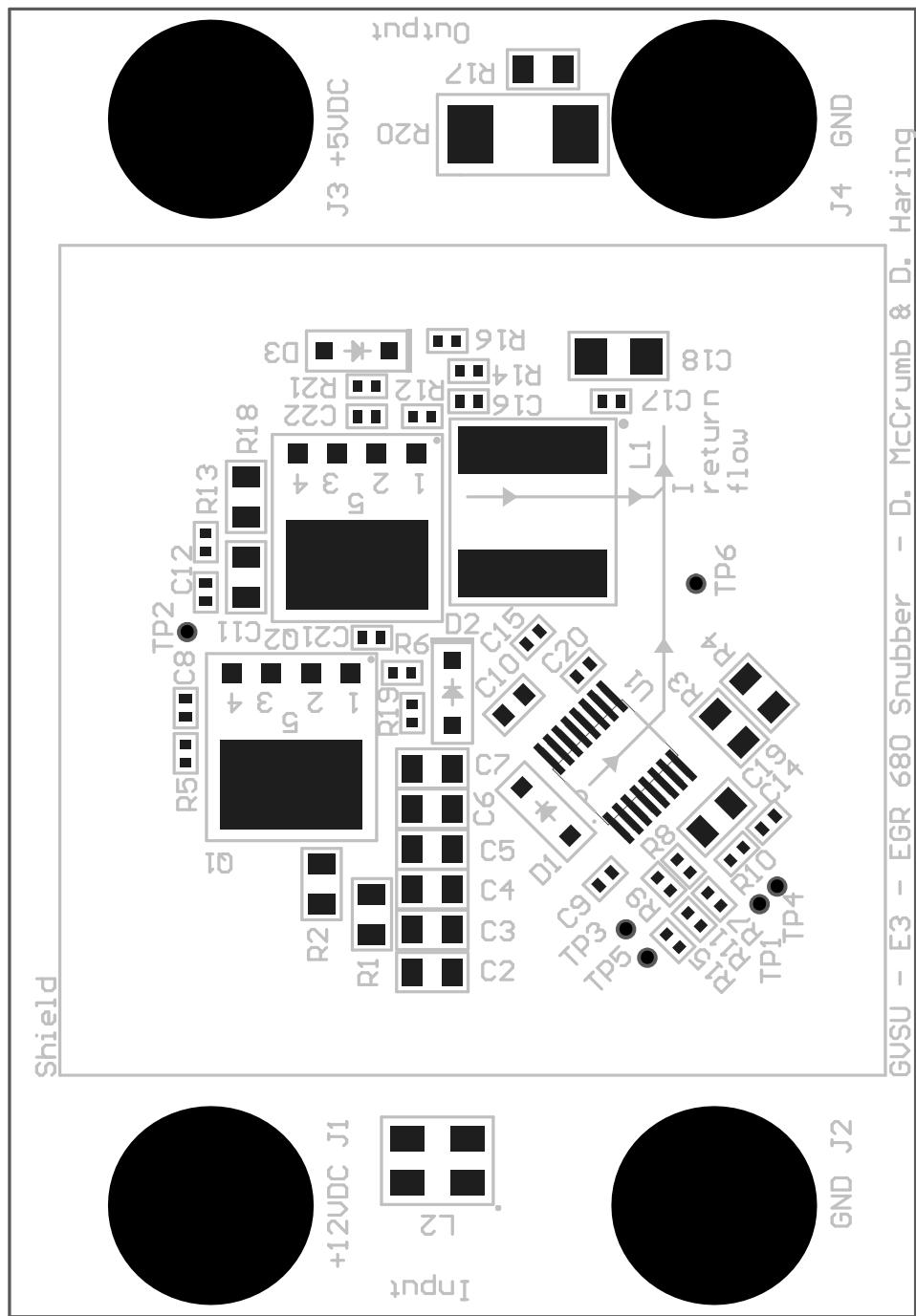


Figure C.4: Switched Mode Power Supply v2 assembly top.

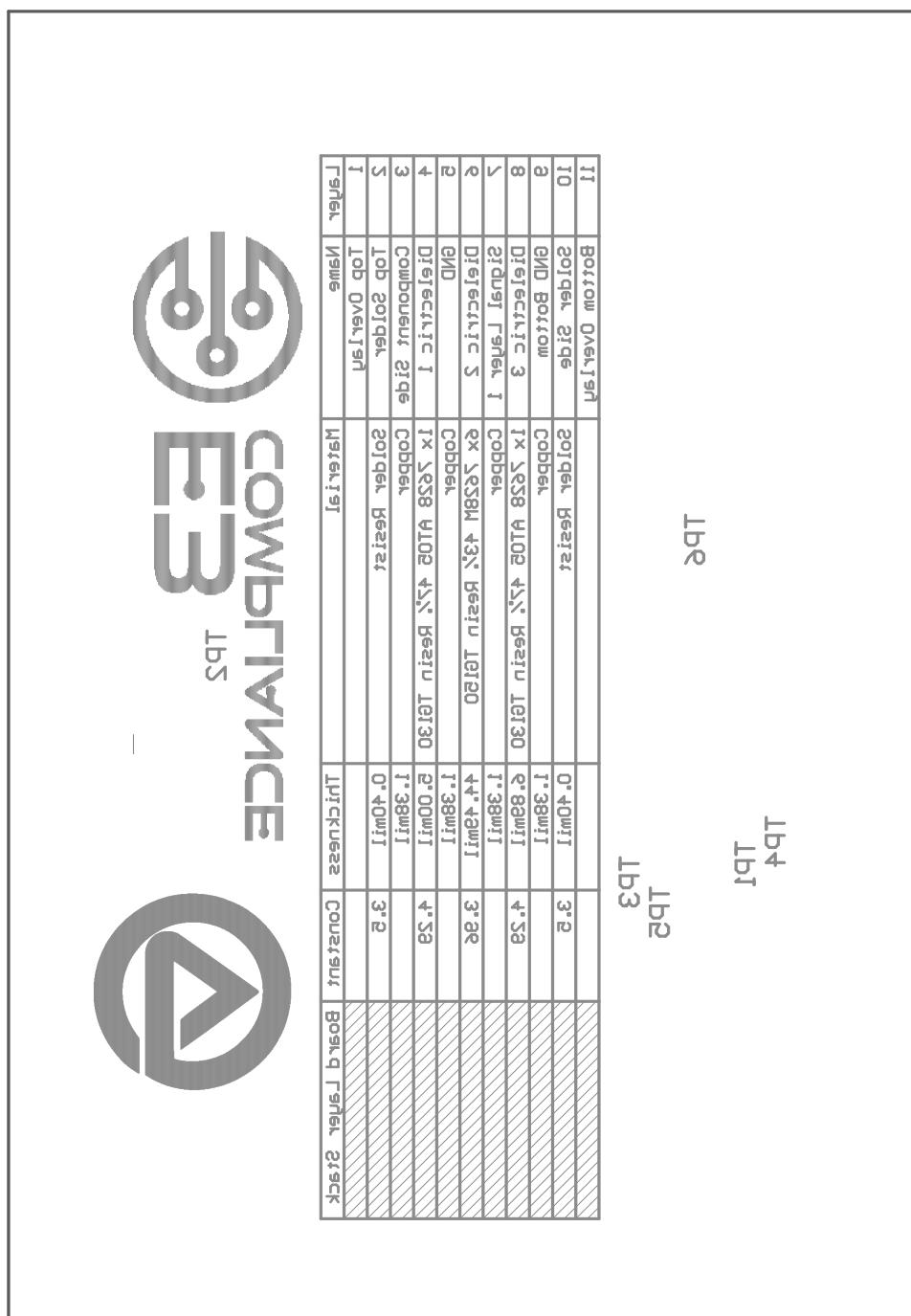


Figure C.5: Switched Mode Power Supply v2 assembly bottom.

C.2.2 Bill of Materials

The BOM is shown in Fig. C.6.

Designator	Description	Manufacturer	Manufacturer No	Supplier 1	Supplier Part Number 1	Quantity	Price	Total
C1	Aluminum Electrolytic Capacitors - Leaded 450Volts 10uF 12.5X20 20%	Nichicon	UCS2W100MH D	Mouser	647-UCS2W100MHD	1	0.85	0.85
C2, C3, C4, C5, C6, C7, C11, C15, C19	0805 Ceramic Chip Capacitor - Standard	AVX	0805A200F4T2 A	Mouser	581-0805A200F4T2A	9	0.52	4.68
C8, C9, C12, C14, C16, C17	0402 Ceramic Chip Capacitor - Standard	Murata Electronics	GCO1555C1H15 0FB01D	Mouser	81-GCO1555C1H150FB1D	6	0.49	2.94
C10	0402 Ceramic Chip Capacitor - Standard	Murata Electronics	GCO1555C1H15 0FB01D	Mouser	GCQ1555C1H150FB01D	1	0.49	0.49
C13	Aluminum Electrolytic Capacitors - Leaded 330uF 35volts AEC-Q200	Panasonic	EEU-TP1V331 1206CA222JAT2A	Mouser	667-EEU-TP1V331	1	1.54	1.54
C18	1206 Ceramic Chip Capacitor - Standard	AVX		Mouser	581-1206CA222JAT2A	1	0.73	0.73
D1	The CENTRAL SEMICONDUCTOR CMHSH-3 is a silicon Schottky diode, epoxy molded in a SOD-123 surface mount package, designed for fast switching applications requiring a low forward voltage drop.	CENTRAL SEMICONDUCTOR	CMHSH-3 TR	Digi-Key	CMHSH-3CT-ND	1	0.59	0.59
J1, J2, J3, J4	150uH Shielded Wirewound Inductor 910mA 478 mOhm Nonstandard	Mueller Electric	BU-00232	Mouser	548-BU-00232	4	2.13	8.52
L1		Wurth Electronics Inc.	74404084151	Mouser	710-74404084151	1	1.22	1.22
Logo						1		0
Q1, Q2	CoolMOS™C7 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The product portfolio provides all the benefits of fast switching superjunction MOSFETs offering better efficiency, reduced gate charge, easy implementation and outstanding reliability.	Infineon Technologies	IPP65R225C7X KSA1 667-ERJ-6RBD3830V	Mouser	726-IPP65R225C7XKSA1	2	2.44	4.88
R1, R2, R3, R4, R18	0805 Chip Resistor - Standard	Panasonic		Mouser	ERJ-6RBD3830V	5	0.15	0.75
R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16	0402 Chip Resistor - Standard	Panasonic	667-ERJ-2RHD2402X	Mouser	ERJ-2RHD2402X	12	0.11	1.32
R17	50Ohm resistor Axial 1"	Vishay / Draloric		Mouser	594-AC01W50R00J	1	0.51	0.51
R100						1		0
U1	PMIC - voltage regulators - DC DC switch controllers Linear Technology LTC3878EGN#PBF SSOP 16					1	2.57	2.57
								31.59

Figure C.6: Snubber circuitry SMPS BOM.

C.3 Snubber Values Calculation

Listing C.1 shows the MATLAB script which was used to calculate the snubber values based on the high frequency ringing content measured with the mixed signal domain oscilloscope.

```
% EMC Snubber
% Calculate Snubber values RC based on measured values.
% Profesor: Dr. B. Adamzyek
% Author: Dimitri Häring
% Date: 4/01/2019
% =====
clear all, close all, clc
%
Cadd = 100e-12; % Cadd capacitor value added to determine
                  % parasitics
fr = 892.9e6; % measured ringing frequency without
                 % snubber
fr_prime = 833.3e6; % measured ringing frequency after Cadd
                     % added
%
%% estimated parasitic capacitance
C_par = Cadd / ( ( fr/fr_prime)^2 - 1 );
%
%% estimated parasitic inductance
L_par = 1 / ( (C_par)*( 2*pi*fr )^2 );
%
%% estimated snubber capacitor minimum value
Csstab_min = 3 / ( (L_par)*( 2*pi*fr )^2 );
%
%% estimated resistor value
Rsstab = sqrt( L_par / ( Cadd/3 ) );
```

Listing C.1: MATLAB Script to Calculate Snubber Values

C.4 CE (V) Test Setup Pictures

Figure C.7: SMPSv3 conducted emissions test voltage method measurement setup - cable .



Figure C.8: SMPSv3 conducted emissions test voltage method measurement setup.

C.5 Tests Plan CE (V)

Table C.1: SMPS EMC test plan, CE (V).

No.	Test	Board	Result
1	Conducted Emissions Test voltage method		
1.1	Measure empty chamber to establish base line, Ambient		
1.2	Measure baseline CE (V) Battery with CMC	Board 3	
1.3	Measure baseline CE (V) Battery	Board 4	
1.4	Measure baseline CE (V) Ground with CMC	Board 3	
1.5	Measure baseline CE (V) Ground	Board 4	
1.6	Measure CE (V) Battery with CMC, Snubber	Board 3	
1.7	Measure CE (V) Battery with Snubber	Board 4	
1.8	Measure CE (V) Ground with CMC, Snubber	Board 3	
1.9	Measure CE (V) Ground with Snubber	Board 4	
1.10	Measure CE (V) Battery with with CMC, Snubber, Filter 1 st order C 6.4 nF	Board 3	
1.11	Measure CE (V) Battery with Snubber, Filter 1 st order C 6.4 nF	Board 4	
1.12	Measure CE (V) Ground with with CMC, Snubber, Filter 1 st order C 6.4 nF	Board 3	
1.13	Measure CE (V) Ground with Snubber, Filter 1 st order C 6.4 nF	Board 4	
1.14	Measure CE (V) Battery with with CMC, Snubber, Filter CL 2 nd order C 6.4 nF, and L 22uH	Board 3	
1.15	Measure CE (V) Battery with Snubber, Filter CL 2 nd order C 6.4 nF, and L 22uH	Board 4	
1.16	Measure CE (V) Ground with with CMC, Snubber, Filter CL 2 nd order C 6.4 nF, and L 22uH	Board 3	
1.17	Measure CE (V) Ground with Snubber, Filter CL 2 nd order C 6.4 nF, and L 22uH	Board 4	

Continuation of Table C.1			
No.	Test	Board	Result
1.18	Measure CE (V) Battery with with CMC, Snubber, Filter LC 2 nd order L 22uH, and C 6.4 nF	Board 3	
1.19	Measure CE (V) Battery with Snubber, Filter LC 2 nd order L 22uH, and C 6.4 nF	Board 4	
1.20	Measure CE (V) Ground with with CMC, Snubber, Filter LC 2 nd order L 22uH, and C 6.4 nF	Board 3	
1.21	Measure CE (V) Ground with Snubber, Filter LC 2 nd order L 22uH, and C 6.4 nF	Board 4	
1.18	Measure CE (V) Battery with with CMC, Snubber, Filter CLC 3 rd order C 6.4 nF, L 22uH, and C 6.4 nF	Board 3	
1.19	Measure CE (V) Battery with Snubber, Filter CLC 3 rd order C 6.4 nF, L 22uH, and C 6.4 nF	Board 4	
1.20	Measure CE (V) Ground with with CMC, Snubber, Filter CLC 3 rd order C 6.4 nF, L 22uH, and C 6.4 nF	Board 3	
1.21	Measure CE (V) Ground with Snubber, Filter CLC 3 rd order C 6.4 nF, L 22uH, and C 6.4 nF	Board 4	
1.22	Measure CE (V) Battery with with CMC, Snubber, Filter CLC 3 rd order C 6.4 nF, L 22uH, and C 6.4 nF, Shield	Board 3	
1.23	Measure CE (V) Battery with Snubber, Filter CLC 3 rd order C 6.4 nF, L 22uH, and C 6.4 nF, Shield	Board 4	
1.24	Measure CE (V) Ground with with CMC, Snubber, Filter CLC 3 rd order C 6.4 nF, L 22uH, and C 6.4 nF, Shield	Board 3	
1.25	Measure CE (V) Ground with Snubber, Filter CLC 3 rd order C 6.4 nF, L 22uH, and C 6.4 nF, Shield	Board 4	

Appendix - D: VHF Auto Tuner Applied EMC in Design

D.1 Design

The schematic and PCB design presented in this section were made with Altium Designer.

D.1.1 rfTuner v 0.1 Schematic

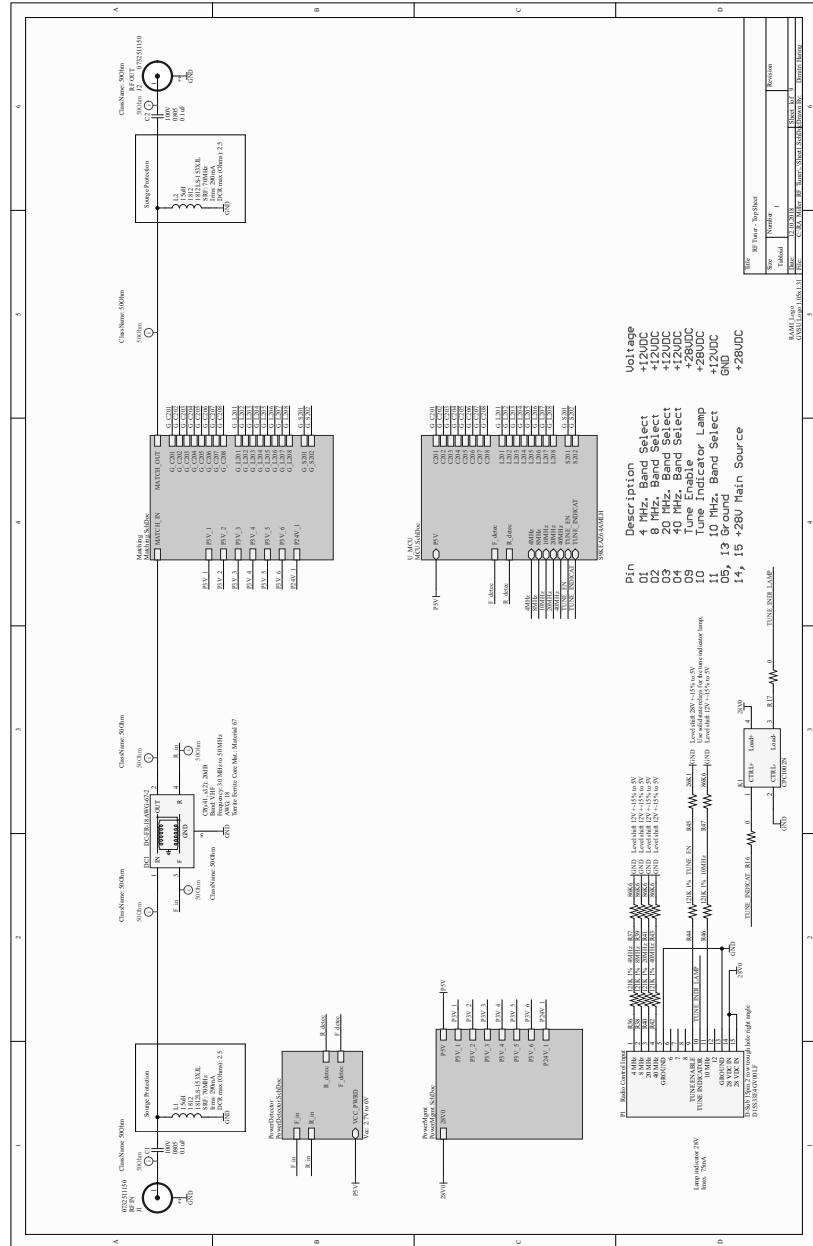


Figure D.1: RF Tuner top schematic.

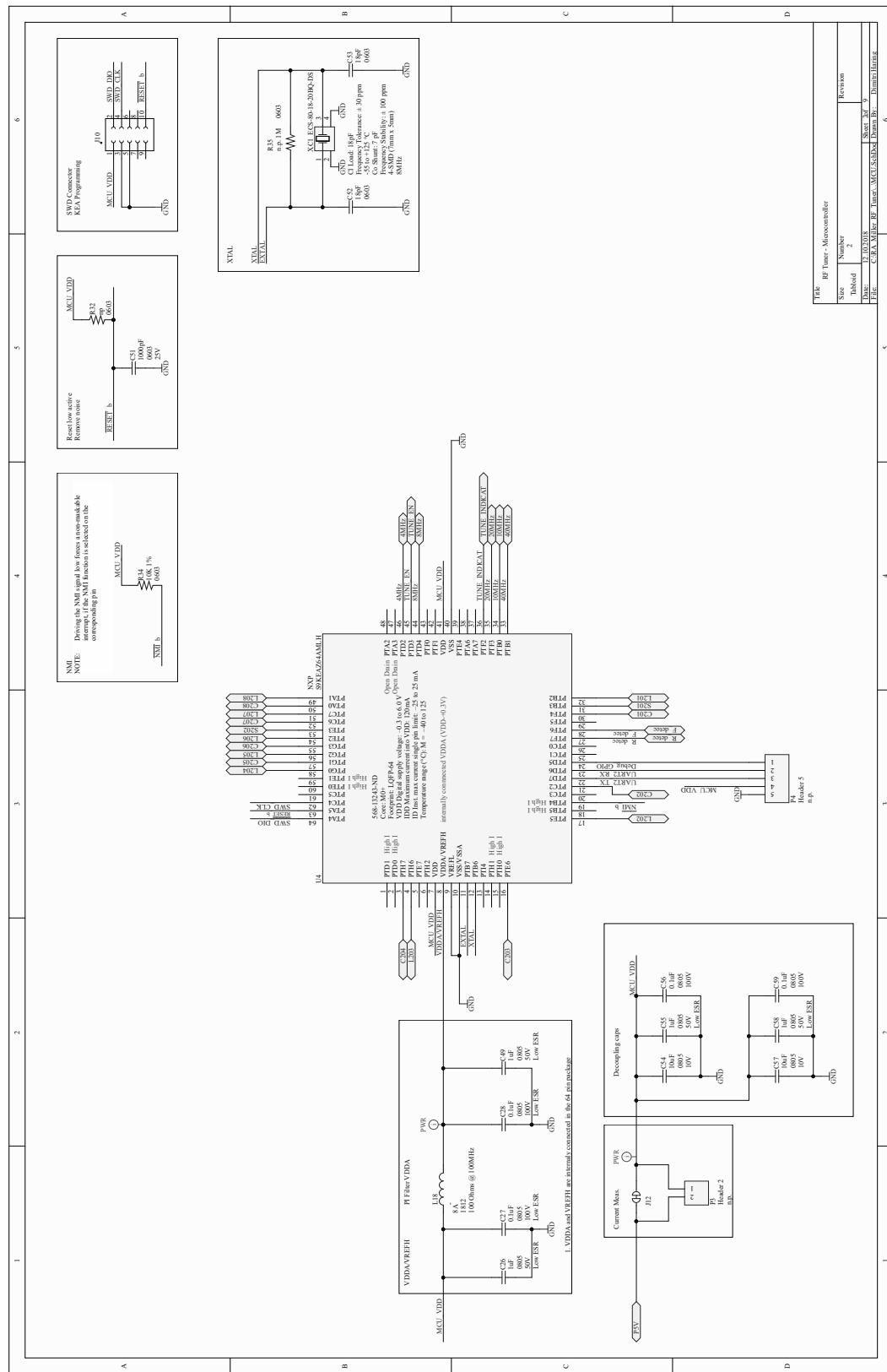


Figure D.2: RF Tuner MCU schematic.

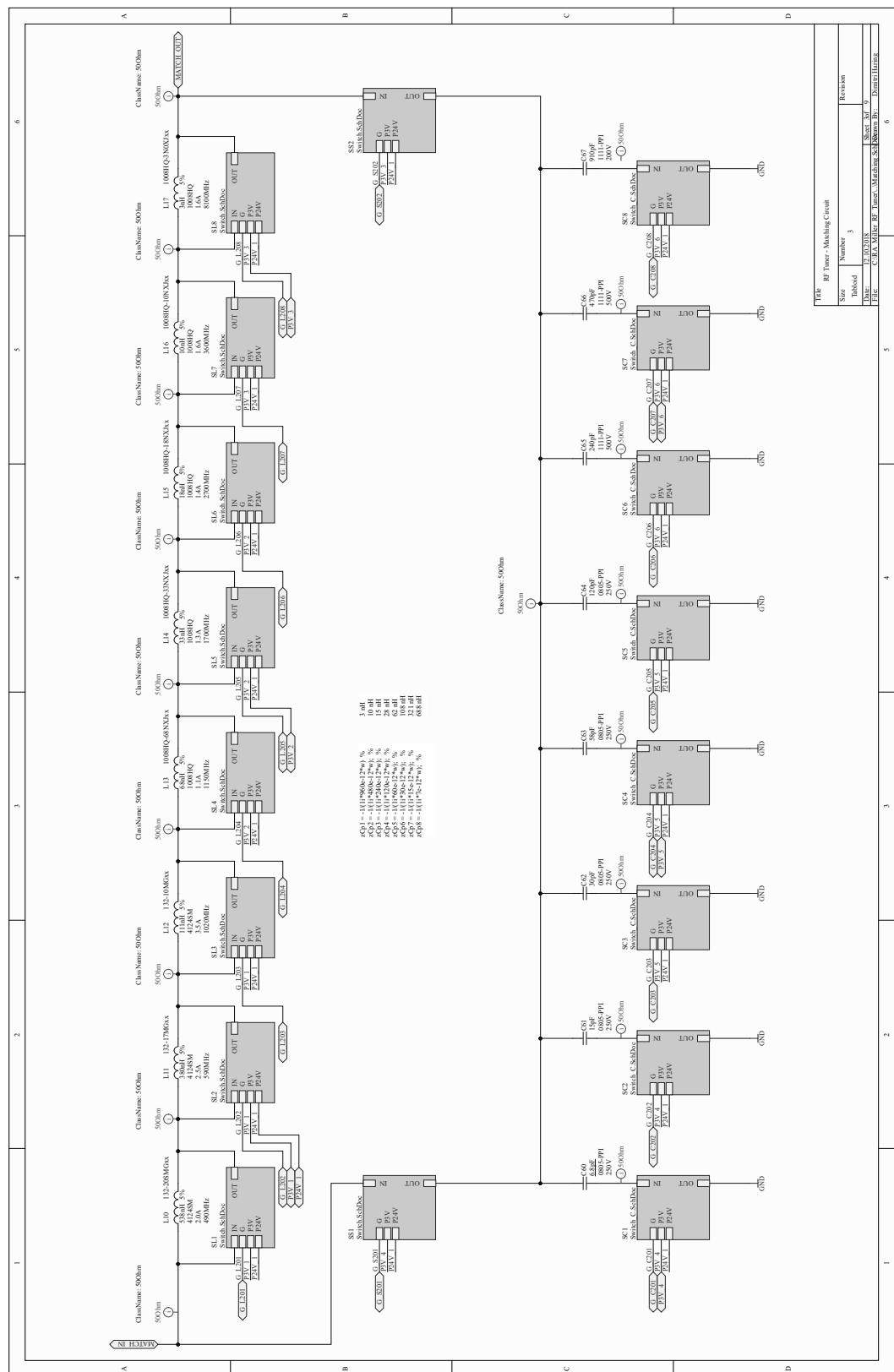
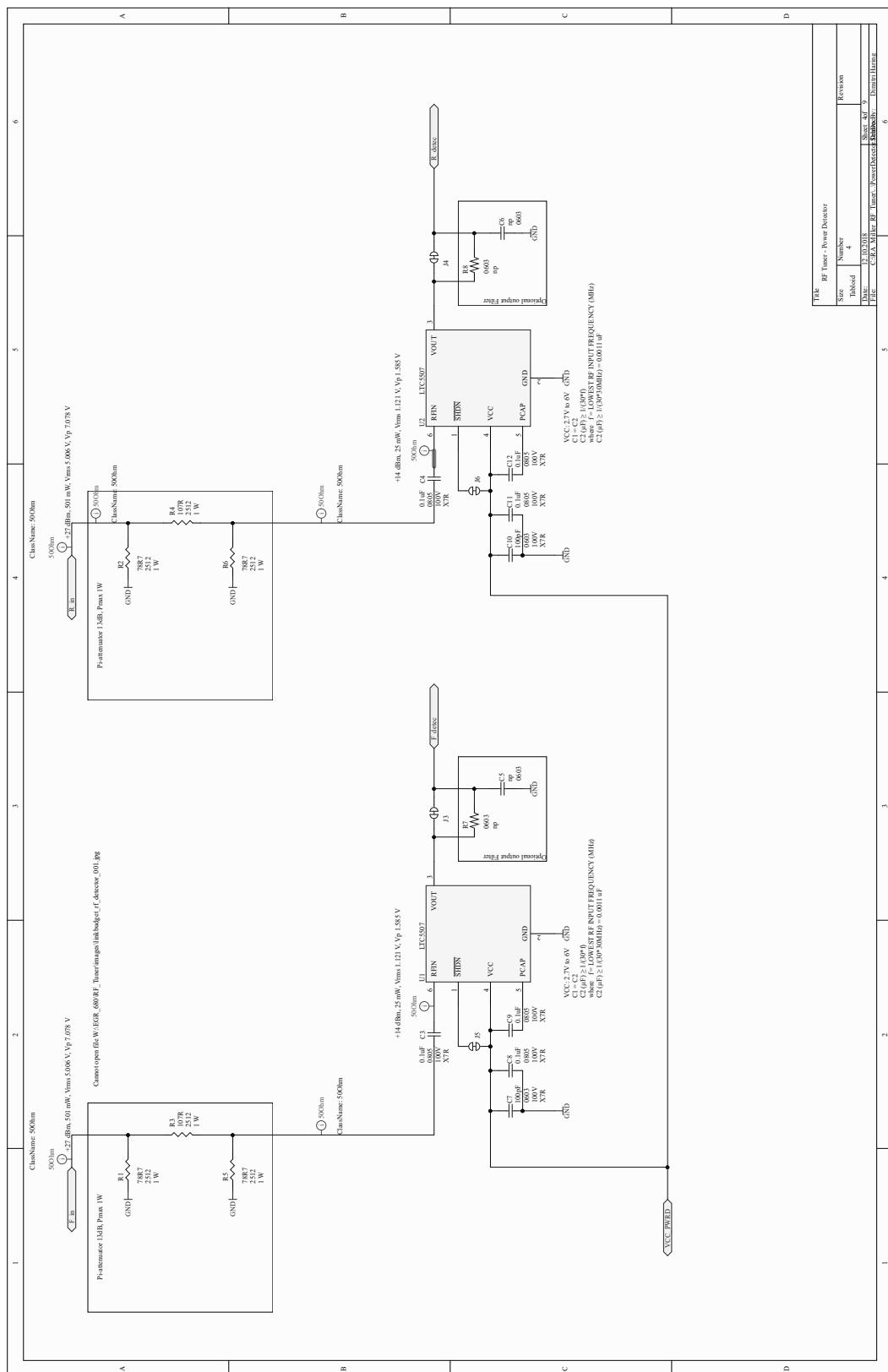


Figure D.3: RF Tuner Matching Network schematic.

Figure D.4: RF Tuner π attenuators and RF power detectors schematic.

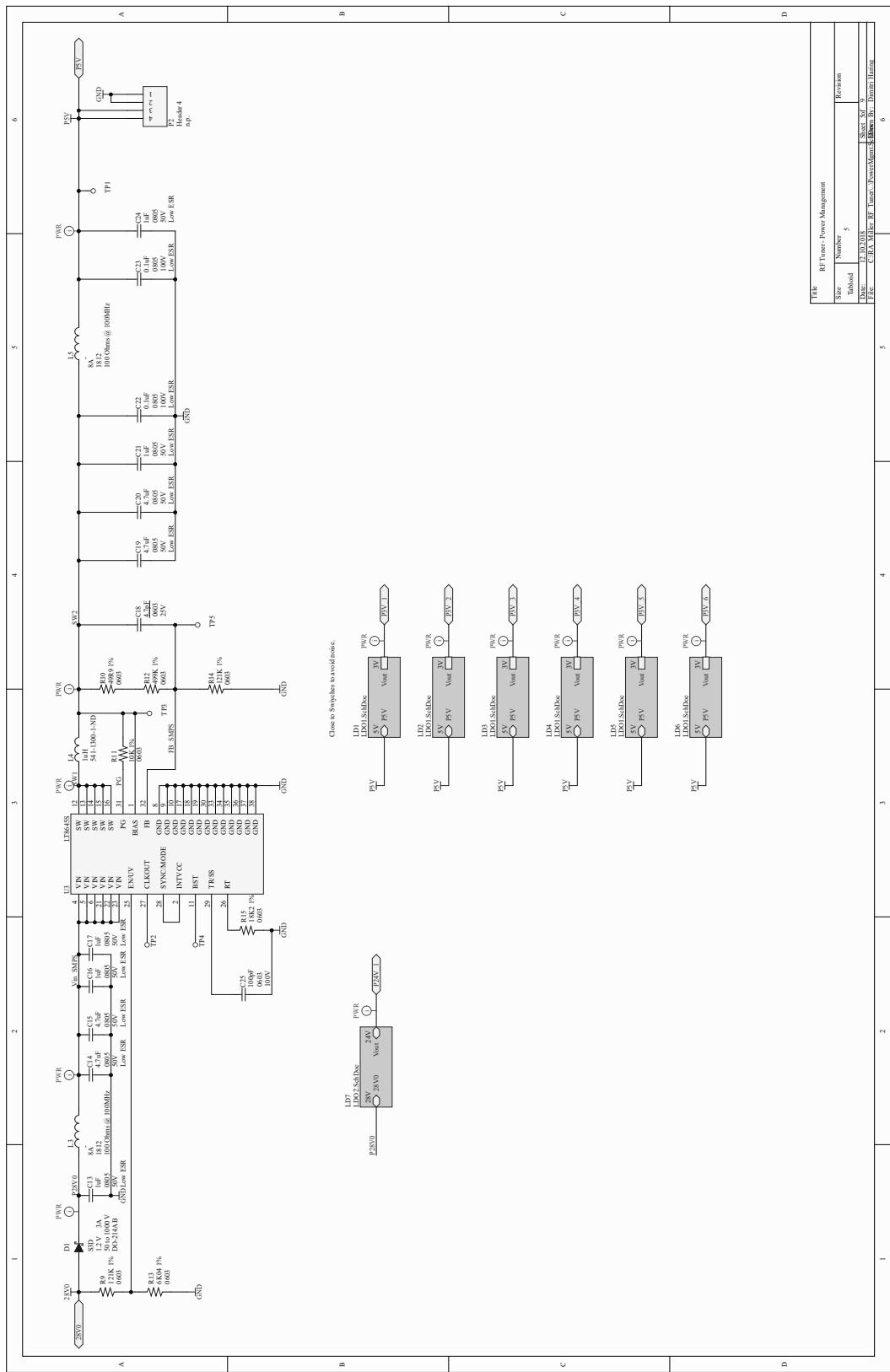


Figure D.5: RF Tuner power management schematic.

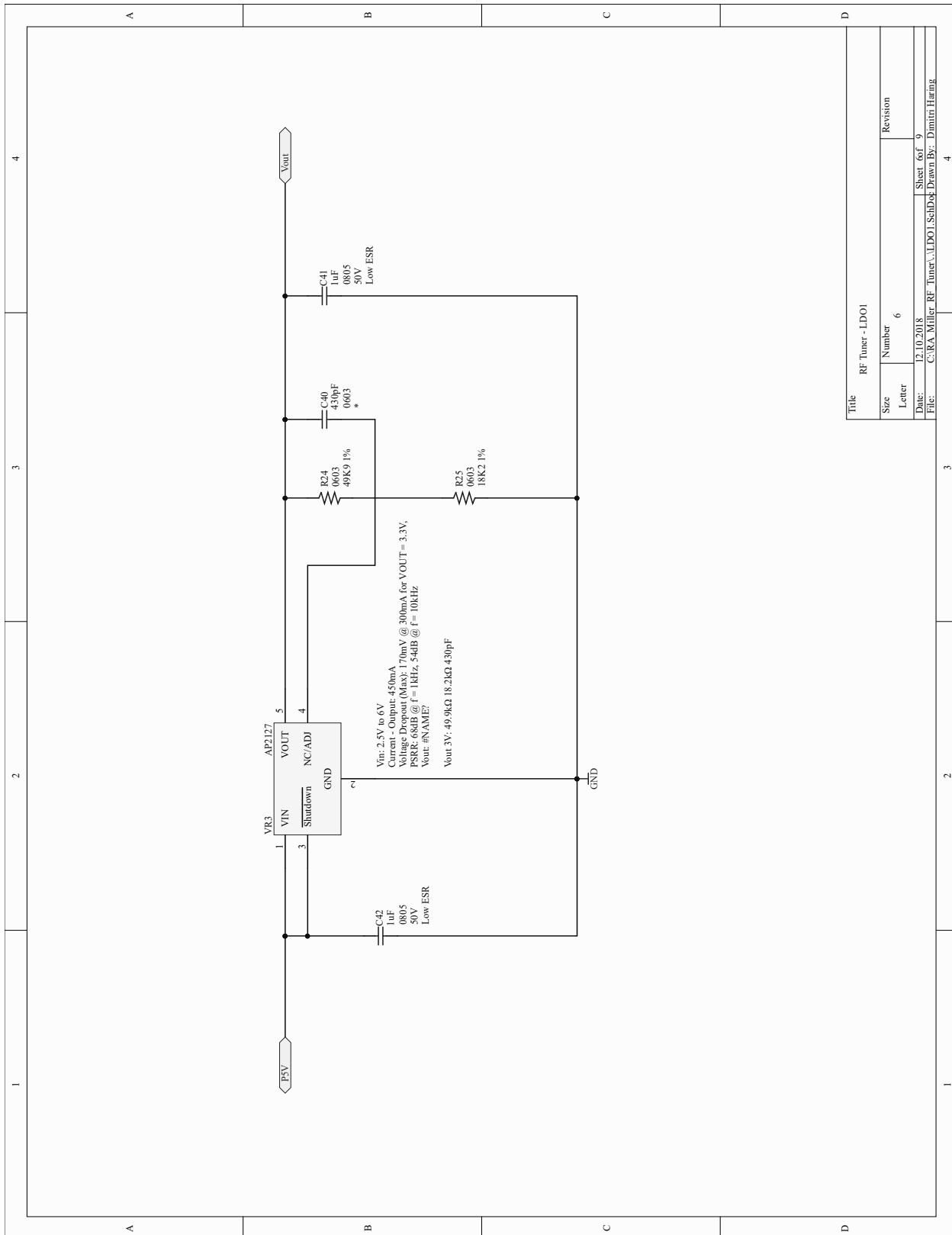


Figure D.6: RF Tuner LDO 3V schematic.

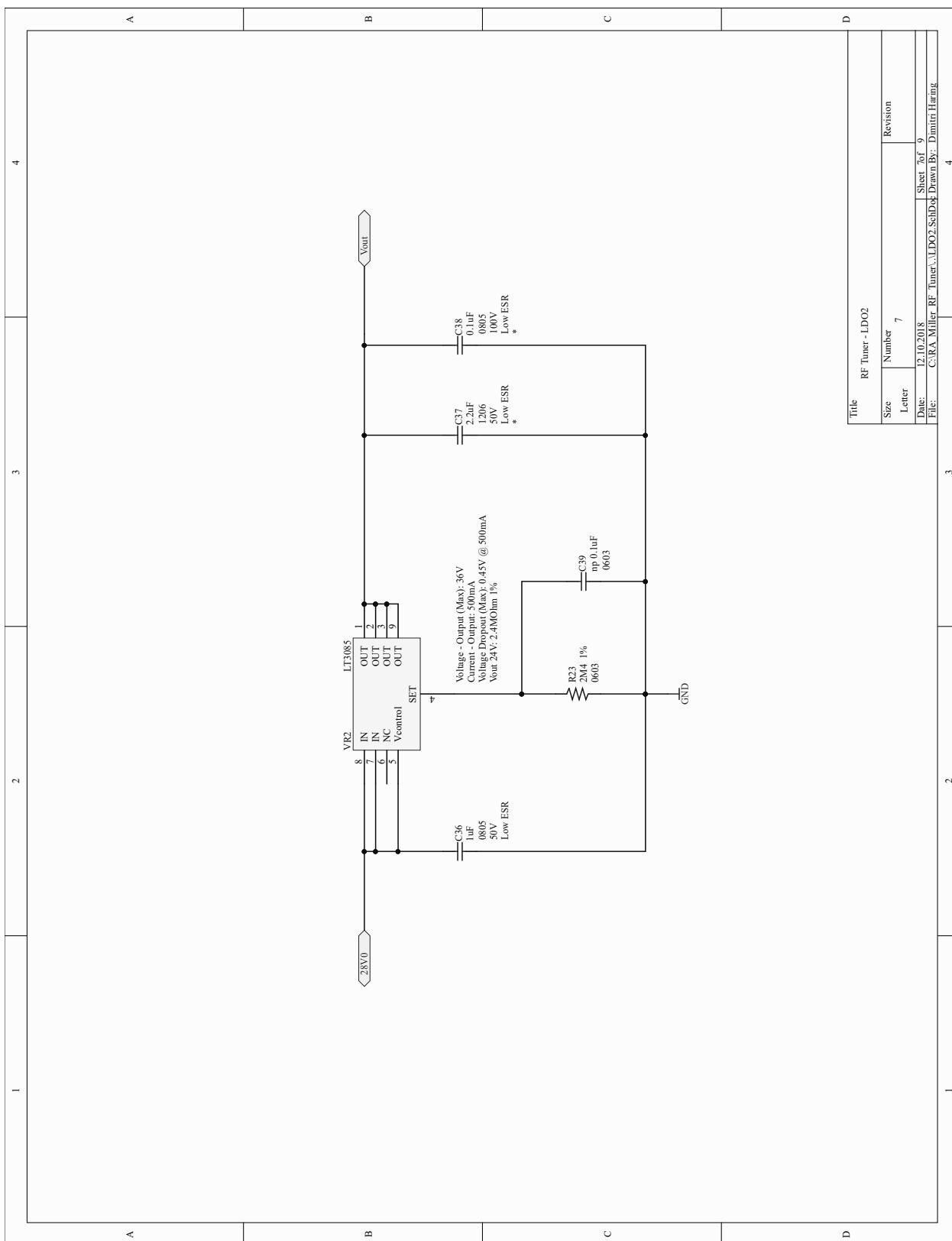


Figure D.7: RF Tuner LDO 24V schematic.

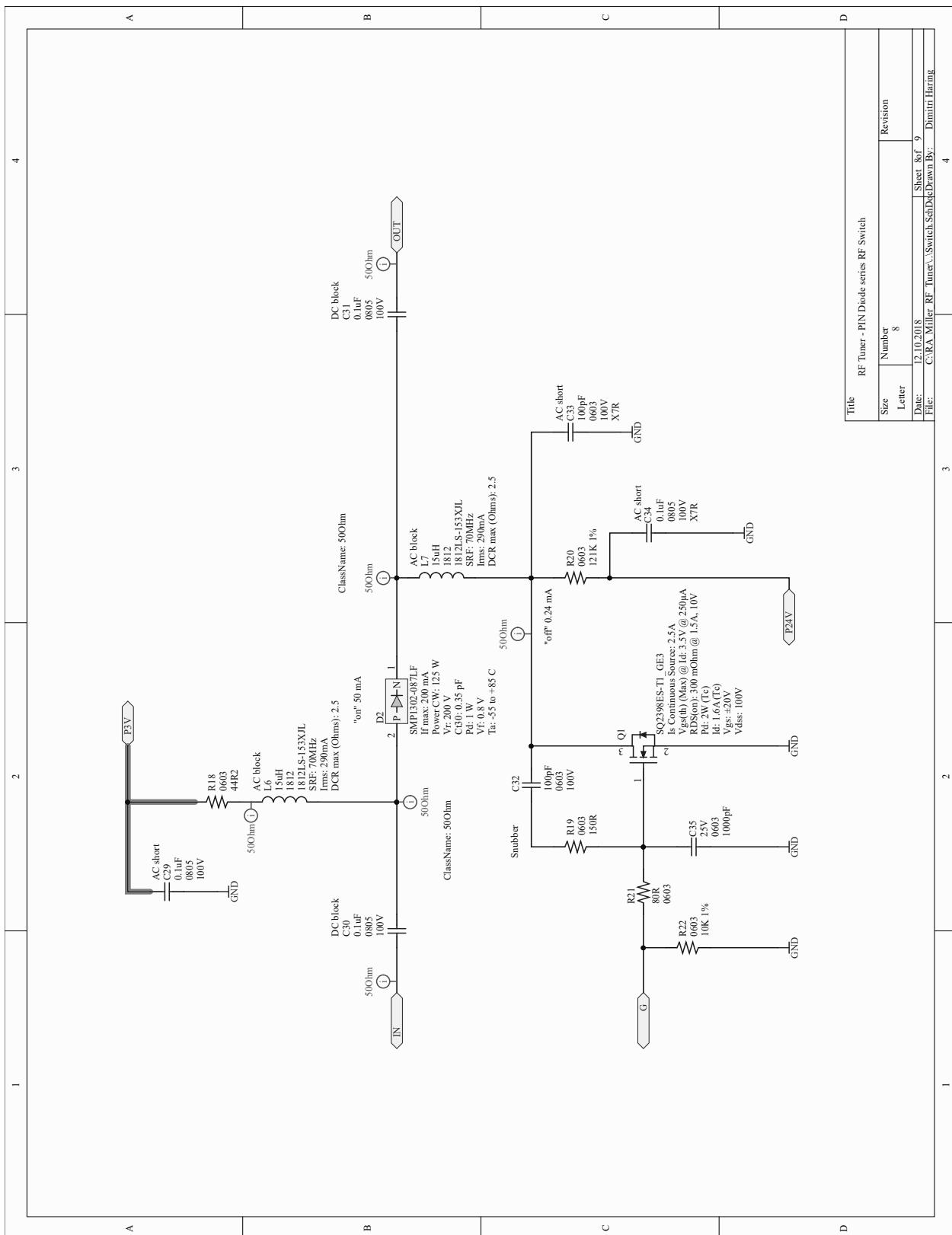


Figure D.8: RF Tuner RF Switch for parallel components schematic.

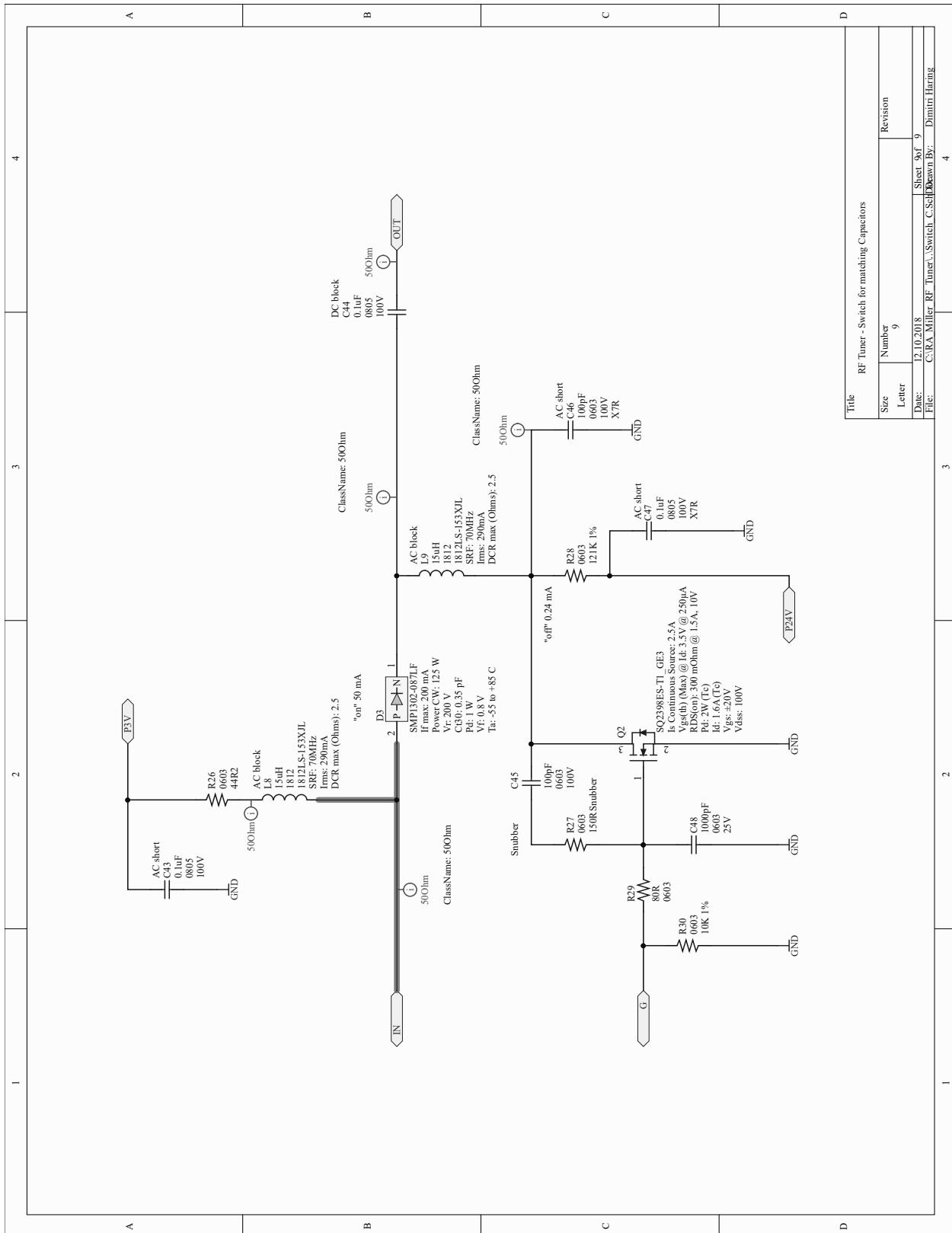


Figure D.9: RF Tuner RF Switch for capacitors schematic.

D.1.2 PCB 3D View

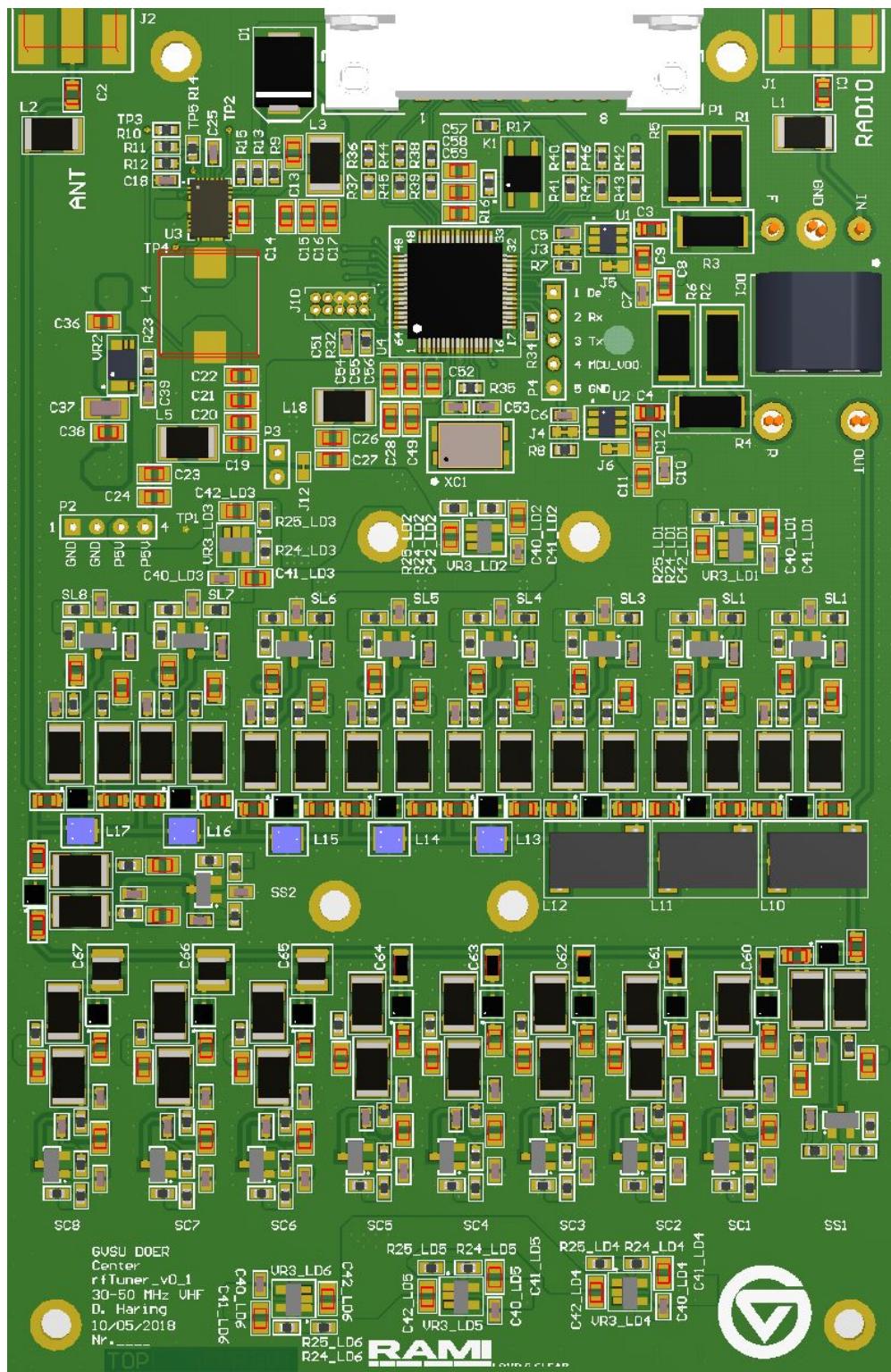


Figure D.10: RF Tuner top PCB 3D view.

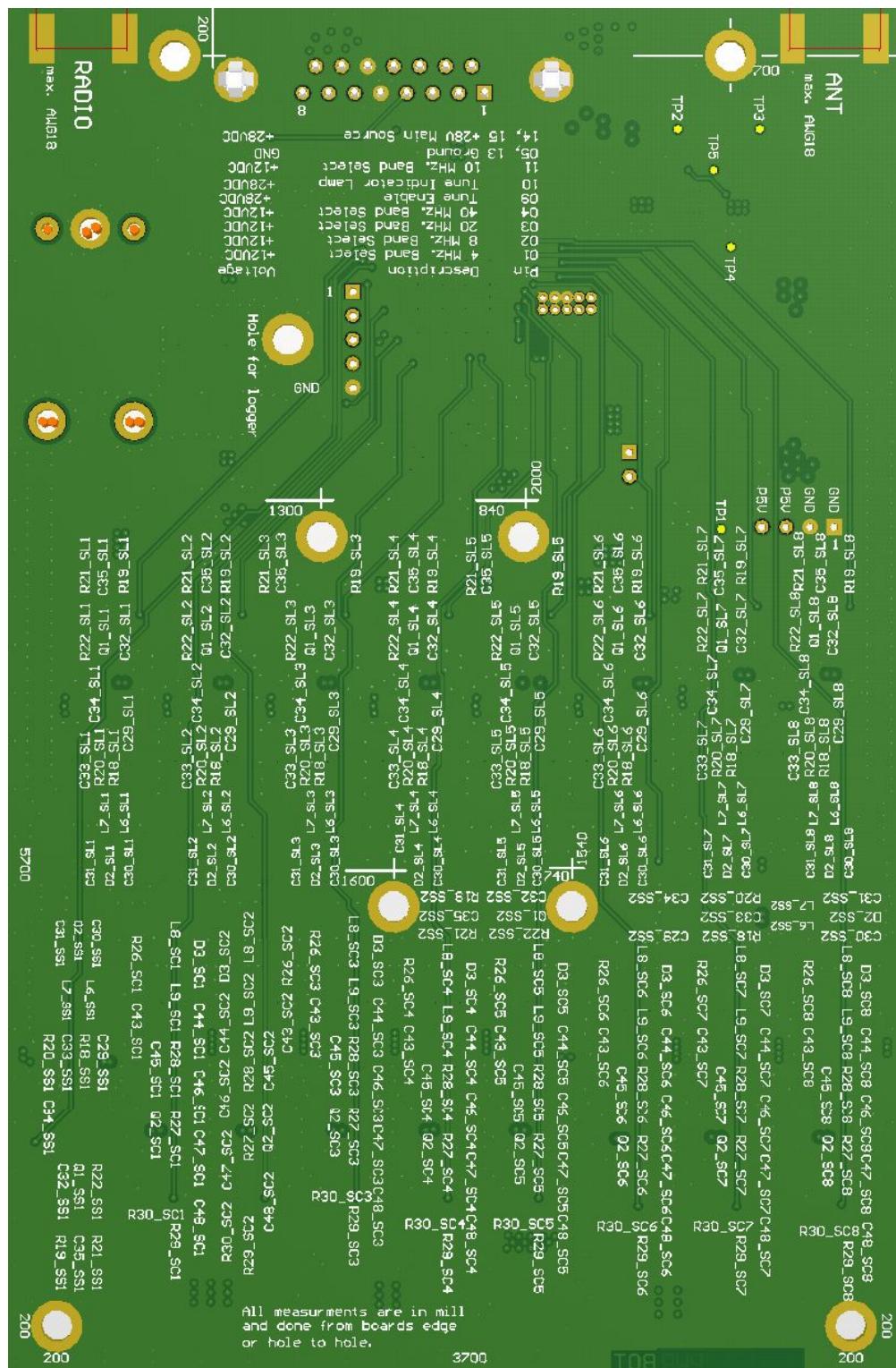


Figure D.11: RF Tuner bottom PCB 3D view.

D.1.3 PCB Drill Drawing

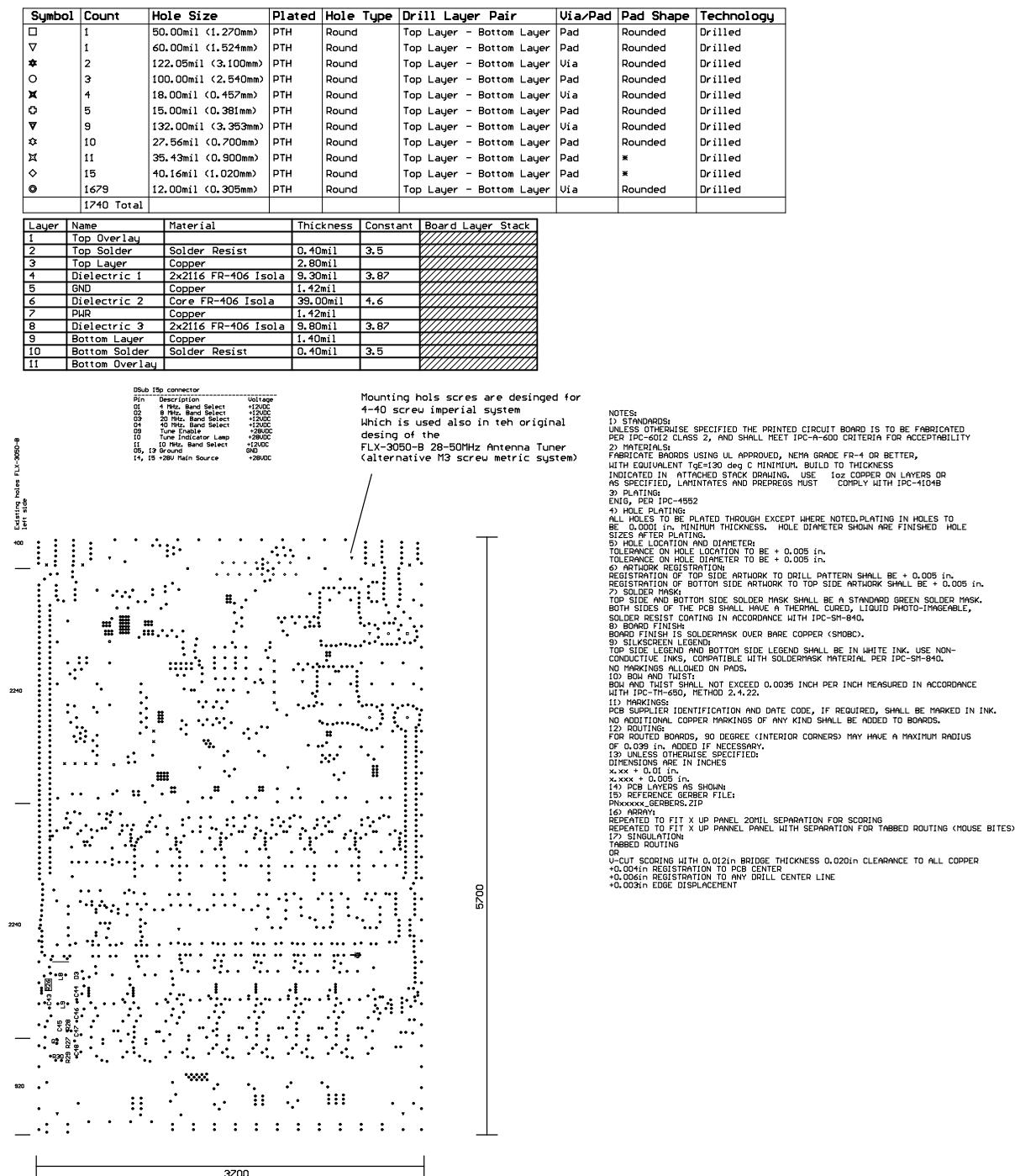


Figure D.12: RF Tuner drill drawing.

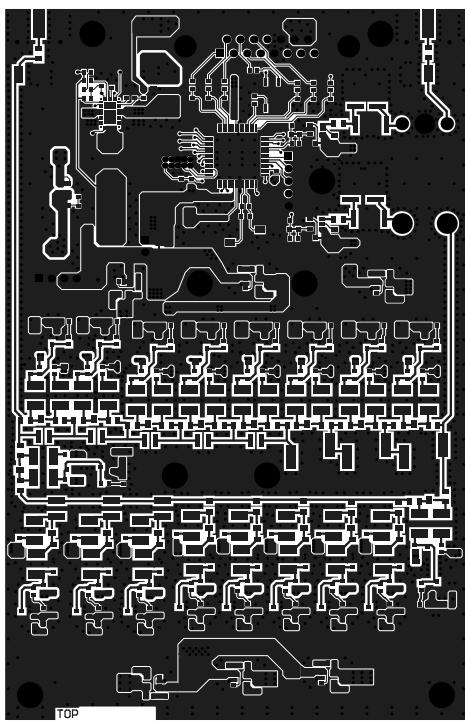
D.1.4 PCB Layers

Figure D.13: RF Tuner PCB top layer L1.

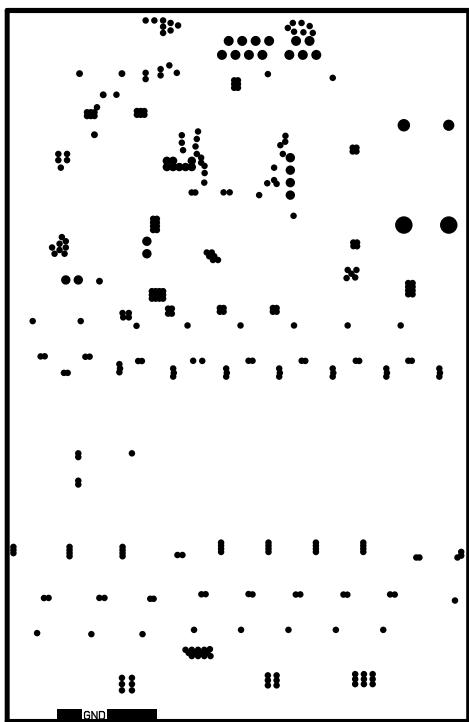


Figure D.14: RF Tuner PCB GND plane L2.

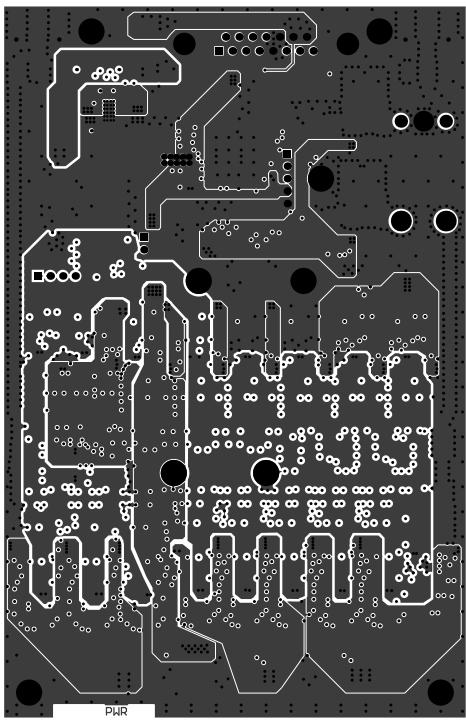


Figure D.15: RF Tuner PCB PWR layer L3.

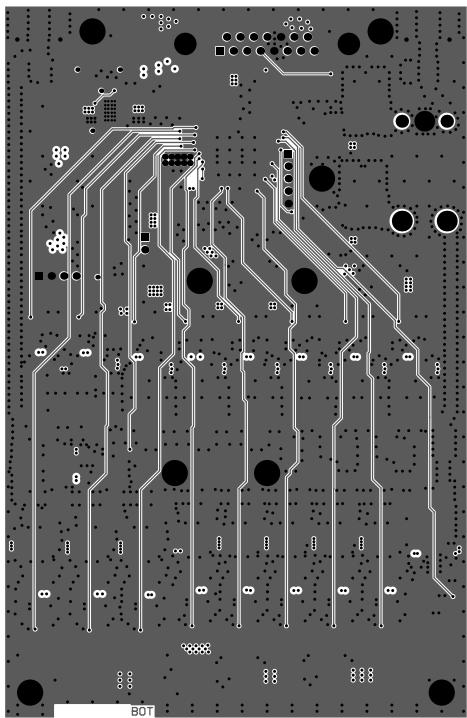
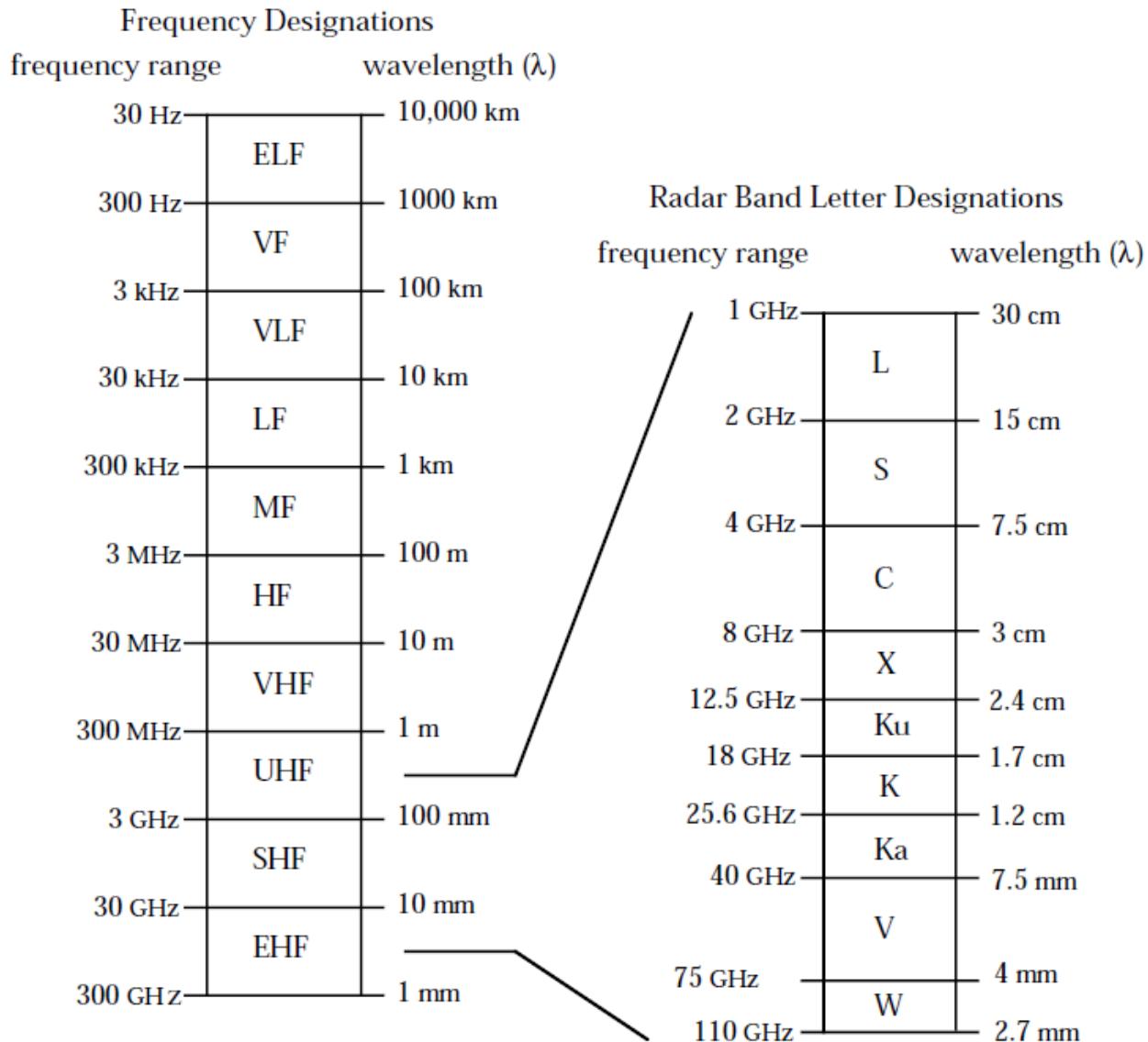


Figure D.16: RF Tuner PCB bottom layer L4.

Appendix - E: Tables and Knowledge

E.1 Frequency Bands



ELF: Extremely Low Frequency
 VF: Voice Frequency
 VLF: Very Low Frequency
 LF: Low Frequency
 MF: Medium Frequency

HF: High Frequency
 VHF: Very High Frequency
 UHF: Ultra High Frequency
 SHF: Super High Frequency
 EHF: Extremely High Frequency

Figure E.1: Frequency bands [14].

E.2 Return Loss vs. VSWR

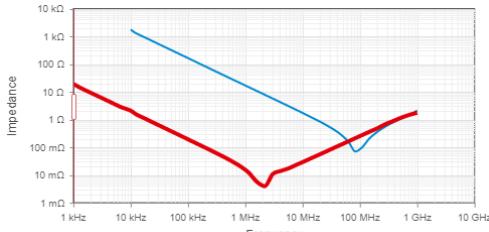
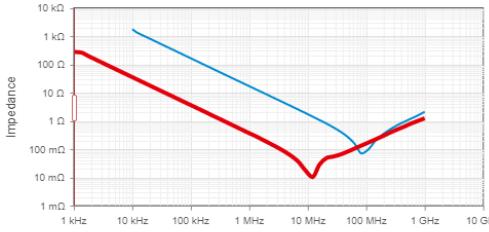
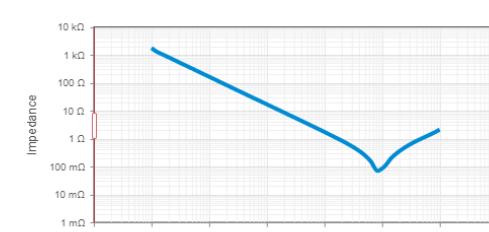
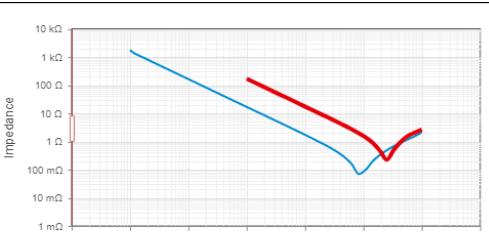
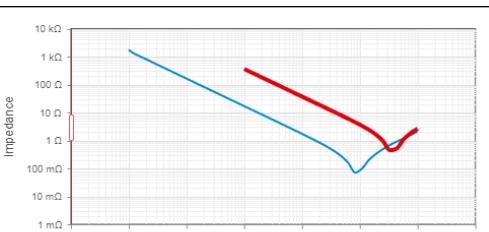
RETURN LOSS (dB)	VSWR	RETURN LOSS (dB)	VSWR	RETURN LOSS (dB)	VSWR	RETURN LOSS (dB)	VSWR	RETURN LOSS (dB)	VSWR
46.064	1.01	13.842	1.51	9.485	2.01	7.327	2.51	5.999	3.01
40.086	1.02	13.708	1.52	9.428	2.02	7.294	2.52	5.970	3.02
36.607	1.03	13.577	1.53	9.372	2.03	7.262	2.53	5.956	3.03
34.151	1.04	13.449	1.54	9.317	2.04	7.230	2.54	5.935	3.04
32.256	1.05	13.324	1.55	9.262	2.05	7.198	2.55	5.914	3.05
30.714	1.06	13.201	1.56	9.208	2.06	7.167	2.56	5.893	3.06
29.417	1.07	13.081	1.57	9.155	2.07	7.135	2.57	5.872	3.07
28.299	1.08	12.964	1.58	9.103	2.08	7.105	2.58	5.852	3.08
27.318	1.09	12.849	1.59	9.051	2.09	7.074	2.59	5.832	3.09
26.444	1.10	12.736	1.60	8.999	2.10	7.044	2.60	5.811	3.10
25.658	1.11	12.625	1.61	8.949	2.11	7.014	2.61	5.791	3.11
24.943	1.12	12.518	1.62	8.899	2.12	6.984	2.62	5.771	3.12
24.289	1.13	12.412	1.63	8.849	2.13	6.954	2.63	5.751	3.13
23.686	1.14	12.308	1.64	8.800	2.14	6.925	2.64	5.732	3.14
23.127	1.15	12.207	1.65	8.752	2.15	6.896	2.65	5.712	3.15
22.607	1.16	12.107	1.66	8.705	2.16	6.867	2.66	5.693	3.16
22.120	1.17	12.009	1.67	8.657	2.17	6.839	2.67	5.674	3.17
21.664	1.18	11.913	1.68	8.611	2.18	6.811	2.68	5.654	3.18
21.234	1.19	11.818	1.69	8.565	2.19	6.783	2.69	5.635	3.19
20.828	1.20	11.725	1.70	8.519	2.20	6.755	2.70	5.617	3.20
20.443	1.21	11.634	1.71	8.474	2.21	6.728	2.71	5.598	3.21
20.079	1.22	11.545	1.72	8.430	2.22	6.700	2.72	5.579	3.22
19.732	1.23	11.457	1.73	8.386	2.23	6.673	2.73	5.561	3.23
19.401	1.24	11.370	1.74	8.342	2.24	6.646	2.74	5.542	3.24
19.085	1.25	11.285	1.75	8.299	2.25	6.620	2.75	5.524	3.25
18.783	1.26	11.202	1.76	8.257	2.26	6.594	2.76	5.506	3.26
18.493	1.27	11.120	1.77	8.215	2.27	6.567	2.77	5.488	3.27
18.216	1.28	11.039	1.78	8.173	2.28	6.541	2.78	5.470	3.28
17.949	1.29	10.960	1.79	8.138	2.29	6.516	2.79	5.452	3.29
17.690	1.30	10.881	1.80	8.091	2.30	6.490	2.80	5.435	3.30
17.445	1.31	10.804	1.81	8.051	2.31	6.465	2.81	5.417	3.31
17.207	1.32	10.729	1.82	8.011	2.32	6.440	2.82	5.400	3.32
16.977	1.33	10.654	1.83	7.972	2.33	6.415	2.83	5.383	3.33
16.755	1.34	10.581	1.84	7.933	2.34	6.390	2.84	5.365	3.34
16.540	1.35	10.509	1.85	7.894	2.35	6.366	2.85	5.348	3.35
16.332	1.36	10.437	1.86	7.856	2.36	6.341	2.86	5.331	3.36
16.131	1.37	10.367	1.87	7.818	2.37	6.317	2.87	5.315	3.37
15.936	1.38	10.298	1.88	7.781	2.38	6.293	2.88	5.298	3.38
15.747	1.39	10.230	1.89	7.744	2.39	6.270	2.89	5.281	3.39
15.563	1.40	10.163	1.90	7.707	2.40	6.246	2.90	5.265	3.40
15.385	1.41	10.097	1.91	7.671	2.41	6.223	2.91	5.248	3.41
15.211	1.42	10.032	1.92	7.635	2.42	6.200	2.92	5.232	3.42
15.043	1.43	9.968	1.93	7.599	2.43	6.177	2.93	5.216	3.43
14.879	1.44	9.904	1.94	7.564	2.44	6.154	2.94	5.200	3.44
14.719	1.45	9.842	1.95	7.529	2.45	6.131	2.95	5.184	3.45
14.564	1.46	9.780	1.96	7.494	2.46	6.109	2.96	5.168	3.46
14.412	1.47	9.720	1.97	7.460	2.47	6.086	2.97	5.152	3.47
14.264	1.48	9.660	1.98	7.426	2.48	6.064	2.98	5.137	3.48
14.120	1.49	9.601	1.99	7.393	2.49	6.042	2.99	5.121	3.49
13.979	1.50	9.542	2.00	7.360	2.50	6.021	3.00	5.105	3.50

Figure E.2: Return loss vs. VSWR [34]

E.3 Capacitors - Rule of Dump

The goal is to evaluate a center frequency which shall suppressed. Based on this frequency a capacitor can be chosen, which acts as a starting point. The next step is to make measurements on the effect of the capacitor and if it helps at the right place. Otherwise chose a lower capacitance value to shift the suppression effect to a higher frequency or a higher capacitance value to reach lower frequencies. Tab. E.1 shows the impedance plot to common capacitor values and gives the reader an estimate what capacitor in what frequency range will have an impact. As reference cap was ten nF chose, which is the blue line in the plot, any deviation is shown in red. The capacitors are from Würth's Red Expert [35] X7R 0805 50V 10% -55 +125 deg C the 10 nF has part number 885012207092.

Table E.1: Relationship between capacitor value and approximate frequency suppressed.

No.	Frequency	Capacitance	Impedance plot blue 10nF
1	2 MHz	10 μ F	
2	10 MHz	100 nF	
3	100 MHz	10 nF	
4	275 MHz	1 nF	
5	350 MHz	470 pF	

Continuation of Table E.1			
No.	Frequency	Capacitance	Impedance plot blue 10nF
6	1000 MHz	100 pF	

E.4 dBuV Conversions

A hansom online calculator can be found under following reference [36]. Tab. E.3 presents the relationship between $\text{dB}\mu\text{V}$ in a 50Ω system with dBm , μV , mV , and V .

Table E.3: Relationship between $\text{dB}\mu\text{V}$ in a 50Ω system with dBm , μV , mV , and V .

$\text{dB}\mu\text{V}$	dBm	μV	mV	V
-33	-140	2.24e-2	2.24e-5	2.24e-8
-20	-127	0.1	0.0001	0.0000001
0	-107	1	0.001	0.000001
20	-87	10	0.01	0.00001
40	-67	100	0.1	0.0001
60	-47	1000	1	0.001
80	-27	10000	10	0.01
100	-7	100000	100	0.1
120	13	1000000	1000	1

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