22/11/17 FN

Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 50384

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2017
Third/Fifth/Sixth Semester
Computer Science and Engineering
CS6303 – COMPUTER ARCHITECTURE
Common to : Electronics and Communication Engineering, Electronics and Instrumentation Engineering, Instrumentation and Control Engineering, Robotics and Automation Engineering, Information Technology
(Regulations 2013)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A (10×2=20 Marks)

1. What are components of a computer system ?
2. What are the addressing modes ?
3. Subtract $(11011)_2 - (10011)_2$ using 2's complement.
4. Devide $(1001010)_2 \div (1000)_2$.
5. Mention the various types of pipelining.
6. Mention the various phase in executing an instruction.
7. Define strong scaling and weak scaling.
8. Difference between Fine-grained multithreading and Coarse-grained multithreading.
9. What is virtual memory ?
10. How many total bits are required for a direct-mapped cache with 16 KB of data and 4-word blocks, assuming a 32-bit address ?

PART – B (5×13=65 Marks)

11. a) Explain various instruction formats and illustrate the same with an example. (13)

(OR)

b) Explain with an example about the operations and Operands of the Computer Hardware ? (13)

12. a) Illustrate the division algorithm with an example. **(13)**

(OR)

b) i) Add the numbers $(0.5)_{10}$ and $(0.4375)_{10}$ using the floating point addition. **(6½)**

ii) Multiply the numbers $(0.5)_{10}$ and $(0.4375)_{10}$ using the floating point multiplication. **(6½)**

13. a) Explain in detail the operation of the data path. **(13)**

(OR)

b) Explain the pipeline hazard in detail. **(13)**

14. a) Explain with diagrammatic illustration Flynn's classification. **(13)**

(OR)

b) Describe Simultaneous Multithreading (SMT) with an example. **(13)**

15. a) Explain in detail about the memory technologies. **(13)**

(OR)

b) What is cache memory ? How to improve cache performance ? Discuss. **(13)**

PART – C **(1×15=15 Marks)**

16. a) i) Suppose you want to achieve a speed-up of 90 times faster with 100 processors. What percentage of the original computation can be sequential ? **(8)**

ii) Suppose you want to perform two sums : one is a sum of 10 scalar variables and one is a matrix sum of a pair of two-dimensional arrays, with dimensions 10 by 10. For now let's assume only the matrix sum is parallelizable; we'll see soon how to parallelize scalar sums. What speed-up do you get with 10 versus 40 processors ? Next, calculate the speed-ups assuming the matrices grow to 20 by 20. **(7)**

(OR)

b) Assume the miss rate of an instruction cache is 2% and the miss rate of the data cache is 4%. If a processor has a CPI of 2 without any memory stalls and the miss penalty is 100 cycles for all misses, determine how much faster a processor would run with a perfect cache that never missed. Assume the frequency of all loads and stores is 36%. **(15)**