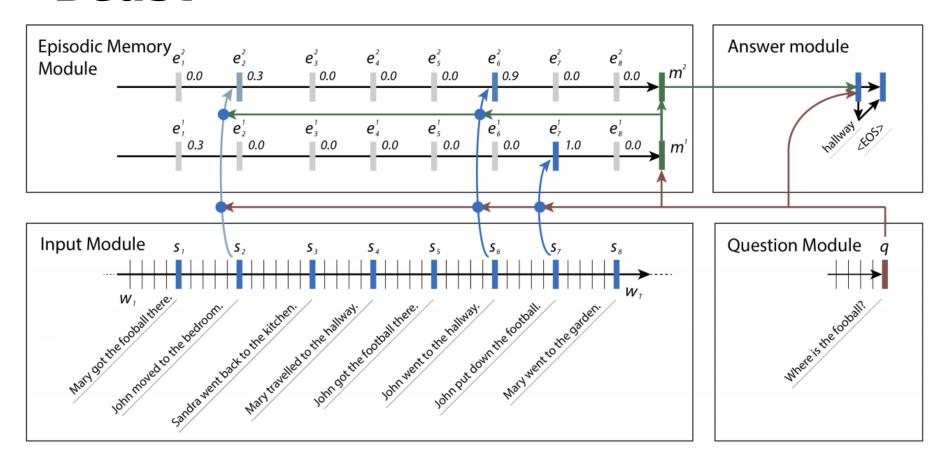
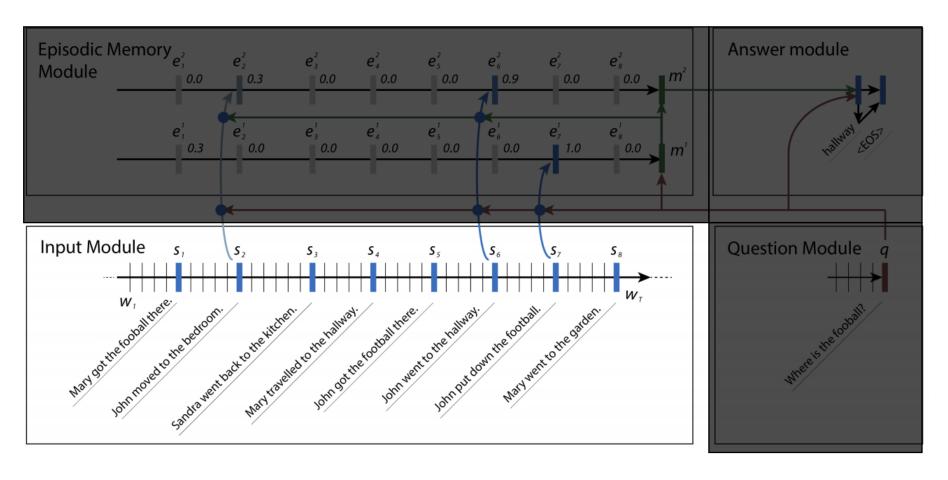
Neural Architectures with Memory By Mohit Kumar(DeepMind)

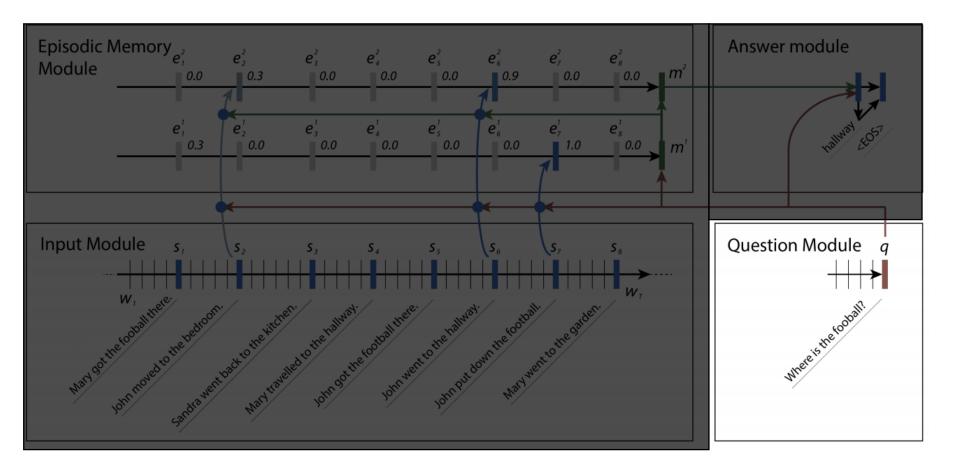
Dynamic Memory Networks - **The Beast**



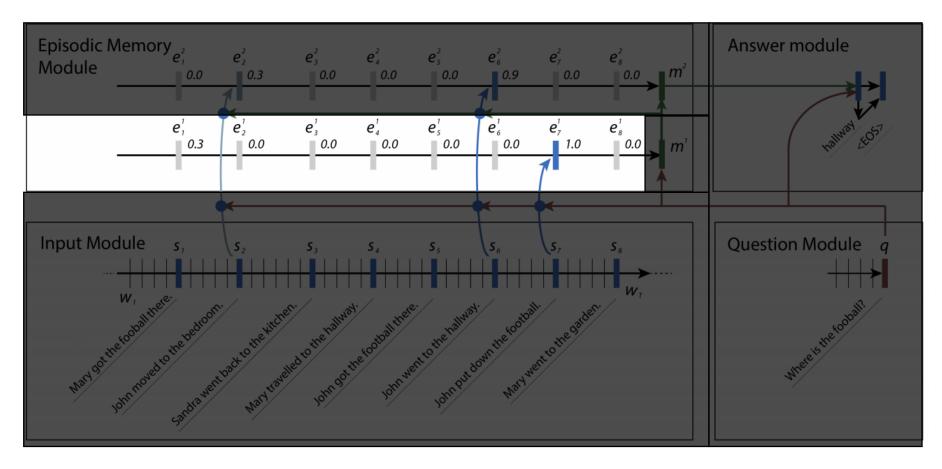
Use RNNs, specifically GRUs for every module

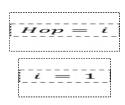


Final GRO utput
$$\longrightarrow c_t = \mathrm{GRU}(w_t^i, c_t^{i-1})$$
 sentence



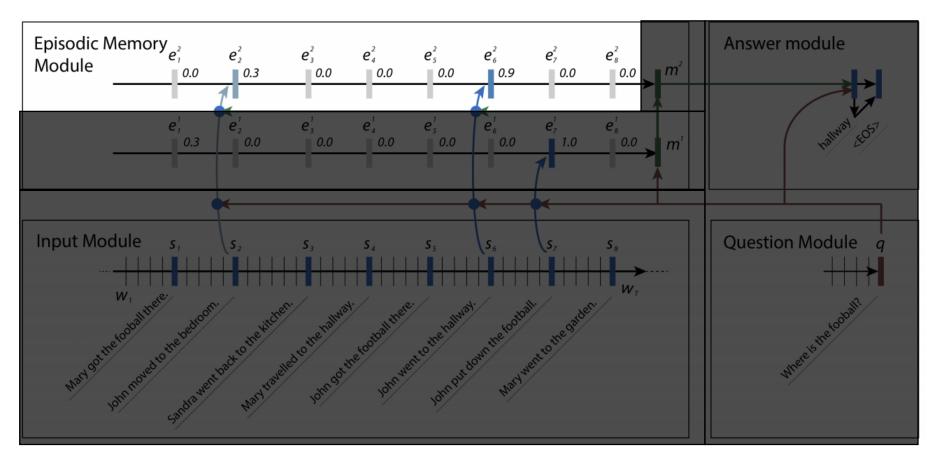
$$q = GRU(q_w^i, q^{i-1})$$

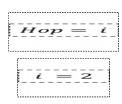




$$h_t^i = g_t^i \text{GRU}(c_t, h_{t-1}^i) + (1 - g_t^i) h_{t-1}^i$$

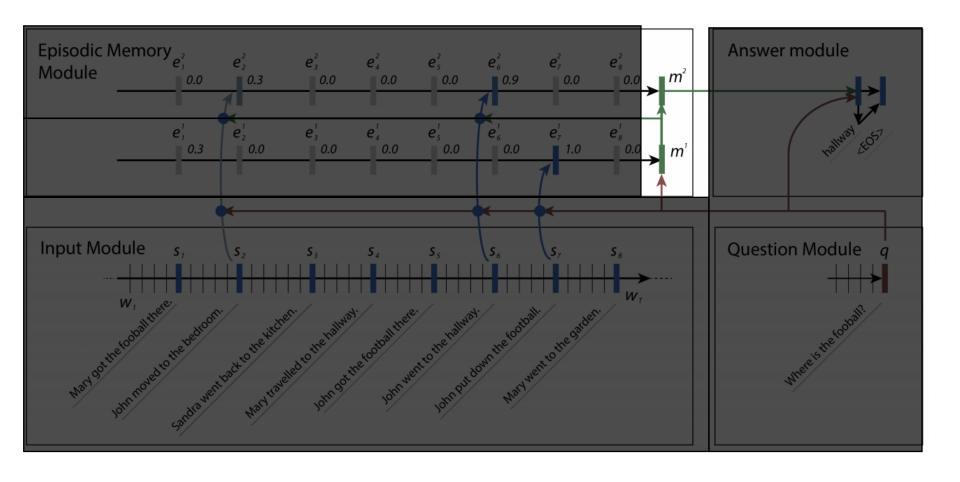
 $e^i = h_{T_C}^i$



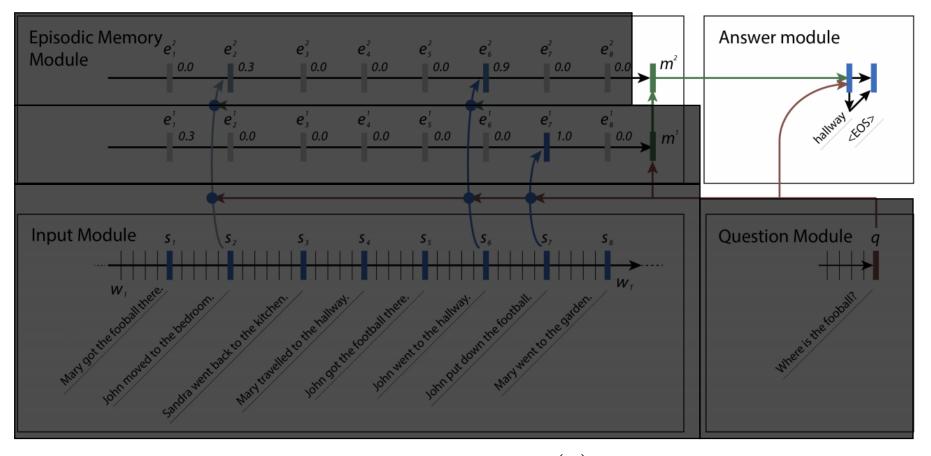


$$h_t^i = g_t^i \text{GRU}(c_t, h_{t-1}^i) + (1 - g_t^i) h_{t-1}^i$$

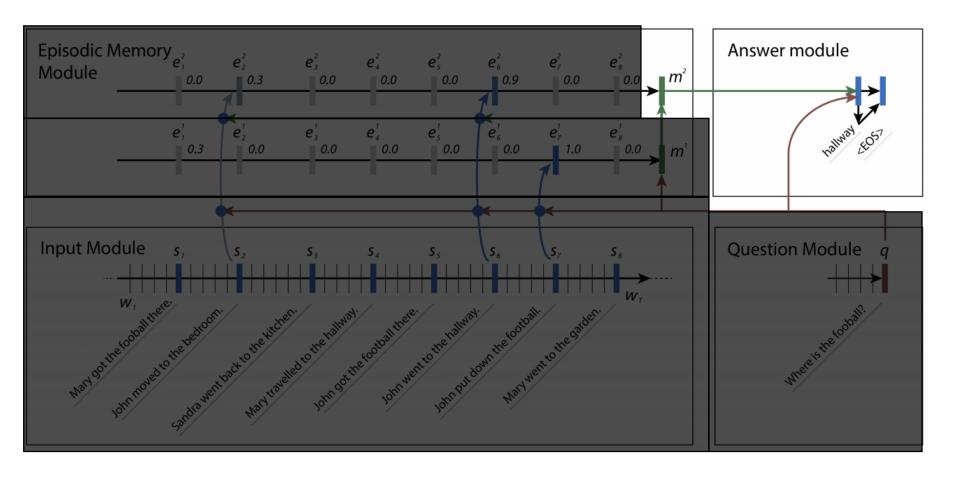
 $e^i = h_{T_C}^i$



$$m^i = GRU(e^i, m^{i-1})$$



$$y_t = \text{Softmax}(W^{(a)}\alpha_t) \qquad \alpha_0 = m^{T_m}$$
$$\alpha_t = \text{GRU}([y_{t-1}, q], \alpha_{t-1})$$

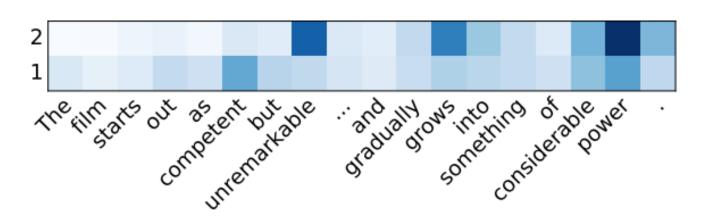


How many GRUs were used with 2 hops?

DMN – Qualitative Results

Question: Where was Mary before the Bedroom? **Answer:** Cinema.

Facts	Episode 1	Episode 2	Episode 3
Yesterday Julie traveled to the school. Yesterday Marie went to the cinema. This morning Julie traveled to the kitchen. Bill went back to the cinema yesterday.			
Mary went to the bedroom this morning. Julie went back to the bedroom this afternoon. [done reading]			



Algorithm Learning

Neural Turing Machine

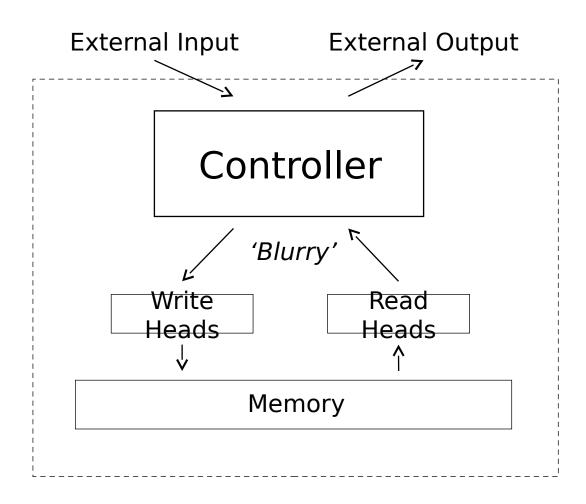
Copy Task: Implement the Algorithm

Given a list of numbers at input, reproduce the list at output

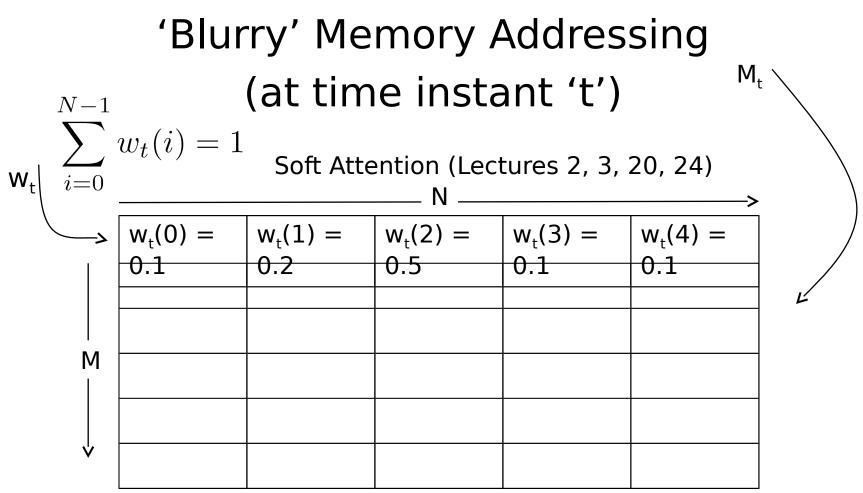
Neural Turing Machine Learns:

- 1. What to write to memory
- 2. When to write to memory
- 3. When to stop writing
- 4. Which memory cell to read from
- 5. How to convert result of read into final output

Neural Turing Machines



Neural Turing Machines



Neural Turing Machines

More formally,

Blurry Read Operation

Given: M_t (memory matrix) of size NxM w_t (weight vector) of length N t (time index)

$$r_t = \sum_{i=0}^{N-1} w_t(i) \mathbf{M}_t(i)$$

Neural Turing Machines: Blurry Writes

Blurry Write Operation

Decomposed into <u>blurry erase</u> + <u>blurry add</u>

Given: M_t (memory matrix) of size NxM

w₊ (weight vector) of length N

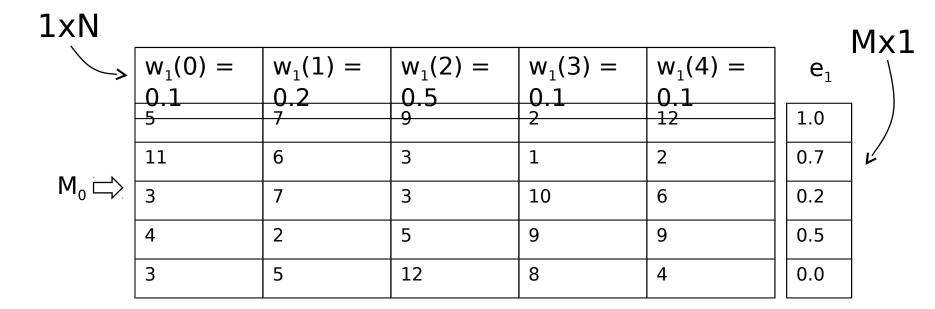
t (time index)

e_t (erase vector) of length M

$$\mathbf{M}_{t}(i) = \mathbf{W}_{t-1}(i) \mathbf{W}_{t}(i) \mathbf{e}_{t} + \mathbf{W}_{t}(i) \mathbf{a}_{t} + \mathbf{W}_{t}(i) \mathbf{a}_{t}$$
 Erase Component Add Component

Neural Turing Machines: Erase

$$\mathbf{M}_t(i) = \mathbf{M}_{t-1}(i)(1 - w_t(i)\mathbf{e}_t)$$



Neural Turing Machines: Erase

$$\mathbf{M}_t(i) = \mathbf{M}_{t-1}(i)(1 - w_t(i)\mathbf{e}_t)$$

$W_1(0) =$	$w_1(1) =$	$w_1(2) =$	$w_1(3) =$	$W_1(4) =$
0.1	0.2	0.5	0.1	0.1
4.5	5.6	4.5	1.8	10.8
10.23	5.16	1.95	0.93	1.86
2.94	6.72	2.7	9.8	5.88
3.8	1.8	3.75	8.55	8.55
3	5	12	8	4

Neural Turing Machines: Addition

$$\mathbf{M}_t(i) = \mathbf{M}_{t-1}(i)(1 - w_t(i)\mathbf{e}_t) + w_t(i)\mathbf{a}_t$$

$W_1(0) =$	$w_1(1) =$	$w_1(2) =$	$w_1(3) =$	$W_1(4) =$
0.1	0.2	0.5	0.1	0.1
4.5	5.6	4.5	1.8	10.8
10.23	5.16	1.95	0.93	1.86
2.94	6.72	2.7	9.8	5.88
3.8	1.8	3.75	8.55	8.55
3	5	12	8	4

Neural Turing Machines: Blurry Writes

$$\mathbf{M}_t(i) = \mathbf{M}_{t-1}(i)(1 - w_t(i)\mathbf{e}_t) + w_t(i)\mathbf{a}_t$$

	4.8	6.2	6	2.1	11.1
B.4.	10.63	5.96	3.95	1.33	2.26
$M_1 \Longrightarrow$	2.74	6.32	1.7	9.6	5.68
	3.8	1.8	3.75	8.55	8.55
	3.2	5.4	13	8.2	4.2

Generating w_t

Content Based

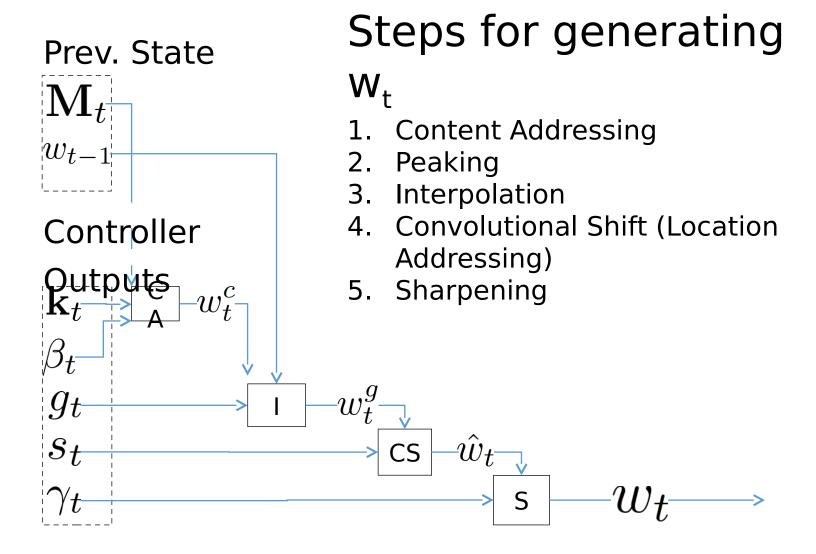
Example: QA Task

- Score sentences by similarity with Question
- Weights as softmax of similarity scores

Location Based

Example: Copy Task

- Move to address
 (i+1) after writing
 to index (i)
- Weights ≈Transitionprobabilities



Prev. State

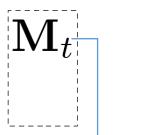
 \mathbf{M}_t

 \mathbf{k}_t :Vector (length M) produced by Controller

Controller

Outputs \mathbf{k}_t

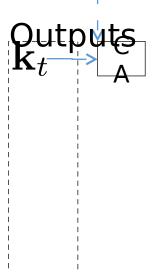
Prev. State



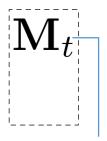
Step 1: Content Addressing

$$\frac{\text{(CA)}}{w_t^c(i)} = \frac{exp < \mathbf{M}_t(i), \mathbf{k}_t >}{\sum_i exp < \mathbf{M}_t(i), \mathbf{k}_t >}$$

Controller



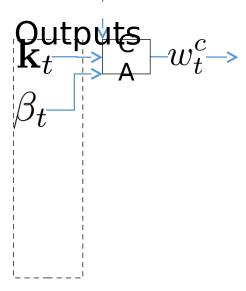
Prev. State



Step 2: Peaking

$$w_t^c(i) = \frac{exp(\beta_t(\langle \mathbf{M}_t(i), \mathbf{k}_t \rangle))}{\sum_i exp(\beta_t(\langle \mathbf{M}_t(i), \mathbf{k}_t \rangle))}$$

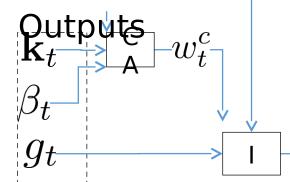
Controller



Prev. State

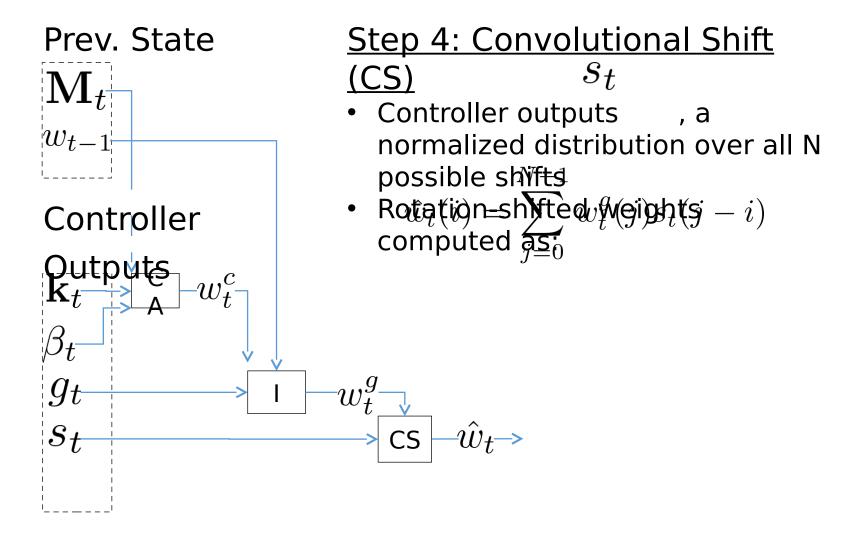


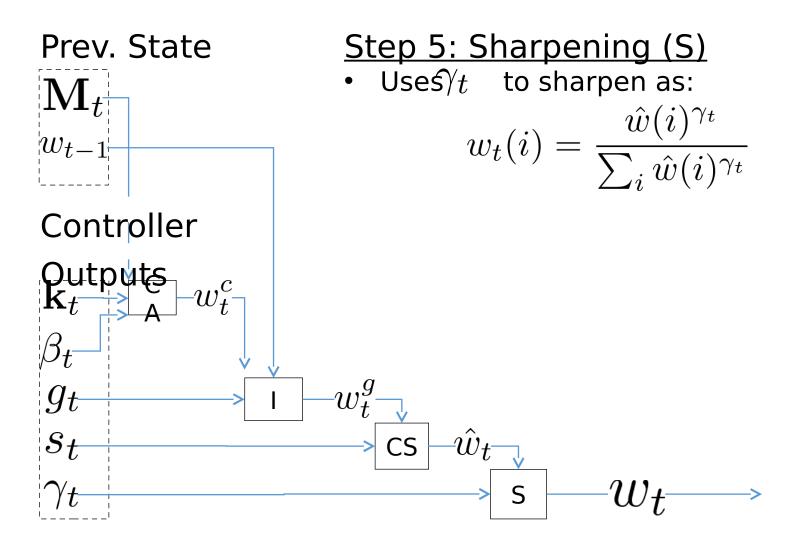
Controller



Step 3: Interpolation (I)

$$w_t^g = g_t w_t^c + (1 - g_t) w_{t-1}$$





Neural Turing Machine: Controller Design

- Feed-forward: faster, more transparency & interpretability about function learnt
- •LSTM: more expressive power, doesn't limit the number of computations per time step

Both are end-to-end differentiable!

- 1. Reading/Writing -> Convex Sums
- 2. w_t generation -> Smooth
- 3. Controller Networks

Neural Turing Machine: Network Overview

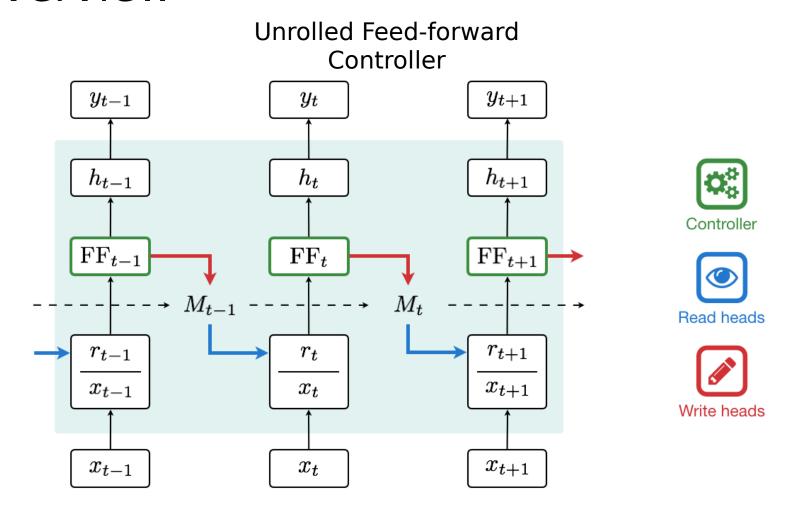


Figure from Snips Al's Medium Post

Neural Turing Machines vs. MemNNs

MemNNs

Memory is static, with focus on retrieving (reading) information from memory

NTMs

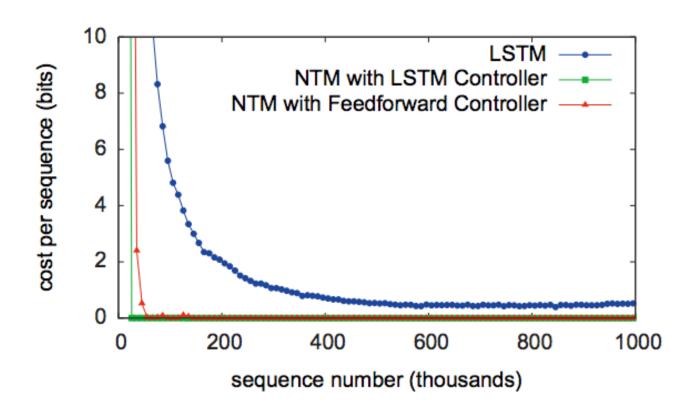
 Memory is continuously written to and read from, with network learning when to perform memory read and write

Neural Turing Machines: Experiments

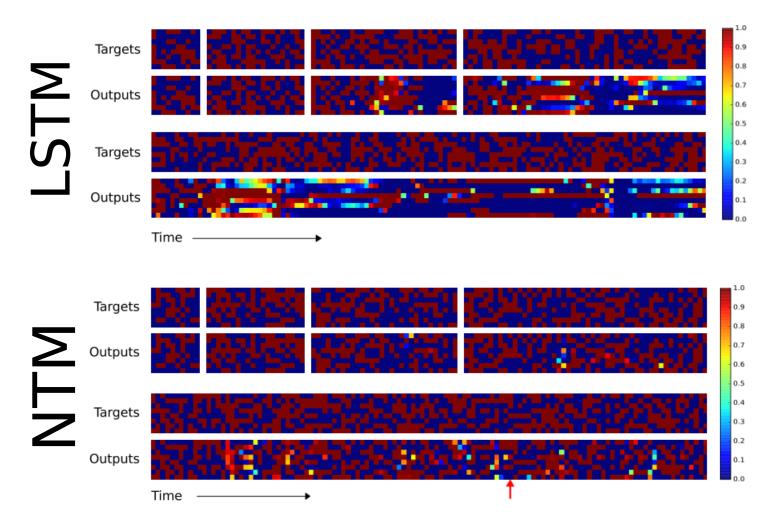
Task	Netwo	rk Size	Number of Parameters		
	NTM w/ LSTM*	LSTM	NTM w/ LSTM	LSTM	
Сору	3 x 100	3 x 256	67K	1.3M	
Repeat Copy	3 x 100	3 x 512	66K	5.3M	
Associative	3 x 100	3 x 256	70K	1.3M	
N-grams	3 x 100	3 x 128	61K	330K	
Priority Sort	2 x 100	3 x 128	269K	385K	

Neural Turing Machines: 'Copy' Learning Curve

Trained on 8-bit sequences, $1 \le \text{sequence length} \le 20$



Neural Turing Machines: 'Copy' Performance



Neural Turing Machines triggered an outbreak of Memory Architectures!

Dynamic Neural Turing Machines

Experimented with addressing schemes

- <u>Dynamic Addresses</u>: Addresses of memory locations learnt in training allows non-linear location-based addressing
- <u>Least recently used weighting</u>: Prefer least recently used memory locations + interpolate with content-based addressing
- <u>Discrete Addressing</u>: Sample the memory location from the contentbased distribution to obtain a one-hot address
- <u>Multi-step Addressing</u>: Allows multiple hops over memory

		Location NTM	Content		Soft A PATM	Discrete DNTM	
	1- step	31.4%	33.6%	,	29.5%	27.9%	
ıamic Neural Turiı	ng Mach	in e with Soft ar	าส์ใหล่ใช้ Addres	sir	ig²\$ch%emes, G	Gulchere et. al., a	ir:

Stack Augmented Recurrent Networks

Learn algorithms based on stack implementations (e.g. learning fixed sequence

Ĉ	Sequence generator	Example		
		aab ba aab bba baaaaab bbbb		
	$\{a^nb^nc^n\mid n>0\}$	aaab bbccca b ca aaaab bbbbccccc		
	$\{a^nb^nc^nd^n\mid n>0\}$	aab bccdda aab bbcccddda b cd		
	$\{a^nb^{2n} \mid n>0\}$	aab bbba aab bbbbba b b		
	$\{a^n b^m c^{n+m} n, m > 0\}$	aabc cca aabbc cccca bc c		
	$n \in [1, k], X \to nXn, X \to =$	(k=2) 12= 21 2122= 2212 11121= 12111		

Uses a stack data structure to store memory (as opposed to a memory matrix)

Stack Augmented Recurrent Networks

•Blurry 'push' and 'pop' on stack. E.g.:

$$s_t[0] = a[Push](h_t) + a[Pop]s_{t-1}[1]$$

•Some results:

method	a^nb^n	$a^nb^nc^n$	$a^nb^nc^nd^n$	a^nb^{2n}	$a^nb^mc^{n+m}$
RNN	25%	23.3%	13.3%	23.3%	33.3%
LSTM	100%	100%	68.3%	75%	100%
List RNN 40+5	100%	33.3%	100%	100%	100%
Stack RNN 40+10	100%	100%	100%	100%	43.3%
Stack RNN 40+10 + rounding	100%	100%	100%	100%	100%

Differentiable Neural Computers

Advanced addressing mechanisms:

- Content Based Addressing
- Temporal Addressing
 - Maintains notion of sequence in addressing
 - Temporal Link Matrix L (size NxN), L[i,j] = degree to which location I was written to after location j.
- Usage Based Addressing

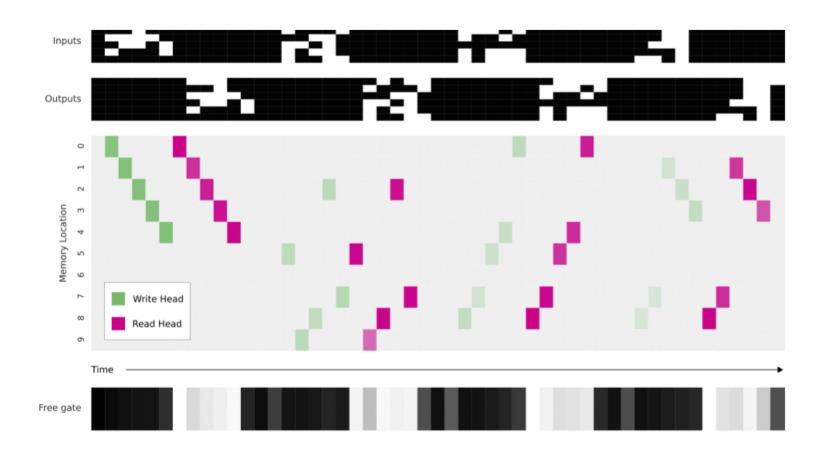
DNC: Usage Based Addressing

 Writing increases usage of cell, reading decreases usage of cell

 Least used location has highest usagebased weighting

 Interpolate b/w usage & content based weights for final write weights

DNC: Example



DNC: Improvements over NTMs

NTM

- Large contiguous blocks of memory needed
- No way to free up memory cells after writing

DNC

- Memory locations non-contiguous, usage-based
- Regular de-allotment based on usage-tracking

Graph Tasks

Graph Representation: (source, edge, destination) tuples

Types of tasks:

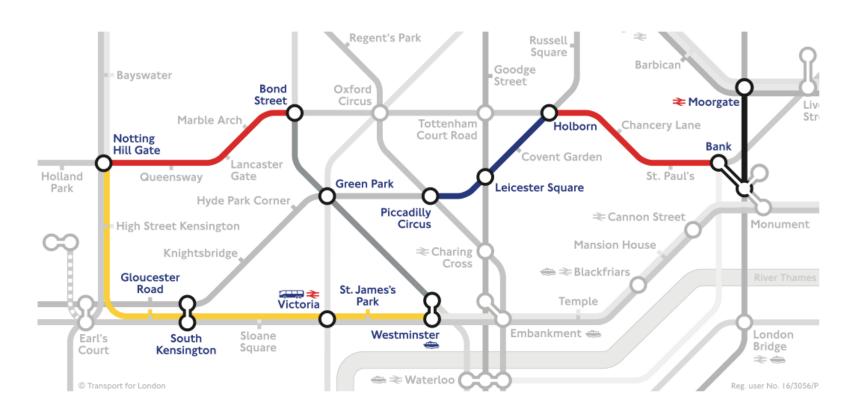
- Traversal: Perform walk on graph given source, list of edges
- Shortest Path: Given source, destination
- Inference: Given source, relation over edges; find destination

Graph Tasks

Training over 3 phases:

- Graph description phase: (source, edge, destination) tuples fed into the graph
- Query phase: Shortest path (source, ____, destination),
 Inference (source, hybrid relation, ___), Traversal (source, relation, relation ...,)
- Answer phase: Target responses provided at output

Graph Tasks: London Underground



Graph Tasks: London Underground

(TottenhamCtRd, OxfordCircus, Central)
(BakerSt, Marylebone, Circle)
(BakerSt, Marylebone, Bakerloo)
(BakerSt, OxfordCircus, Bakerloo)

(OxfordCircus, TottenhamCtRd, Central)

Input Phase

(LeicesterSq, CharingCross, Northern)
(TottenhamCtRd, LeicesterSq, Northern)
(OxfordCircus, PiccadillyCircus, Bakerloo)
(OxfordCircus, NottingHillGate, Central)
(OxfordCircus, Euston, Victoria)

Graph Tasks: London Underground Traversal Task

```
(BondSt, _, Central),
(_, _, Circle), (_, _, Circle),
(_, _, Circle), (_, _, Circle),
(_, _, Jubilee), (_, _, Jubilee),
```

```
(BondSt, NottingHillGate, Central)
(NottingHillGate, GloucesterRd, Circle)
:
(Westminster, GreenPark, Jubilee)
(GreenPark, BondSt, Jubilee)
```

Query Phase

Answer Phase

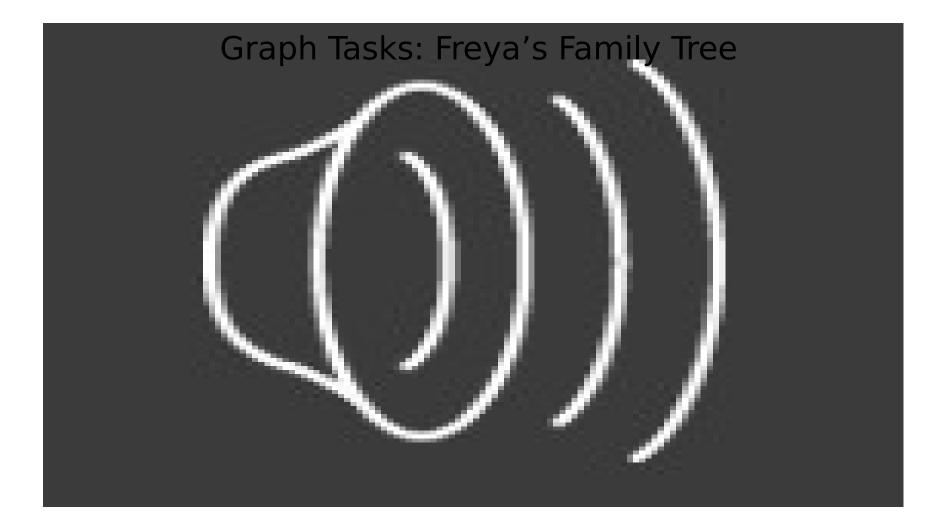
Graph Tasks: London Underground Shortest Path Task

(Moorgate, PiccadillyCircus, _)

(Moorgate, Bank, Northern)
(Bank, Holborn, Central)
(Holborn, LeicesterSq, Piccadilly)
(LeicesterSq, PiccadillyCircus, Piccadilly)

Query Phase

Answer Phase



Conclusion

- Machine Learning models require memory and multi-hop reasoning to perform AI tasks better
- Memory Networks for Text are an interesting direction but very simple
- Generic architectures with memory, such as Neural Turing Machine, limited applications shown
- Future directions should be focusing on applying generic neural models with memory to more AI Tasks.

Reading List

- Karol Kurach, Marcin Andrychowicz & Ilya Sutskever Neural Random-Access Machines, ICLR, 2016
- Emilio Parisotto & Ruslan Salakhutdinov Neural Map: Structured Memory for Deep Reinforcement Learning, ArXiv, 2017
- Pritzel et. al. **Neural Episodic Control**, ArXiv, 2017
- Oriol Vinyals, Meire Fortunato, Navdeep Jaitly Pointer Networks, ArXiv, 2017
- Jack W Rae et al., Scaling Memory-Augmented Neural Networks with Sparse Reads and Writes, ArXiv 2016
- Antoine Bordes, Y-Lan Boureau, Jason Weston, Learning End-to-End Goal-Oriented Dialog, ICLR 2017
- Junhyuk Oh, Valliappa Chockalingam, Satinder Singh, Honglak Lee, Control of Memory, Active Perception, and Action in Minecraft, ICML 2016
- Wojciech Zaremba, Ilya Sutskever, Reinforcement Learning Neural Turing Machines, ArXiv 2016