EE1200

DIGITAL CLOCK

AIM: To build an 8-hour digital clock and display the hours and minutes using an LED display.

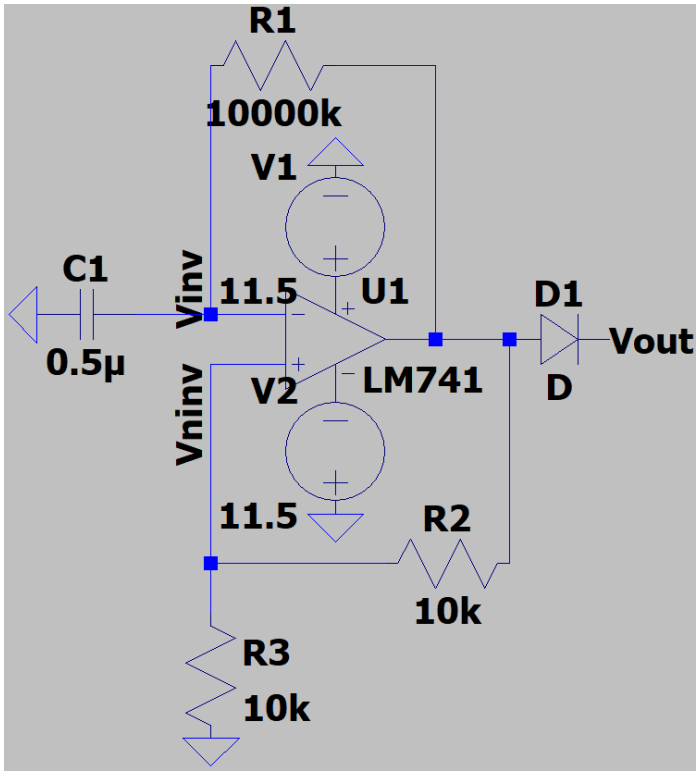
Components used:

For the square wave generator: IC 741, Resistors, Capacitor Wires, Breadboard.
For the Digital Counters: IC 7474(Flip flops), IC 7400(NAND gate), IC 7408 (AND gate), Wires, Breadboard.
For the 7- segmented display: 7- segment display, Breadboard, Wires IC 7447(7-segment display decoder).

Theoretical aspects and Design

Clock

The clock is a square wave generator rectified to remove the negative output.



The square wave generator is an astable multivibrator. The output of the op-amp is switched between positive saturation and negative saturation voltages at fixed intervals, leading to the formation of a square waveform.

Let us assume that the capacitor is uncharged (V_{inv} = 0) initially and there is some voltage at the output (V_{ninv} >0) initially. Hence , the difference between the two inputs is a nonzero value, which leads to a positive saturation voltage at the output. This leads to the charging of the capacitor, and the Vine starts increasing. Once its crosses the value of the V_{ninv}, the output goes to negative saturation voltage and the capacitor discharges. Eventually, the V_{inv} becomes less than the V_{ninv} and output again goes to the positive saturation voltage. This cycle repeats. Thus, a square wave is generated at the output. The amplitude of the square can be adjusted by adjusting the saturation voltage of the op-amp which is via controlling the input power supply.

The time period of the clock is 1s

The Digital Counter

The 60s Clock

The clock consists of D flip-flops which are made to function like T flip-flops (with T=1, so that it always complements the previous input) by connecting the complement of output(Q') to the input of the D flip-flop. The circuit is made using 6 flip flops and the number of states is 60(0-59 states). It can have a total of 64 states but we restrict it to 60 states by using a combinational circuit connected to the clear terminal of the flip-flops. The pre-set terminal is connected to the High voltage level throughout the experiment. The circuit same as a mod 60 counter

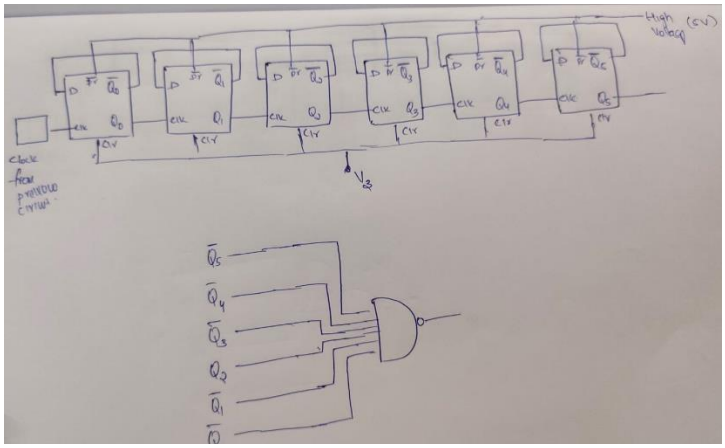
The flip-flops used here are rising edge-sensitive flip-flops and also the 1st state of the circuit when represented in binary format is 111111(all clocks are at a Low state initially and when they suddenly rise to one all the clocks simultaneously rise to a High state and go to the state corresponding to the binary format 111111).

Output	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5
State	1	1	1	1	1	1

Now it will count the states till the 60th state. For the 60th state, the corresponding binary format is 000100.

Output	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5
State	0	0	0	1	0	0

After that, it again jumps to the 1tt state. The output of the clock 60s clock (Q_5) is connected to the minute clock.



Since 6 input NAND gates are not available in lab, the combinational logic is accomplished by cascading 3 two-input AND gates and 1 two-input NAND.

The Minute Clock

Mod 10 counter

The clock input to the mod 10 counter is the output from the 60s clock. Thus, the clock counts after every minute.

The connections are similar to that of the 60s clock with a few changes. The number of flip-flops required is only 4 and it will count 10 states. Also, the combinational circuit connected to the clear terminal of the flip-flops is different which is as described below

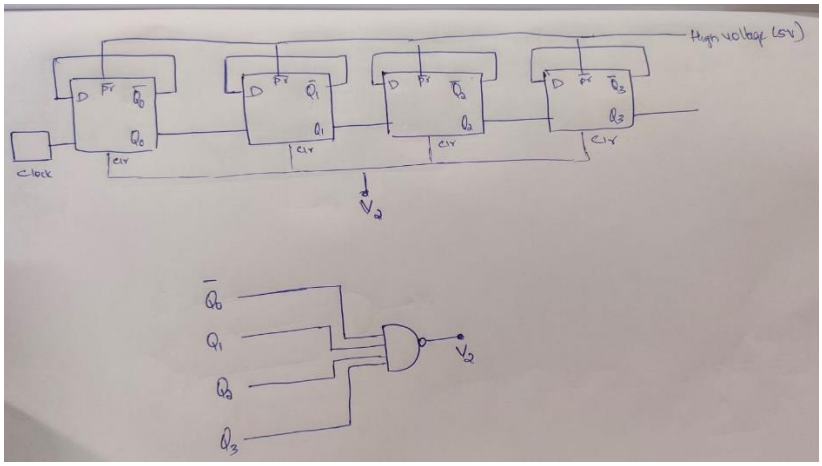
The flip-flops used here are rising edge-sensitive flip-flops and also the 1`utugcjhjbst state of the circuit when represented in binary format is 1111(all clocks are at a Low state initially and when they suddenly rise to one all the clocks simultaneously rise to a high state and go to the state corresponding to the binary format 1111).

State	Q_0	Q_1	Q_2	Q_3
Output	1	1	1	1

Now it will count the states till the 10th state. For the 10th state, the corresponding binary format is 0110.

State	Q_0	Q_1	Q_2	Q_3
Output	0	1	1	0

After that, it again jumps to the 1st state. The output of the clock minute clock (Q_5) is connected to the 10-minute clock.



Since 6 input NAND gates are not available in lab, the combinational logic is accomplished by cascading 2 two-input AND gates and 1 two-input NAND.

Mod 6 counter

The clock input to the mod 6 counter is the output from the minute clock. Thus, the clock counts after every 10 minutes.

The connections are similar to that of the 60s clock with a few changes. The number of flip-flops required is only 3 and it will count 6 states. Also, the combinational circuit connected to the clear terminal of the flip-flops is different which is as described below

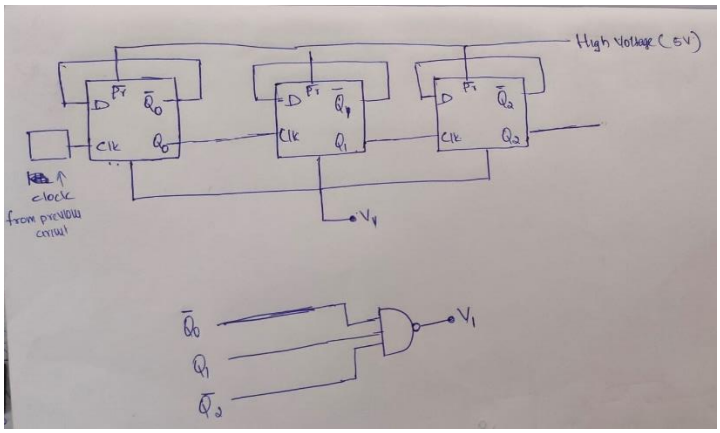
The flip-flops used here are rising edge-sensitive flip-flops and also the 1st state of the circuit when represented in binary format is 111(all clocks are at a Low state initially and when they suddenly rise to one all the clocks simultaneously rise to a high state and go to the state corresponding to the binary format 111).

State	Q_0	Q_1	Q_2
Output	1	1	1

Now it will count the states till the 6th state. For the 6th state, the corresponding binary format is 010.

State	Q_0	Q_1	Q_2
Output	0	1	0

After that, it again jumps to the 1st state**.** The output of the clock minute clock (Q_5) is connected to the hour clock.



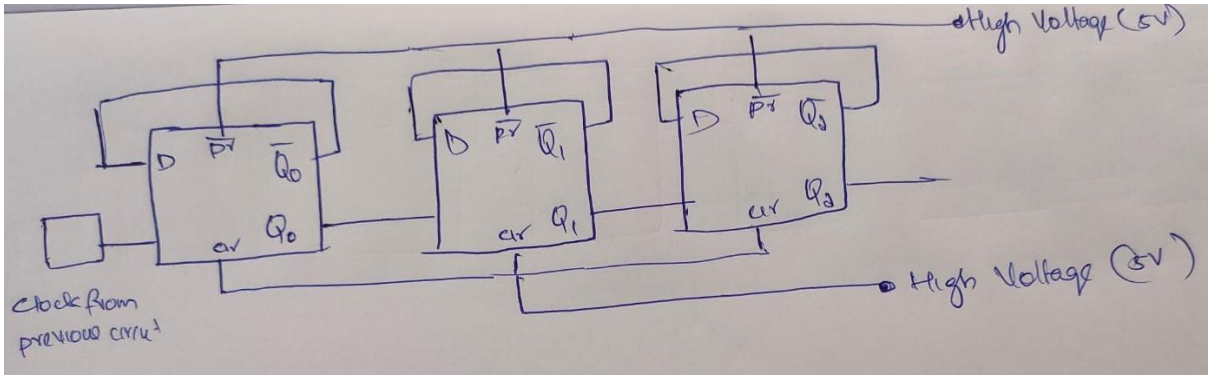
Since 6 input NAND gates are not available in lab, the combinational logic is accomplished by cascading 1 two-input AND gate and 1 two-input NAND.

The Hour clock

Mod 8 counter

The clock input to the mod 8 counter is the output from the 10-minute clock. Thus, the clock counts after every 1 hour.

The connections are similar to that of the 60s clock with a few changes. The number of flip-flops required is only 3 and it will count 8 states.



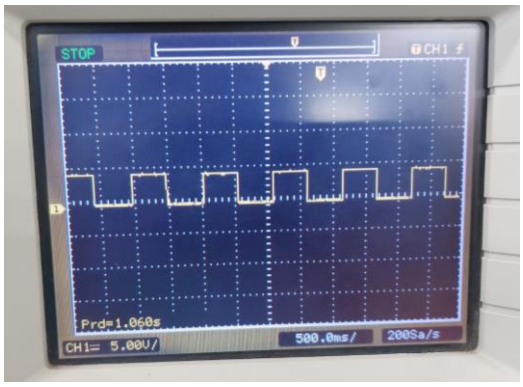
The LED Display

The outputs from the mod 10 and mod 6 counters are connected to the respective drivers of the 7 segmented display(IC 7447, works as a decoder converting the input in BCD format to the code required for lighting up the display). Then the drivers are connected to the 7 segmented display

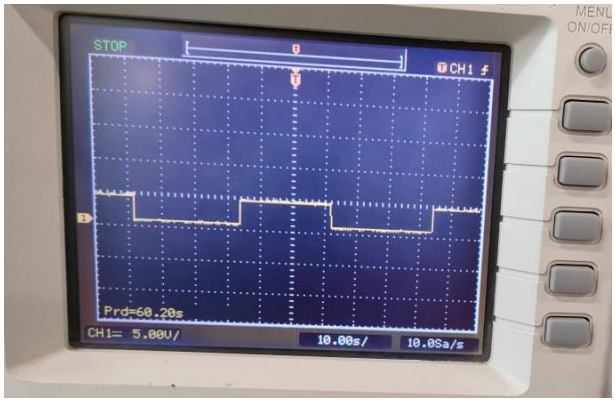
The output from the mod 8 counter is connected to the respective drivers of the 7 segmented display.

Observation and Conclusion

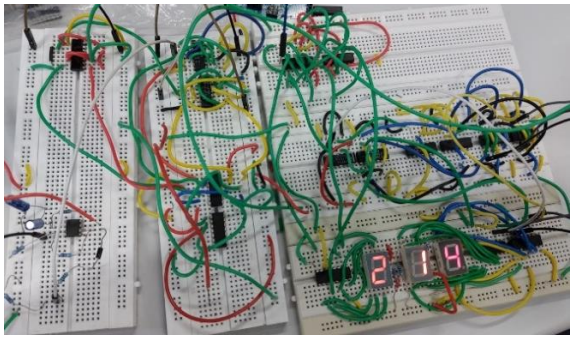
The output of the 1Hz clock is as follows

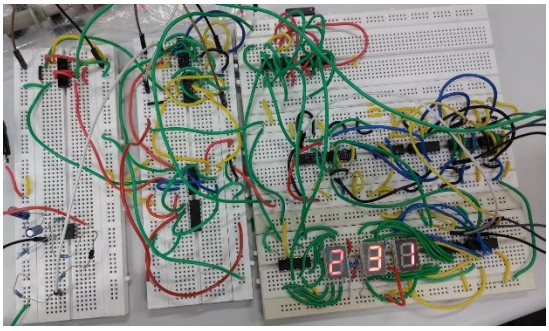


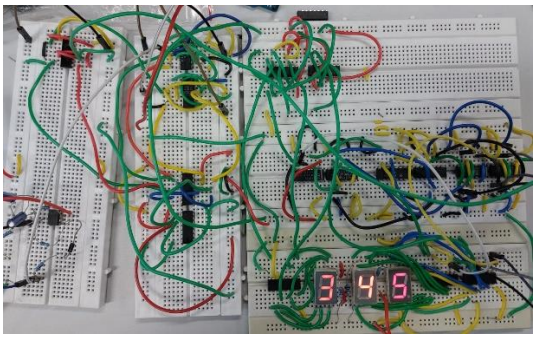
The output of the 60s clock is as follows



The output of the clock as displayed on the 7-segmented display.







Hence a clock which can display minutes and 8 hours is made and the displayed using 7 segment display