Status Register

19 June 2025 10:49

- → Tells the status of the current usart communication happening.
- → The 3 bits we need to know are TXE, TC, RXNE
- → TXE : this bit is set by the hardware, when data is transferred from TDR to transmit shift register. And so it tells a message that the data is transferred and TDR is empty and new byte can be sent.
- → TC : (Transmission Complete) It is also set by the hardware when the TXE bit is set and when the transmission of the entire frame containing the data is complete.
- → RXNE : set by the hardware when the Receive shift register transfers data to the RDR, from there to the usart data register (DR).

Baud Rate Register

19 June 2025 11:10

- → This register has 2 main blocks : DIV_Mantissa(USART_DIV) and DIV_Fraction.
- → DIV_Mantissa is the before decimal part.
- → DIV_Fraction is the after decimal part.
- → Fractional Baud Rate Generation: (Standard)
  Tx/Rx Baud = fCK(freq clk) / 8*(2-OVER8)* USARTDIV
  fcK is clk fed to USART(APB1 Or APB2).
  USARTDIV is an unsigned fixed point number that is coded on the USART_BRR register. (Refer pg 981 = rm-stm32f429xx).
- → The formula for calculating the BRR depends on the oversampling mode:
- → OVER8 = 0: Oversampling by **16,** USARTDIV**=**fCK / (16 * baud)
- → OVER8 = 1: Oversampling by **8,** USARTDIV**=**fCK / (8 * baud)
- → Here baud is desired baud rate.

Control Register

19 June 2025 11:46

- → UE is essential to enable only rs 232 or rs485 protocols. So do not enable for the uart protocol.
- → CR1 :
  set OVER8 to 1, for opting OVER8 sampling
  UE bit, enable UE bit
  M bit set 0, for 8-bit data
  Set TE and RE bits for Tx and Rx.
- → CR2 :
  set 00 for the STOP bit
- → CR3 :
  No changes all default values.