Placement Hardware Tests

3/10/2018 - **Intel** (Hardware Profile) - Basic Software, Hardware (Forgot the topics covered - nothing out of the ordinary though)

6/10/2018 - **Qualcomm** - (ML for Hardware)

- Aptitude(was tough), Coding, Hardware.
- Solid state devices, Computer Organization, Digital Logic, Setup/Hold time
- Hardware questions were simple

25/10/2018 - **Samsung Semiconductors** (Hardware Profile)

- 38 questions, 90mins, no -ve. [1*12 + 2*19 + 3*2 + 5*5] (marks * no. of questions)
- Fairly easy
- Digital Logic, Many questions of Setup/Hold, RC circuits, Opamps, Very Basic Digital IC design, Computer Organization (Pipelining and stuff), Basic C coding, Verilog

27/10/2018 - **Texas Instruments**

- All possible combinations of Software+Hardware+Signal Processing were offered
- Hardware Profile
    - Analog 20 questions - 45min (**Opamps**, poles, zeros , RC circuits, Transistors)
    - Digital 20 questions - 45min (Digital Logic(Morris Mano), Verilog)
    - Aptitude 20 questions - 30min (Medium)

28/10/2018 - **Analog Devices**

- **Digital paper -** Consisted of 8 digital logic questions and some DSP questions - 90 mins
- Pen and Paper exam
- Questions fairly simple
- Digital logic, Setup/Hold time

28/10/2018 - **ON Semiconductors**

- They were particularly looking for analog engineers for their image sensing group
- Almost all were analog questions
- Small signal analysis, Differential Opamps, (Analog Circuits, and Analog IC Design)

1/11/2018 - **Western Digital**

- These guys didn't come for a PPT. HackerRank platform MCQs
- 20 Digital, 20 Analog, 20 Programming, 10 Aptitude - 70mins
- Aptitude is compulsory, U can choose 2 out of the remaining 3 sections (I chose Digital and Programming)
- Aptitude was easy
- Programming was mostly about pointers and (--j, j++)

- They covered almost all the topics in Digital. One of the best papers in terms of coverage. Memory addressing, Digital logic, IC design, Setup/hold (obviously).Not much about computer architecture
- I have noticed few questions from previous years GATE. As it is
- Only lack of time was the problem

8/11/2018 - **Google Hardware**

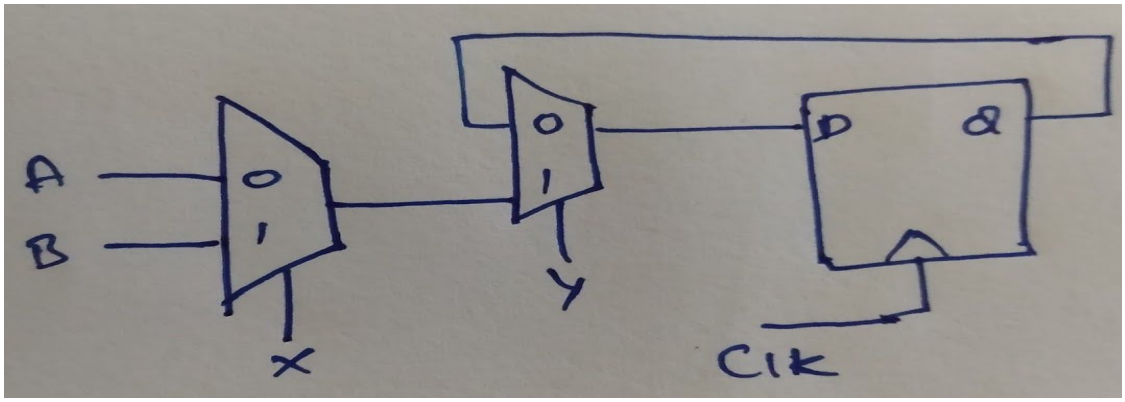
- (30 MCQs + 1 Subjective) - 1 hour
- No Aptitude. Only trick questions were asked.
- Setup/hold, Pointers, Boolean logic, Verilog (tricky questions)

29/11/18 **- Cisco Hardware**

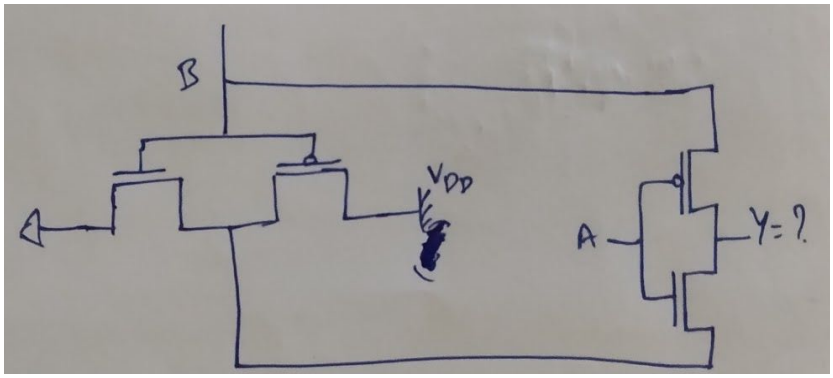
- 20 aptitude questions + 30 technical questions - 1 hour
- Technical questions covered almost every topic, not just digital. But more questions were asked on digital

30/11/18 - **Nvidia - DFT engineer**

- Pen and paper exam - 8 Questions (1 aptitude + 7 technical) - 1 hour
- In the given circuit Y is zero 95% of the time. Can you make changes to the circuit so that the power consumption goes down without changing the functionality (I have observed a trend in these kind of questions)



- What is the logic that the given circuit implements, and implement it using minimum number of 2-input NAND gates



- Some questions on **setup time** and **hold time, clock jitter**
- Two questions related to **testing** - If you have done *Digital Systems Testing and Testable Design Course* (CS dept) - these will be a cake walk. Even otherwise if you know basics you can solve them