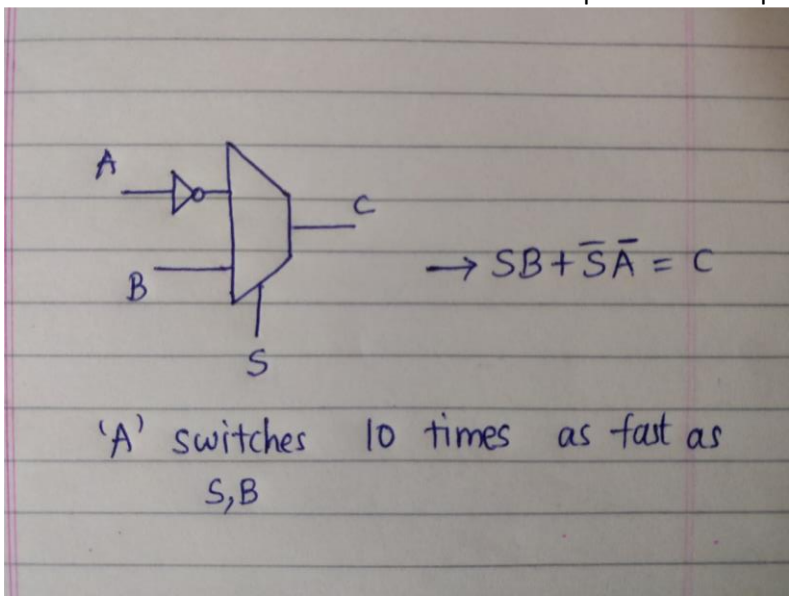
Digital Design, VLSI Design- Guide For Tests and Interviews

List of things- 1.Digital Systems-Morris Mano, 2.Computer Organization- William Stalling & http://www.geeksforgeeks.org/, 3.Digital IC Design- Lecture Notes & Weste-Harris(Ref.)

- Various binary codes conversions- BCD-Grey-Excess3-Binary-Weighted Codes.
- A is a number from 0 to 9 represented in BCD format. Number of gates(NAND, XOR etc) required to implement A*5 multiplier- Ans. Zero https://asicdigitaldesign.wordpress.com/2008/12/21/interview-question-bcd-digit-multiply-by-5/
- What are self-complementing codes?
- Advantages of 2's complement over 1's?
- Parity generating and Parity error checking circuit
- What are functionally complete gates? How do u come to conclusion that a given gate is universal gate? Is AOI gate a universal gate?
- EXOR using NAND minimum number of gates-4, EXNOR using NOR minimum number of gates-4
- 4:1 MUX using only 2:1 MUX; Number of 2:1 Mux needed to construct a 2^n :1 mux; OR, AND, NAND gates using 2:1 MUX only
- Static and Dynamic Hazards; How do we remove static hazards in a circuit using K-maps?
- OR using NAND gates
- What is a model file used in Spice simulations? Explain the flow from drawing layouts till simulations? What tools have u used?
- What is a mirror symmetry adder circuit? Draw transistor level with sizes. What other adder architectures do u know?
- What is Carry Look Ahead adder? Any idea on Bent-Kung structures?
- What is Cache Memory? How does it work? What is principle of locality of reference? https://en.wikipedia.org/wiki/Locality_of_reference
- How does pipelining works? How many clock cycles does execution of 4 instructions takes for 6-deep pipelined structure?
- What are pipeline hazards? Explain them
- Many questions on J-K Flip flop in exams.
- Design a circuit that generates a pulse output for every alternate falling edges of input? – Slightly tricky. Better draw the circuit directly without going for FSM
- What is Setup time? What happens when setup time violates? What is meta-stability? What happens over the time when the system enters meta-stability?
- What if FIFO? Where is it used? How do u calculate the depth of the FIFO-What factors does it depend upon? What is clock domain crossing?
- Divide by 3/4/5/6/7 counters? How do u generally approach such a problem? https://drive.google.com/file/d/1nAy5x4FbAyrCeDuzwgx7i0eZzN8XaQpG/view?usp=sharing
- What is a latch and a Flip-flop? What is the difference between latch and flip-flop? Construct a flip-flop from a latch?
- Draw any latch at transistor level? Construct D-flip flop from that? How will u insert asynchronous reset in this FF – Add MUX inside the slave stage appropriately

- What are the various types of encodings u know while designing an FSM? – OHE, Binary, Grey
- What is use of One hot encoding(OHE)? U need to design an ASIC- How will u decide on the type of encoding? https://drive.google.com/file/d/1dCnwzvllq9_o808TH5TR6IqnGZbkWHUF/view?usp=sharing
- What is clock-gating? Where is it used? What are the dis-advantages?
- Difference between testing and Verification?
- Why is verification important? How does writing system Verilog assertions help?
- What input vector do u give to detect a single stuck at fault in a simple circuit without branches
- Cell structures of SRAM and DRAM? How do we read and write into them? Which of them is faster and why? On what factors final voltage of the DRAM cell depend on after a read operation?
- What is charge sharing?
- FPGA and ASIC design flow?
- Calculate max. frequency of the circuit given setup-time, Clk-Q delay(Max, Min), Clock uncertainity?
- What is Clock skew? What is clock Jitter? How do they effect timing conditions?
- What is NMOS-Stack? Why do we use it?
- What are high V-t cells? How do they decrease static power leakage? What is the disadvantage of using these cells- Ans. (Higher dynamic power leakage- Think how)
- Verilog code for D-FF with asynchronous reset?
- What are blocking and Non-Blocking statements in verilog?
- In test-bench what does `timescale means?
- What does incomplete if-else statements synthesize to? – Ans. Latch
- Under what conditions a latch is synthesized for a Verilog code?
- 8085 instructions – Rotate instructions – Practice Gate questions on this will be enough
- R-2R DAC voltage calculation? https://training.ti.com/precision-dacs-r-2r
- 555 timer- frequency formula- change R1 and R2 to change clock frequency- duty cycle of the clock?
- SSD Basics- pn=ni^2; depletion width of pn junction; reverse junction capacitance of pn-junction; resistivity of a given extrinsic semiconductor?
- Question on sheet resistance? What is sheet resistance?
- What is pseudo n-mos? Advantages over standard cmos? Disadvantages?
- Given a wire which causes a delay 'RC'. U need to place buffers each with delays=P such that they divide the wire equidistantly. Find the optimum number of buffers needed.
- Draw the stick diagram of NAND and optimize?
- What does 'Z' stand for in digital logic? Module1 truth table {00-Z,10-1,01-Z,11-Z} Module2 truth table {00-Z, 10-Z, 01-Z, 11-0} construct an inverter using these two modules? – Simple. Tie the outputs together and inputs together appropriately.
- What does 'X' stand for in digital logic? Given a 2:1 mux, 's' is the select line, output y= s*d1 + s' * d2, what is the output when s= 'X'?
- There are two long rails Vdd and Gnd. A ramp signal (changing from 0 to 1) is given at the one end of this rail. How will the output waveform at the other end look like? – Hint- The two rails act like a low pass filter and there will be also some delay.

- Colpitts oscillator? https://en.wikipedia.org/wiki/Colpitts_oscillator
- What is a ring counter? Johnson counter? Modulo-4 counter?
- Ring counter with inverter? Odd number or even number? What happens if we have even number of inverters?
- What is critical path?
- There is a multiplexer given as shown in the figure. 'A' toggles very high almost 10 times as much as 'S' or 'B' does. How will u reduce the power consumption in such a circuit?



You could start a discussion by saying some obvious things like reduce Vdd for the inverter etc. The interviewer will guide u to what he actually wants. Simple hint is that we could redraw the circuit such that A switches only when S=0.
Final Ans. Is as shown