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**10CS36**

**USN**

**R. V. COLLEGE OF ENGINEERING**

**Autonomous Institution affiliated to VTU**

**III Semester B. E. Examinations Dec-11 /Jan-12(Makeup)**

Computer Science and Engineering

**DIGITAL ELECTRONICS THEORY**

***Time: 03 Hours Maximum Marks: 100***

*Instructions to candidates:*

1. Answer all questions from Part-A and Part-A questions should be answered in the first two pages of the answer book.
2. Answer Five full questions from Part-B

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| --- | --- | --- | --- |
|  |  | **PART- A** |  |
| 1 | 1.1 | The output of the gated network shown in figure below is  C:\Documents and Settings\user\Local Settings\Temporary Internet Files\Content.Word\k1.jpg   1. .. 2. ++ 3. AB+CD+EF 4. (A+B)(C+D)(E+F) | 1 |
|  | 1.2 | The logic gate which produces a 0 or low level output when one or both of the inputs are 1 is called \_\_\_\_\_\_\_\_\_ gate | 1 |
|  | 1.3 | What is the Boolean expression for the logic diagram shown below Evaluate if A=1, B=1, C=1  C:\Documents and Settings\user\Local Settings\Temporary Internet Files\Content.Word\k1 001.jpg | 1 |
|  | 1.4 | End around carry is used with \_\_\_\_\_\_\_\_\_\_ subtraction | 1 |
|  | 1.5 | Converting the BCD number 0001 0111 to binary you get \_\_\_\_\_\_\_ | 1 |
|  | 1.6 | Parallel adder are \_\_\_\_\_\_\_\_\_\_\_\_ logic circuits | 1 |
|  | 1.7 | An encoder converts \_\_\_\_\_\_\_\_\_\_\_ information into \_\_\_\_\_\_\_\_\_\_\_form | 1 |
|  | 1.8 | How many data select lines are required to select eight inputs\_\_\_\_\_ | 1 |
|  | 1.9 | \_\_\_\_\_\_\_\_\_ flip flop is considered the universal flip flop | 1 |
|  | 1.10 | JK flip flop is in “No change” condition when \_\_\_\_\_\_\_\_\_\_\_ | 1 |
|  | 1.11 | A modulus-10 counter must have \_\_\_\_\_\_\_\_ flip flops | 1 |
|  | 1.12 | A 4 bit up/down binary counter is in the DOWN mode and in the 1100 state. On the next clock pulse, to what state does the counter go | 1 |
|  | 1.13 | To serially shift a (nibble) four bits of data into a shift register there must be \_\_\_\_\_\_\_\_\_\_\_\_\_ clock pulses | 1 |
|  | 1.14 | \_\_\_\_\_\_\_\_\_\_\_ depicts state transition of a circuit pictorially | 1 |
|  | 1.15 | A condition when more than one feedback variable try to change its value is called \_\_\_\_ | 1 |
|  | 1.16 | A model in which output depends on both state variable and input is called \_\_\_\_\_\_\_\_\_\_\_ | 1 |
|  | 1.17 | The output structure of a TTL gate is often referred as \_\_\_\_\_\_\_ arrangement | 1 |
|  | 1.18 | The greater the propagation delay\_\_\_\_ is the maximum frequency | 1 |
|  | 1.19 | Fan-out is specified in terms of \_\_\_\_\_\_\_\_\_\_\_ | 1 |
|  | 1.20 | The terms low speed and high speed applied to logic circuit refers to \_\_\_\_\_\_ |  |
|  |  | **PART- B** |  |
|  |  |  |  |
| 2 | a | Simplify the following expression using Quine Mc Cluskeys method f(A,B,C,D)=Σ(1,2,8,9,10,12,13,14) | 06 |
|  | b | Simplify the Boolean equation y= + AB | 04 |
|  | c | Explain three different models for writing a module body in Verilog HDL with example for each | 06 |
|  |  |  |  |
|  |  | **OR** |  |
|  |  |  |  |
| 3 | a | What is the simplified Boolean equation for the following logic expression, expressed in min terms (Using K-map)  Y=F(A,B,C,D)=Σm(7,9,10,11,12,13,14,15) | 08 |
|  | b | Prove that, A(A′ +C)(A′B+C)(A′BC+C′)=0 | 04 |
|  | c | Realize, Y=AB+ using only NAND gate | 04 |
|  |  |  |  |
| 4 | a | Design a 32:1 multiplexer using two 16:1 multiplexers and one 2:1 multiplexer | 04 |
|  | b | Show how two IC’s 7485 can be used to compare magnitude of two 8 bit number | 04 |
|  | c | How does PLA differ from PAL | 04 |
|  | d | Sketch and explain logic circuit that can add 3 bits at a time with necessary logic diagram and truth table | 04 |
|  |  |  |  |
|  |  | **OR** |  |
|  |  |  |  |
| 5 | a | Implement the following Boolean function using an appropriate PLA. F1(A,B,C)=Σm(0,4,7) and F2=(A,B,C)=Σm(4,6) | 08 |
|  | b | Show the 8 bit subtraction of these decimal numbers in 2’s complement representation.   1. -43, -78 ii) +68, -27 | 04 |
|  | c | Design decimal to BCD encoder | 04 |
|  |  |  |  |
| 6 | a | What is the advantage offered by an edge triggered RS flip flop over a clocked or gated RS flip flop | 04 |
|  | b | Why flip flop conversion is needed? Show how D-flip flop can be converted to SR flip flop. | 04 |
|  |  |  |  |
|  | c | Analyze the following circuit  C:\Documents and Settings\user\Local Settings\Temporary Internet Files\Content.Word\k1 002.jpg | 04 |
|  | d | Show how a number 0100 is entered serially in a shift register using necessary FIF with the following details   1. Logic diagram 2. State table | 04 |
|  |  | **OR** |  |
|  |  |  |  |
| 7 | a | Design 4 bit Johnson counter with the following details   1. Logic diagram 2. State table | 04 |
|  | b | Explain the working of a JK flip flop write its truth table, state diagram and excitation table | 08 |
|  | c | Analyze the give circuit and obtain state table, state transition diagram  C:\Documents and Settings\user\Local Settings\Temporary Internet Files\Content.Word\k1 003.jpg | 04 |
|  |  |  |  |
| 8 | a | Design 3 bit binary counter with the following   1. Logic diagram or circuit 2. Truth table 3. Wave forms | 06 |
|  | b | How synchronous counter is different from asynchronous counters | 04 |
|  | c | Write Verilog HDL code for modulo 8 counter | 06 |
|  |  |  |  |
|  |  | **OR** |  |
|  |  |  |  |
| 9 | a | Discuss counter design as a synthesis problem taking an example giving necessary steps | 06 |
|  | b | Design up/down synchronous counter and explain operation with help of state table and logic diagram | 08 |
|  | c | Determine number of flip flops required to build counters   1. Mod-6 ii) Mod-11 iii) Mod-15 iv) Mod-19 | 02 |
|  |  |  |  |
| 10 | a | Design a binary ladder with digital input of 1000, giving equivalent circuit for a digital input of 1000 and also determine output voltages. | 06 |
|  |  |  |  |
|  |  |  |  |
|  | b | Reduce state transition diagram (Moore Model) of fig shown below   1. Row elimination method 2. Implication table method   C:\Documents and Settings\user\Local Settings\Temporary Internet Files\Content.Word\k1 004.jpg | 06 |
|  | c | What is the resolution of 9 bit D/A converter which uses a ladder network? What is the resolution if expressed as percent? If the full scale output voltage of this converter is +5v, what is the resolution in volts? | 4 |
|  |  | **OR** |  |
| 11 | a | Discuss simultaneous A/D conversion method with a neat diagram | 06 |
|  | b | What is state transition diagram? How does state transition diagram of Moore machine differ from Mealy machine? Give necessary block diagrams | 04 |
|  | c | For the following state transition diagram design equations for Moore model and generate state table and transition table.  **D:\scans\New Folder (2)\k1 005.jpg** | 06 |