

EHD LAB

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ROLL NO : 20171402

Video link : <https://goo.gl/n3vM4e>

Aim:

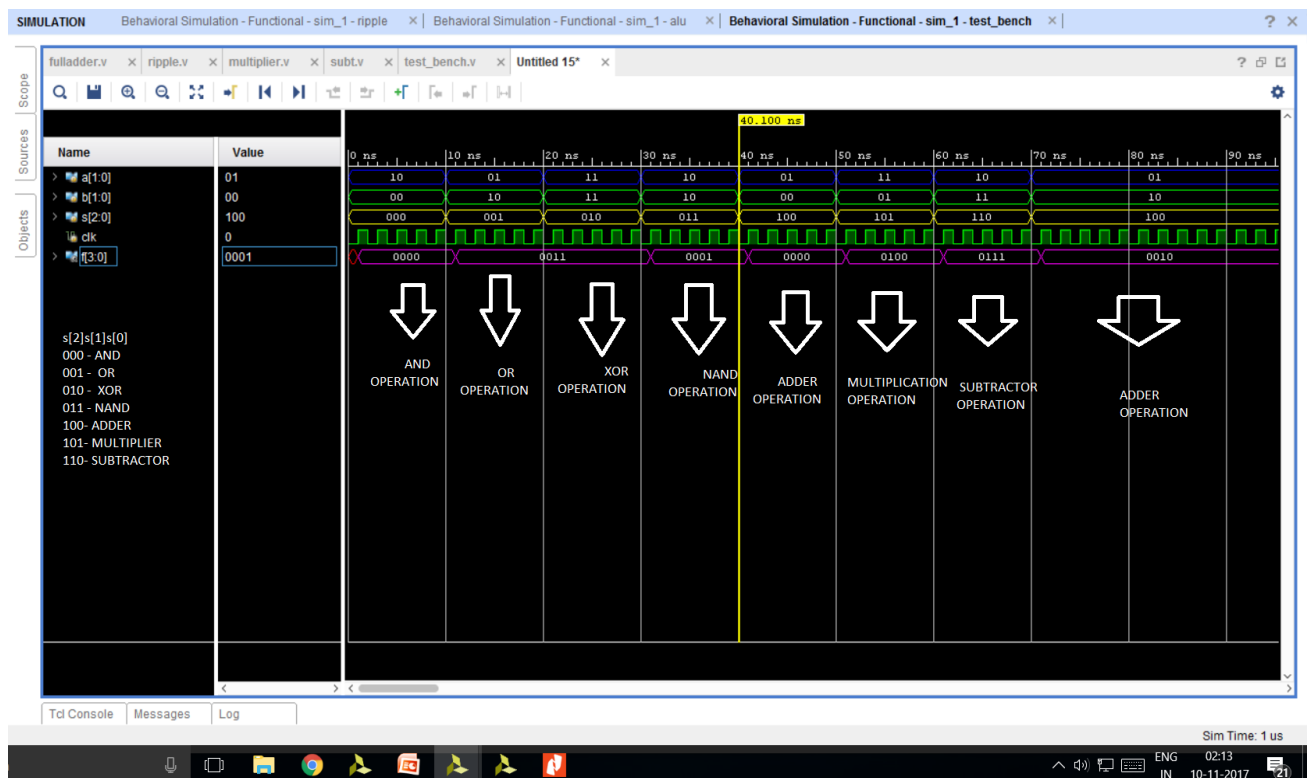
An arithmetic logic unit (ALU) is a multi-operation, combinational-logic digital function. It can perform a set of basic arithmetic operations and set of logic operations. The ALU has a number of selection lines to select a particular operation in the unit. The two data inputs from A are combined with the four inputs from B to generate an operation at the output F. The modes of operation are selected by using the select lines S[2:0].

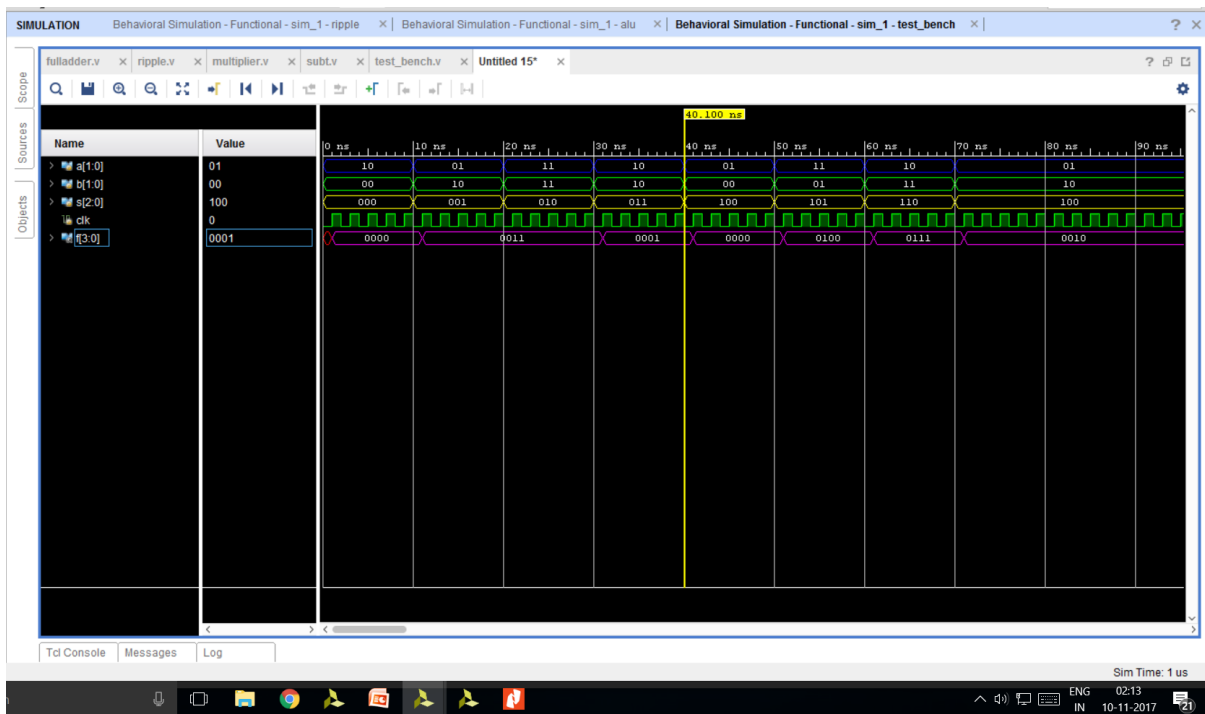
SELECT LINE (S)	OPERATION
000	AND (&)
001	XOR ()
010	OR (^)
011	NAND
100	MULTIPLY (*)
101	ADDER(+)
110	SUBTRACT (-)
111	Default

CONSTRAINTS AND WORKING CONDITIONS:

- Operations 0,1,2,3 are logical operations (000, 001, 010, 011).
- Operations 4,5,6 are arithmetic operations (100, 101, 110).
- All the logical operations are done bitwise i.e
 $a \& b \Rightarrow f$
 Where: $f[0] = a[0] \& b[0]$
 $f[1] = a[1] \& b[1]$
- We are using a 4-bit output, since 4-bits are required to represent the answer in multiplication.
 Eg. $3 \times 3 = 9$ (1001)
- In Subtraction we are doing $a - b$.
- In Subtraction the answer comes in 3 bits, as the 4th bit is not required during output and is set to 0. If the answer is negative the third bit ($f[2]$) will be 1. In this case the output will have magnitude equal to the 2's complement of the 3 bit number, and will be less than 0.
 Eg.
 $1 - 3$ will give output as 0110.,but expected output is -2.
 Since it is only a 3 bit output we will consider 110.
 Since $F[2]$ is 1, it means that the number is negative.
 Therefore magnitude = 2's complement(110) = 010 = 2, and it is negative.
 Therefore the output will be interpret as -2, which is the expected output.

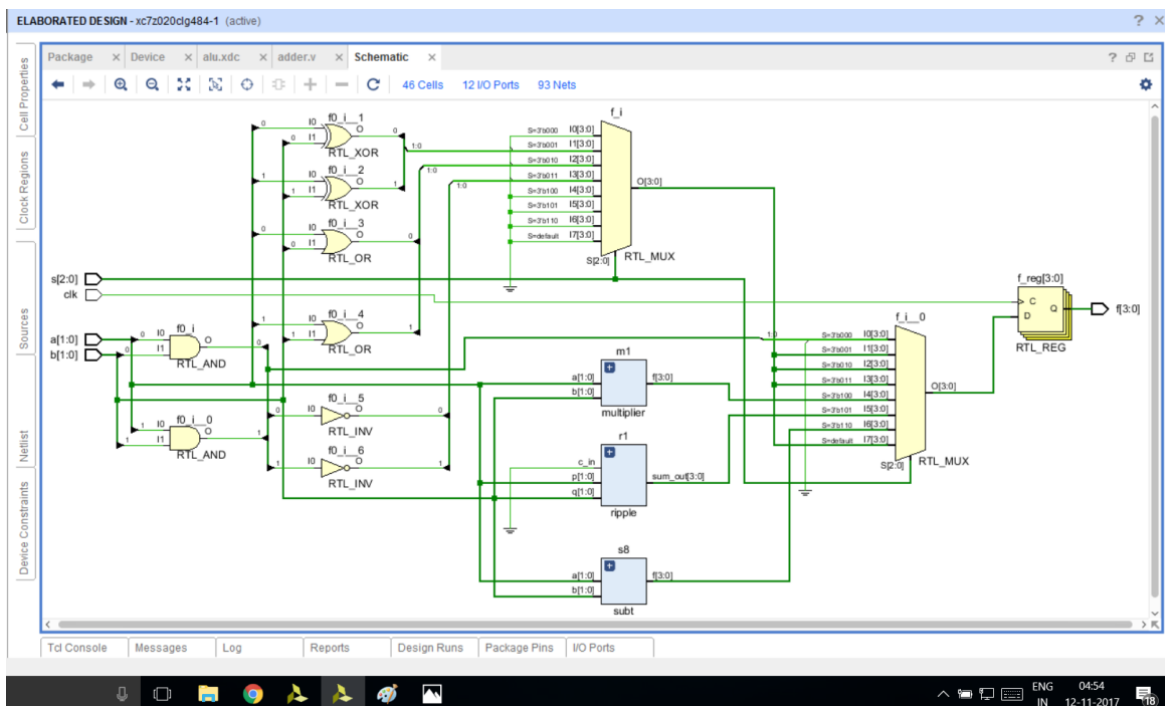
TEST BENCH OUTPUT



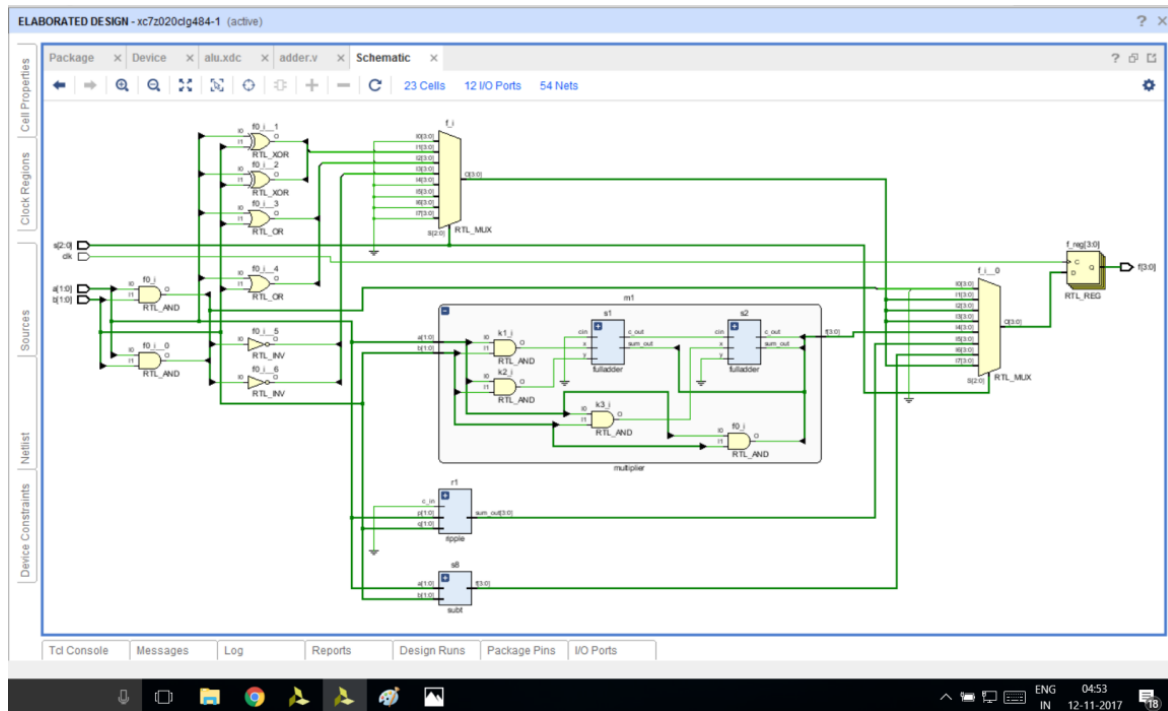


RTL ANALYSIS :(Schematic)

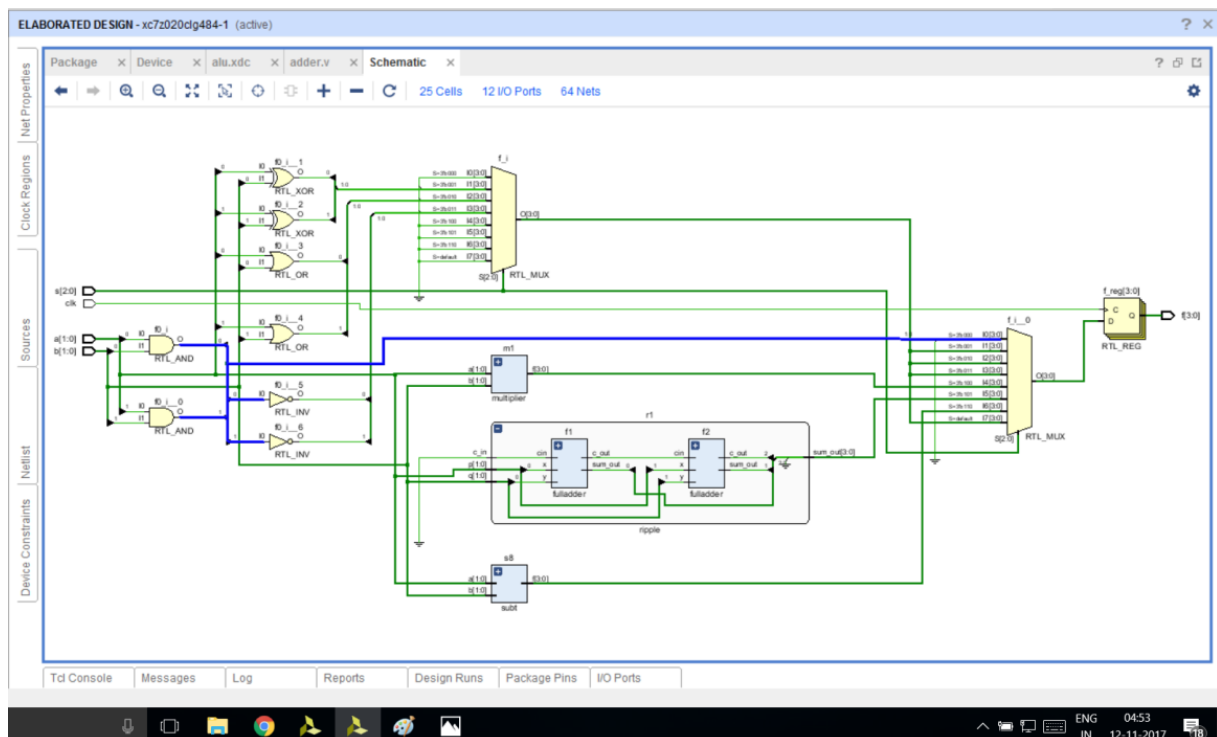
Gate level



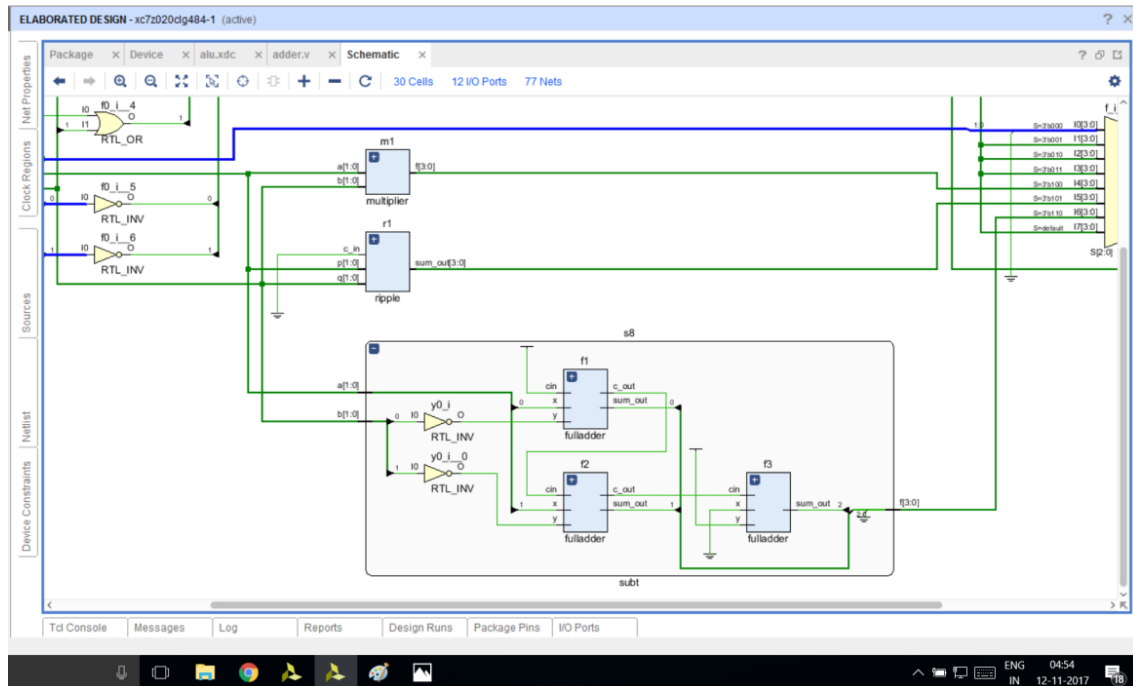
INSIDE MULTIPLIER



Inside Ripple (2 bit) adder :



Inside Subtractor :

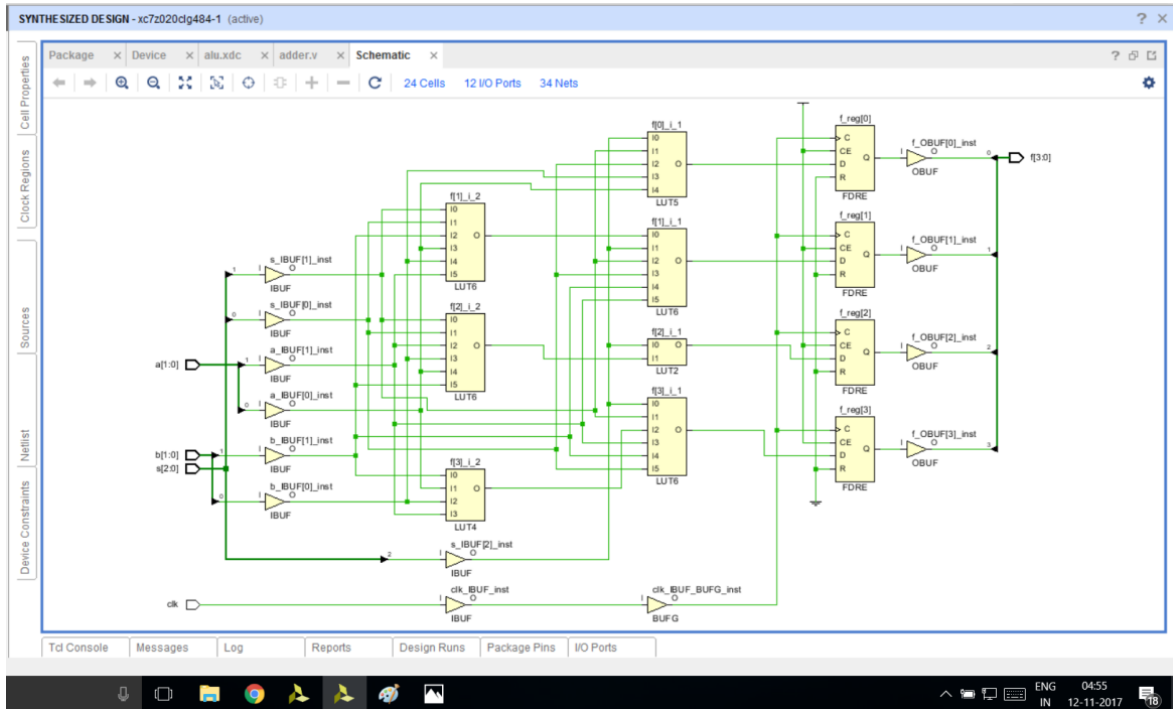


INPUTS AND OUTPUTS :

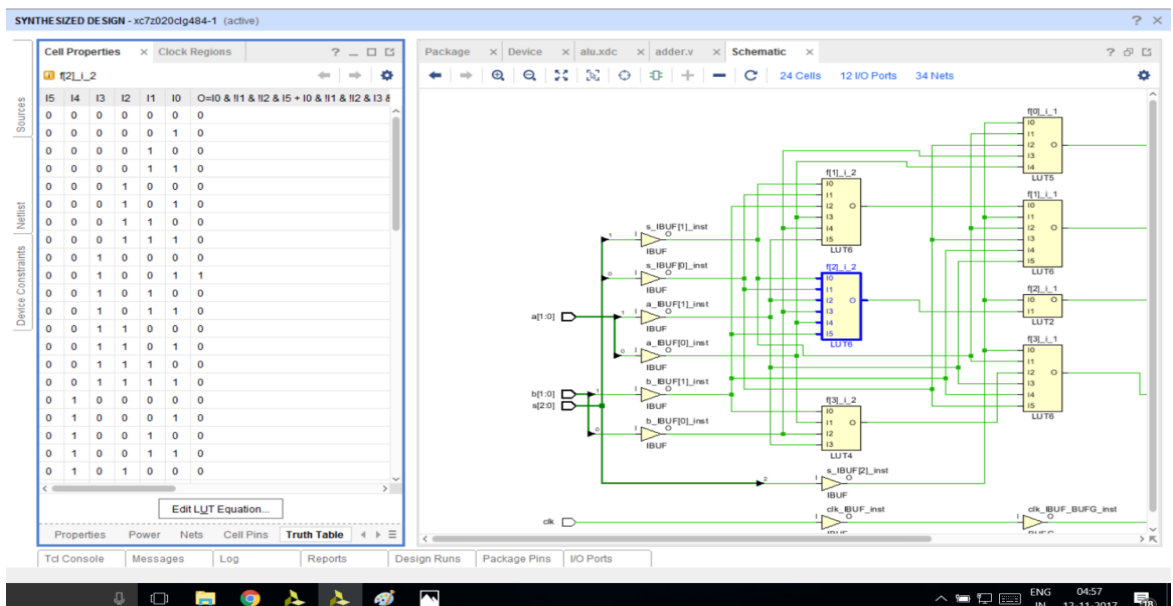
Name	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type	Off-Chip Termination	IN
All ports (12)															
a (2)	IN					✓	35	LVC MOS33*	3.300				NONE	NONE	✓
a[1]	IN				G22	✓	35	LVC MOS33*	3.300				NONE	NONE	✓
a[0]	IN				F22	✓	35	LVC MOS33*	3.300				NONE	NONE	✓
b (2)	IN					✓	35	LVC MOS33*	3.300				NONE	NONE	✓
b[1]	IN				F21	✓	35	LVC MOS33*	3.300				NONE	NONE	✓
b[0]	IN				H22	✓	35	LVC MOS33*	3.300				NONE	NONE	✓
f (4)	OUT					✓	33	LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT_50	✓
f[3]	OUT				U21	✓	33	LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT_50	✓
f[2]	OUT				U22	✓	33	LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT_50	✓
f[1]	OUT				T21	✓	33	LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT_50	✓
f[0]	OUT				T22	✓	33	LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT_50	✓
s (3)	IN					✓	35	LVC MOS33*	3.300				NONE	NONE	✓
s[2]	IN				H17	✓	35	LVC MOS33*	3.300				NONE	NONE	✓
s[1]	IN				H18	✓	35	LVC MOS33*	3.300				NONE	NONE	✓
s[0]	IN				H19	✓	35	LVC MOS33*	3.300				NONE	NONE	✓
Scalar ports (1)															
clk	IN				M15	✓	34	LVC MOS33*	3.300				NONE	NONE	✓

SYNTHESIS SCHEMATIC :

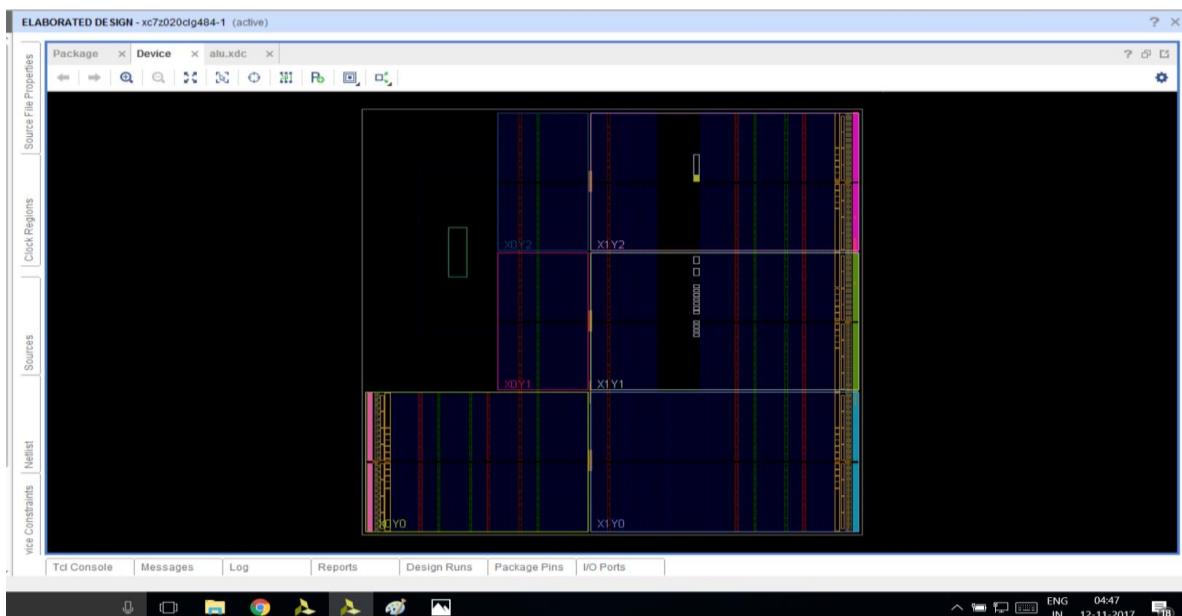
LUT IMPLEMENTATION



LUT 6 (Ex) :



IMPLEMENTATION (PLACE AND ROUTE)



Synthesis and Implementation Report

Start RTL Hierarchical Component Statistics

Hierarchical RTL Component report

Module alu

Detailed RTL Component Info :

+---XORs :

2 Input 1 Bit XORs := 2

+---Registers :

4 Bit Registers := 1

Module adder

Detailed RTL Component Info :

+---XORs :

2 Input 1 Bit XORs := 1

Finished RTL Hierarchical Component Statistics

Start Part Resource Summary

Part Resources:

DSPs: 220 (col length:60)

BRAMs: 280 (col length: RAMB18 60 RAMB36 30)

Finished Part Resource Summary

Start Cross Boundary and Area Optimization

Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:17 ; elapsed = 00:00:24 .
Memory (MB): peak = 687.617 ; gain = 440.613

Report RTL Partitions:

+--+-----+-----+-----+

	RTL Partition		Replication		Instances	
--	---------------	--	-------------	--	-----------	--

+--+-----+-----+-----+

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Start Applying XDC Timing Constraints

Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:29 ; elapsed = 00:00:36 . Memory
(MB): peak = 687.617 ; gain = 440.613

Start Timing Optimization

Finished Timing Optimization : Time (s): cpu = 00:00:29 ; elapsed = 00:00:36 . Memory (MB): peak =
687.617 ; gain = 440.613

Report RTL Partitions:

+--+-----+-----+-----+

	RTL Partition		Replication		Instances	
--	---------------	--	-------------	--	-----------	--

+--+-----+-----+-----+

+--+-----+-----+-----+

Start Technology Mapping

Finished Technology Mapping : Time (s): cpu = 00:00:29 ; elapsed = 00:00:36 . Memory (MB): peak
= 687.617 ; gain = 440.613

Report RTL Partitions:

+--+-----+-----+-----+

| |RTL Partition |Replication |Instances |

+--+-----+-----+-----+

+--+-----+-----+-----+

Start IO Insertion

Start Flattening Before IO Insertion

Finished Flattening Before IO Insertion

Start Final Netlist Cleanup

Finished Final Netlist Cleanup

Finished IO Insertion : Time (s): cpu = 00:00:30 ; elapsed = 00:00:37 . Memory (MB): peak = 687.617
; gain = 440.613

Report Check Netlist:

+-----+-----+-----+-----+-----+-----+						
	Item	Errors	Warnings	Status	Description	
+-----+-----+-----+-----+-----+-----+						
1	multi_driven_nets	0	0	Passed	Multi driven nets	
+-----+-----+-----+-----+-----+-----+						

Start Renaming Generated Instances

Finished Renaming Generated Instances : Time (s): cpu = 00:00:30 ; elapsed = 00:00:37 . Memory (MB): peak = 687.617 ; gain = 440.613

Report RTL Partitions:

+-+-----+-----+-----+				
	RTL Partition	Replication	Instances	
+-+-----+-----+-----+				
+-+-----+-----+-----+				

Start Rebuilding User Hierarchy

Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:30 ; elapsed = 00:00:37 . Memory (MB): peak = 687.617 ; gain = 440.613

Start Renaming Generated Ports

Finished Renaming Generated Ports : Time (s): cpu = 00:00:30 ; elapsed = 00:00:37 . Memory (MB): peak = 687.617 ; gain = 440.613

Start Handling Custom Attributes

Finished Handling Custom Attributes : Time (s): cpu = 00:00:30 ; elapsed = 00:00:37 . Memory (MB): peak = 687.617 ; gain = 440.613

Start Renaming Generated Nets

Finished Renaming Generated Nets : Time (s): cpu = 00:00:30 ; elapsed = 00:00:37 . Memory (MB): peak = 687.617 ; gain = 440.613

Start Writing Synthesis Report

Report BlackBoxes:

	BlackBox name	Instances
1	BUFG	1
2	LUT2	1
3	LUT4	1
4	LUT5	1
5	LUT6	4
6	FDRE	4
7	IBUF	8
8	OBUF	4

Report Cell Usage:

	Cell	Count
1	BUFG	1
2	LUT2	1
3	LUT4	1
4	LUT5	1
5	LUT6	4
6	FDRE	4
7	IBUF	8
8	OBUF	4

+-----+-----+-----+

Report Instance Areas:

+-----+-----+-----+-----+

	Instance		Module		Cells	
--	----------	--	--------	--	-------	--

+-----+-----+-----+-----+

1	top			24	
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+-----+-----+-----+-----+

Finished Writing Synthesis Report : Time (s): cpu = 00:00:30 ; elapsed = 00:00:37 . Memory (MB):
peak = 687.617 ; gain = 440.613

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1. Slice Logic

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Site Type	Used	Fixed	Available	Util%
Slice LUTs*	7	0	53200	0.01
LUT as Logic	7	0	53200	0.01
LUT as Memory	0	0	17400	0.00
Slice Registers	4	0	106400	<0.01
Register as Flip Flop	4	0	106400	<0.01
Register as Latch	0	0	106400	0.00
F7 Muxes	0	0	26600	0.00
F8 Muxes	0	0	13300	0.00

* Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt_design after synthesis, if not already completed, for a more realistic count.

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
0	Yes	-	Set
0	Yes	-	Reset
0	Yes	Set	-
4	Yes	Reset	-

2. Memory

-----+-----+-----+-----+-----+				
Site Type	Used	Fixed	Available	Util%
+-----+-----+-----+-----+-----+				
Block RAM Tile	0	0	140	0.00
RAMB36/FIFO*	0	0	140	0.00
RAMB18	0	0	280	0.00
+-----+-----+-----+-----+-----+				

* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1

3. DSP

-----+-----+-----+-----+-----+				
Site Type	Used	Fixed	Available	Util%
DSPs	0	0	220	0.00
+-----+-----+-----+-----+-----+				

4. IO and GT Specific

+-----+-----+-----+-----+-----+				
Site Type	Used	Fixed	Available	Util%
+-----+-----+-----+-----+-----+				
Bonded IOB	12	0	200	6.00
Bonded IPADs	0	0	2	0.00
Bonded IOPADs	0	0	130	0.00
PHY_CONTROL	0	0	4	0.00
PHASER_REF	0	0	4	0.00
OUT_FIFO	0	0	16	0.00
IN_FIFO	0	0	16	0.00

IDELAYCTRL	0	0	4	0.00	
IBUFDS	0	0	192	0.00	
PHASER_OUT/PHASER_OUT_PHY	0	0	16	0.00	
PHASER_IN/PHASER_IN_PHY	0	0	16	0.00	
IDELAYE2/IDELAYE2_FINEDELAY	0	0	200	0.00	
ILOGIC	0	0	200	0.00	
OLOGIC	0	0	200	0.00	

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5. Clocking

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Site Type	Used	Fixed	Available	Util%	
-----------	------	-------	-----------	-------	--

+-----+-----+-----+-----+

BUFGCTRL	1	0	32	3.13	
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BUFIO	0	0	16	0.00	
-------	---	---	----	------	--

MMCME2_ADV	0	0	4	0.00	
------------	---	---	---	------	--

PLLE2_ADV	0	0	4	0.00	
-----------	---	---	---	------	--

BUFMRCE	0	0	8	0.00	
---------	---	---	---	------	--

BUFHCE	0	0	72	0.00	
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BUFR	0	0	16	0.00	
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+-----+-----+-----+-----+

6. Specific Feature

+-----+-----+-----+-----+

Site Type	Used	Fixed	Available	Util%	
-----------	------	-------	-----------	-------	--

+-----+-----+-----+-----+

BSCANE2	0	0	4	0.00	
---------	---	---	---	------	--

CAPTUREE2	0	0	1	0.00	
-----------	---	---	---	------	--

DNA_PORT	0	0	1	0.00
EFUSE_USR	0	0	1	0.00
FRAME_ECCE2	0	0	1	0.00
ICAPE2	0	0	2	0.00
STARTUPE2	0	0	1	0.00
XADC	0	0	1	0.00

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7. Primitives

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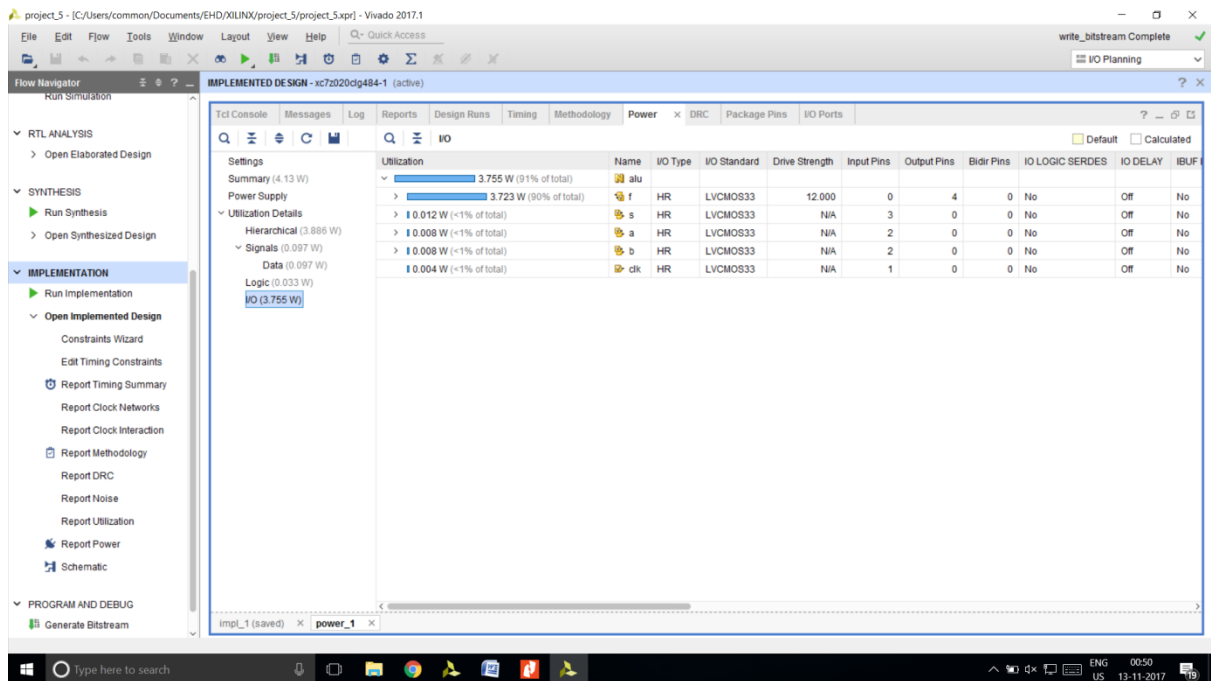
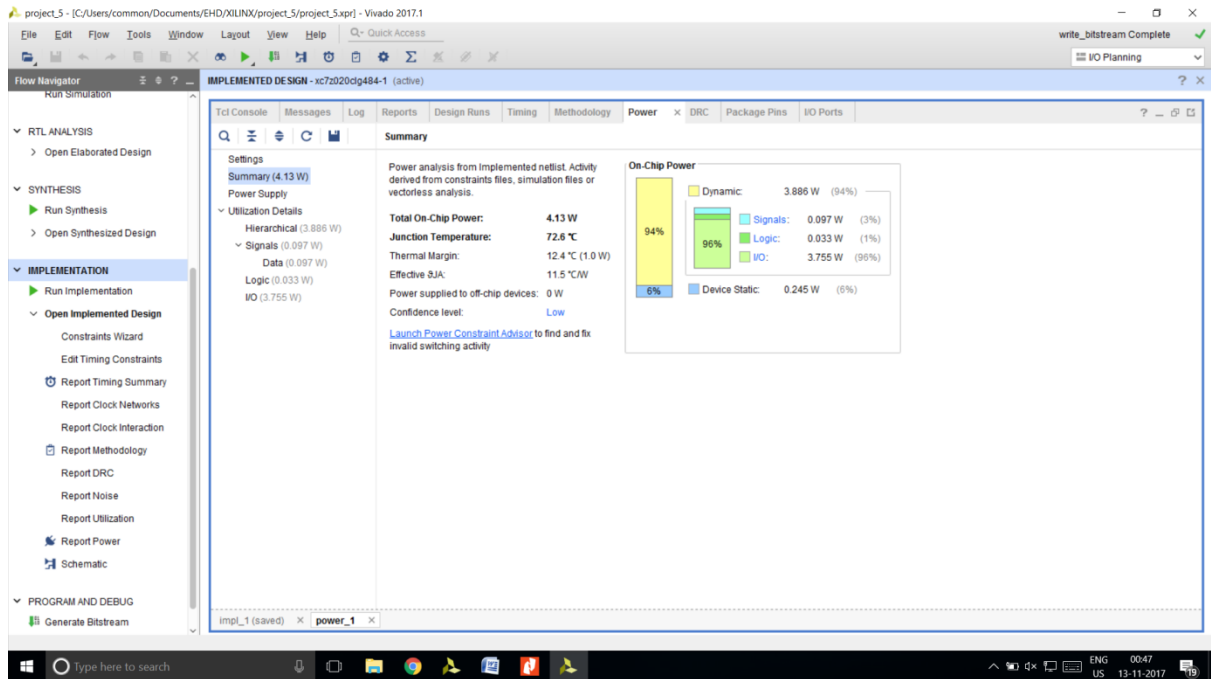
Ref Name	Used	Functional Category
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IBUF	8	IO
OBUF	4	IO
LUT6	4	LUT
FDRE	4	Flop & Latch
LUT5	1	LUT
LUT4	1	LUT
LUT2	1	LUT
BUFG	1	Clock

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POWER REPORT



The screenshot shows the Vivado 2017.1 interface with the Power report selected. The left sidebar shows the project hierarchy with 'IMPLEMENTATION' expanded. The main window displays the 'I/O' tab of the Power report.

I/O

Utilization

Utilization	Name	IO Type	IO Standard	Drive Strength	Input Pins	Output Pins	BiDir Pins	IO LOGIC SERDES	IO DELAY	IBUF
3.755 W (91% of total)	alu									
3.723 W (90% of total)	f	HR	LVCMOS33	12.000	0	4	0	No	Off	No
0.012 W (<1% of total)	s	HR	LVCMOS33	N/A	3	0	0	No	Off	No
0.008 W (<1% of total)	a	HR	LVCMOS33	N/A	2	0	0	No	Off	No
0.008 W (<1% of total)	b	HR	LVCMOS33	N/A	2	0	0	No	Off	No
0.004 W (<1% of total)	clk	HR	LVCMOS33	N/A	1	0	0	No	Off	No

Reference for Video :

clk	S[2]	S[1]	S[0]	B[1]	B[0]	acc[4:0]	
	F[3]	F[2]	F[1]	F[0]			
AND →	0	0	0	1			→ A = 11 B = 01 S = 000
XOR →	0	0	1	0			→ A = 11 B = 00 S = 000
OR →	0	1	1	1			→ A = 11 B = 01 S = 100
NAND →	0	1	0	0			→ A = 11 B = 00 S = 010
MULTIPLIER →	1	0	0	1			→ A = 11 B = 01 S = 011
ADDER →	1	0	1	0			→ A = 11 B = 10 S = 100
SUBTRACTOR →	1	1	0	0			→ A = 11 B = 10 S = 100

Test Bench :

→ A = 11 B = 10 S = 110	o/p = 0001
→ A = 10 B = 01 S = 101	o/p = 0011
→ A = 11 B = 10 S = 100	o/p = 0110
→ A = 11 B = 01 S = 011	o/p = 0010
→ A = 10 B = 00 S = 010	o/p = 0010
→ A = 11 B = 10 S = 100	o/p = 1001