A primer on USB Type-C[®] and USB Power Delivery Applications and Requirements



Nate Enos

Analog Field Applications North America Sales & Marketing Texas Instruments

Brian Gosselin

Analog Field Applications North America Sales & Marketing Texas Instruments



The USB Type-C[®] connector ecosystem continues to evolve with the needs of modern platforms and devices.

At a glance

This paper serves as an introduction to USB Type-C and USB Power Delivery (PD), examining various applications and their data and power requirements.



1

Data and power roles

Typical data and power roles vary within end equipment with regards to the USB Type-C specification.





USB 3.1 Gen 1 (SuperSpeed) and Gen 2 (SuperSpeed+)

Applications that require transfer rates faster than 480 Mbps will need to leverage either USB 3.1 Gen 1 (SuperSpeed) or Gen 2 (SuperSpeed+).





USB Type-C pinout and reversibility

The USB Type-C connector includes several new pins compared to USB Type-A and Type-B connectors.

The USB Type-C connector ecosystem addresses the evolving needs of modern platforms and devices, and the trend toward smaller, thinner and lighter form-factor designs. Additionally, the modification of USB PD for the Type-C connector helps address the needs of power-hungry applications.

Introduction

You may have heard about USB Type-C's reversible cable. When you think about the requirements for a particular

system, however, you may be unsure about what's necessary and what's just "nice to have." In this paper, we will introduce the most basic USB Type-C applications and work our way up to full-featured USB Type-C and USB PD applications. But first, let's review the evolution of USB data, starting with USB 1.0 through USB 3.1 Gen 2.

Table 1 lists the maximum transfer rate of each USB data transfer-related specification. The standard started with USB 1.x supporting 1.5 Mbps (low speed) and 12 Mbps (full speed), but evolved to support 10 Gbps (SuperSpeed+) with USB 3.1 Gen 2.

Specification	Data rate name	Maximum transfer rate	
USB 1.0 and USB 1.1	Low Speed	1.5 Mbps	
	Full Speed	12 Mbps	
USB 2.0	High Speed	480 Mbps	
USB 3.0	SuperSpeed	5 Gbps	
USB 3.1	SuperSpeed+	10 Gbps	

Table 1. USB specification and maximum voltage, current and power.

Table 2 shows the evolution of USB power, starting with USB 2.0 through USB PD 3.0. The overall trend has been to increase the maximum power to address the growing needs of platforms and devices. Without USB PD, you can support up to 5 V at 3 A (15 W) with just USB Type-C alone. However, with USB PD, you can support up to 20 V at 5 A (100 W) within the USB Type-C ecosystem.

Specification	Maximum voltage	Maximum current	Maximum power
USB 2.0	5 V	500 mA	2.5 W
USB 3.0 and USB 3.1	5 V	900 mA	4.5 W
USB BC 1.2	5 V	1.5 A	7.5 W
USB Type-C 1.2	5 V	3 A	15 W
USB PD 3.0	20 V	5 A	100 W

Table 2. USB specification and maximum voltage, current and power.

Data and power roles

There are three types of data flow in a USB connection:

- The downstream-facing port (DFP) sends data downstream; it is typically the port on a host or a hub to which devices connect. A DFP will source VBUS power (the power path between host and device) and can also source VCONN power (to power electronically marked cables). An example of an application that may include a DFP is a docking station.
- The upstream-facing port (UFP), which connects to a
 host or DFP of a hub, receives the data on a device or
 hub. These ports usually sink VBUS. An example of an
 application that may include a UFP is a display monitor.
- The dual-role data (DRD) port can operate as either a DFP (host) or a UFP (device). The port's power role at attach determines its initial role. A source port takes on the data role of a DFP, while the sink port takes on the data role of a UFP. Using USB PD data-role swap can dynamically change the port's data role, however. Example applications that may include DRD ports include laptops, tablets and smartphones.

There are three types of power flow in a USB connection:

 A sink is a port that when attached consumes power from VBUS and a sink is most often a device. A sink could include USB peripherals such as a USB-powered light or fan.

- A source is a port that when attached provides power over VBUS. Common sources are a host or hub DFP. An example of a source application is a USB Type-C wall charger.
- A dual-role power (DRP) port can operate as either a sink or source, and may alternate between these two states. When a DRP initially operates as a source, the port takes the data role of a DFP. Alternatively, when a DRP initially operates as a sink, the port takes the data role of a UFP. Using USB PD power-role swap can dynamically change the DRP's power role, however. For example, a laptop may include a DRP port that can receive power to charge the laptop's battery, but it can also deliver power to charge external accessories. Additionally, there are two special subclasses of a DRP:
 - A sourcing device is capable of supplying power, but not capable of acting as a DFP. One example of this subclass is a USB Type-C and USB PD-compatible monitor that receives data from a laptop's DFP, but also charges the laptop.
 - A sinking host is capable of consuming power, but not capable of acting as a UFP. An example could be a hub's DFP that sends data to an accessory while being powered by that accessory.

Figure 1 below highlights common end equipment and what their typical data and power roles are with regards to the USB Type-C specification.

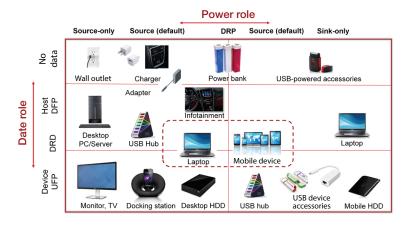


Figure 1. USB Type-C version 1.2 example applications.

USB Type-C UFP sink: USB 2.0 without USB PD

The most simple and likely most common application is a UFP USB 2.0 without USB PD (≤15 W). Common applications include anything USB-powered today that does not require SuperSpeed data, such as a mouse, keyboard, wearables or various other small electronics. Figure 2 highlights the necessary functional blocks for a USB Type-C UFP USB 2.0 system.

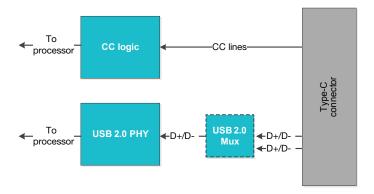


Figure 2. Type-C UFP USB 2.0 without PD block diagram.

At this point, we will assume that you understand the USB Type-C connector pinout and how reversibility works; if not, see Figure 13. Note that the USB 2.0 physical layer (PHY) is no different than previous USB 2.0 designs with a Type-A or Type-B connector. It serves as the physical layer between the data from USB's D+ and D- lines to the USB 2.0 Transceiver Macrocell Interface (UTMI) plus low-pin interface

(ULPI) for the application processor to manage.

USB 2.0 PHYs are often integrated into processors or microcontrollers; however, there are discrete PHYs available to integrate USB functionality into your design. The configuration channel (CC) logic block introduced in the USB Type-C specification determines cable detection, cable orientation and current-carrying capability.

- Cable detection occurs when one of the two CC lines pulls down (see Figure 3). A DFP will have both of its CC pins pull up with resistor Rp, and a UFP will have both of its CC pins pull down with resistor Rd [1]. Once a DFP detects that one of its CC lines is pulled down, the DFP will know that a connection has been made.
- Cable orientation is based on which CC line pulls down (if CC1 pulls down, the cable is not flipped; but if CC2 pulls down, the cable is flipped). For nonactive cables, the remaining CC line remains open; for active cables, the remaining CC line will pull down with Ra.
- The values of Rp determine the current-carrying capability. USB Type-C can natively support either 1.5 A or 3 A. A DFP can advertise its current-carrying capability with a specific value pullup resistor. A UFP has a fixedvalue pulldown resistor (Rd) such that when connected, it forms a voltage divider with Rp. By sensing the voltage at the center tap of the voltage divider, a UFP can detect the DFP's advertised current.

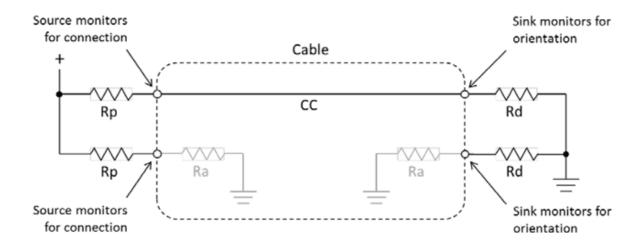


Figure 3. CC logic pullup and pulldown termination. (Source: USB Type-C specification v1.2, Figures 4 and 5 pullup/pulldown CC model)

The last block is a USB 2.0 multiplexer (often called a high-speed mux). The dotted outline in Figure 2 represents an optional block not required by the USB Type-C specification. To understand the purpose of the mux, it's important to understand how flipping the cable affects data flow. In a USB Type-C receptacle, there are two pairs of D+/D- lines for a single channel of USB 2.0 data. In one orientation, data flows down one of the pairs. In the flipped orientation, data flows down the other pair. The USB Type-C specification allows shorting the pairs together, D+ to D+ and D- to D-, to create a stub. Although it's not required, some designers elect to include a USB 2.0 mux in their system to improve signal integrity.

Texas Instruments (TI) offers a variety of <u>devices</u> for UFP applications with USB 2.0 data and no USB PD. These devices from TI offer a compact solution for CC logic that can determine cable detection, orientation and current-carrying capability.

USB Type-C DFP: USB 2.0 without USB PD

Another simple and common application is a DFP USB 2.0 without USB PD, as shown in Figure 4. One example is a 5-V AC/DC adapter.

Figure 4 represents the blocks necessary for a USB Type-C DFP USB 2.0 without USB PD. Note the similarities to Figure 2 with a few extra blocks added, while the CC logic block is still the same. In the case of a DFP, the device presents Rp and monitors for a pulldown caused by Rd. Once Rp detects a pulldown, the DFP knows that there is a device connected and provides 5 V. Providing 5 V only on the VBUS line after detecting a device (cold-plugging), versus always providing 5 V is a new feature introduced in USB Type-C.

The USB 2.0 ULPI PHY is the same as in the previous section. For applications that do not transfer data, such as a 5-V wall adapter, you can omit the USB 2.0 ULPI PHY from the design. Because USB Type-C implements cold-plugging, Figure 4 adds a 5-V VBUS field-effect transistor (FET). As a result, the design requires a switch for the 5-V rail.

Additionally, the USB Type-C specification requires that all sources monitor current and protect themselves if a sink tries to draw in excess of what it can supply [1]. This is

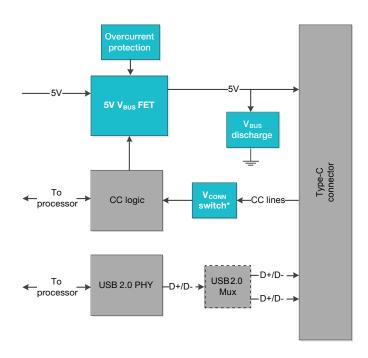


Figure 4. USB Type-C DFP USB 2.0 without USB PD block diagram.

where the overcurrent protection block comes into play.

These two blocks can be integrated into the point-of-load power converter, or integrated into the USB Type-C device.

Figure 4 also includes the VBUS discharge block. When no device is attached, VBUS should sit at 0 V. The USB Type-C specification requires a source to discharge VBUS within 650 ms of a detached sink [1]. VBUS discharge is often integrated into a USB Type-C device, but can also be integrated with a bleeder resistor.

VCONN can power passive electronically marked or active cables (cables that support USB PD communication and provide a method for determining cable characteristics) by switching 5 V onto the unused CC line (see the appendix). Figure 3 shows that one CC line in the USB Type-C cable connects Rp to Rd, while the other is left floating (a passive cable) or pulled down to ground with Ra (a passive electronically marked or active cable).

VCONN is required for all applications that support USB 3.1 speeds or power delivery higher than 3 A [1]. The VCONN switch is also required if you want to support active cables, such as longer-distance cables that require signal conditioning with an integrated redriver or retimer.

TI's portfolio of USB Type-C source controllers are a good fit for DFP USB 2.0 data without USB PD applications. These devices include CC logic, a 5-V VBUS FET, overcurrent protection, VBUS discharge and a VCONN switch. To learn more about these devices, see the <u>USB Type-C portal</u> on Tl.com.

USB Type-C DRP/DRD USB 2.0 without USB PD

The last USB 2.0 non-USB PD application available is the DRP/DRD. For non-USB PD applications, DRD and DRP are identical. A common example is a slower-speed laptop port that can send power in either direction – to charge or be charged, and act as either a host or a device. Another common application for this system type is tablets and smartphones. **Figure 5** is an updated block diagram.

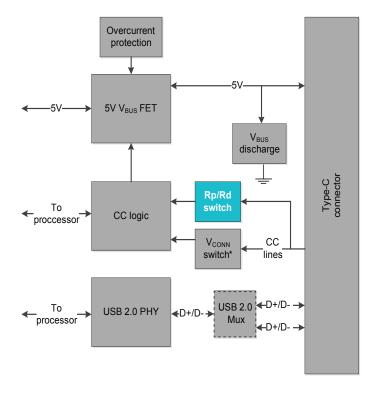


Figure 5. USB Type-C DRP/DRD USB 2.0 without USB PD block diagram. Note that the VCONN switch is not always required.

The only noticeable change from Figure 4 is adding the Rp/Rd switch. A DRP/DRD can present itself as either a UFP or DFP. As a result, this design must have a method to pull the CC lines up with Rp or pull the lines down with Rd (default

on a dead battery in order to charge), as shown in Figure 6. Notice how the switch can toggle between pulling the CC line up (in this case, with a current source to create a specific voltage across Rd), or pulling the CC line down to GND.

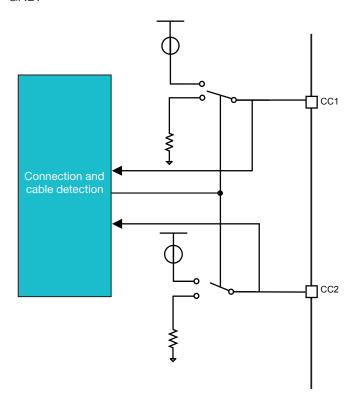


Figure 6. Rp/Rd switch schematic.

TI has a variety of <u>devices</u> that address DRP/DRD USB 2.0 without USB PD applications. These devices integrate the CC logic, Rp/Rd switch and – depending on the device – the VCONN switch.

USB Type-C DRP/DRD: USB 2.0 with USB PD

Applications with increasing complexity require USB PD. As mentioned in the introduction, systems with USB PD can support power levels of up to 20 V and 5 A (100 W). This is possible by first increasing the voltage on VBUS while holding the maximum current at 3 A. After reaching the maximum voltage of 20 V, you can increase the current up to 5 A, as shown in **Figure 7.**

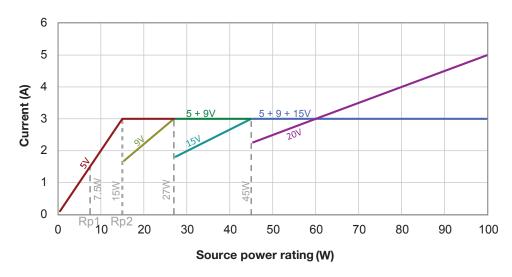


Figure 7. USB PD profiles (power rails and maximum current). (Source: Figure 10-2 in USB PD specification v3.0)

Figure 7 shows that:

- The discrete voltage levels required are 5 V, 9 V, 15 V and 20 V (modified in USB PD specification v3.0).
- The current can vary continuously, depending on the required power level (up to 3 A).
- At any given power level, a source is required to support all previous voltages and power levels.

For example, a 60-W source must be able to supply 20 V at 3 A, 15 V at 3 A, 9 V at 3 A and 5 V at 3 A. This is an update in version 3.0 of the USB PD specification, in order to ensure that higher power supplies could support lower-powered devices. An example is a charger for both your laptop and phone.

Figure 8 highlights four new blocks that come into play for USB PD applications. The VBUS FET introduced earlier can now handle 5 V to 20 V (at discrete levels, depending on the desired power level), and potentially up to 5 A (again, only when providing 20 V). Figure 8 also shows the addition of a gate-driver block for the higher-power FET. Some devices integrate a high-power FET as well as a gate driver to drive an even higher-power external FET (TI's USB PD controllers, for example), while other devices integrate just the gate driver, or integrate neither.

Up to this point, we have not discussed electrostatic discharge protection in the block diagrams because it is not any different from non-USB Type-C systems (outside of

the higher channel count). The exception is with VBUS-to-short protection. The USB Type-C connector has a higher pin density than legacy USB connectors. As a result, it is easier to accidentally short VBUS to adjacent pins (see the appendix). Since VBUS can be as high as 20 V, it is possible to have a short between the 20 V and a 5-V line (such as sideband use [SBU], CC and so on). To protect against this

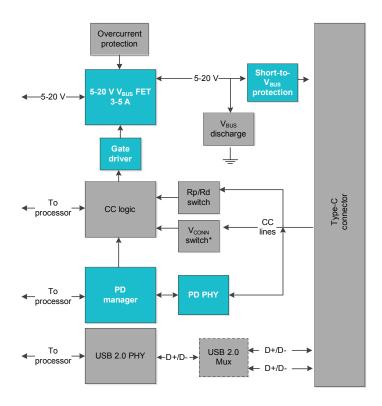


Figure 8. USB Type-C DRP/DRD USB 2.0 with USB PD block diagram. Note that the VCONN switch is not always required.

potentially catastrophic event, TI introduced a <u>family of USB</u>

<u>Type-C protection integrated circuits</u>.

Two other new blocks are the USB PD PHY and USB PD manager. Together, these blocks send packets of data across the CC lines, enabling communication between the DFP and UFP. This communication enables the source to advertise what power levels it can support, and the sink can then request a supported power level. Once a power level is set, the voltage and current levels are adjusted.

It is important to distinguish the difference in roles between the USB PD manager and the USB PD PHY; several USB Type-C devices may include one but not the other. For example, a general-purpose microcontroller can act as a USB PD manager, but does not have the USB PD PHY. The USB PD PHY's responsibility is to drive the CC lines, but it is not intelligent by itself.

The USB PD manager is the brains, containing a complex state machine to support USB PD negotiation and to control the PHY. (The USB PD manager also performs Alternate Mode negotiation.) The USB PD manager does this by telling the PHY which packets to send, such as advertising the power level, requesting the power level and acknowledging the channel power level. For a more detailed explanation, see reference [2].

The main takeaway is that if USB PD is required, you need a USB PD PHY and a USB PD manager. You can implement a USB PD PHY and USB PD manager by using an integrated solution with the USB PD manager and USB PD PHY solution in the same device, or implementing a USB PD manager on a microcontroller and using a separate PHY with a USB Type-C port controller.

For DFP applications implementing USB PD, see the <u>USB</u>

Type-C portal on Tl.com.

USB 3.1 Gen 1 (SuperSpeed) and Gen 2 (SuperSpeed+)

Applications that require transfer rates faster than 480 Mbps will need to leverage either USB 3.1 Gen 1 (SuperSpeed) or Gen 2 (SuperSpeed+). As stated in the introduction, SuperSpeed supports data-transfer rates up to 5 Gbps, while SuperSpeed+ supports up to 10 Gbps. To enable these higher transfer rates in a USB Type-C application, you

need to include a USB 3.1 PHY interface for the PCI Express (PCIe) (PIPE) PHY (Serial Advanced Technology Attachment and USB architectures) and a bidirectional differential switch that supports USB 3.1, as shown in **Figure 9**.

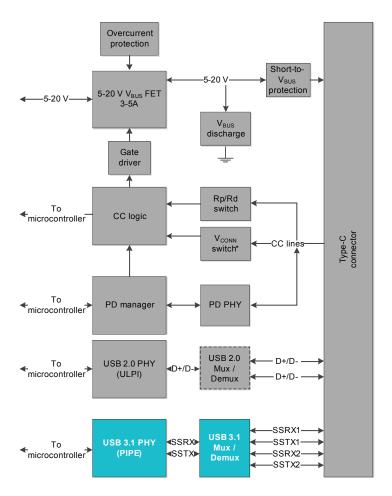


Figure 9. USB Type-C USB 3.1 block diagram. Note that the VCONN switch is not always required.

The USB 3.1 PIPE-compliant PHY provides a bridge between the media access control, the open systems interconnection model layer and the physical medium. For example, TI offers a variety of PIPE-compliant USB 3.1 PHY transceivers that support up to 5-Gbps data rates.

The bidirectional differential switch operates in mux and demultiplexer (demux) operation. Unlike USB 2.0 data, the mux/demux is not optional and is required for all applications, except USB Type-C plugs that connect directly to a host (versus a female receptacle).

One example is a USB 3.1 flash drive with a USB Type-C

plug that is physically incorporated into the device. In this type of application, the USB 3.1 data bus is fixed by design, as shown in **Figure 10**. Thus, there are only two possible connected states that exist when viewed by a USB Type-C host.

Figure 10 shows a host, which is required to have the USB 3.1 mux/demux route the USB 3.1 signal pairs. USB Type-C cables are wired such that the CC wires are position-aligned with the USB 3.1 signal pairs. As a result, the host can configure the switch based on which CC pins (CC1/CC2) terminate at the receptacle.

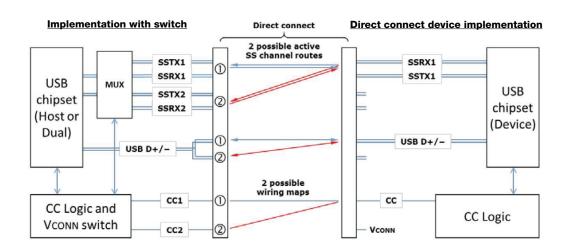


Figure 10. USB 3.1 data bus connection for a USB Type-C plug directly connected to USB Type-C host. (Source: Figure 4-4 in USB Type-C specification v1.2)

All USB 3.1 applications incorporating a USB Type-C receptacle must include the USB 3.1 switch, because when you have a USB Type-C cable connecting two USB Type-C receptacles, the cable orientation and twist are not fixed. As a result, four possible connected states exist when viewed by either the USB Type-C host or device, as illustrated in **Figure 11**.

It does not matter whether the application is for a DFP or UFP. If it incorporates a USB Type-C receptacle, the USB 3.1 switch is required to route the transceiver (TX) and receiver (RX) signal pairs. TI has a variety of <u>active and passive muxes</u> to meet the USB 3.1 switching needs of USB Type-C.

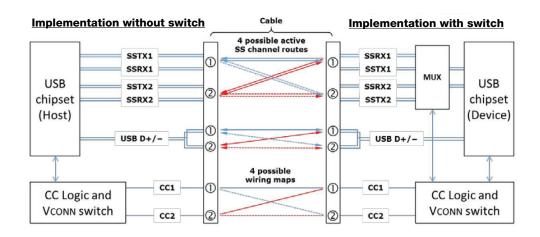


Figure 11. USB 3.1 data bus connection for Type-C receptacle connected to Type-C receptacle. (Source: Figure 4-3 in the USB Type-C Specification v1.2)

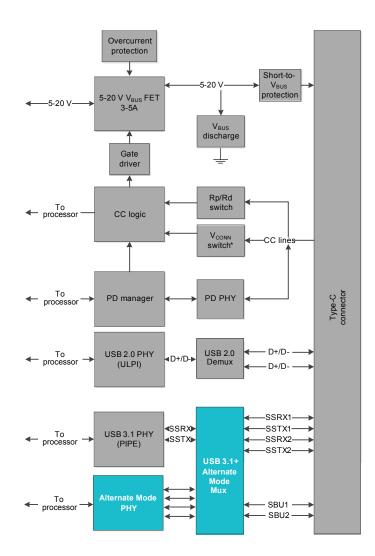


Figure 12. Type-C Alternate Mode block diagram. *VCONN switch is not always required as will be discussed.

As with any high-speed interface, some USB 3.1 applications may require signal conditioning to maintain signal integrity. To address this need, TI has a variety of USB Type-C active muxes that incorporate both USB mux/demux needs, as well as receiver equalization and transmitter de-emphasis, in order to maintain signal integrity on both the TX and RX data paths for Gen1 and Gen 2 data rates.

For USB 3.1 applications with USB PD, TI offers a complete solution including the USB PD manager and PHY, a 20-V and 3-A FET, CC logic, and a SuperSpeed mux. See the USB Type-C portal for more details.

Alternate Mode

An important benefit of USB Type-C is its ability to eliminate the need for nearly every cable in consumer devices (High-Definition Multimedia Interface [HDMI], DisplayPort/
Thunderbolt, power barrels, USB Type-A/B). To do this, USB
Type-C needed additional functionality beyond USB 3.0,
which led the USB Implementers Forum to define Alternate
Mode. Alternate Mode enables the repurposing of USB
Type-C pins (TX/RX pairs and SBU) for a different function
[1]. Up to this point, video has been the primary focus for
Alternate Mode with DisplayPort and Thunderbolt being the
main two Alternate Modes for implementing video across a
USB Type-C cable.

It is possible to transfer 4K video over USB Type-C cables, but not without Alternate Mode. Note that the USB Implementers Forum requires that they both approve and certify any Alternate Mode. **Figure 12** highlights two new blocks required to support Alternate Mode.

The first new block is the Alternate Mode PHY. For example,

with DisplayPort, you need a DisplayPort source (from the graphics processing unit). The second is the Alternate Mode mux. A USB Type-C USB 3.0 system requires a SuperSpeed mux in order to support different cable orientations. Alternate Mode needs the ability to support switching in the Alternate Mode PHY while still supporting different cable orientations.

Alternate Mode and USB 3.0 multiplexing is typically integrated into a single active or passive USB Type-C Alternate Mode mux. Two other important blocks required for Alternate Mode are the USB PD PHY and USB PD manager. It is possible to support USB PD and Alternate Mode simultaneously (imagine a monitor that takes in HDMI video but also charges a laptop when connected).

Even if USB PD power levels are not required, you must include a USB PD PHY and USB PD manager to support Alternate Mode because it is negotiated the same way as USB PD – a vendor-defined message over the CC line. Without a USB PD PHY and USB PD manager, the system could not advertise and settle on an Alternate Mode.

One final note on Alternate Mode is how to handle an incompatible connection. Imagine that the user connects their USB Type-C laptop into a USB Type-C monitor. This laptop has two USB Type-C ports: one port supports USB PD with DisplayPort as an Alternate Mode at USB 3.1 speeds, while the second port supports only USB 2.0 over USB Type-C. In this case, it is likely that the monitor requires Alternate Mode to function; for example, DisplayPort for video. If the user connects the monitor to the USB 2.0 Type-C port, the monitor will not work.

If Alternate Mode negotiation fails, there are two options:

• Support USB functionality without Alternate Mode

Provide a USB billboard message over the D+/D- lines
to communicate information that identifies the device.
 Once a monitor sees that the USB 2.0 USB Type-C port
cannot support DisplayPort, it will provide a billboard to
communicate to the operating system (OS) that it requires
DisplayPort to function. At this time, the OS could notify
the user to use the other full-featured USB Type-C port on
the laptop to support DisplayPort [1].

A full-featured system that supports Alternate Mode, USB PD and USB 3.1 can be quite powerful, but also complex. TI has solutions specifically addressing this need. For example, TI USB PD controllers integrate the USB PD manager and PHY, the high-voltage power path and CC logic, and can control an external SuperSpeed/Alternate Mode mux.

USB Type-C pinout and reversibility

The USB Type-C connector includes several new pins compared to USB Type-A and Type-B connectors. These pins enable USB Type-C features such as higher power, Alternate Mode and reversibility. **Figure 13** illustrates the pinout.

From left to right, Figure 13 shows:

- GND: the return path for the signal.
- TX/RX: SuperSpeed twisted pairs for USB 3.1 data (5 to 10 Gbps).
- VBUS: the main system bus (5 V to 20 V).
- CC1/CC2: CC lines used for cable detection, orientation and current advertisement. With USB PD, the CC lines can also communicate higher power levels and Alternate Mode. Note that one of the CC lines may become VCONN.



Figure 13. Type-C receptacle pinout.

- SBU1/SBU2: these are low-speed lines used only for Alternate Mode and accessory mode. For example, with DisplayPort, AUX+/AUX- transmit over the SBU lines. For audio adapter accessory mode, these lines are used for the microphone input and analog GND.
- D+/D-: a high-speed twisted pair for USB 2.0 data (up to 480 Mbps).

A new aspect of the USB Type-C connector is that the pins are almost symmetrical (both vertically and horizontally). This is why the connector can be reversible. Unfortunately, it's

not possible to passively realize reversibility, so additional electronics are required. Figure 14 shows how a USB Type-C receptacle (top) and a USB Type-C plug (bottom) are essentially flipped relative to each other.

A new aspect of the USB Type-C connector is that the pins are almost symmetrical (both vertically and horizontally). This is why the connector can be reversible. Unfortunately, it's not possible to passively realize reversibility, so additional electronics are required. Figure 14 shows how a USB Type-C receptacle (top) and a USB Type-C plug (bottom) are essentially flipped relative to each other.



Figure 14. Type-C pinout - receptacle (top), plug (bottom).

- The GND and VBUS lines are still in the same position.
- The D+/D- pair is in the same orientation; however, the plug contains only one D+/D- twisted pair. The USB Type-C specification allows shorting of the D+/D- lines together (D+ to D+ and D- to D-) on the receptacle side. Regardless of cable orientation, the PHY will always see the cable's D+/D- pair.
- The CC1 and CC2 lines are flipped and can determine the cable orientation. The orientation determines which CC line is connected and which one is left open.
- The TX/RX pairs are also flipped. Resolving this was a bit more complicated. Unlike the D+/D- lines, you cannot simply short the common lines together, because that will

create a stub. At USB 2.0 speeds, a stub is acceptable, but at USB 3.1 speeds, a stub degrades signal integrity too much. To avoid this, there are two options:

- Use two PHYs and cable-orientation detection to know which PHY to use.
- Have a single PHY and a SuperSpeed mux that switches the correct SuperSpeed lines to the PHY (given the known orientation). This is typically the more economical solution.
- The SBU lines are also flipped; however, this is typically handled within the Alternate Mode PHY (remember that these are slow-speed lines).

Conclusion

Although USB Type-C can appear to be very complicated at first, we believe that the initial learning curve is worth all of the advantages. We hope that we have given you an understanding of how to include USB Type-C in your next design, regardless of the application, and that you will consider many of the solutions TI has to offer for all of the various USB Type-C applications.

References

- 1. "USB Type-C® Cable and Connector Specification Revision 2.0." USB Implementers Forum, Inc.: Beaverton, Oregon, October 2020.
- 2. "<u>USB Power Delivery.</u>" USB Implementers Forum, Inc.: Beaverton, Oregon, December 2020.

Important Notice: The products and services of Texas Instruments Incorporated and its subsidiaries described herein are sold subject to TI's standard terms and conditions of sale. Customers are advised to obtain the most current and complete information about TI products and services before placing orders. TI assumes no liability for applications assistance, customer's applications or product designs, software performance, or infringement of patents. The publication of information regarding any other company's products or services does not constitute TI's approval, warranty or endorsement thereof.

All trademarks are the property of their respective owners.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (https://www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2021, Texas Instruments Incorporated