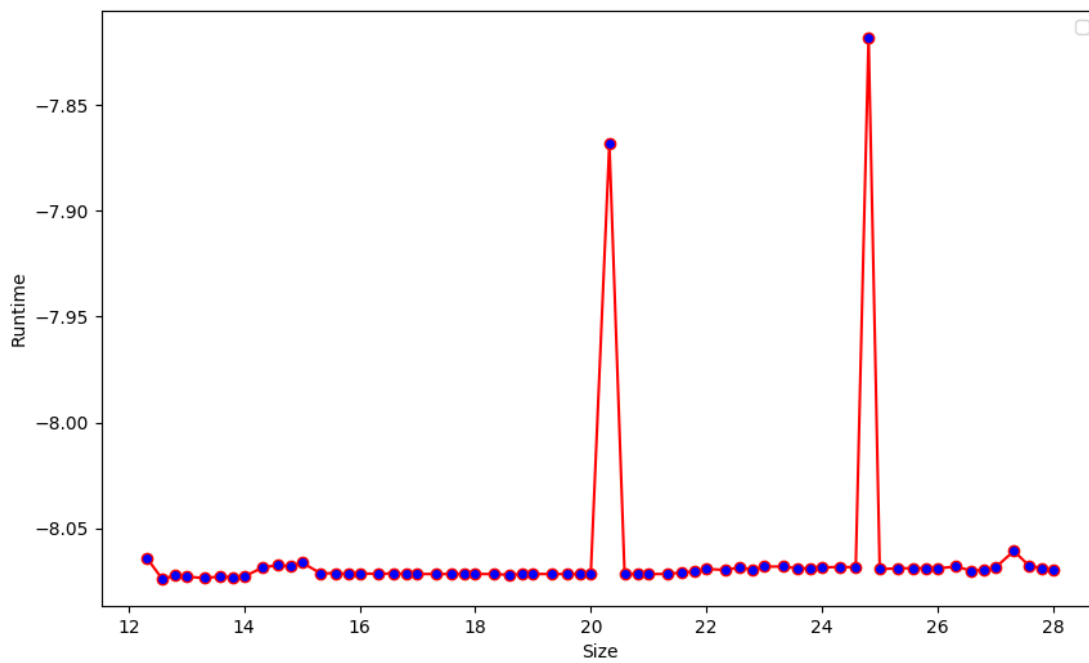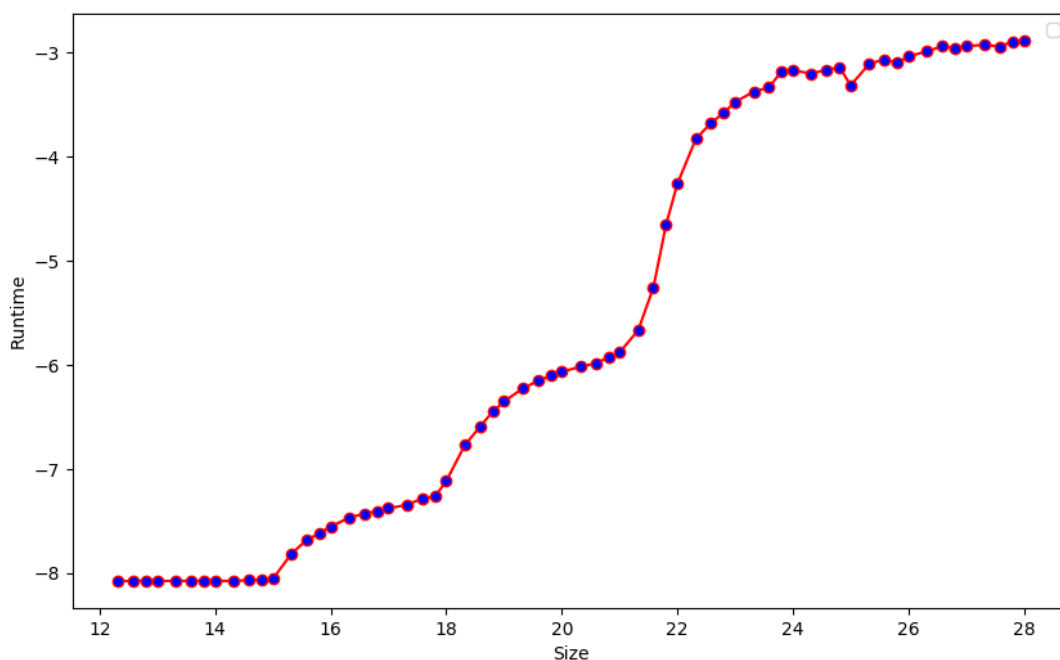# COMP554 Lab Report

Plots

- Without shuffle

- With shuffle

1. Where did you run your code? Do you know anything about the memory configuration of this computer?

- I run the code on my Mac book 2014 version
  The RAM configuration lists following:
  hw.cacheconfig: 4 2 2 4 0 0 0 0 0 0
  hw.cachesize: 4294967296 32768 262144 3145728 0 0 0 0 0 0
  hw.cachelinesize: 64
  hw.l1icachesize: 32768 = 32KB
  hw.l1dcachesize: 32768 = 32KB
  hw.l2cachesize: 262144 = 256KB
  hw.l3cachesize: 3145728 = 3MB

2. Do you think stride prefetching is being done on your architecture?

- When shuffle on, there is no stride prefetching
- When shuffle off, there is stride prefetching

## 3. What factors could be influencing the quality of your measurements?

- Probably opened too many tasks in background process.
- The computer used for too long therefore performance degradation.
- The iteration may cause computer to skip at the point of cache.
- The interrupt mechanism may slow down the running time of program.

4. What steps did you, or could you, use to improve the quality of your measurements?

- Switch to another computer with better CPU and better cache therefore to reducing the hit time and reduce the miss penalty.
- Keep background process running as less as possible tasks.
- Prohibits interrupt during the program running that can reduce the running time therefore improve the measurement.

5. Estimate the L1 cache size. Label this point on your two plots.

- 2^{15} = 32768 = 32KB
- With shuffle
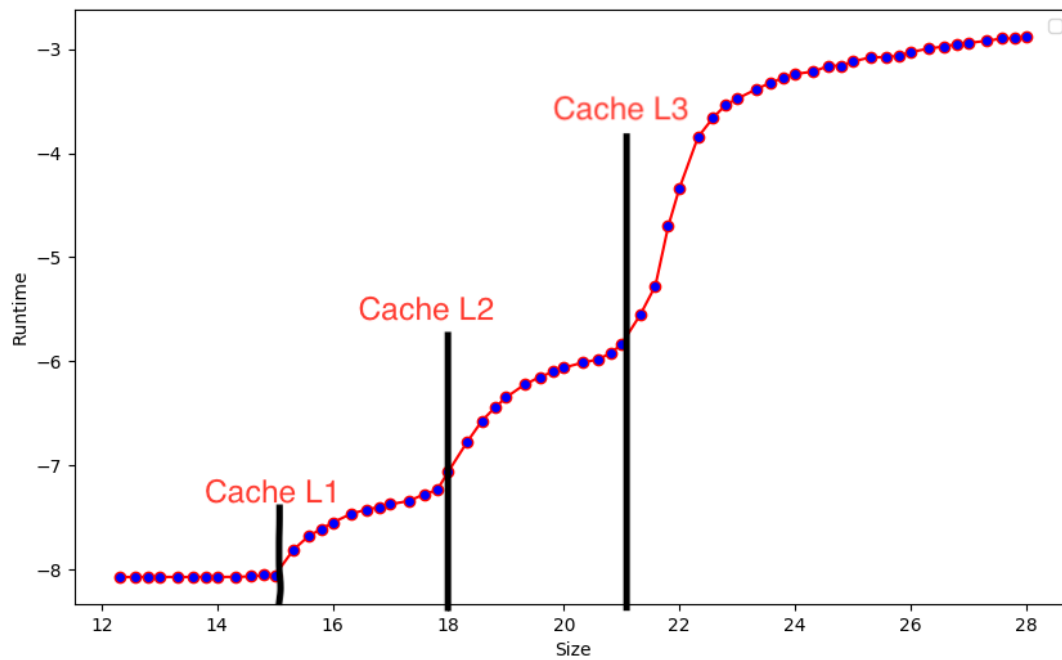
- Without shuffle
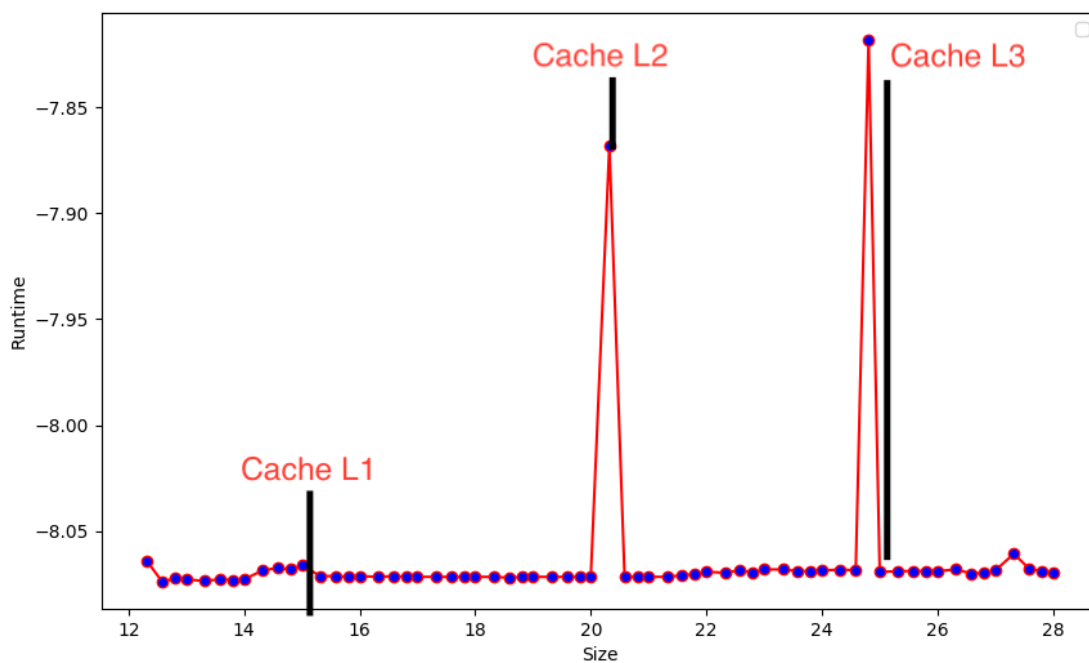
6. How many levels of memory hierarchy do you detect? Explain and label these on your two

plots.

- 3 levels. Cache L1, L2, and L3.
- There are three rapid increasing on slope of the size-runtime line.
- The three peak points indicate the three caches.

7. Estimate the memory bandwidth (=Mbytes per second) your are seeing in the L1 part of the curve.

$32768 \div 1024 \div 1024 \div 0.00376201 = 8.3 Mb/s$