LAU
School of Arts and Sciences

Department of Computer Science & Mathematics

Course Title	Algorithms for Physical VLSI Design
Semester	Fall 2012
Course Coordinator	Haidar Harmanani
Instructor	Haidar Harmanani
Class Time and location	T 5:00 – 8:00 am, 502 Zakhem Engineering Hall
Last Revised on	August 22, 2016

CSC 688E

INSTRUCTOR

Name: *Haidar M. Harmanani*
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Course Page**:** http://vlsi.byblos.lau.edu.lb/csc688e.html
Office: *810 Block A*
Office Hours: *TR 8:00-9:30 am* ***and*** *TR 3:00-4:30*

CURRENT CATALOG DESCRIPTION

Algorithms and methodologies for the synthesis, analysis, and verification of digital systems. Topics include: modeling languages (VHDL, Verilog, …) and hardware compilers. Silicon compilation. High-level synthesis, logic synthesis, and layout synthesis. Logic and circuit simulation. Placement and routing algorithms. Introduction to digital testing. A major part of this course includes the integration of CAD tools into complete design automation systems.

COURSE PREREQUISITE/CO-REQUISTE

Students should have familiarity with the fundamentals of IC design in addition to a strong programming background.

TEXTBOOK AND REFERENCES

1. Sabih H. Gerez, Algorithms for VLSI Design Automation, John Wiley and Sons, 1998.
2. Giovanni De Micheli, Synthesis and Optimization of Digital Circuits, McGraw-Hill, 1994.

COURSE TYPE

Required ☐ **E**lective ☒ **S**elective **E**lective ☐

COURSE LEARNING OUTCOMES

CLO.1 An understanding of the VLSI CAD process and methodologies.
CLO.2 An understanding of what CAD tools available for digital design and where they are used.
CLO.3 An understanding of different design capture methods and the tools that support them
CLO.4 A knowledge of synthesis algorithms, and the underlying strengths and weaknesses of the tools
CLO.5 An understanding of algorithms for VLSI placement, routing, and floorplanning

Course Grading and Performance Criteria

Midterm: 25%
Final: 25%
Course Project: 50%

The objectives of the project are to initiate students into research by converting the theoretical description of one or more algorithms into a functioning implementation while making a minor contribution. The following should be handed over upon the termination of the project:

- A short report (5 to 10 pages) documenting the program. It consists of a description of the main data structures and procedures (using pseudo-code), a motivation of the choices made, an analysis of the time complexity, and a presentation of some results;
- A listing of all the code written with sufficient comment to make the code easily understandable;
- The program itself (delivered e.g. by email) such that it can be tested.

Please check CADathlon Contest for projects selection and references

Topics Covered in the Course

1) Algorithmic techniques for VLSI Design Automation
    a. Graph algorithms, Tractable and intractable problems
2) Combinatorial optimization problems
    a. Unit-size Placement, backtracking, branch-and-bound, Dynamic Programming, Integer and Linear Programming, Local Search, Simulated Annealing, Tabu Search, Genetic Algorithms.
3) Logic Synthesis and Verification
    a. Combinational Logic Synthesis, Binary-decision Diagrams, Two-level Logic Synthesis, Optimization of logic functions. Symbolic optimization and constrained encoding. Technology mapping as a link to PDA
4) Architectural Synthesis Under Constraints
    a. Hardware Models for High-level Synthesis, internal Representation, allocation, assignment and scheduling. Resource binding. Structural synthesis: datapath and control; pipelining.
5) Simulation Modeling
    a. Introduction to simulation as a modeling activity and as a verification activity (switch-level). Mixed domain simulations
6) Physical Design Automation
    a. Layout Compaction.
7) Placement and Partitioning
    a. Circuit Representation, wire length estimation, types of Placement Problem, placement Algorithms, and Partitioning.
8) Floorplanning and Routing
    a. Concepts, Shape Functions and floorplan Sizing, Local Routing Problems, Area Routing, Channel Routing, Introduction to Global Routing, Algorithms for Global Routing,

Assessment Plan for the Course

End of semester self-assessment. Embedded Assessment. Systematic Progression of Assignments. Reviewed every Spring semester by the coordinators for possible updates in the following Fall. Detailed review of all materials of the course once every three years by the CSC Curriculum Committee.

Policy on Cheating and Plagiarism

Students caught cheating on an exam receive a grade of zero on the exam in their first cheating attempt and receive a warning. Students caught cheating for the second time will receive a grade of "F" in the course and another warning. Plagiarism on assignments and project work is a serious offense. If plagiarism is detected, a student will be subject to penalty, similar to the cheating case, which ranges from receiving a zero on the assignment concerned to an "F" in the course in addition to a warning.

UNIVERSITY ATTENDANCE POLICY

Students are advised to attend all classes keeping in mind that according to the *University Academic Rules and Regulations* missing more than five weeks of the classes implies that a student has to drop the course.

WITHDRAWAL POLICY

Students are advised to consult the University Official Policy regarding courses withdrawal at the following link: http://www.lau.edu.lb/academics/arp/u/withdrawal-from-university.php. In specific:

- WI (Early Withdrawal) Indicates withdrawal from the course, after the Late Registration Period and until the end of the 5th week of the Fall and Spring semesters, and until the 10th day of the Summer modules. It has no quality points. It does not count in the GPA, and no credits will be added to the student's record.
- WP (Withdrawal Pass) indicates withdrawal from the course, after the 5th week and until the end of the 10th week of the Fall and Spring semesters, and from the 11th day of classes until 18th day of the Summer modules. It has no quality points. It does not count in the GPA, and no credits will be added to the student's record.
- WF (Withdrawal Fail) indicates withdrawal from the course, after the 5th week and until the end of the 10th week of the Fall and Spring semesters, and from the 11th day of classes until 18th day of the Summer modules. It has no quality points. It does not count in the GPA, and no credits will be added to the student's record, but is counted as repeat.

A Withdrawal Form must be submitted to the Registrar's Office.

Deadline for withdrawal from the course with a WP/WF: **November 9, 2016** (It is the student's responsibility to drop the course).