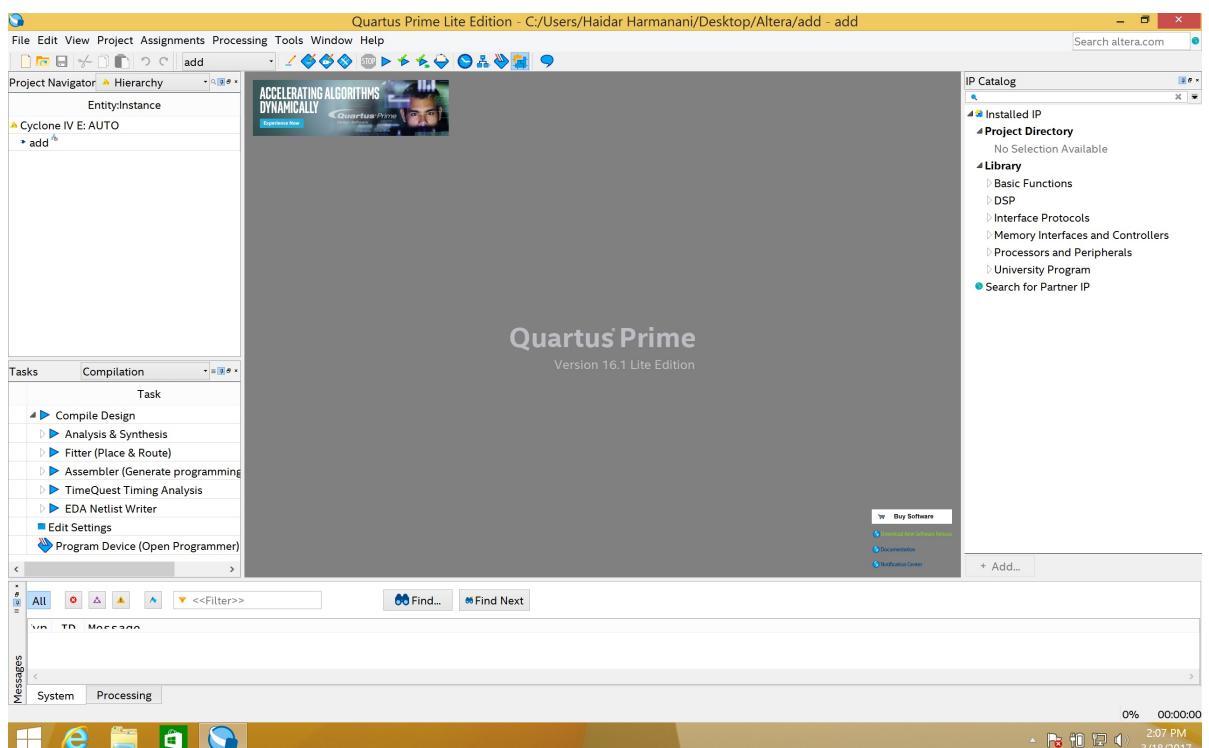


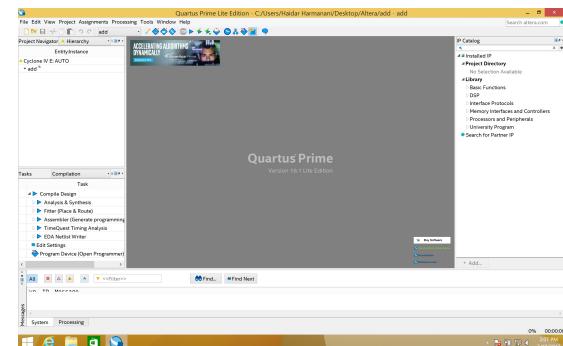
# CSC 322: Computer Organization Lab

## Lecture 3: Using Quartus Prime



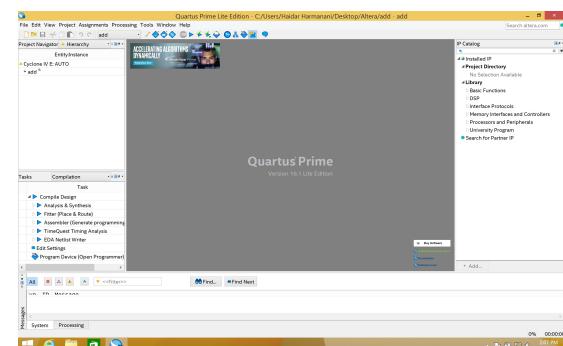
# Software & Development Tools

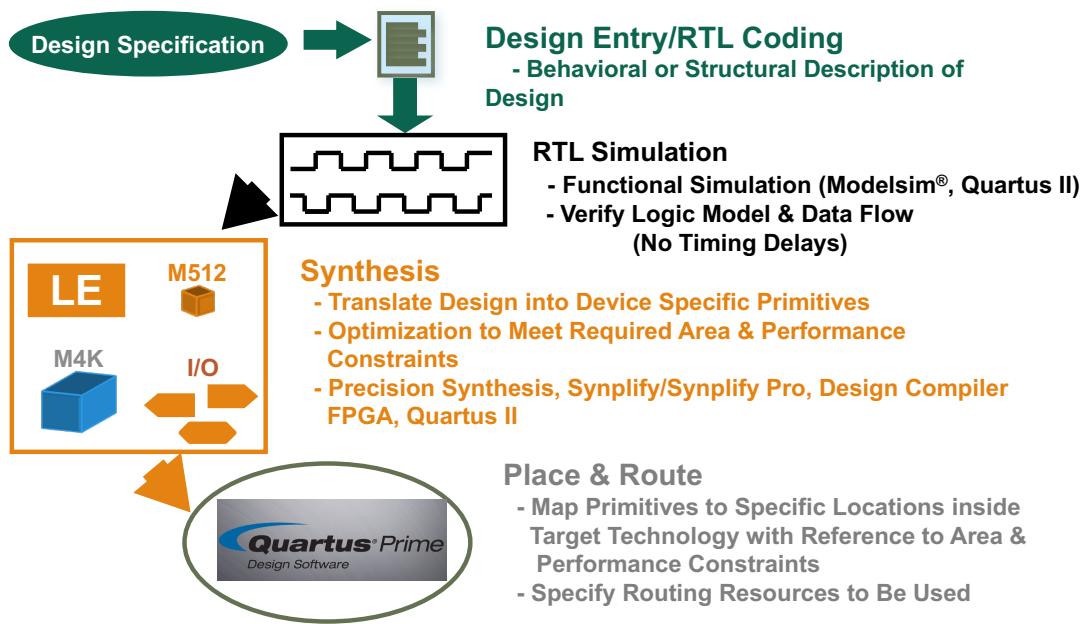
- Intel Quartus Prime Design Software
  - Lite Edition
    - Not All Features & Devices Included
      - Cyclone®, MAX®, and Arria II device support
      - Qsys
      - ModelSim\*-Intel Starter Edition software
      - ModelSim\*-Intel FPGA Edition software
      - Fitter (Place and Route)
      - TimeQuest Static Timing Analyzer
      - SignalTap™ II Logic Analyzer
      - PowerPlay Power Analyzer
  - Windows/Linux 64 bit support Only!



# Intel Quartus Prime Design Software

- Fully-Integrated Design Tool
    - Multiple Design Entry Methods
    - Logic Synthesis
    - Place & Route
    - Simulation
    - Timing & Power Analysis
    - Device Programming



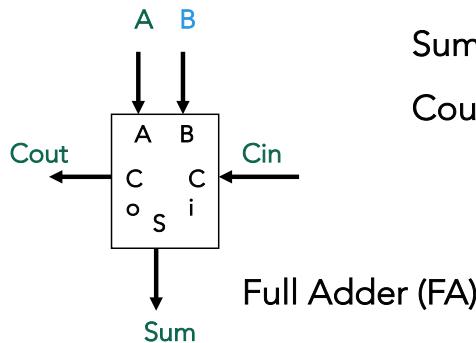


## Using Intel Quartus Prime Design Software: Design and Simulate a One Bit Adder

- Create a project using the New Project Wizard
  - File ➔ New Project Wizard
  - Set up the project directory
  - Set up the proper device
    - Although it does not matter at this stage
  - Create a new schematic file
    - Import the gate symbols into the Graphic Editor window
    - Connect the gates
  - Simulate and verify the design

# Binary Adder Equations

$$F(A,B,C) = A \oplus B \oplus C \quad G = AB + AC + BC$$

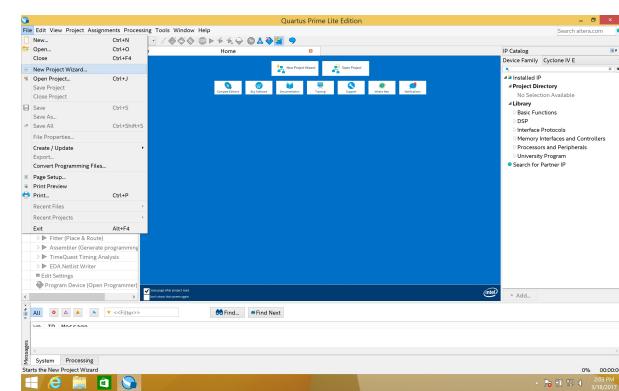


$$\text{Sum} = A \text{ xor } B \text{ xor } \text{Cin}$$

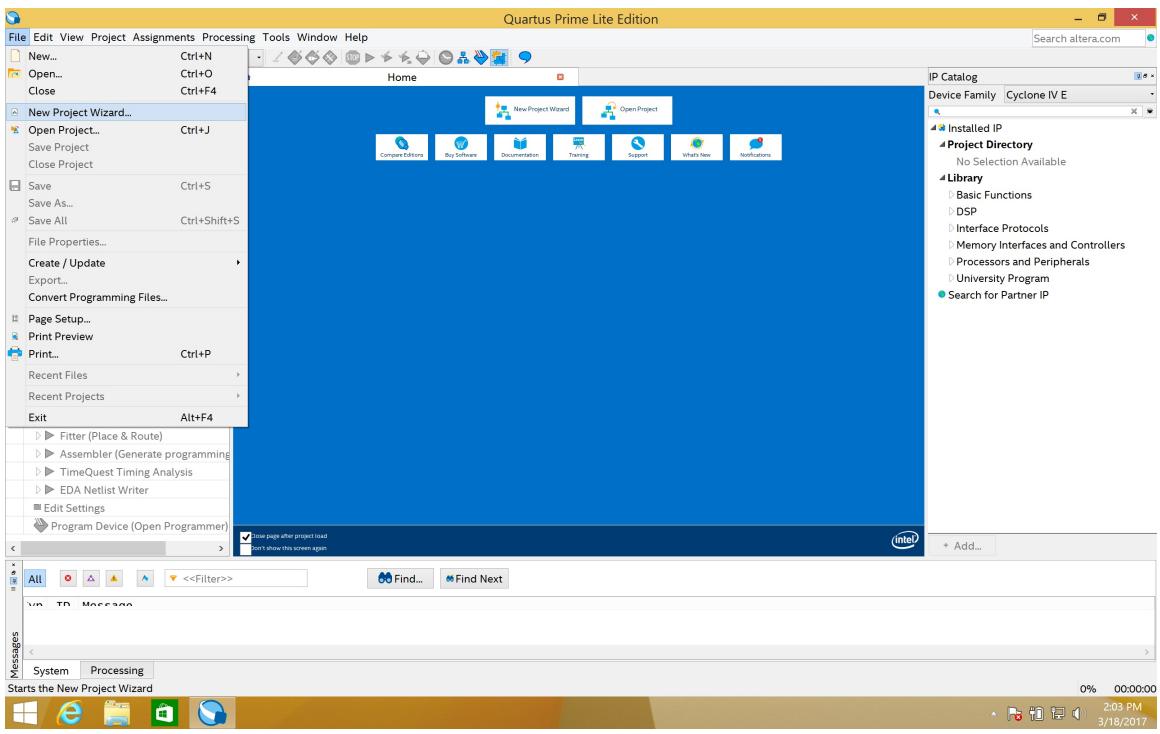
$$\begin{aligned} \text{Cout} &= AB + \text{Cin A} + \text{Cin B} \\ &= AB + \text{Cin}(A + B) \end{aligned}$$

# Step 1: Create a Project

- Complete the following steps:
    - Select the working directory for the project
    - Select a name for the project
    - Select a name for the top-level design entity



## Step 1: Create a Project

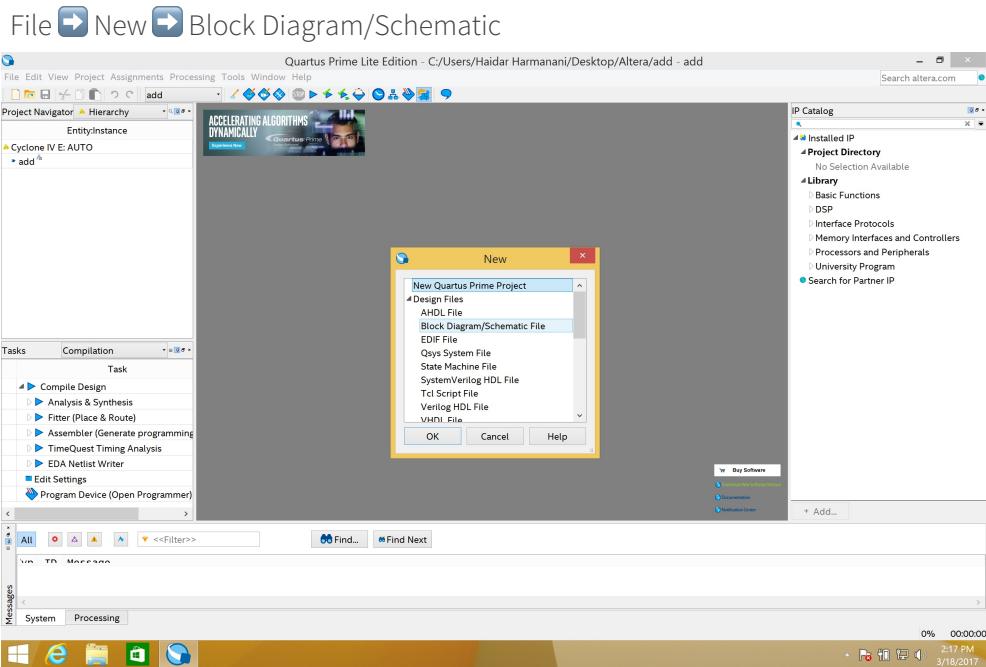


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## Step 2: Create Schematic File

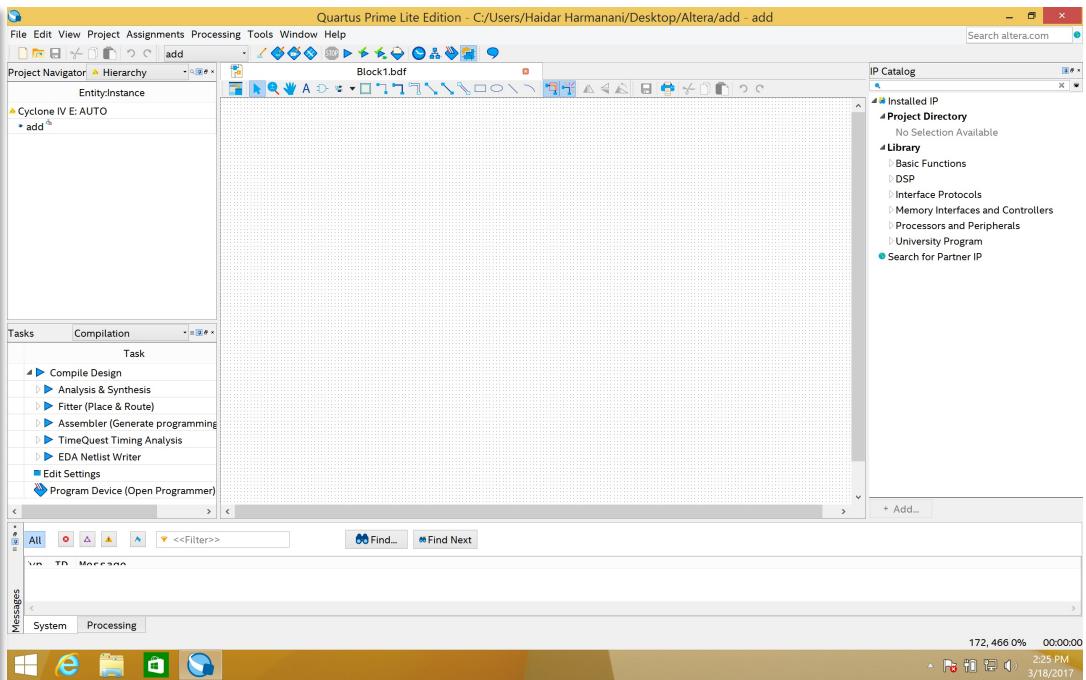


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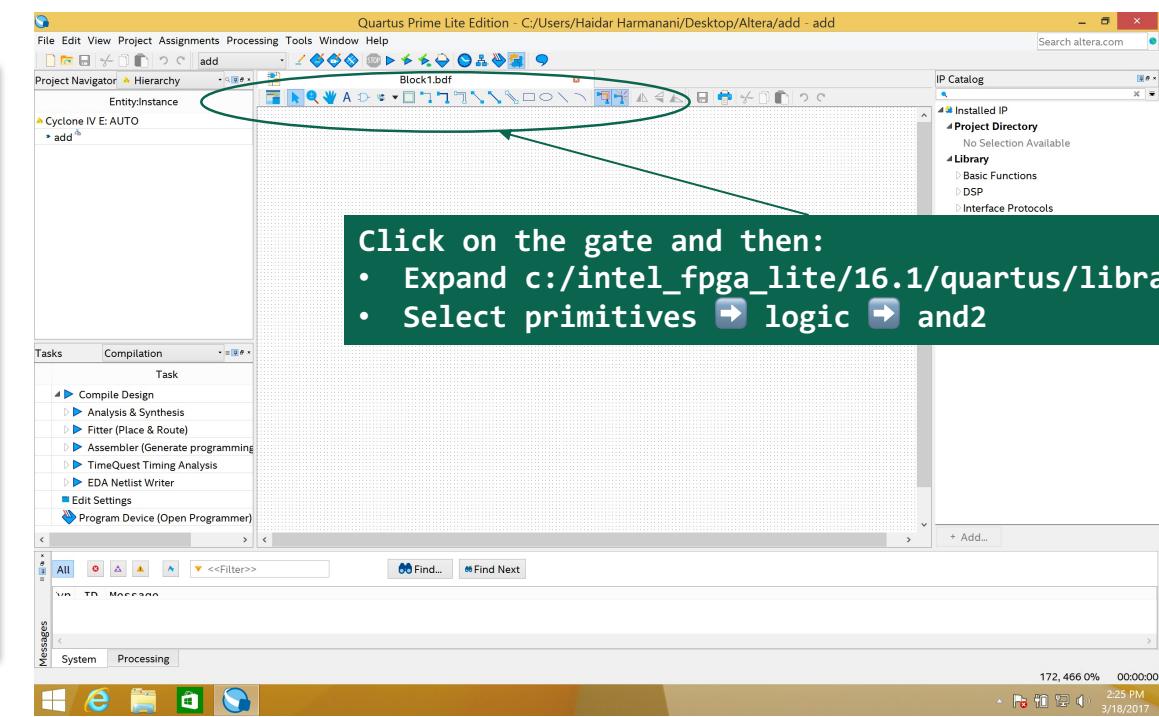


## Step 3: Library Selection

## Step 2: Create Schematic File



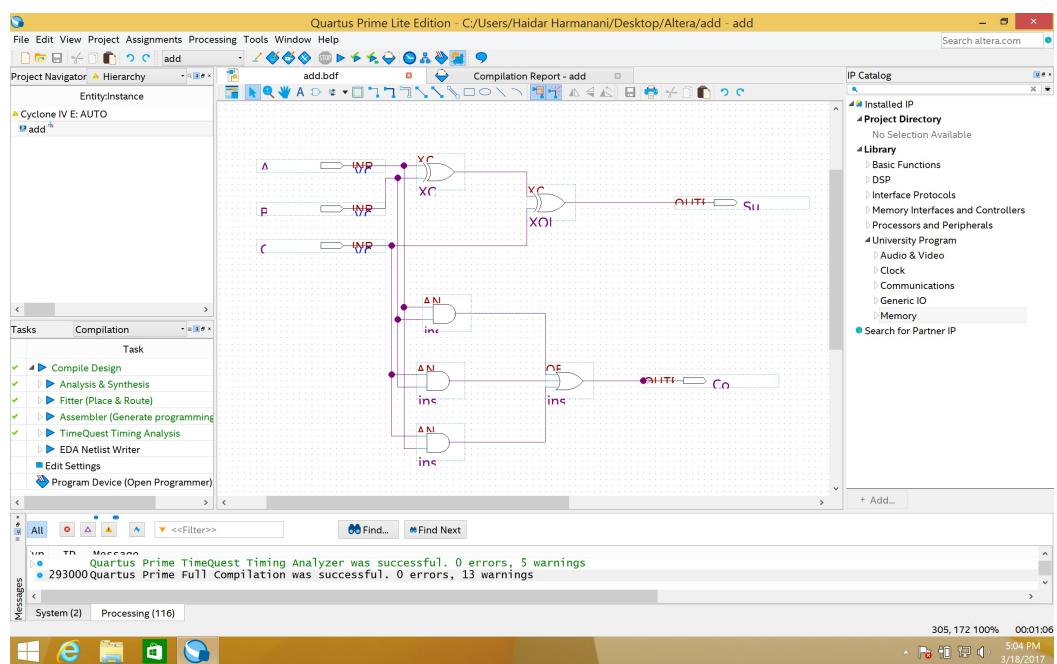
Click on the gate and then:  
• Expand c:/intel\_fpga\_lite/16.1/quartus/libraries/  
• Select primitives ➔ logic ➔ and2



# Step 4: Create the Schematic File

- Import the necessary logic gates from the library
- Connect using wires
- Add input and output ports

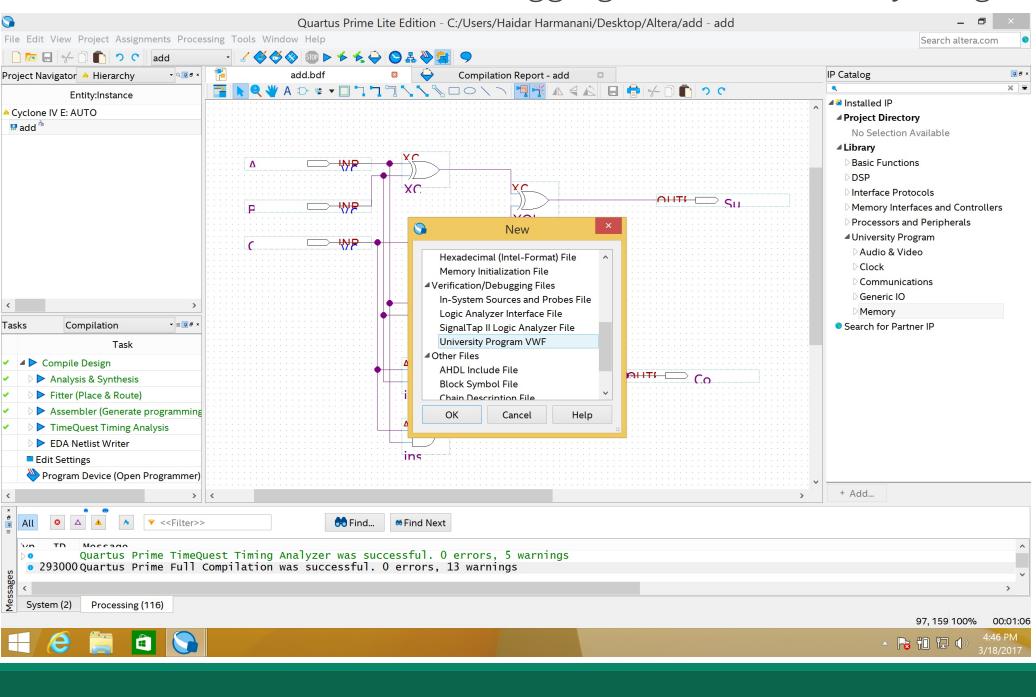
## Step 4: Final Schematic



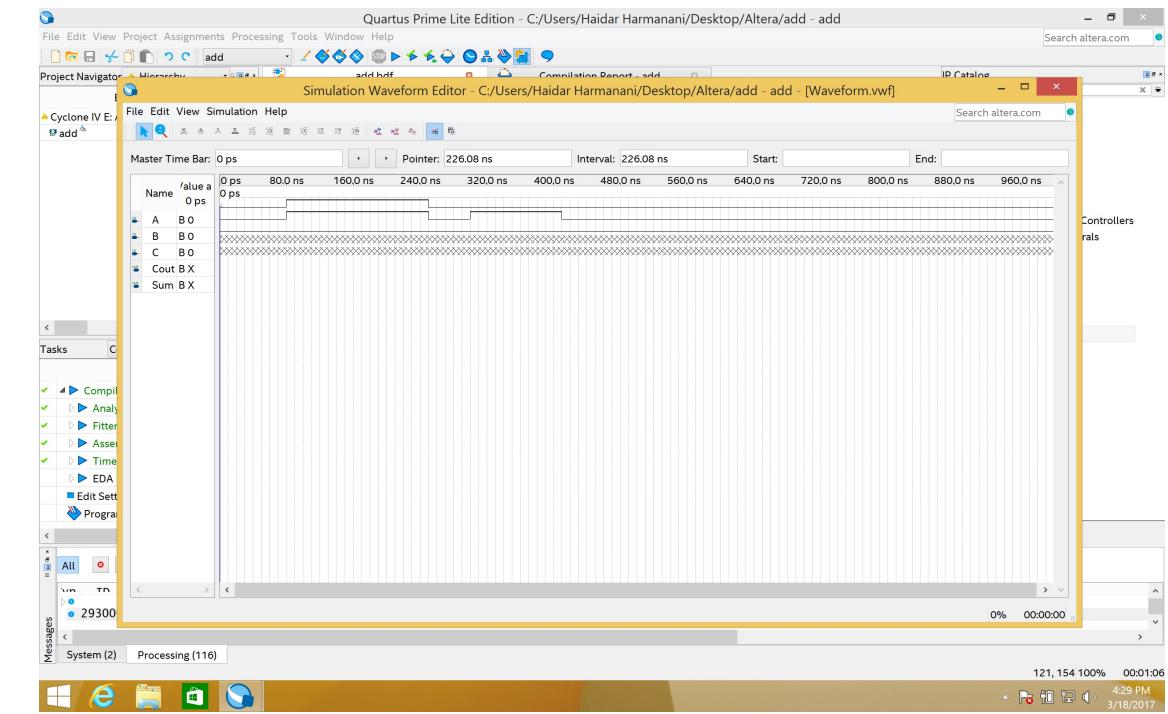
## Step 5: Create a Wave File

## Step 5: Create a Simulation File

File → New → Verification/Debugging Files → University Program VWF



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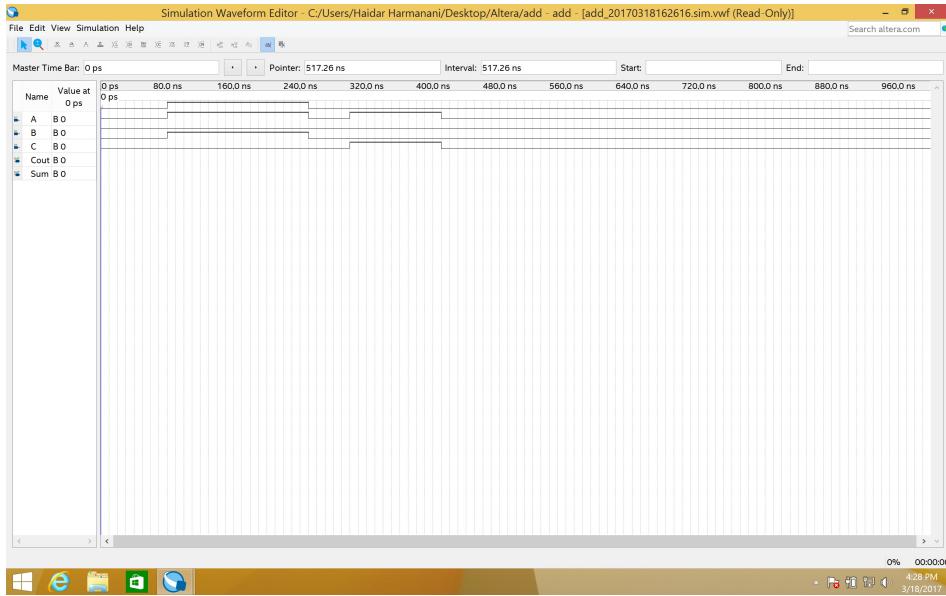


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## Step 6: Simulate and Verify

- 1) Compile: Control L or 2) Processing → Start Compilation
- 2) File → New → Verification/Debugging Files → University Program VWF



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## Pin Assignment

## Step 1

1. Choose Assignments ⇒ Assignment editor.
2. From the View menu, select Show All Known Pin Names.
3. Please click Pin in Category

	To	Location	I/O Bank	I/O Standard	General Function	Sp
1	7_out			LVTTL		
2	7_out[0]			LVTTL		
3	7_out[1]			LVTTL		
4	7_out[2]			LVTTL		
5	7_out[3]			LVTTL		
6	7_out[4]			LVTTL		
7	7_out[5]			LVTTL		
8	7_out[6]			LVTTL		
9	reset			LVTTL		
10	sys_clk			LVTTL		
11	<>new>>	<>new>>				

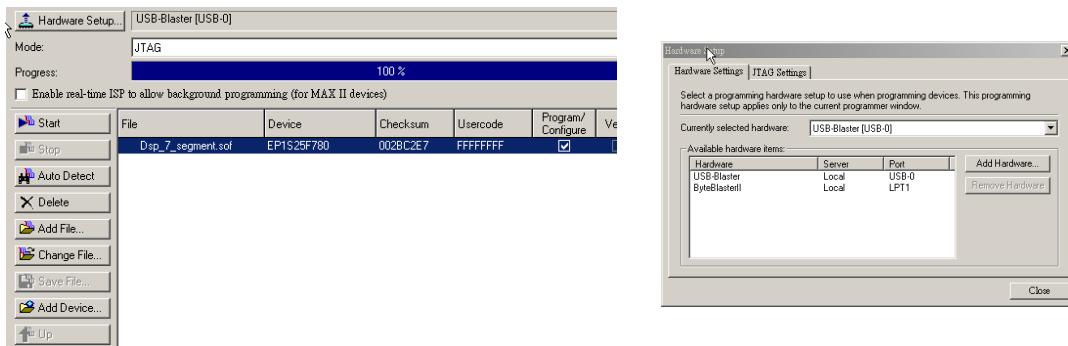
## Step 2

1. Pls install DSP Development Kit Stratix edition CD
2. Open ds\_stratix\_dsp\_bd.pdf from C:\megacore\stratix\_dsp\_kit-v1.1.0\Doc
3. Check clk , pushbutton and seven segment display pin location from ds\_stratix\_dsp\_bd.pdf
4. Key your pin number in location
5. Click on the Save button in the toolbar
6. From Assignments, select Device. Click Device & Pin options. Click Unused pins .Select As input tri-stated from Reserve all unused pins
7. From the Processing menu, select Start Compilation

	To	Location
1	7_out[0]	PIN_L18
2	7_out[1]	PIN_D24
3	7_out[2]	PIN_L23
4	7_out[3]	PIN_L24
5	7_out[4]	PIN_L22
6	7_out[5]	PIN_L20
7	7_out[6]	PIN_L19
8	reset	PIN_F24
9	sys_clk	PIN_K17
10	7_out	

## Step 3

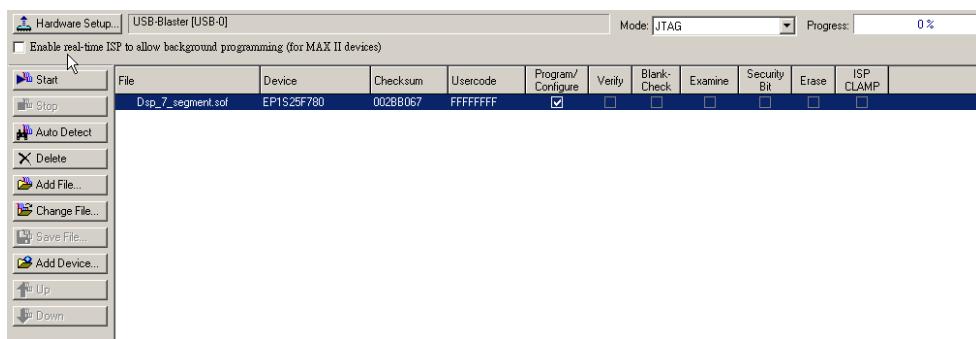
1. From the Tools menu, select programmer
2. Click on Add File. Select Dsp\_7\_segment.sof.
3. Check Hardware Setup. Select your download cable on Currently selected hardware(ByteBlasterII)
4. Select JTAG from Mode



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## Step 4

1. Turn on Program/configure. Or see figure below
2. Click Start
3. See 7-segment status



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