Efficient Shaped Quantizer Dithering Implementation for Sigma Delta Modulators

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***Abstract*— A well-known limitation of sigma delta modulators is the generation of limit cycle oscillations for DC and slow varying inputs. These limit cycles give rise to undesired tones at the output of the modulator which result in the deterioration of the signal to noise ratio (SNR). However, the use of high dither signal amplitude results in raising the in-band noise floor level. Based on the analysis presented in this paper, it is shown that the required dithering amplitude can be minimal depending on the oversampling ratio (OSR). Moreover, a new dither injection technique for sigma delta modulators is presented based on the analysis findings. The proposed circuit effectively eliminates the undesired tonal components of the modulator though the randomization of the comparator's threshold levels. Simulation results using a first order single bit ΣΔ modulator show the suppression of the tonal components while deteriorating the SQNR by less than 1 dB.**

I. INTRODUCTION

With greater system on chip (SOC) integration, more design for observability and testability features (DFT) are required. Oversampled sigma-delta modulators make very suitable candidates for analog-to-digital (A/D) converters that are economical both in power and die area [1], [2].

A limitation of ΣΔ modulators (first order in particular) is their susceptibility to the generation of tonal components and pattern noise [3]. Injection of dither has been effectively used to eliminate the limit cycle tones. This is achieved through the partial restoration of the decorrelation between the input of the quantizer and its output forcing the quantizer error to behave like white noise [3,4]. Another approach is the deliberate incorporation of chaos in the modulator's noise transfer function (NTF). This approach was not widely adopted due to the increased susceptibility to instability [5-7]. While both solutions provide adequate spurious tone suppression, they do so with the penalty of increased in-band noise floor. Dithering in ΣΔ modulators can be divided into two categories, subtractive and none subtractive. In subtractive dithering, a large out of band pseudo-random signal or a filtered random signal are added to the input, then subtracted from the output of the modulator after quantization by means of digital filtering. On the other hand, none subtractive dithering entails the addition of a low-level random signal to the input such that its effective amplitude remains below the LSB level. The latter technique is ineffective for first-order modulators since the dither signal power required to effectively suppress the tonal spurs is a function of the quantizer step size. If the modulator has a 1-bit comparator, then forcing the quantizer error to behave like white noise would require the dither signal to cover the entire quantizer input range and would result in high dither signal power that is comparable to the modulator's input signal. Additionally, this approach results in loss of peak signal to noise ratio (SNR) of the modulator and negatively impacts the modulator's stability and dynamic range. In this work, a none subtractive dithering technique is presented. It allows for the injection of very small dither signal amplitudes that are used to randomize the comparator's decision threshold level. The technique is demonstrated to effectively break the limit cycles and remove the undesired tones at the output of the modulator through transistor level simulations of a first order sigma delta modulator implementation. Furthermore, detailed mathematical analysis is presented to prove the efficacy of the proposed technique and derive key design relations.

The rest of this paper is organized as follows: section II presents the analysis showing the dependency of dither signal amplitude on OSR. Section III presents the proposed circuit for efficient dithering of a 1-bit comparator using threshold randomization. Simulation results of the first order modulator are presented in section IV. Finally, section V concludes this work.

II. DITHER AMPLITUDE OSR DEPENDENCY ANALYSIS

Fig. 1 shows the linearized 1st order sigma delta modulator with dither d(n) added to the input of the quantizer where both the quantizing error and injected dither noise are shaped by the modulator loop filter.

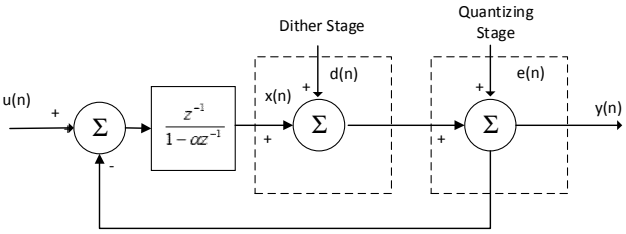


Figure 1: First order sigma delta modulator linear model with injected dither noise.

The step size $\Delta = \frac{V_{max}-V_{min}}{2^N-1}$, 'N' is the resolution of the quantizer and V_{max} and V_{min} are the maximum and minimum quantizer output values respectively (for a 1-bit

qantizer $\Delta = V_{max} - V_{min}$ and the range is $\left[-\frac{\Delta}{2}, +\frac{\Delta}{2}\right]$). The noise and dither transfer functions (NTF and DTF respectively) are equivalent given by :

$$NTF = \frac{Y(z)}{E(z)}\Big|_{U=D=0} = DTF = \frac{Y(z)}{D(z)}\Big|_{U=E=0} = 1 - \alpha z^{-1}$$

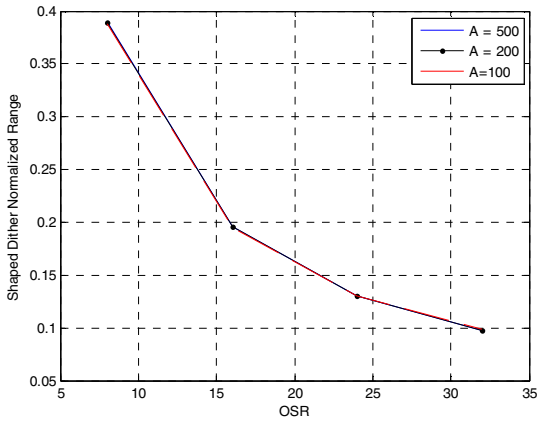
where α is the leakage factor and (1-α) is inversely proportional to the open loop gain 'A' of the integrator, as such for ideal integrator $\lim_{A\to\infty}\ \alpha = 1 - \frac{1}{A} = 1$.
The amplitude frequency response of the $DTF(e^{jw}) = 1 - \alpha e^{jw}$ can be calculated as

$$\left|DTF(e^{jw})\right| = \sqrt{1 + \alpha^2 - 2\alpha cosw} = \sqrt{1 + \alpha^2 - 2\alpha cos\left(\frac{\pi}{OSR}\right)} \quad (1)$$

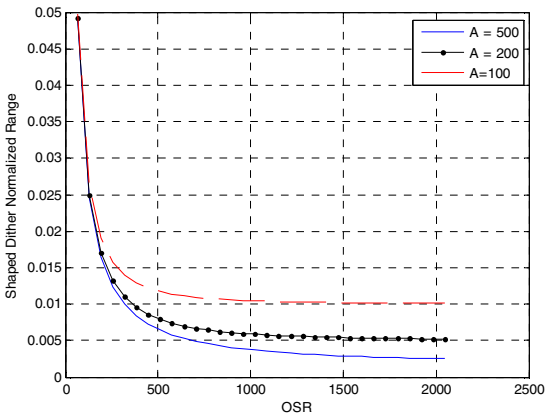
Where 'w' is the digital frequency given by $w = \frac{2\pi f_B}{f_S} = \frac{\pi}{OSR}$, where f_B is the maximum input signal bandwidth, f_S is the sampling frequency and OSR is the oversampling ratio. From Eq. (1), it can be seen that the injected dither noise shaping is based on the leakage factor and the oversampling ratio. Thus the dither amplitude is reduced to $\left[-\frac{\Delta}{2}\left(\sqrt{1 + \alpha^2 - 2\alpha cosw}\right), +\frac{\Delta}{2}\left(\sqrt{1 + \alpha^2 - 2\alpha cosw}\right)\right]$. The normalized amplitude dither range (with respect to Δ)can be written as:

$$R_{normalized} = \frac{2\left(\frac{\Delta}{2}\left(\sqrt{1 + \alpha^2 - 2\alpha cosw}\right)\right)}{\Delta} = \left(\sqrt{1 + \alpha^2 - 2\alpha cosw}\right)$$

Fig 2(a) shows $R_{normalized}$ at low OSR (between 8 and 32). It can be seen that the integrator gain has no effect on the required dither range, moreover the range decreases almost linearly with OSR increase. Fig. 2 (b) shows $R_{normalized}$ for mid to high values of OSR (between 64 and 2048); clearly the range decreases exponentially for OSR greater than 256 reaching a minimal ranges below 0.005. For example, for the case for Δ= 1V, corresponding to a 1-bit quantizer with 1V full scale, the dither full range needed is less than 5 mV for an OSR = 1024. In addition, the sensitivity analysis with regards to integrator gain 'A' shows the minimal impact for A > 200 which is easily achieved in current state of the art [8]. It is worth noting that injecting random dither noise at the input of the quantizer is equivalent to changing the quantizer level thresholds randomly. The minimal dithered range required for mid to high OSR will be exploited in the next section proposing an efficient dithered comparator that randomly changes the threshold level of the quantizer to be used in sigma delta modulators.



(a)



(b)

Figure 2. Input dither range in function of OSR; (a) for low OSR, (b) for mid to high OSR

III. PROPOSED IMPLEMENTATION

The proposed dithering technique is presented in the context of a very low cost first order discrete time modulator, intended for analog DFT applications. Since the modulator is to be instantiated multiple times on the SOC, it needs to have minimal footprint and power consumption.
Fig. 3 shows the schematic of the low cost sigma delta converter analog core. It consists of a class C inverter amplifier (Amp), an inverter based comparator (Dcomp), and a D-flip-flop gate (DFF) to function as a 1-bit none return-to-zero DAC. C_s and C_I are the sampling and integrations capacitors. The sizes of the capacitors are approximately 20fF and 100fF, respectively. In addition to the integration coefficient, the capacitor sizes were optimized based on the tradeoff between leakage current tolerance, associated parasitic capacitances and total die size requirements. Instead of using a high gain OTA (Operational Transconductance Amplifier) for the integrator, we opted for a class-C inverter amplifier [8]. Merits of this approach include, excellent operation with low supply voltage (1 V supply), high slew rate, power efficiency and a wide common mode input range. However, class C inverter amplifiers have low DC gain and no virtual ground node,

therefore they suffer from a low common mode rejection ratio. To address the low DC gain and power supply rejection ratio (PSRR), as well as to reduce the effect of offset variation, auto zeroing is used.

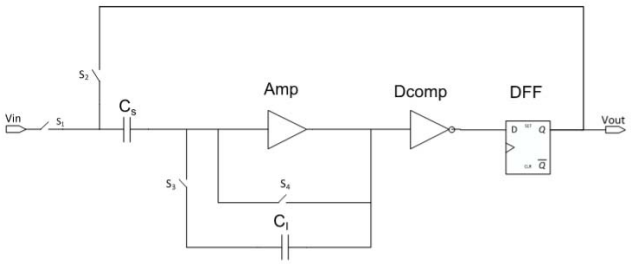


Figure 3. Low complexity 1-bit 1st order modulator schematic

Several previous dither implementations have relied on the generation of a pseudo random binary sequence using a linear feedback shift register (LFSR), then injecting it at various points into the modulator's loop. However, it has been demonstrated that the optimal point for dither injection is at the quantizer's input [3]. This is because the injected dither will get shaped by the noise transfer function of the loop filter and hence have lower impact to the in-band noise floor.

Circuit level dither injection implementations relied on multi-bit DACs to inject the random signal to the desired nodes depending on the modulator's implementation. Discrete time modulators necessitate the use of capacitive DACs connected to the pseudo random noise generator (PN) and to the summing node. This implementation is costly since it requires multiple capacitors and switches to implement. Another mainstream implementation is the use of current steering DACs in order to generate differential currents that are proportional to the dither value. The currents are typically fed into the quantizer to pre bias the comparator decision depending on the dither value [9]. The described implementations either suffer from a large area or large power consumption in addition to poor suitability for integration with the low cost modulator.

Consider the proposed circuit for the dithered comparator (Dcomp) shown in Fig 4.when switches S1 and S2 are open, devices W_P and W_n form an inverter with a switching point V_{sp} representing the threshold of the comparator given by (2).

$$V_{sp} = \frac{rV_{THN}+(V_{dd}-V_{THP})}{1+r}; \quad \text{Where } r = \sqrt{\frac{K_{P_n}\frac{W_n}{L_n}}{K_{P_p}\frac{W_p}{L_p}}} \tag{2}$$

Where K_{P_n} , K_{P_p} and V_{TH_N}, V_{TH_P} are the transconductances and the thresholds of the NMOS and PMOS transistors respectively. From (2), it is can be deduced that the V_{sp} of the inverter is only a function of the W/L ratio between the PMOS and NMOS transistors, provided that K_{P_n} , K_{P_p} and V_{TH_N}, V_{TH_P} are constant. Therefore, adjustment of the W_p or W_n through engaging switches S1 and S2 in a complementary fashion will have the effect of introducing a shift ε to V_{sp} either to W_p or W_n. If the switching action of S1 and S2 is controlled by the PN, then this will have the effect of introducing randomization in the comparator's decision threshold.

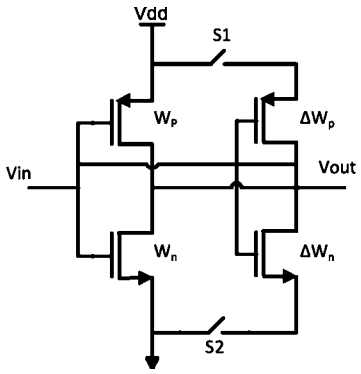


Figure 4. Inverter with randomized threshold level

Next, we present the relationship between the switch threshold voltage in the proposed circuit implementation and Equ. (1). V_{sp} in (2) can be rewritten as:

$$r = \frac{Vdd-V_{THP}-V_{sp}}{V_{sp}-V_{TH_N}} \tag{3}$$

Where

$$V_{sp} = \frac{\Delta}{2} \pm \varepsilon = \frac{V_{dd}}{2} \pm \varepsilon = \frac{V_{dd}}{2} \pm \frac{V_{dd}}{2}\left(\sqrt{1+\alpha^2-2\alpha cosw}\right) \tag{4}$$

Where for a 1-bit quantizer, the full range is $\Delta = V_{dd}$. To move V_{sp} upwards, a smaller value of r is required, which means adjusting the PMOS to become wider. Substituting (4) into (3) with $V_{sp} = \frac{V_{dd}}{2} + \varepsilon$:

$$r_{adjusted_P} = \frac{\frac{V_{dd}}{2}-V_{THP}-\frac{V_{dd}}{2}\left(\sqrt{1+\alpha^2-2\alpha cosw}\right)}{\frac{V_{dd}}{2}-V_{THN}+\frac{V_{dd}}{2}\left(\sqrt{1+\alpha^2-2\alpha cosw}\right)} \tag{5}$$

Using (2) in (5)

$$W_{adjusted_p} = \frac{\left(\frac{K_{P_n}}{K_{P_p}}\right)\left(\frac{L_p}{L_n}\right)W_n}{\left(\frac{\frac{V_{dd}}{2}-V_{THP}-\frac{V_{dd}}{2}\left(\sqrt{1+\alpha^2-2\alpha cosw}\right)}{\frac{V_{dd}}{2}-V_{THN}+\frac{V_{dd}}{2}\left(\sqrt{1+\alpha^2-2\alpha cosw}\right)}\right)^2} \tag{6}$$

Where $W_{adjusted_p} = W_P + \Delta W_P$. To move V_{sp} downwards, a larger value of 'r' is required, which means adjusting the NMOS to become wider. Following the same approach with $V_{sp} = \frac{V_{dd}}{2} - \varepsilon$, we get:

$$W_{adjusted_n} = \left(\frac{K_{Pp}}{K_{Pn}}\right)\left(\frac{L_n}{L_p}\right)W_p\left(\frac{\frac{V_{dd}}{2}-V_{THP}+\frac{V_{dd}}{2}\left(\sqrt{1+\alpha^2-2\alpha cosw}\right)}{\frac{V_{dd}}{2}-V_{THN}-\frac{V_{dd}}{2}\left(\sqrt{1+\alpha^2-2\alpha cosw}\right)}\right)^2 \tag{7}$$

Where $W_{adjusted_n} = W_n + \Delta W_n$.

IV. SIMULATION RESULTS

The design was implemented in .18um standard bulk CMOS technology. Transient simulations using Cadence have been conducted for the following cases: I) without dithering, II) with the application of dither sized in accordance to Eqs. (6) and (7), and III) with the application of dither in accordance to [3]. For all three cases the input signal was a single tone sinusoid with input level set to -73dB relative to full scale at Fin = 12.94 kHz, OSR = 1024 and A = 200V/V. Fig. 5 shows the output power spectral density of the modulator for case I, whereas Figs. 6 and 7 are for cases II and III respectively. From the above, it is clear that the tonal content present in Fig. 5 is completely eliminated after dithering in case (II) with little impact to the in-band noise floor level, whereas the application of dither in case (III) results in the elimination of tones at the expense of a significantly higher noise floor. Furthermore, simulations for the three cases were carried out with the input signal power set to 0 dB relative to full scale for peak SQNR analysis. For case (II), deterioration of the SQNR was less than 1 dB compared to the no dithering case, whereas case (III) peak SQNR degraded by more than 10 dB.

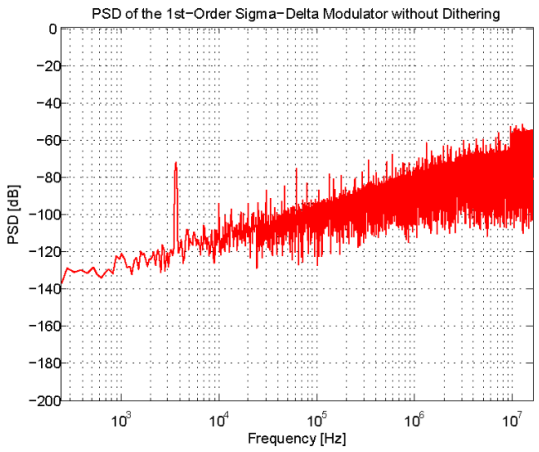


Figure 5: case (I) no dithering applied

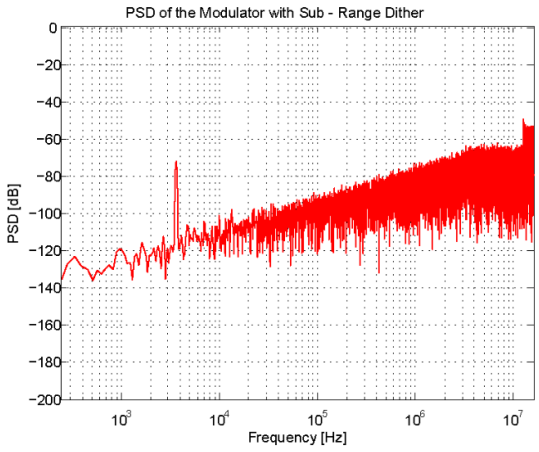


Figure 6: case (II) dithering

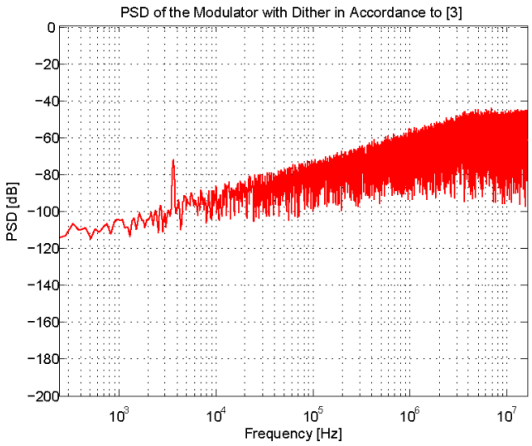


Figure 7: case (III) dithering

V. CONCLUSION

This paper presented a new scheme to inject dither in quantities below the LSB level that can eliminate undesired tonal content and maintain SNR performance of the modulator. Implementation costs are negligible compared to current state of the art methods since no pre-filtering, oversampling or DAC circuitry are required. Simulation results showing removal of the undesired tones for small input signal amplitude are in line with the presented analysis.

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