Modulator Module

Description:

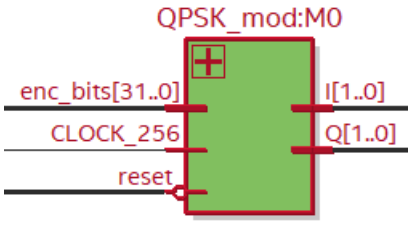

Figure 1: QPSK Modulator

QPSK (Quadrature Phase Shift Keying) is used for its efficiency in bandwidth and power. It has the lowest error probability compared to other higher modulation techniques so it would reliably guarantee BER of 10-5. Gray coding is chosen for constellation ordering to minimize bit errors, as adjacent symbols differ by only one bit. Unlike the Simulink, for the FPGA implementation the phase offset was chosen as pi/2 to prevent phase ambiguity but more importantly not needing to use floating point values and use integers. The table below shows the symbol mapping for the distinct phase shifts.

Symbol Mapping	Phase shift (rad)
00	0
01	Pi/2
11	Pi
10	3pi/2

The RTL diagram below shows detailed working of the modulator.

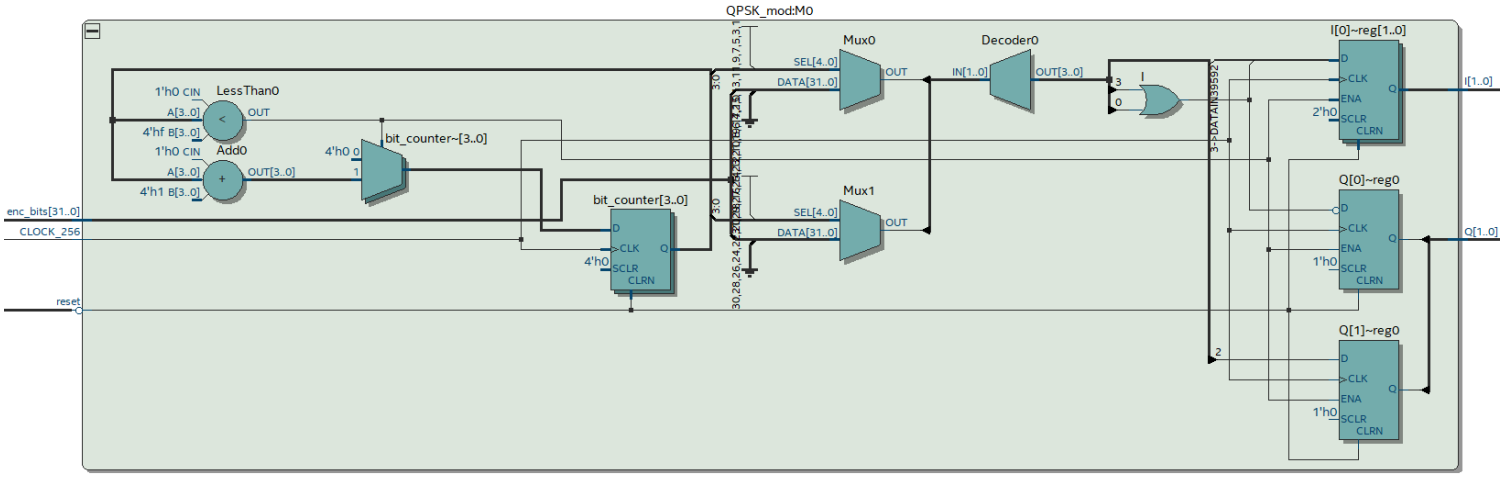

Figure 2: RTL diagram of the QPSK modulator

The modulator takes an input of 32 bits from the encoder module and processes 2 bits every clock cycle at 32 MHz, the same clock frequency as the convolutional encoder. Based on the 2 bits selected I and Q symbols are outputted. I represents the real bits and is the In-phase component. Q represents the imaginary bits and is the Quadrature-phase component. The table below shows the combinations of values that I and Q can be based on the symbol received.

Symbol	I	Q	Reason
00	01	00	cos(0) = 1 and sin(0) = 0
01	00	01	cos(pi/2) = 0 and sin(pi/2) = 1
11	11	00	cos(pi) = -1 and sin(pi) = 0
10	00	11	cos(3pi/2) = 0 and sin(3pi/2) = -1

Testing strategy:

Noted the values of the output to expect when reset is toggled. Checked the bits from the enc_bits input correctly outputted as I and Q. Also made sure that the analog representation of the signal I and Q looks like the signals observed in the Simulink model.

Waveform:

The simulated waveform below shows the expected results. Every clock cycle of this 32MHz clock, 2 bits of I and Q each are sent as output.

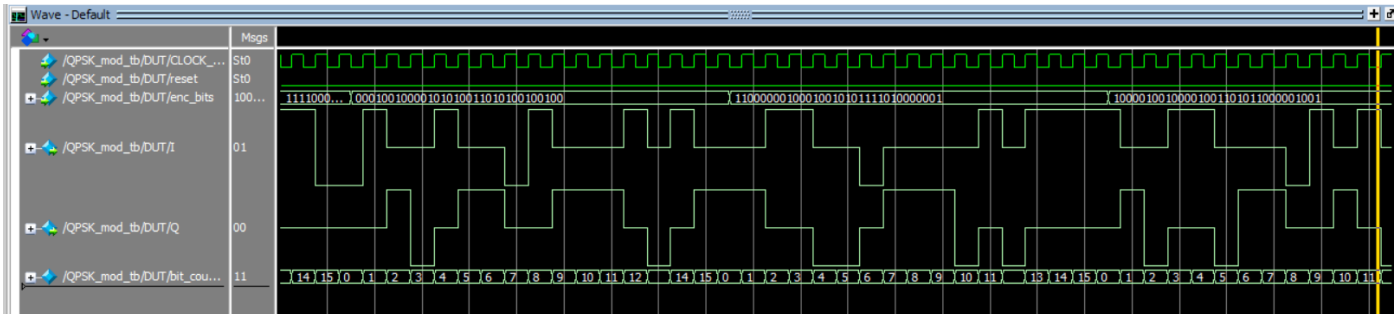

Figure 3: Simulation of QPSK Modulator testbench