Clock Divider Module for 10kHz

Description of the Module

The clock divider formula basically works with taking the 2MHz clock as an input to output lower frequency clock signal of 10kHz clock. This is done by using an 8-bit counter to count 200 clock cycles of the input clock, toggling the output after every 200 input clock cycles. We want to have a lower clock frequency so that we can have our Gilbert-Fading channel Model more smoothly.

The counter's value was selected by using the formula:

Counter = (Input clock) / (Desired Output clock) = (2*10^6)/(10*10^3) = 200

For verifying our design, we made a very brief testbench for it. We then integrated the overall design and instantiated in the top-level module to see if our system was working or not, especially the gilbert-fading since we had made a lower clock frequency for that.

The diagram below summarizes what our module is supposed to do:

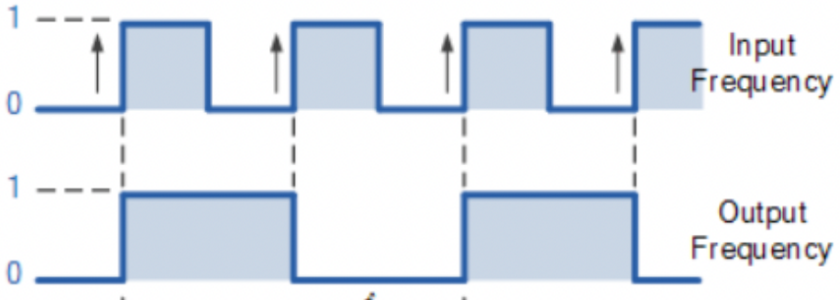

Fig. 1: The depiction of clock divider*

*image obtained from: https://electronics.stackexchange.com/questions/666251/flip-flop-as-frequency-divider-precision