Demodulator Module

Description:

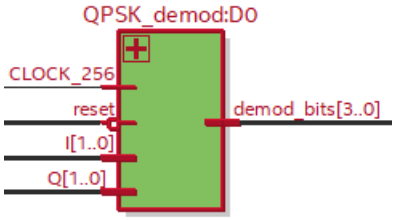

Figure 1: QPSK demodulator

The QPSK demodulator parameters are configured to match the modulator settings. Hard decisions are used to simplify the decision-making process during demodulation. Matching the constellation ordering and phase offset ensures proper demodulation of the received signal. At 32 MHz clock, for every clock cycle the receiver module sends I and Q as inputs with noise added from the channel when they were transmitted. The module processes 4 bits from I and Q in concatenation and maps the symbols to audio bits. The output demod_bits is sized to 4 because the Viterbi decoder takes 4 bits as input at once. The table below shows the symbol mapping.

I	Q	Demodulated bits
01	00	0000
00	01	0001
11	00	0011
00	11	0010

The RTL diagram below shows the detailed implementation.

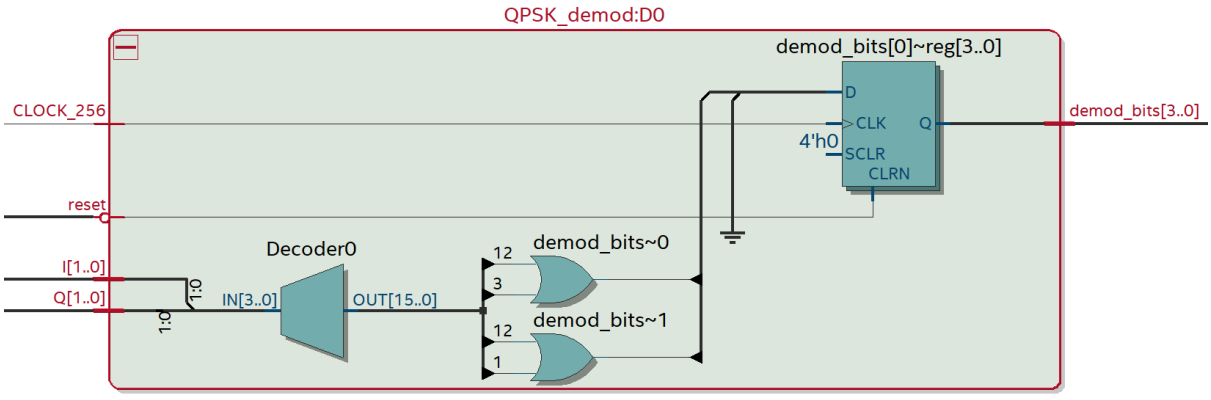

Figure 2: RTL diagram of QPSK demodulator

Testing strategy:

To check the output demod_bits was being correctly outputted when any of the 4 combinations of I and Q were inputs.

Waveform:

The simulated waveform below shows the expected results. Every clock cycle of this 32MHz clock, 4 bits of I and Q are demodulated and outputted as demod_bits.

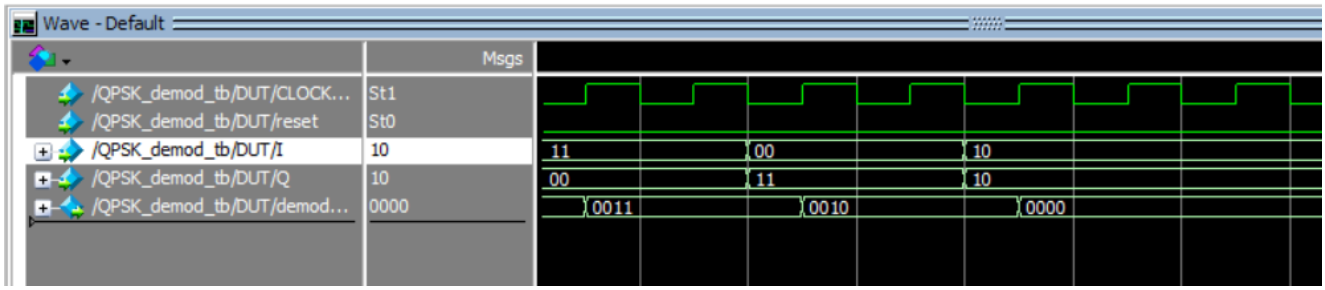

Figure 3: Simulation of QPSK demodulator