May/2016

Printed Pages : 2 Roll No. .....

i) Questions : 7 Sub. Code : 6 8 5 0

Exam. Code : 0 9 2 2

B.Engg. (Information Technology) 4th Semester

1046

COMPUTER ARCHITECTURE AND ORGANIZATION

Paper : ITE-406

Time Allowed : Three Hours] **[Maximum Marks : 50**

Note : Question No. **I** is compulsory. Attempt any **two** questions each from Part A and Part B.

I. Explain the following terms :

(a) Memory Hierarchy

(b) Hit Ratio

(c) Microprogram

(d) Multiprocessor

(e) Cycle Stealing

(f) Address Space

(g) Instruction Format

(h) Locality of Reference

(i) Synchronous of Asynchronous data transfer

(j) Virtual Memory. 10×1=10

VII. a) Explain the working ...

b) Explain the architecture of e-mail system.

Describe TCP segment header.

PART–A

II. (a) What is the need of Common Bus System ? Discuss with example how basic computer registers can be connected to common bus. 5

(b) Differentiate between Hardwired and Microprogrammed control unit. 5

III. (a) Define the term Instruction format. Explain the various organization for instruction. 5

(b) Compare RISC and CISC characteristics. 5

IV. Explain the various addressing modes with suitable examples. 10

PART–B

V. (a) Explain the concept of daisy-chain priority with the help of an example. 5

(b) Explain the block diagram of DMA controller. 5

VI. (a) What is Associative memory ? Explain in detail with suitable diagram. 5

(b) Explain the three types of mapping in cache organization. 5

VII. (a) Explain any two Interconnection structures for multiprocessors. 5

(b) Explain the term memory management hardware. 5

Printed Pages : 2 Roll No. .....

Questions : 7 Sub. Code : 6848

Exam. Code : 922

B.Engg. (Information Technology) 4th Semester

1045

COMPUTER ARCHITECTURE AND ORGANIZATION

Paper : IT-424/434

Time Allowed : Three Hours] [Maximum Marks : 50

Note :– Question No. 1 is compulsory. Attempt any two questions each from Part-A and Part-B.

1. Explain the following terms :
   (a) Addressing mode
   (b) Memory Hierarchy
   (c) Priority Interrupt.
   (d) Multiprocessor
   (e) RISC
   (f) CISC
   (g) Microinstruction
   (h) I/O processor
   (i) Virtual memory
   (j) Opcode. 10

PART—A

2. (a) What is meant by processor level design ? Explain. 5
   (b) Compare RISC and CISC characteristics. 5

ciphers ?

VII. a) Explain the working of DNS.

b) Explain the architecture of e-mail system

3. Explain the various addressing modes with suitable examp

4. (a) What is the need of a common bus System ? Device th control gates associated with the program counter PC in th basic computer. 5

(b) Explain the micro-programmed control organization. 5

PART—B

5. (a) What is virtual memory ? Explain the concept of Paging and Segmentation in detail. 5

(b) What is Associate Memory ? Explain in detail with the block diagram of associative memory. 5

6. (a) What is the need of Input-output interface ? Explain the connection of input-output devices to I/O Bus and the communication of peripherals with processor. 5

(b) Explain the concept of DMA transfer with the help of a block diagram. 5

7. (a) Differentiate between tightly coupled and loosely coupled multiprocessor system. 5

(b) Explain the multiport memory and cross bar switch Interconnection structures in detail. 5

Exam.Code:922
Sub. Code: 6848

1015

B.E./B.E. MBA (Information Technology) Fourth Semester

IT-424: Computer Architecture and Organization

Time allowed: 3 Hours

Max. Marks: 50

NOTE: *Attempt five questions in all, selecting at least two questions from each unit.*

x-x-x

UNIT – I

I. a) What do you understand by Gate Level and Register Level Design? Discuss in brief.

b) The content of PC in the basic computer is 3AF (all numbers are in hexadecimal). The content of AC is 7EC3. The content of memory at address 3AF is 932E. The content of memory at address 32E is 09AC. The content of memory at address 9AC is 8B9F.

i) What is the instruction (in binary) that will be fetched and executed next?

ii) Show the effect of instruction on AC if the operation to be performed is AND,

iii) Give the contents of registers PC, AR, DR, AC and IR in hexadecimal and the values of E, I and sequence counter (SC) in binary at the end of instruction cycle. (4,6)

II. a) Differentiate between memory-reference, register-reference and input-output instructions. Give examples of each.

b) Explain the different phases of instruction cycle. (5,5)

III. a) What do you mean by Micro-programmed Control Unit? Explain with the help of an example.

b) What do you understand by RISC? What are the characteristics of these systems? Discuss. (6,4)

IV. Write notes on the following:-

a) Common Bus System b) General Register Organization (5,5)

UNIT – II

V. a) Explain Parallel Priority Interrupt method in detail.

b) Differentiate between isolated I/O and memory-mapped I/O. (6,4)

VI. a) Explain the block diagram of a DMA controller-

b) Explain time-shared common bus interconnection structure. (5,5)

VII. a) Explain the block diagram of associative memory.

b) What do you mean by parallel processing? What are the characteristics of multiprocessors? Discuss. (5,5)

VIII. Write notes on the following:-

a) Interrupt-initiated I/O

b) Virtual Memory (4,6)

x-x-x

Exam.Code:0921
Sub. Code: **6836**

1127

B.E. (Information Technology) Third Semester

ITE-375/344: Computer Architecture and Organization

Time allowed: 3 Hours Max. Marks: 50

NOTE: *Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Part.*

x-x-x

Q1. Explain the following terms:

a) address space
b) CAM
c) effective address
d) Control data register
e) SELD
f) Operation Code Field
g) Bus request and Bus grant
h) locality of reference
i) control word
j) Instruction Code (10 X1=10)

PART-A

Q2. (a) How following register transfer statements are implemented during timing signal T_0 and T_1

T0 : AR <---- PC

T1 : IR <----M[AR], PC<----- PC+1

(b) Explain with the help of diagram how various computer registers are connected to common bus? (5,5)

Q3. Explain the internal structure of microprogram sequencer for a control memory. (10)

Q4. (a) What are the various types of interrupts that a program can encounter?

(b) What are the various components required for system design at register level? Explain any one component in detail. (5,5)

PART-B

Q5. What is priority interrupt? Explain how hardware priority function can be established? (10)

Q6. Explain various types of mapping procedures required in the organisation of cache memory. (10)

Q7. (a) What is multistage switching network? Using 2x2 switch as a building block build a multistage network.

(b)What is multiprocessing? Explain various types of multiprocessors. (5,5)

x-x-x

Exam. Code: 0921
Sub. Code: 6836

1128

Bachelor of Engineering (Information Technology)

3rd Semester

ITE – 375/344/304: Computer Architecture and Organization

Time allowed: 3 Hours **Max. Marks: 50**

Note: Attempt any five questions, including Question No. 1 which is compulsory and selecting two questions each from Unit I – II.

0-0-0

I. Attempt the following questions:-

a) Differentiate between Direct and Indirect address.
b) What are the various instruction formats?
c) Explain the terms hardwired and microprogrammed control.
d) Explain the term microinstruction and microprogram.
e) What is the purpose of various addressing modes?
f) Explain the terms strobe and handshaking.
g) Define the term locality of reference.
h) Define the term virtual memory.
i) Define the term Associative memory.
j) What are the various interconnection structures? (10×1)

UNIT – I

II. Write notes on the following:-

a) Common Bus System
b) General Register Organization. (5,5)

III. a) What do you understand by RISC? What are the characteristics of these systems?
b) What is the purpose of addressing modes? Explain various addressing techniques. (5,5)

IV. a) What are the various Data Transfer and Data Manipulation instruction?
b) Explain the block diagram for a Microprogram sequencer. (5,5)

UNIT – II

V. a) What is associative memory? Explain the Block diagram of associative memory.
b) Explain the Daisy Chaining Priority in detail. (5,5)

VI. a) Explain the time-shared common bus interconnection structures.
b) What is memory management Hardware? (5,5)

VII. Write notes on the following:-

a) Interrupt initiated I/O
b) Virtual Memory (5,5)

0-0-0

Exam.Code:0916
Sub. Code: 6785

1018

B.E. (Computer Science and Technology)

Fourth Semester

CS-405: Computer Architecture and Organization

Time allowed: 3 Hours Max. Marks: 50

NOTE: *Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Unit.*

x-x-x

I. Attempt the following:-

a) What is an effective address?

b) What do you understand by Divide Overflow?

c) What are the advantages of Hardwired control unit over Micro-programmed control unit?

d) What is the purpose of Memory Management Unit (MMU)?

e) Give the formulae to calculate speedup of a pipeline processing over an equivalent non-pipeline processing. (5x2)

UNIT – I

II. a) Explain the instruction cycle of a computer system with the help of a diagram.

b) Compare the characteristics of RISC architecture with CISC architecture. (2x5)

III. a) A 36-bit floating-point binary number has eight bits plus sign for the exponent and 26 bits plus sign for mantissa. The mantissa is a normalized fraction. Numbers in the mantissa and exponent are in signed-magnitude representation. What are the largest and smallest positive quantities that can be represented, excluding zero? Appropriately assume any required information yourself.

b) Briefly discuss the design of a Micro-programmed Control Unit. (2x5)

IV. a) Explain the following addressing modes with examples:-

i) Implied Mode

ii) Register Mode

iii) Relative Address Mode

b) Write assembly language program to multiply two positive numbers by repeated addition method. Appropriately assume any required information yourself. (2x5)

P.T.O.

UNIT – II

V. a) What is Virtual Memory? What is its purpose? Discuss with diagram how the program-generated addresses are translated into correct main memory locations?

b) Write a short note on Parallel Processing. (2x5)

VI. a) What is Handshaking? How source-initiated and destination-initiated transfer operation is performed using handshaking? Discuss with the help of suitable diagrams.

b) Give an example of a Data Hazard and discuss its resolution mechanism. (2x5)

VII. a) Explain Arithmetic Pipeline for floating point addition and subtraction operation. Appropriately assume any required information yourself.

b) Explain the working of Programmed 1- 0 with the help of a diagram. (2x5)

x-x-x

Exam.Code:0930
Sub. Code: 6273

1057

B.E. (Electronics and Communication Engineering)
Sixth Semester
EC-610: Computer Architecture and Organization

Time allowed: 3 Hours Max. Marks: 50

NOTE: *Attempt five questions in all, including Question No. I (Section-A) which is compulsory and selecting two questions each from Section B-C.*

x-x-x

Section - A

1. (a) What is a pseudo Instruction? Give examples.

(b) What must the address field of an indexed addressing mode instruction be to make it the same as a register indirect mode instruction?

(c) Explain the difference between hardwired control and microprogrammed control. Is it possible to have a hardwired control associated with a control memory?

(d) Determine the no. of clock cycles that it takes to process 200 tasks in a six segment pipeline.

(e) Differentiate between internal, external and software interrupts.

(f) What is the condition for the stack overflow to occur?

(g) What is virtual memory?

(h) Differentiate between BUN and BSA.

(i) How many times does the control unit refer to memory when it fetches and executes an indirect addressing mode instruction if the instruction is a branch type instruction.

(j) What is the advantage of DMA. (10 X 1=10)

Section – B

2. (a) Design a bus system for four registers using multiplexers. (5)

(b) Explain the control unit of basic computer in detail. (5)

3. (a) Draw and explain flowchart for second pass of an assembler. (5)

(b) A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part.

i. How many bits are there in the operation code, the register code part, and the address part?
ii. Draw the instruction word format and indicate the number of bits in each part.
iii. How many bits are there in the data and address inputs of the memory? (5)

P.T.O.

Sub Code: 6273

4. (a) Write a program to multiply two unsigned positive numbers, each with 16 significant bits, to produce an unsigned double-precision product. (5)

(b) Differentiate between BUN, BSA and ISZ with suitable examples. (5)

Section-C

5. (a) What is control memory? Explain the micro-instruction format and give the symbolic microprogram for any 3 computer instructions. (5)

(b) Explain booth algorithm for multiplication of signed 2's complement numbers. (5)

6. (a) Draw and explain flowchart for divide operation of two fixed point binary numbers in signed magnitude representation. (5)

(b) Briefly explain various types of mapping procedure for cache memory. (5)

7. Write notes on the following:

(a) Memory management Hardware
(b) Asynchronous Data Transfer

(5x2=10)

X-X-X

Exam. Code: 0930
Sub. Code: 7975

1018

B. Engg. (Electronics and Communication Engg.)-6th Semester
EC-610: Computer Architecture and Organization

Time allowed: 3 Hours

Max. Marks: 50

Note: *Attempt <u>five</u> questions in all, including Question No. 1 (Section-A) which is compulsory and selecting two questions each from Section B & C.*

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Section - A

1. a) Define instruction set completeness.
   b) What is the difference between a software interrupt and a sub routine call?
   c) List out the data manipulation and data transfer instructions.
   d) Write the microoperations needed to execute the instruction LDA.
   e) Let SP = 000000 in the stack. How many items are there in the stack if FULL = 1 and EMPTY = 0, FULL = 0 and EMPTY = 1

(2x5)

Section – B

2. a) Design a 4 bit combinational circuit decrementer using four full adder circuits. (5)

   b) Explain and show the timing diagram for the following microoperation:
   D_3T_4 : SC ← 0 (5)

3. a) Draw and explain instruction cycle with the help of an example. (5)
   b) Draw and explain flowchart for first pass of an assembler. (5)

4. a) Write a program to subtract two double precision numbers. (5)

   b) Compare stack organization with general register organization. (5)

Section-C

5. a) Explain booth algorithm for multiplication of signed 2's complement numbers. (5)
   b) Differentiate between comparison and non-restoring method of fixed point binary division. (5)

6. a) Briefly explain various types of mapping procedure for cache memory. (5)
   b) Explain the concept of virtual memory. (5)

7. Write the symbolic microprogram for the following instructions:

Symbol	Opcode	Symbolic Function
AND	0100	AC←AC ^M [EA]
SUB	0101	AC←AC -M[EA]
BPNZ	1010	If (AC>0) then (PC←EA)
ADM	0110	M[EA]←M[EA]+AC

(2.5x4)

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Exam.Code:0921
Sub. Code: **6836**

1127

B.E. (Information Technology) Third Semester
ITE-375/344: Computer Architecture and Organization

Time allowed: 3 Hours

Max. Marks: 50

NOTE: Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Part.

x-x-x

Q1. Explain the following terms:

a) address space
b) CAM
c) effective address
d) Control data register
e) SELD
f) Operation Code Field
g) Bus request and Bus grant
h) locality of reference
i) control word
j) Instruction Code

(10 X1=10)

PART-A

Q2. (a) How following register transfer statements are implemented during timing signal T_0 and T_1

T0 : AR <---- PC

T1 : IR <----M[AR], PC<----- PC+1

(b) Explain with the help of diagram how various computer registers are connected to common bus? (5,5)

Q3. Explain the internal structure of microprogram sequencer for a control memory. (10)

Q4. (a) What are the various types of interrupts that a program can encounter?
(b) What are the various components required for system design at register level? Explain any one component in detail. (5,5)

PART-B

Q5. What is priority interrupt? Explain how hardware priority function can be established? (10)

Q6. Explain various types of mapping procedures required in the organisation of cache memory. (10)

Q7. (a) What is multistage switching network? Using 2x2 switch as a building block build a multistage network.
(b)What is multiprocessing? Explain various types of multiprocessors. (5,5)

x-x-x