(i) Printed Pages : 2 Roll No. .....

CSE
2nd Sem

. Code : 6 6 6 9

. Code : 9 0 6

& Engg.) 2nd Semester

1045

DIGITAL ELECTRONICS AND LOGIC DESIGN

Paper : CS–203

Time Allowed : Three Hours] **[Maximum Marks : 50**

Note :– There are **seven** questions in all. Q. 1 is compulsory. Attempt any **two** questions each from Part A and Part B.

1. (a) Differentiate between an analog and a digital signal.
   (b) Explain the cut off and saturation region of a bipolar transistor.
   (c) Explain the inverse operation of a transistor.
   (d) What are Karnaugh maps ?
   (e) Differentiate between a combinational circuit and a sequential circuit.
   (f) What is an FPGA ? What are its applications ?
   (g) Explain the different modes of operation of a shift register.
   (h) Differentiate between a half subtractor and a full subtractor.
   (i) What is a CMOS transmission gate ?
   (j) Explain the working of a parity generator. 1×10=10

PART–A

2. Give a classification of the digital IC families. Explain the evolution process of the digital logic families. What are the characteristics of digital ICs ? Explain them. 10

Q6. i) Explain the difference between structures and unions
ii) Explain different input and output functions in C.

Write a C Program to compare two files, printing the

3. Using a neat diagram, explain the working of a 2 input TTL NAND gate. Compare the TTL NAND gate with an emitter coupled logic gate. 10

4. Using a neat diagram, explain the working of a MOS transistor. Explain how it can be used as a gate. Differentiate it with the gates designed using the bipolar technology. 10

PART–B

5. Explain the working of a multiplexer. Differentiate it with the encoder. What are demultiplexers ? How are they different to decoders ? Explain. Also give some examples of the ICs of multiplexers and decoders. 10

6. What is a flip flop ? Explain the use of clock in a flip flop. Using a neat diagram, explain the working of a J-K flip flop. 10

7. Write notes on :
   (a) Ring counter
   (b) Random Access memories. 5,5.

21/8/2016

Printed Pages : 2 Roll No. .....

i) Questions : 7 Sub. Code : 6 6 7 7

Exam. Code : 0 9 0 6

B.Engg. 1st Year (2nd Semester)

1046

(Computer Science and Engineering)-DIGITAL ELECTRONICS AND LOGIC DESIGN

Paper–CS-203

Time Allowed : Three Hours] **[Maximum Marks : 50**

Note : Attempt any **five** questions out of **seven** questions selecting two from each Part. Each question carries 10 marks. Question No. **1** is compulsory. It contains 10 questions of 1 mark each.

1. (a) What are the characteristics of a digital IC ?

(b) Differentiate between TTL and a DTL gate.

(c) What are SOP and POS implementations ?

(d) Differentiate between a half adder and a full adder.

(e) Explain the working of a 8:1 encoder.

(f) What is a flipflop ?

(g) What is a MOS device ?

(h) Differentiate between a counter and a register.

(i) What are programmable logic devices ?

(j) Give some applications of shift registers. 1×10=10

[Turn over

Q6. i) Explain the difference between structures and unio

ii) Explain different input and output functions in C.

compare two files, printing t

PART–A

2. Explain the working of a three input TTL NAND gate. Compare its performance with a CMOS NAND gate. What are the different characteristics of a TTL gate ? 10

3. (a) What is a half subtractor ? Differentiate between a half subtractor and a full subtractor.

   (b) What is a carry look ahead adder ? Explain using a neat diagram. 5,5

4. Write notes on :

   (a) CMOS transmission gate

   (b) BCD to 7 segment decoder. 5,5

PART–B

5. (a) What is a comparator ? Give its types and explain them.

   (b) Differentiate between a J-K flipflop and a R-S flipflop. What is the difference between a latch and a flipflop ? 5,5

6. Differentiate between synchronous and asynchronous counters. Explain how these counters are designed. What are their types ? 10

7. Write notes on :

   (a) Multiplexer and a demultiplexer

   (b) FPGA and its applications. 5,5

Exam.Code:915
Sub. Code: 6803

1075

B.E./B.E.M.B.A. (Computer Science and Engineering) Third Semester

EC-316: Digital Electronics

Time allowed: 3 Hours

Max. Marks: 50

NOTE: *Attempt five questions in all, including Question No. 1 which is compulsory and selecting two questions from each Section.*

x-x-x

1. (a) Perform the subtractions of following decimal numbers using 10's complement method: 5250-321, 753-864.
   (b) Represent the decimal number 6935 in BCD code, excess-3 code, and binary code.
   (c) Reduce the following Boolean expression to four literals:
   $$Y = BC + AC' + AB + BCD$$
   (d) Describe the specifications of A/D converter.
   (e) Determine the conversion time of a 10-bit counter type A/D converter for an input clock frequency of 1.2 MHz.
   (f) Describe how noise margin is used for comparing the characteristics of digital circuits.
   (g) Describing the Refreshing operation in Dynamic RAM cell.
   (h) Compare CMOS with other logic families based on rise time and fall time.
   (i) Explain the applications of open collector TTL.
   (j) Determine the resolution of a 10-bit A/D converter having a full scale analog input voltage of 5V. (10×1=10)

Section-A

2. (a) With the use of maps, find the simplest form of the functions $F_1 = f.g$ and $F_2 = f + g$, where $f = wxy' + y'z + w'yz' + x'yz'$ and $g = (w + x + y' + z')(x' + y' + z)(w' + y + z')$ (5)
   (b) Design a combinational circuit using a ROM. The circuit accepts a 3-bit number and generates an output binary number equal to raised to power three of the input binary number. (5)
3. (a) Design a combinational circuit that generates the 9's complement of a BCD number. (5)
   (b) Describe Dual-slope type A/D converter. Derive the expression for time taken by this converter and compare it with other converters. (5)
4. (a) Construct a MOD-12 Ripple counter using J-K flip-flops. (5)
   (b) Design a universal shift register having serial inputs, parallel inputs, and complement facilities. (5)

Section –B

5. (a) Describe the working of CMOS NAND gate. What should be done with unused CMOS gates? What are the precautions in handling CMOS devices? (5)
   (b) Derive the PLA program table that squares a 3-bit number. Minimize the number of product terms. (5)
6. (a) Describe Tristate logic and explain its applications. (5)
   (b) Explain the reading and writing operation in Bipolar RAM cell. (5)
7. Describe the following:
   a. FPGA
   b. Emitter coupled logic
   c. Interfacing of TTL and ECL (4, 3, 3)

x-x-x

Consider schedule S with transaction ... locking protocol (4 m

Exam Code: 915
Sub. Code: 6836

1125

B.E./B.E. MBA (Computer Science and Engineering) Third Semester

EC-316: Digital Electronics (OLD)

Time allowed: 3 Hours

Max. Marks: 50

NOTE: *Attempt five questions in all, including Question No. I which is compulsory and selecting atleast two questions from each Part.*

x-x-x

Q1. Answer in brief: (10)

(a) When does a TTL circuit act as a current sink and source?
(b) Which are the fastest and the slowest logic family? Discuss the reasons.
(c) What do you mean by bubbled OR gate & it is equivalent to which gate?
(d) How can a NOR gate can be used as an inverter?
(e) What is a parity bit? Discuss one application of it.
(f) What do you mean by toggling?
(g) What is the main difference a gated latch & edge triggered flip-flop?
(h) What are buffer registers?
(i) What do mean by the length of sequence and the pulse train generator?
(j) What type of programs are not subject to change & in which memory they are stored?

PART-A

Q2. Design a synchronous BCD/mod-10 counter using J-K flip flop? (10)

Q3. (a) How many gate inputs are required to realise the following expressions- (5)

$f_1 = ABC + A\bar{B}CD + E\bar{F} + AD$

$f_2 = A(B + C + \bar{D})(\bar{B} + C + \bar{E})(A + \bar{B} + C + E)$

(b) Use Karnaugh map to find the minimum-cost SOP and POS expressions for the function $f_1 = \overline{x_1}\ \overline{x_3}\ \overline{x_4} + x_3\ x_4 + \overline{x_1}\ \overline{x_2}\ x_4 + x_1\ x_2\ \overline{x_3}\ x_4$ assuming that there are don't cares defined as $D = \sum(9,12,14)$. (3)

(c) The message below coded in the 7-bit hamming code is transmitted through a noisy channel. Decode the message assuming that at most a single error occurred in each code word 1001001, 0111001, 1110110, 0011011. (2)

Q4. (a) What are the applications of the shift register? Discuss the data transmission in shift registers. (5)

(b) In a 4-bit DAC, for a digital input of 0100 an output current of 10mA is produced. What will be the output current for a digital input of 1011. (3)

(c) Use a 4×1 MUX to implement the logic function $F(A, B, C) = \sum m(1,2,4,7)$. (2)

PART-B

Q5. (a) Define the following terms- (5)

Fan-in
Fan-out
Noise Margin
Power Dissipation
Transmission gate

(b) Compare TTL, ECL, MOS, CMOS, TIL logic families in terms of propagation delay (ns), power dissipation per gate (mW), noise margin, fan-in, fan-out (5)

Q6. Give the general structure of PLA and PAL. Differentiate between PROM, PLA, PAL logic devices. (10)

Q7. (a) Discuss the applications of CPLD's and FPGA. (5)

(b) Draw the circuit diagram for two input TTL NAND gate along with I/O characteristics. (5)

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(i) Printed Pages : 2 Roll No. .....

CSE
2nd Sem

. Code : 6 6 6 9

. Code : 9 0 6

& Engg.) 2nd Semester

1045

DIGITAL ELECTRONICS AND LOGIC DESIGN

Paper : CS–203

Time Allowed : Three Hours] **[Maximum Marks : 50**

Note :– There are **seven** questions in all. Q. 1 is compulsory. Attempt any **two** questions each from Part A and Part B.

1. (a) Differentiate between an analog and a digital signal.
   (b) Explain the cut off and saturation region of a bipolar transistor.
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2. Give a classification of the digital IC families. Explain the evolution process of the digital logic families. What are the characteristics of digital ICs ? Explain them. 10

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Write a C Program to compare two files, printing the

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PART–B

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21/8/2016

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i) Questions : 7 Sub. Code : 6 6 7 7

Exam. Code : 0 9 0 6

B.Engg. 1st Year (2nd Semester)

1046

(Computer Science and Engineering)-DIGITAL ELECTRONICS AND LOGIC DESIGN

Paper–CS-203

Time Allowed : Three Hours] **[Maximum Marks : 50**

Note : Attempt any **five** questions out of **seven** questions selecting two from each Part. Each question carries 10 marks. Question No. **1** is compulsory. It contains 10 questions of 1 mark each.

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(b) Differentiate between TTL and a DTL gate.

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Exam.Code:915
Sub. Code: 6803

1075

B.E./B.E.M.B.A. (Computer Science and Engineering) Third Semester

EC-316: Digital Electronics

Time allowed: 3 Hours

Max. Marks: 50

NOTE: *Attempt five questions in all, including Question No. 1 which is compulsory and selecting two questions from each Section.*

x-x-x

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x-x-x

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Exam Code: 915
Sub. Code: 6836

1125

B.E./B.E. MBA (Computer Science and Engineering) Third Semester

EC-316: Digital Electronics (OLD)

Time allowed: 3 Hours

Max. Marks: 50

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