UNIVERSITY OF
TEXAS
ARLINGTON

CSE 2312: Computer Organization & Assembly Language Programming
Summer 2015

Homework #3

Student Name: _____

Student ID: _____

Directions: Answer the questions on the following pages. Show all applicable steps for any problems requiring the use of formulas or calculations. Submit your completed assignment electronically as a single PDF document with this completed coversheet as the first page and your name written at the top of all additional pages. You may also submit the document in person before the deadline, in which case this coversheet must be completed and stapled to your solution pages.

1. Consider the following instructions implemented on the simplified MIPS processor described in figure 4.2 of the textbook...

```
Instruction 1:          and rd, rs, rt
Instruction 2:          lw rt, rs
Instruction 3:          ori rt, rs
Instruction 4:          bne rs, rt
```

What would be the value of the following control lines for the above instructions (0 = false, 1 = true, x = don't care)?

RegWrite	MemRead	ALUMux	MemWrite	ALUop	RegMux	Branch
(1 bit)	(1 bit)	(1 bit)	(1 bit)	(4 bits)	(1 bit)	(1 bit)

2. Suppose the logic blocks in a processor have the following latencies...

Instruction fetch	Register read	ALU operation	Data access	Register write
200ps	100ps	120ps	300ps	150ps

a) In a single cycle, non-pipelined processor, what is the minimum time between instructions for an application executing only R-type instructions?

b) In a single cycle, non-pipelined processor, what is the minimum time between instructions for an application executing R, I, and J-type instructions?

c) If the logic blocks above are each implemented as individual pipeline stages, what would be the minimum time between instructions for this pipelined CPU if hazards are ignored?

3. Consider the following instruction fetched by the MIPS processor as described in figure 4.24 of the textbook...

```
10101100011000100000000000010100
```

Assume the data memory is all zeros and the processor's registers have the following values at the beginning of the cycle in which the instruction above is fetched:

r0	r1	r2	r3	r4	r5	r6	r8	r12	r31
0	-1	2	-3	-4	10	6	8	2	-16

a) What would the outputs of the sign-extend and the jump “shift left 2” unit be for this instruction?

b) What are the values of the ALU control unit's inputs for this instruction (ALUOp[1-0] and Instruction[5-0])?

c) What is the new PC address after this instruction is executed?

d) For the ALU and the two add units (PC and Branch), what are their data input values?

4. Consider the following sequence of instructions executed on the basic 5 stage pipeline...

```
add  r3, r2, r1
or   r5, r3, r4
andi r6, r7, r4
add  r7, r2, r1
```

a) Assuming our processor has no forwarding or hazard detection, insert a minimal amount of `nops` to ensure correct execution (do not rearrange the instructions, only insert `nops`).

b) Assuming our processor has no forwarding or hazard detection, rearrange the instructions and add `nops` only if necessary to ensure proper execution. The values contained in the registers after executing your modified code should be equivalent to the unmodified execution.