An Analog Bayesian Classifier Implementation, for Diabetes Disease Detection, based on a Low-Power, Voltage-Mode Gaussian Function Circuit

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***Abstract*—Diabetes is a chronic metabolic disease characterized by elevated levels of blood glucose, which over time can lead to serious damage to the heart, blood vessels, eyes, kidneys, and nerves. The increasing global prevalence of diabetes necessitates developing efficient and rapid diagnostic tools. Early and accurate detection allows for timely intervention and management, which can significantly reduce the risk of long-term complications. This work proposes a novel low-power, low-voltage (0.6V) analog architecture of a Bayesian classifier for diabetes detection. The architecture is based on a new voltage-mode Gaussian function circuit and the Lazzaro Winner-Take-All circuit. The proper operation of the analog classifier is verified using a real-world diabetes dataset. The proposed architecture is realized in IHP 130nm CMOS process and was simulated using the Cadence IC Suite.**

I. Introduction

The current global trends indicate a growing demand for advanced medical diagnostic tools that implement machine learning techniques, particularly in the field of real-time health monitoring.

Diabetes, as one of the most prevalent chronic conditions, requires innovative solutions for early detection and continuous monitoring. The integration of analog VLSI circuits in medical devices presents a promising approach to achieving low-power, real-time processing capabilities, essential for effective diabetes management.

The remainder of this paper is organized as follows. Section II provides an overview of Diabetes, as well as the Bayesian classifier on a theoretical level. Section III describes the proposed analog architecture for the Bayesian classifier, while Section IV presents the behavior of the circuit using a real-world diabetes dataset. Finally, Section V concludes the paper with a summary of the key findings.

II. Background

A. Diabetes Mellitus

Diabetes mellitus is a chronic endocrine disorder characterized by persistently high levels of blood glucose [1]. The condition stems from one of two primary issues: either the pancreas does not produce a sufficient amount of the hormone insulin, or the body's cells cannot effectively use the insulin that is produced.

The onset of diabetes is often indicated by symptoms including excessive thirst (polydipsia), frequent urination (polyuria), and increased hunger (polyphagia). If the disease is left unmanaged, it can lead to severe health complications, including damage to the cardiovascular system, eyes, kidneys, and nerves. The global health impact is significant, with poorly controlled diabetes contributing to millions of deaths each year, underscoring the critical need for timely detection and management.

B. Bayesian Model

A Naive Bayes classifier applies Bayes' theorem assuming feature independence [2]. Using Bayes' rule, the posterior probability of class C_k given input $\mathbf{X}$ is

$$p(C_k \mid \mathbf{X}) \;=\; \frac{p(C_k)\, p(\mathbf{X} \mid C_k)}{p(\mathbf{X})}. \tag{1}$$

Here, $p(C_k)$ is the class prior, $p(\mathbf{X})$ is the evidence, and $p(\mathbf{X} \mid C_k)$ is the class-conditional likelihood. Under a Gaussian PDF with a diagonal covariance (independent features), the likelihood factorizes as

$$p(\mathbf{X} \mid C_k) \;=\; \prod_{n=1}^{N} \frac{1}{\sqrt{(2\pi)\,\sigma_{kn}^2}}\, \exp\!\left(-\frac{1}{2}\,\frac{(x_n-\mu_{kn})^2}{\sigma_{kn}^2}\right), \tag{2}$$

where N is the number of features, and μ_{kn}, σ_{kn}^2 are the mean and variance of the n-th feature for class k.

Since $p(\mathbf{X})$ is common across classes, the decision reduces to

$$y = \underset{k\in[1,K]}{\arg\max}\{p(C_k \mid \mathbf{X})\} = \underset{k\in[1,K]}{\arg\max}\{p(C_k)p(\mathbf{X} \mid C_k)\}. \tag{3}$$

III. Proposed Architecture

We now present the proposed analog architecture that implements the Bayesian classifier based on the mathematical analysis previously discussed. The primary building block required for a Gaussian Bayesian Model is a circuit that can generate the Gaussian function. Such analog circuits are commonly known as 'Bump' circuits. In this work, we introduce a novel voltage-mode Bump circuit which uses a Lazzaro Winner-take-All (WTA) neuron as a basic building block.

The proposed Bump circuit is depicted in Fig. 1. It consists of a symmetric current correlator [3], a differential difference used to handle the input voltages as well as a cascoded current mirror for circuit biasing.

The design allows for the electronic tuning of all characteristics of a Gaussian function. The mean value is controlled by the voltage parameter V_{REF}, the variance by the voltage parameter V_C and the height by the bias current I_{bias}. All transistors operate in the sub-threshold region with power supply rails set to $V_{DD} = 0.3V$ and $V_{SS} = -0.3V$. The corresponding

characteristic curves and transistor dimensions are available in Figs. 2 and 3 and Table I, respectively.

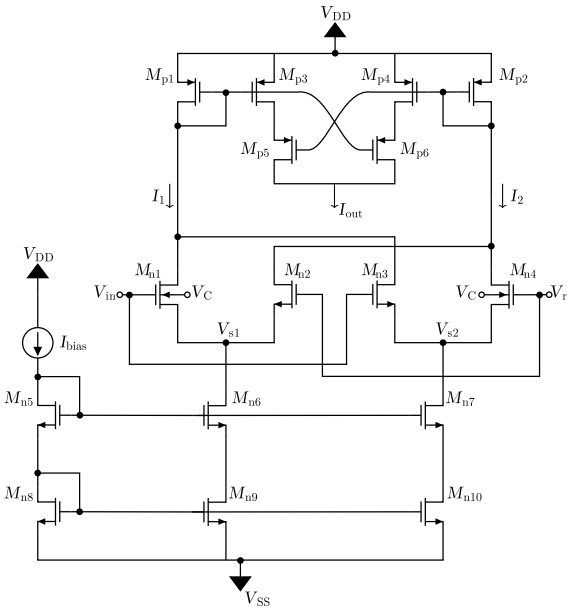

Fig. 1. Proposed Bump circuit architecture.

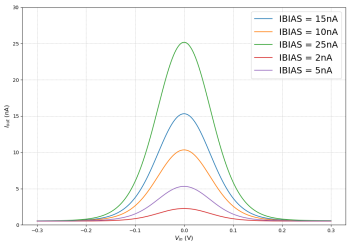

Fig. 2. Bump circuit characteristics for different values of I_{bias}.

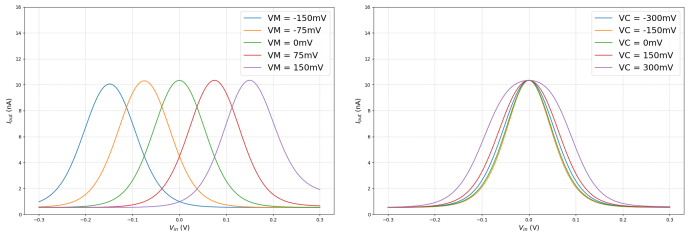

Fig. 3. Bump circuit characteristics for different values of V_{ref} (left) and V_C (right).

TABLE I
MOS TRANSISTORS' DIMENSIONS (FIG. 1).

Block	W/L (μm/μm)	Current Correlator	W/L (μm/μm)
M_{n1}-M_{n4}	1.2/1.2	M_{p1}-M_{p6}	2.4/0.2
M_{n5}-M_{n10}	0.6/1.8	-	-

The mathematical foundation of the Gaussian Bayes model is a multivariate Gaussian Probability Density Function (PDF). This is constructed by multiplying together univariate Gaussian PDFs. In hardware, this multiplication is achieved by connecting two or more "Bump" circuits in a cascaded fashion. The connection is made by feeding the output current of one Bump circuit into the bias current input of the next in the chain. The initial bias current I_{bias} supplied to the first circuit represents the prior probability, $p(C_k)$, of the corresponding class.

The second basic building block of the analog Bayesian classifier is the Winner-Take-All (WTA) circuit, which is responsible for performing the argmax operator. Given a set of N input signals, the WTA circuit identifies the single maximum value among them and produces a non-zero output (the "winner") only on that channel, while all other outputs remain zero. This selective behavior is achieved by operating all transistors in the sub-threshold region, with their dimensions set to W/L = 0.4µm/1.6µm. Based on Equation (3) and utilizing the aforementioned Bump circuits and the WTA, the complete proposed classifier is realized, as shown in Fig. 5.

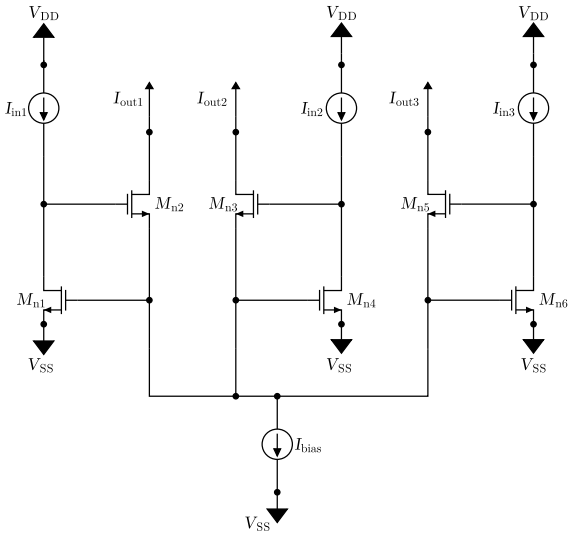

Fig. 4. Lazzaro Winner-Take-All Circuit Architecture.

IV. APPLICATION EXAMPLE AND SIMULATION RESULTS

To validate the performance of the proposed Bayesian classifier, we apply it to a practical, real-world diabetes detection task. The classifier architecture was designed using an IHP 130nm CMOS process and simulated within the Cadence IC suite. The entire circuit operates on a low-voltage supply of $V_{DD} = -V_{SS} = 0.3V$.

The validation utilizes a multiclass diabetes dataset sourced from Kaggle [4]. This dataset provides eleven key biomarkers and physiological measurements per subject, including critical indicators like HbA1c, Body Mass Index (BMI), and cholesterol profiles. Each subject is categorized as Non-Diabetic, Diabetic, or Predict-Diabetic. These features serve as direct inputs to the classifier, and the statistical parameters of the model—the mean, variance, and prior probabilities for each class—are calculated directly from the dataset.

To benchmark the hardware's effectiveness, its performance was compared against a conventional software-based implementation of the same Bayesian algorithm.

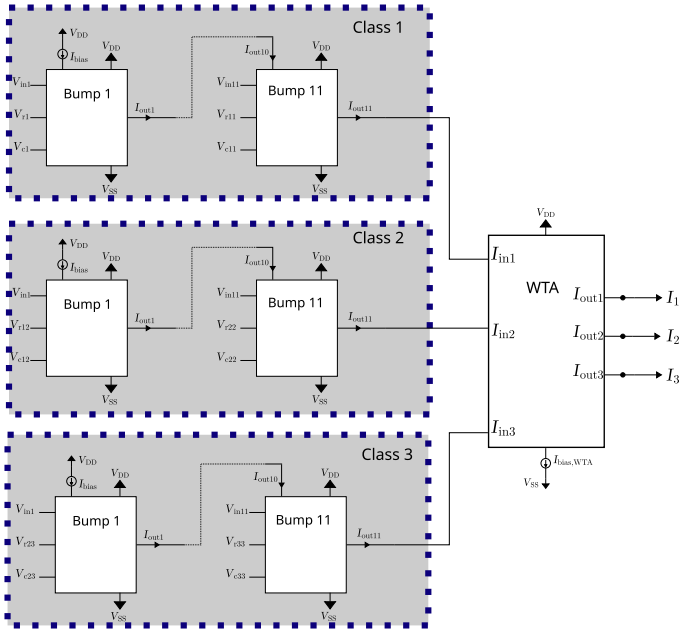

Fig. 5. Proposed Analog Bayesian Classifier Architecture.

The primary metric for this comparison is classification accuracy, which was evaluated across 20 different training test-cases. The results of this comparative analysis are illustrated in Fig. 6 and summarized in Table II. Additionally, Table III provides a summary of the performance characteristics of the proposed architecture, including power supply, power consumption, and classification speed.

TABLE II
ACCURACY RESULTS (OVER 20 ITERATIONS).

Method	Best	Worst	Mean	Std.
Software	0.9875	0.8750	0.9331	0.0323
Proposed	0.8875	0.7500	0.7950	0.0354

TABLE III
PERFORMANCE SUMMARY

Technology	Power Supply	Power Consumption	Classification speed
130nm	0.6V	114nW	20K $\frac{\text{classifications}}{\text{second}}$

V. CONCLUSION

This paper presented the design and validation of an innovative analog Bayesian classifier, demonstrating a low-power hardware solution for on-chip diabetes detection. The core of the architecture combines a new voltage-mode Bump circuit for realizing the Gaussian function with a Lazzaro Winner-Take-All circuit for final class selection. This classifier serves as a proof-of-concept for developing more sophisticated, fully integrated diagnostic systems suitable for wearable health monitoring.

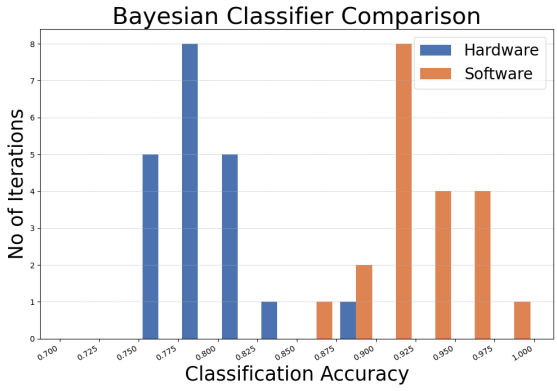

Fig. 6. Classification accuracy comparison between the proposed analog Bayesian classifier and a software-based implementation across 20 test cases.

Simulations showed the architecture achieved a mean classification accuracy of 79.5% on a real-world dataset. While lower than software-based implementations, this performance reflects a deliberate trade-off in favor of ultra-low power consumption (114nW), confirming that analog computing is a viable pathway for creating efficient, intelligent medical devices.

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