الكلية العالمية للهندسة والتكنولوجيا

GLOBAL COLLEGE OF ENGINEERING AND TECHNOLOGY

In partnership with the University of the West of England - UK

MODULAR PROGRAMME

COURSEWORK ASSESSMENT SPECIFICATION

Module Details

Module Code **UFMFE8-30-2**	**Run** Feb 2023	**Module Title** **Digital Design**
Module Leader Irfan Memon	**Module Coordinator** Dr Irfan Memon	**Module Tutors** Irfan Memon
Component and Element Number Component B		**Weighting:** 75%
Element Description Group design, report & demonstration		**Total Assignment time** 24 hrs

Dates

Date Issued to Students TBC	**Date to be Returned to Students** TBC
Submission Place **Online through Moodle +Hardcopy submission in Robotics Lab**	**Submission Date** 12/05/2023
	Submission Time 16.00

Deliverables

These are clearly provided in Instructions to candidate and brief

Module Leader Signature

Dr Irfan Memon

Digital Design – UFMFE8-30-2

Group design, report, & demonstration

Instruction to candidates

1. You are required to work in a group of three and submit one final report including the full description of the tasks completed, complete VHDL code and simulation results.
2. The project contributes 75% of the module.
3. All group members are expected to contribute to the group project and in your report highlight the contribution of each person.
4. The last date to submit your report is 12/05/2023.
5. The presentation schedule will be shared on Moodle.
6. It is your responsibility to complete your project on time **and DO NOT WAIT till the last date of the submission**.
7. There will question and answer session for each student during the demonstration.

Table: Marking Criteria

S No	Task	Marks
1	Project Completion + Report	75
2	Demonstration / Presentation (10 Minutes)	25
3	Total Marks allocated	100

Late submissions policy

5- days grace time: students are allowed to submit their CW up to five days from the deadline (no form is required). Submissions made after the grace period will not be accepted. Find more information at this link.

Good Academic Practice and Assessment Offenses:

GCET is fully committed to ensuring that students follow 'good academic practice' in the writing/producing and submission of all types of assessments to ensure honesty and integrity in academic practice. Every student is expected to act with integrity in relation to the production and representation of academic work and in acknowledging the contributions of others in their work.

Engaging in any academic breach constituting an assessment offense such as collusion, plagiarism, Fabrication or Misrepresentation, contractual cheating. will be investigated and could lead to penalties under the UWE Assessment Offences Policy.

Task 1

In Computer systems, random access memory (RAM) plays a vital role in storage and retrieval of information. Single port RAM allows only one access at a time while the dual port RAM allows multiple accesses at the same times.

Figure 1 **128×8 RAM module**

Figure 1 illustrates the 128×8 single port RAM in 'Data_In' is 8 bit input data to be written during the write operation, 'Address' is 6bit memory address from where the data is read or written. 'WE' is a single bit write enable and it is enabled during the writing operation. 'Clk' is a clock signal. 'Data_Out' is the 8-bit output data read out from the provided input address.

To better understand physical memory in the computing system, you are required to develop and test static 128×8 RAM module by implement single port 128×8 RAM module using VHDL with synchronous read/write operations. Maximum of 70% marks will be awarded for the design and implementations. The remaining 30% marks will be awarded on the simulation and discussion of results.

[20 Marks]

Task 2

In this task you are required to design an electronic dice game as shown as block diagram in the Figure 2 in which two counters are employed to simulate the roll of the dice. Each counter counts in the sequence 1,2,3,4,5,6,1,2, …

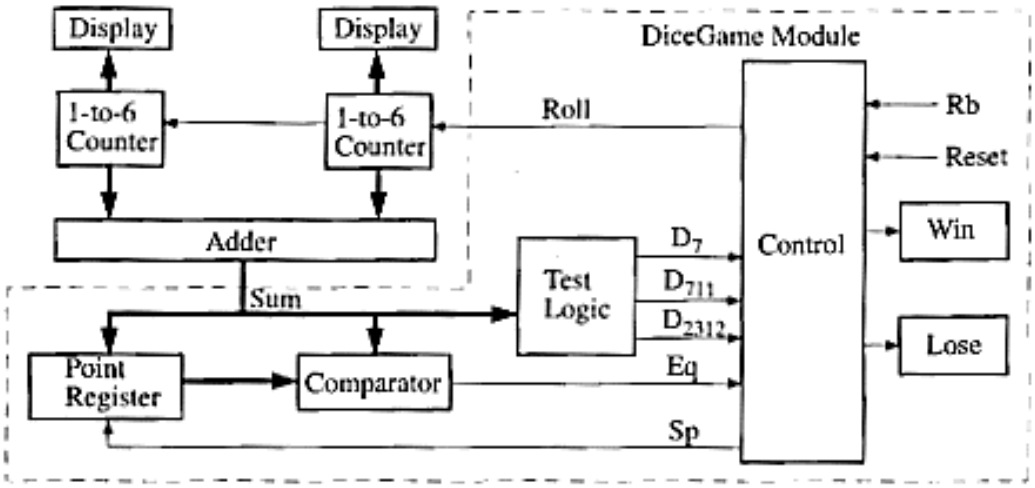

Figure 2 Block diagram for Dice game

So, after the dice 'roll', the sum of values in the two counters will be in the range 2 through 12. Consider the following as the game rules:

1. The player wins if the sum is 7 or 11 after the first dice roll. However, if the sum is 2,3, or 12 then the player losses the game. Else, the sum obtained on the first roll is referred to as a point in the point register, as the player must roll the dice again until the result of the game is decided.
2. On the second or subsequent roll dice, the player wins if and only if the sum is equal to the point value stored in the point register and loses when sum is 7. Otherwise, the player must roll again until the game result is decided.

To perform this task you are required to design algorithmic state machine (ASM) for the above described dice game and then implement it in VHDL. Please note, the maximum of 70% marks will be awarded for the design and implementations. The remaining 30% marks will be awarded on the simulation and discussion of results.

[40 Marks]

Task 3

Greatest common divisor (GCD) of two nonzero integers is the largest positive integer that divides each of these integers with a zero remainder. Figure 3 shows a C-program segment to implement GCD calculator using Euclidean algorithm.

```
1       tempA = A;
2       tempB = B;
3               while (tempA != tempB)
4               {
5                       if (tempA < tempB)
6                           tempB = tempB-tempA;
7                       else
8                           tempA = tempA-tempB;
9                }
10      gcd = tempA;
```

Figure 3 **C Program segment for GCD calculator using Euclidean algorithm.**

In this task you are required to understand Euclidean algorithm to compute GCD and design a digital logic circuit in VHDL that computes the GCD of two N-bit unsigned integers for instance N can be taken equals to 8. Prior to that make sure you understand the basic algorithm for calculating the GCD of two numbers. A suitable datapath for the GCD calculator is shown in Figure 4.

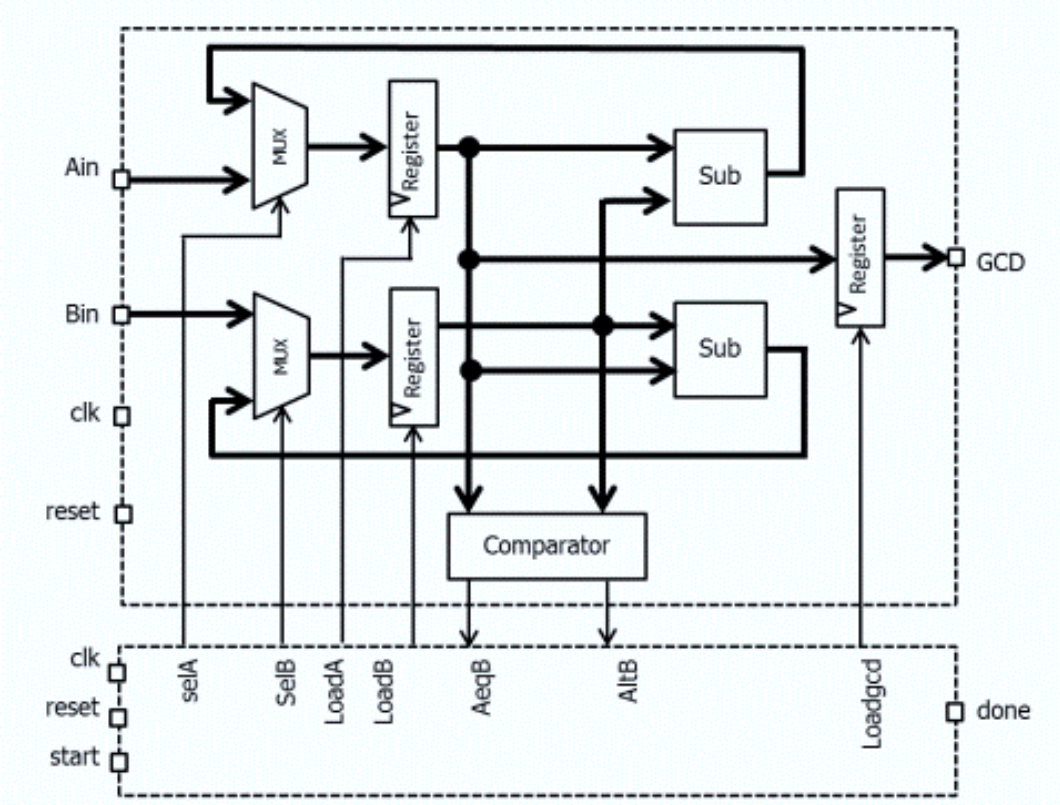

Figure 4 Illustration of GCD calculator data-path and control unit

When the two N-bit unsigned integers are set as the X and Y inputs, then the "start" signal is enabled to compute their GCD. Note that once GCD computation has started, a new calculation cannot be started until the "done" signal goes high or the system is reset by pulling up the Reset signal.

Maximum of 70% marks will be awarded for the design and implementations. The remaining 30% marks will be awarded on the simulation and discussion of results.

[40 Marks]

Verification

The verification of a design will normally take about 80% of the total development time. You should consider exactly what you are verifying. Implement a verification plan... what values will the inputs to the system be? For how long? What are the expected outputs? Consider the 'corner cases'.

Individual Marks Calculations

$$i = g + \left(g * \frac{a - e}{100}\right)$$

$Where$
i is the individual mark,
g is Group marks,
a is agreed percentage contribution.
e is expected percentage contribution.

Considerations for Document Quality

Your report is due on the **12th of May 2023**. The report may not exceed 10 pages.

References

[1] John D. Carpinelli, *Computer Systems Organization and Architecture*. Addison-Wesley Longman Publishing, Boston, USA, 2000