

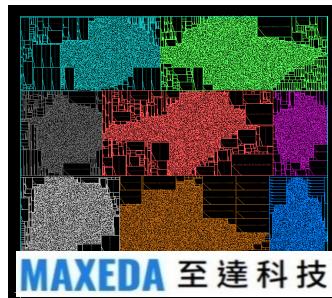
NTU EDA Lab

電子設計自動化

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National Taiwan University
7/30/2021



美中對抗 (半導體)



天下雜誌 台積電向美靠攏，美國最致命的一擊，分析師：華為氣數已盡，台積電可全身而退
編譯 張毓思 2020-05-19

經濟日報 美方軟硬夾擊 EDA成壓垮華為最後一根稻草？
2020-08-19 01:53 經濟日報 記者張家瑜

失去它華為就癱瘓！帶你認識美國的制裁王牌：EDA 產業
anue 鉅亨 斬向華為的屠龍刀「EDA」產業

TechOrange 2020/05/20
失去它華為就癱瘓！帶你認識美國的制裁王牌：EDA 產業
TECHNEWS 作者 MoneyDJ | 發布日期 2020 年 06 月 10 日

華為避過海思繞道用別家 IC 設計廠？中國政府大買 EDA 軟體
TechNews EDA 美國寡占，中國落差 20 年
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自由時報 2020/12/04 重演台灣半導體之痛！中國挖角美EDA設備大廠高層

EE Times C. Johnson: "**The Best and Brightest Worldwide**"
(4/6/2015): "The best engineering minds on the planet compete each year in the ACM's ISPD design contest, which was won this year by the National Taiwan University." 張耀文教授EDA團隊

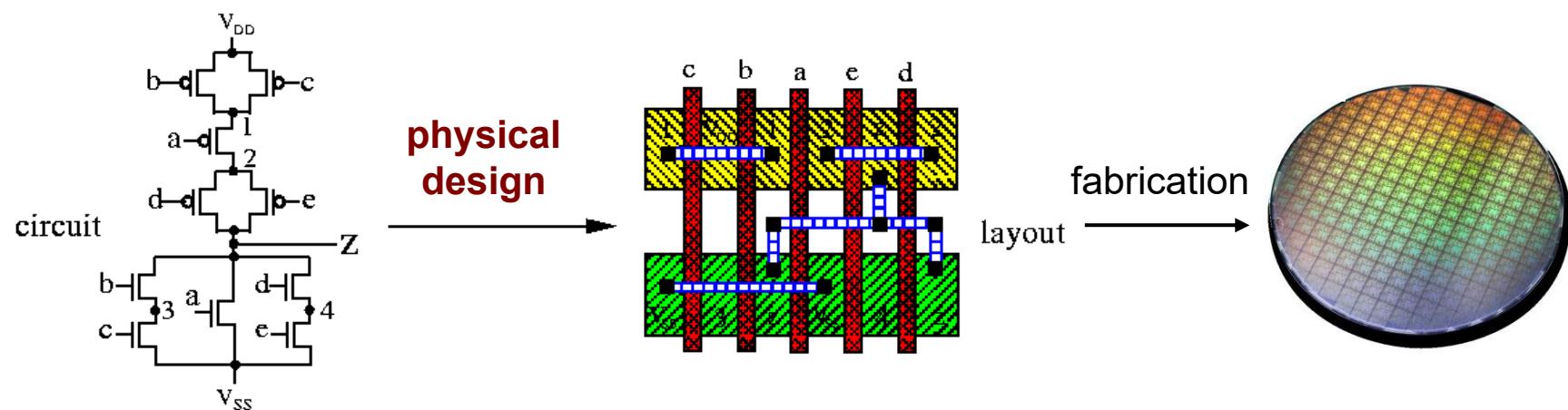
大綱

實驗室概況

業界計畫實例

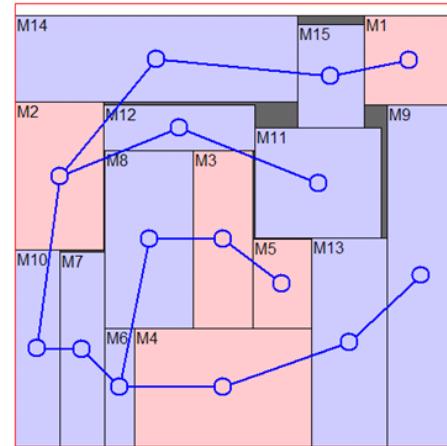
Recent Research Focuses

- Physical design for nanometer IC's
- More Moore: Design for manufacturability
- More than Moore: 2.5D/3D Heterogeneous Integration

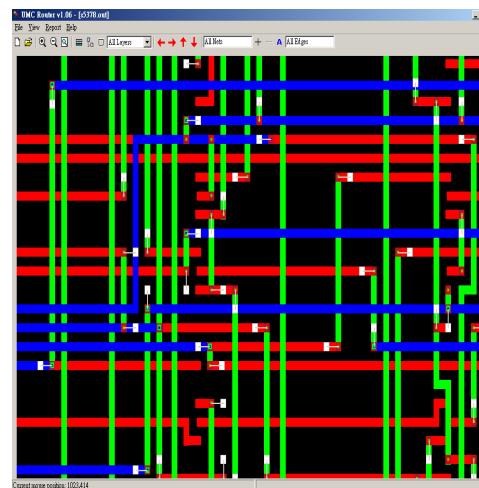
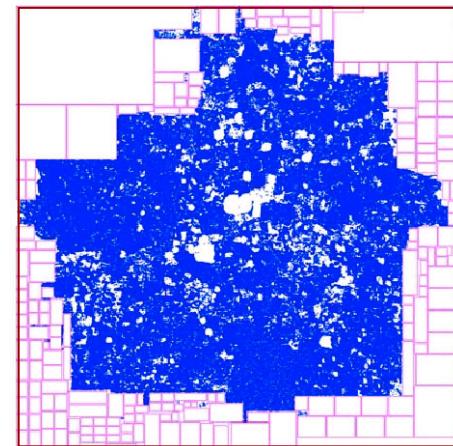


Current Research Topics

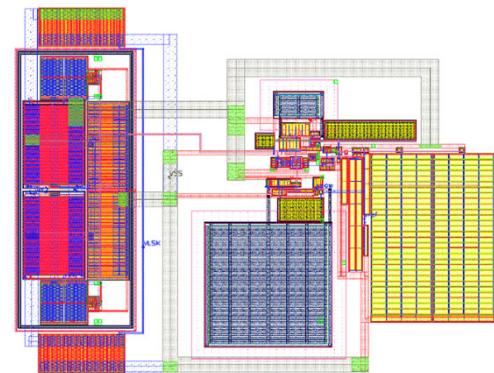
- Physical Design
 - Floorplanning, placement, routing, clock network
- Manufacturability
 - OPC, CMP, DPT/MPT, **EUV**, e-beam, DSA, **nanowire**
- 3D Heterogeneous Integration
 - Flip-chip, **InFO** package, Chip/package/system co-design
- Analog Layout Design



MP-tree based macro placement

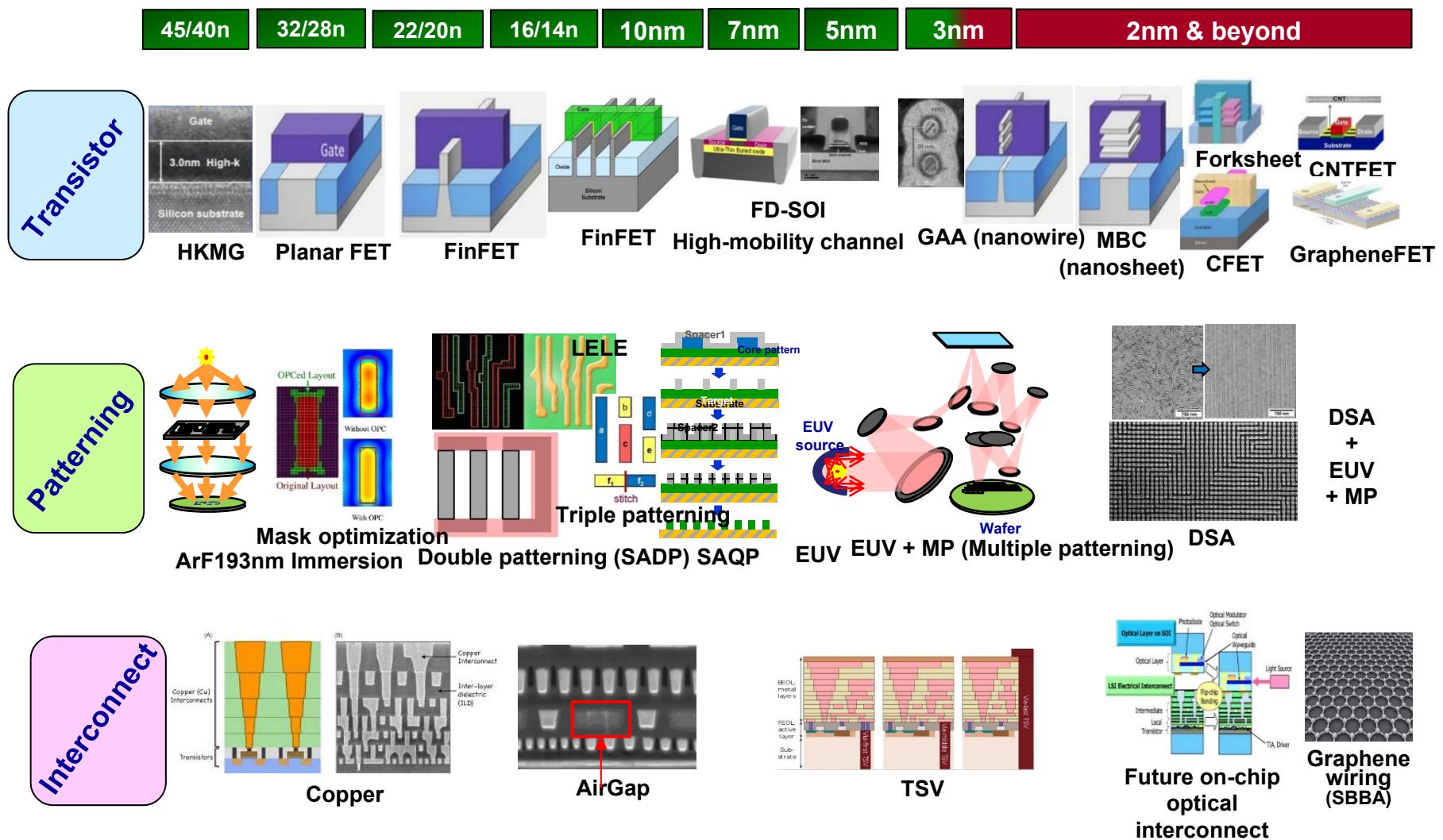


Redundant-via insertion



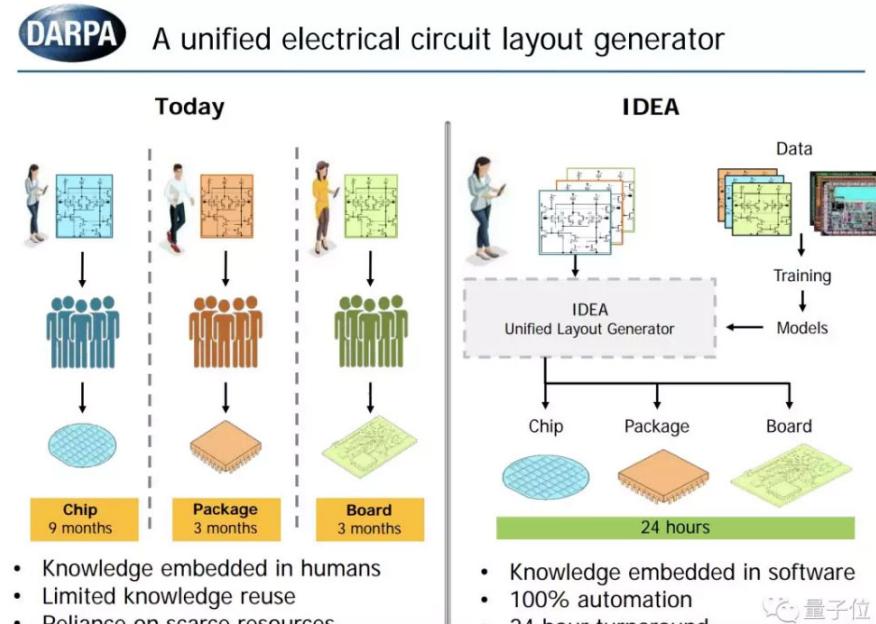
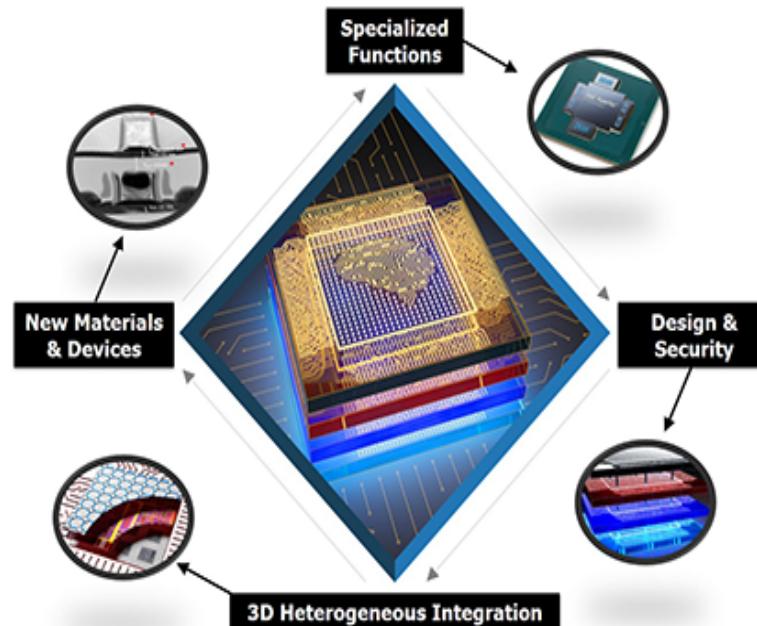
Analog P&R

More Moore Technology Landscape



US DARPA ERI Program on HI & EDA

- US\$1.65B DARPA ERI: **3D Heterogeneous Integration + EDA (IDEA) + Architecture & Materials & Devices**
- Heterogeneous integration provides better economic advantages than technology scaling



IDEA (Intelligent Design of Electronic Assets)

Source: DARPA Electronics Resurgence Initiative (ERI)

HI (InFO Package) for TSMC's Success

- Dr. Morris Chang (2016): InFO is key for TSMC to beat Samsung for Apple's chip orders
 - 財經新報: 《台積電藉 InFO 晶圓級封裝技術 獨拿 A10 處理器產能訂單》

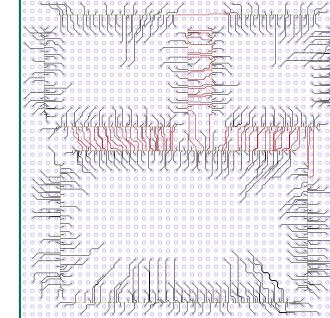
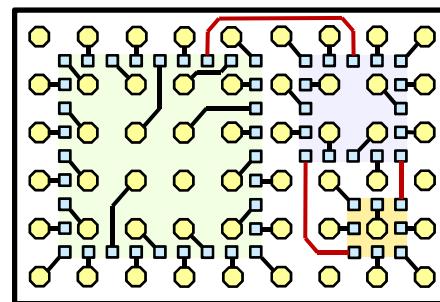
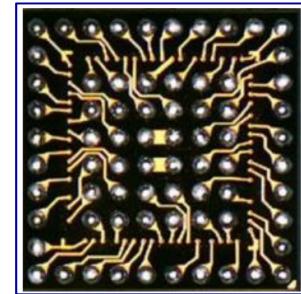
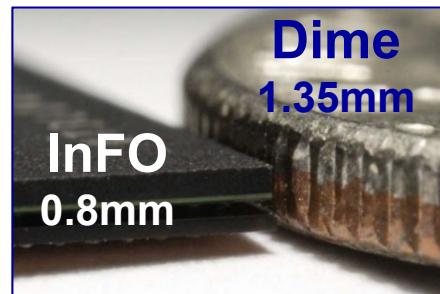
天下雜誌 一個「小媳婦部門」為何能讓台積電擊敗三星、獨吃蘋果？
2018年04月22日

財經新報 台積電藉 InFO 晶圓級封裝技術 獨拿 A10 處理器產能訂單
作者 Atkinson | 發布日期 2016年04月14日

FOCUS TAIWAN

05/30/2020

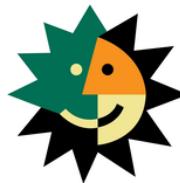
TSMC's IC packaging, testing plant to become operational in mid-2021



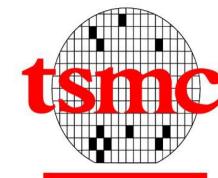
First published InFO package router
[Lin et al., ICCAD'16]
US Patent 9,928,334, 2018
(with AnaGlobe)

Sponsors

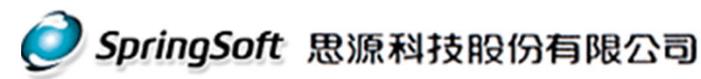
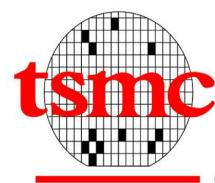
- Current Sponsors (9 projects)



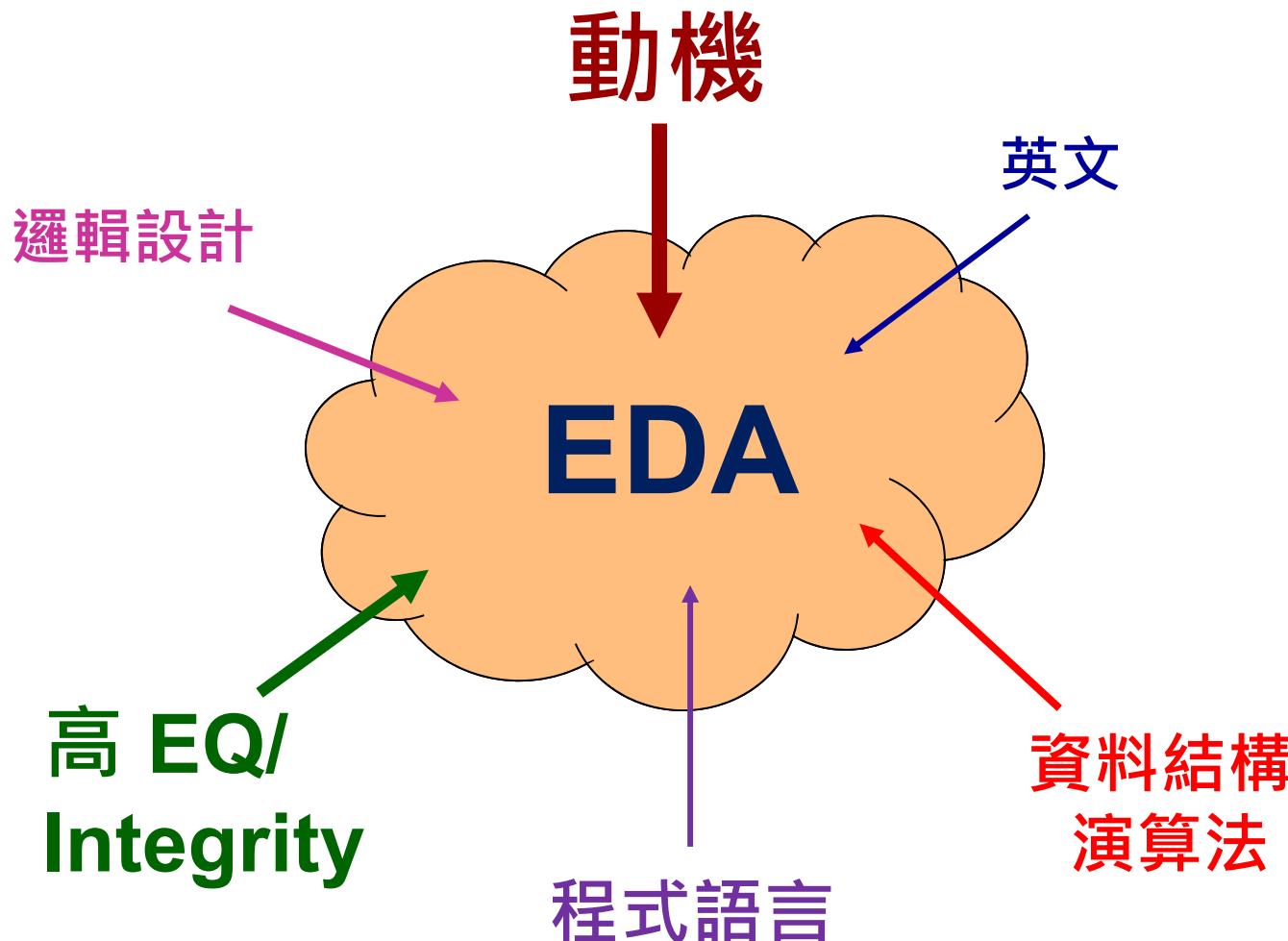
Maxeda



- Past Sponsors

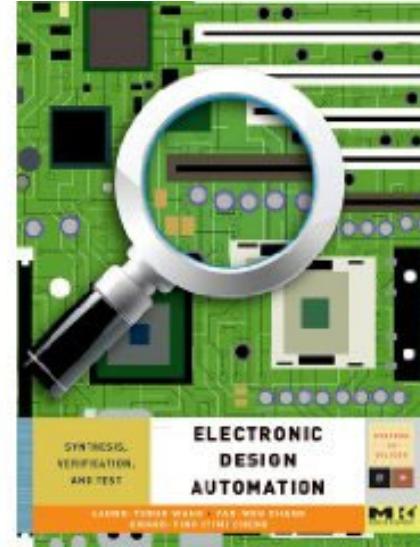


我適合做EDA研究嗎??

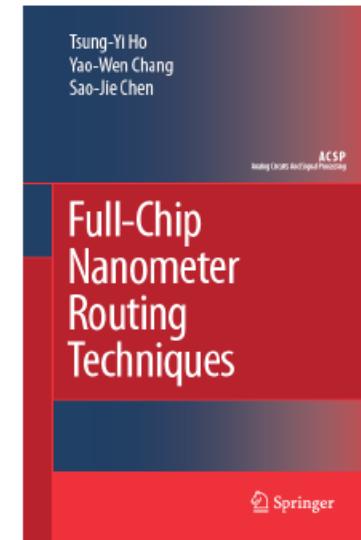


Lab Resources

- Lab members/alumni
- 400+ books
- 30+ servers
- PC and laptop for every student
- Student international travel grants
- Domestic industrial collaboration
- International academic & industrial collaboration (**IBM T. J. Watson Res. Ctr, MIT, Synopsys, CMU, UIUC, UC-Berkeley, UT-Austin, Waseda, etc.**)
- Software: major EDA tools, LEDA, CPLEX, MATLAB, etc.



Edited
EDA
Textbook
(934 pages)



Routing
book

EDA Lab 研究生畢業出路統計

- Total: **110+** 畢業生; Ph.D. (24) + M.S. (86+)
- 學術界 (**9**): 臺大電機 (1), 臺大資訊 (1), 台科大電機(1),
交大電機 (2), 清大資訊 (1), 南華資訊 (1), 成大電機 (1),
中山資訊 (1) (**香港中文大學 1**)
- 創業 (**6**): **Maxeda** (Ph.D.: 2; M.S.: 3), **LinkWish** (1)
- IC設計公司 (**33**): 聯發科 **MediaTek** (**30**)
 - 其他: 瑞昱, 凌揚, 美商**Broadcom**
- 晶圓廠 (**22**): 台積電 **TSMC** (**22**; 3 top-notch program)
- EDA公司 (**24**): **Synopsys** (**18**), **Cadence** (5), ...
- IC設計服務 (**3**): 智原 **Faraday** (**1**), 芯原 **VeriSilicon** (**2**)
- 國外研究所 (**9**): UC-Berkeley (2), Stanford, UT-Austin,
UIUC, Columbia, UCLA, UCSD, UWisc等
- 其他公司 (**8**): **Google** (3), **Apple** (1), **Facebook** (2), etc.
- 政府部門 (**2**): **CIC**, 經濟部

Salary in EDA

BloombergBusiness



Glassdoor: These Are The 15 Highest Paying Companies in America

4/10/2015

12. Cadence Design Systems

- Median Total Compensation: \$145,000
- Median Base Salary: \$130,000
- Industry: Tech

#2 EDA Company

13. Google

- Median Total Compensation: \$143,500
- Median Base Salary: \$116,000
- Industry: Tech

#1 EDA Company

14. Synopsys

- Median Total Compensation: \$143,000
- Median Base Salary: \$123,000
- Industry: Tech

專題型態: 依所需自由選擇



領域初探



國際競賽



業界巡禮



獨立研究

升大三同學: 2/2021申請科技部大學生專題研究計畫!

今年專題生申請:

MIT, Stanford, UC-Berkeley, Princeton, UT-Austin, UCLA,...

2021 CAD Contest @ ICCAD

- Default project: Problem B, C, D, or E of the 2021 IC/CAD Contest at <http://iccad-contest.org/2021/tw/>
- Teamwork is encouraged (1-4 persons)
- Preference: B > (C, D) > E
- Contest Problems

Problem B Routing with Cell Movement Advanced
(Synopsys Taiwan, Corp.)

Problem C GPU-Accelerated Logic Rewriting
(Nvidia Corp.)

Problem D
(domestic) Macro Legalization
(Maxeda Technology Inc.)

Problem E
(domestic) Component Copper Configuration Design
Optimization for PCB Manufacturing Process
(Footprintku Inc.)

2021 CAD Contest Awards

2017/2018:臺大學務處額外獎勵:20 萬; 2019:10+電資 8 萬!!

競賽獎項

國際賽 第一名 (A,B,C題各1隊)	- 每人獲 ICCAD 英文獎牌1面 - 每隊獲獎金5萬元 - 每隊獲補助最多2位學生出國參加 ICCAD 接授頒獎
國際賽 第二名 (A,B,C題各1隊)	- 每人獲 ICCAD 英文獎牌1面 - 每隊獲獎金3萬元 - 每隊獲補助最多2位學生出國參加 ICCAD 接授頒獎
國際賽 第三名 (A,B,C題各1隊)	- 每人獲 ICCAD 英文獎牌1面 - 每隊獲獎金3萬元 - 每隊獲補助最多2位學生出國參加 ICCAD 接授頒獎
國內賽 特優 (A,B,C,D,E題各1隊)	- 每人獲教育部中英文對照獎狀1紙 - A,B,C題 每隊獲獎金2萬5仟元 - D,E題 每隊獲獎金1萬5仟元 - 僅報名國際賽(未報名國內賽)恕無法獲得此獎
國內賽 優等 (A,B,C,D,E題各2隊)	- 每人獲教育部中英文對照獎狀1紙 - A,B,C題 每隊獲獎金2萬元 - D,E題 每隊獲獎金1萬元 - 僅報名國際賽(未報名國內賽)恕無法獲得此獎
國內賽 佳作 (A,B,C,D,E題各3~6隊)	- 每人獲教育部中英文對照獎狀1紙 - 僅報名國際賽(未報名國內賽)恕無法獲得此獎
國內賽 入選 (A,B,C,D,E題各若干隊)	- 每人獲主辦團隊核發中文入選證明1紙 - 僅報名國際賽(未報名國內賽)恕無法獲得入選

You Can Be the Next Winner!!

學術典藏 | 圖書館 | 博物館群 | 課程 | 招生 | 推廣教育 | 行事曆 | 捐款

認識臺大 學術單位 研究發展 行政組織 常見詢問 服務資源

臺大電機團隊獲2019年ACM ISPD國際細部繞線研發競賽第二名

本校電機團隊於電子設計自動化最重要的國際研發競賽再度獲得佳績！今年於美國加州舊金山市舉辦的「國際積體電路實體設計會議」公布為期四個多月的「ISPD初始細部繞線研發競賽」最終結果，由電機系與電子所張耀文教授和電機系大四學生張家銘、張振嘉、劉維凱以及電子所碩士生徐晨皓所共同研發的初始細部繞線器NTUidRoute獲得了第二名的榮耀！
...more



★ 最新消息

校長遴選相關業務精進檢討報告

活動

臺大其他粉絲團

► 活動快報

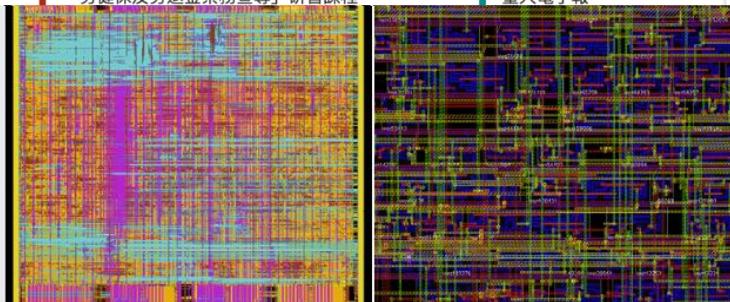
養鶯劇集《白噪音White Noise》

「勞健保及勞退金業務宣導」研習課程

► 校園推廣

NTU Highlights

臺大電子報



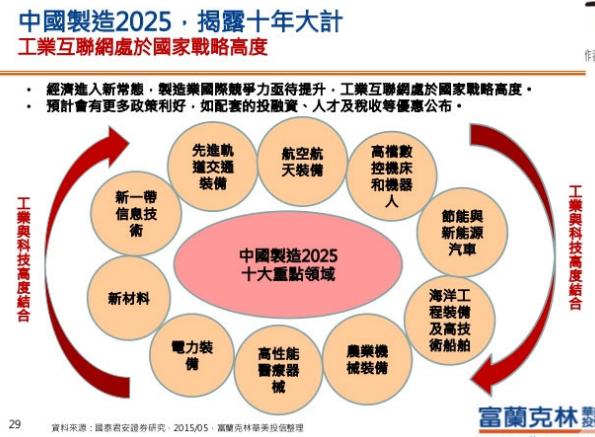
2nd Place at the 2019 ISPD Contest

中國2025製造計畫 vs. 美國電子復興計畫

- 2015: 中國2025製造計畫, 從製造大國成為製造強國 (已改為2035)
 - 2016: 中國高階晶片逾95%依賴進口(2270億美元)
 - 2018: 美國對中國製造2025產品加關稅, 中國淡化中國製造2025宣傳
- 2017: 美國電子復興計畫(ERI), 5年16.5億美元, 重振美國EDA&材料
 - 設計(全自動晶片設計) + 結構(軟體定義的硬體) + 材料與製程(三維晶片)
 - 2019: 台灣 ERI
- 美國國會跨黨跨院1100億美元《Endless Frontier Act 無盡邊疆法案》對抗中國 (5/27/2020)

自由時報
Honest Times News
2018-08-22

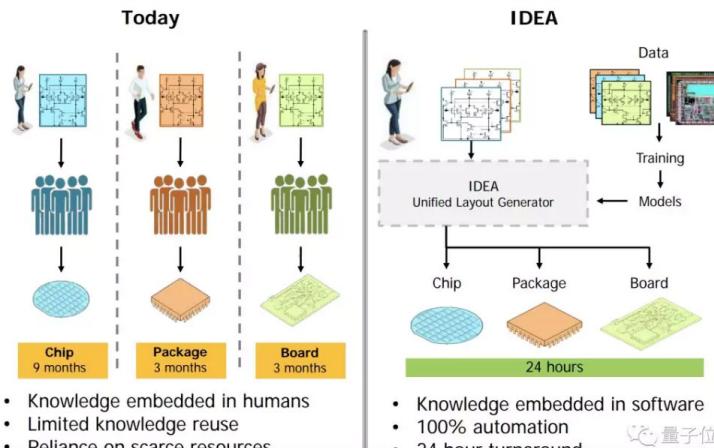
美啟動電子復興 打擊中國半導體野心



TechNews
作者: MoreDJ | 發表日期: 2021年04月13日
半導體將決定美領導地位！拜登：晶片為「基礎建設」



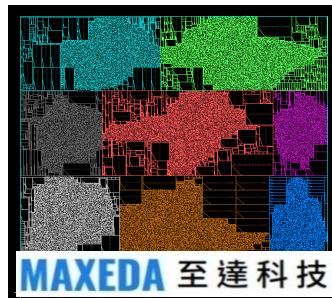
A unified electrical circuit layout generator



ERI 智慧設計: 完全自動的晶片佈局生成器

Y.-W. Chang

美中對抗 (半導體)



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編譯 張毓思 2020-05-19

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鉅亨網編輯江泰傑 2020/05/19

TechOrange 2020/05/20
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TECHNEWS 作者 MoneyDJ | 發布日期 2020 年 06 月 10 日

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TechNews EDA 美國寡占，中國落差 20 年
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Y.-W. Chang

EDA in China

EDA已成为中国集成电路的命门所在！国产EDA究竟如何追赶 ...

<https://www.iczhiku.com> › hotspotDetail › 轉為繁體網頁

2019年9月27日 - 在日前举行的2019中国集成电路设计大会上，国产EDA龙头企业华大九天董事长刘伟平指出，全球前5大EDA公司都是美国企业，总市占率高达95% ...

【人才】芯片人才缺口超30万,南京每年培养全国近1/5毕业生

<https://www.laoyaoba.com> › html › share › news › 轉為繁體網頁

... 报道（记者/小北）5月18日，2019年世界半导体大会半导体才智论坛暨第三届集成电路 ... 新区人才港授牌仪式及集成电路EDA设计暑期学校暨精英挑战赛启动仪式。

国内第一届EDA专业竞赛总决赛在江北新区举办- 壹读

<https://read01.com> › 教育 › 科技

12月1日，“2019年集成电路EDA设计精英挑战赛”总决赛高端论坛暨颁奖典礼在江北 ... 上海科技大学、杭州电子科技大学与南京集成电路产业服务中心(ICisC)承办。



2020/11/25

蘋果 加速晶片自給自足 中企挖美晶片設計軟體商牆角

中國晶片新創正在從美國EDA大廠挖角人才。路透社

據報導，自去年9月以來成立的3家中國晶片新創，正在從全球最大EDA（電子設計自動化）工具廠商新思科技（synopsys）及益華國際電腦科技（cadence）招募人才，這3家中國企業分別為芯華章科技、全芯智造及Hejian Industrial Software。

Taiwan's EDA Dream

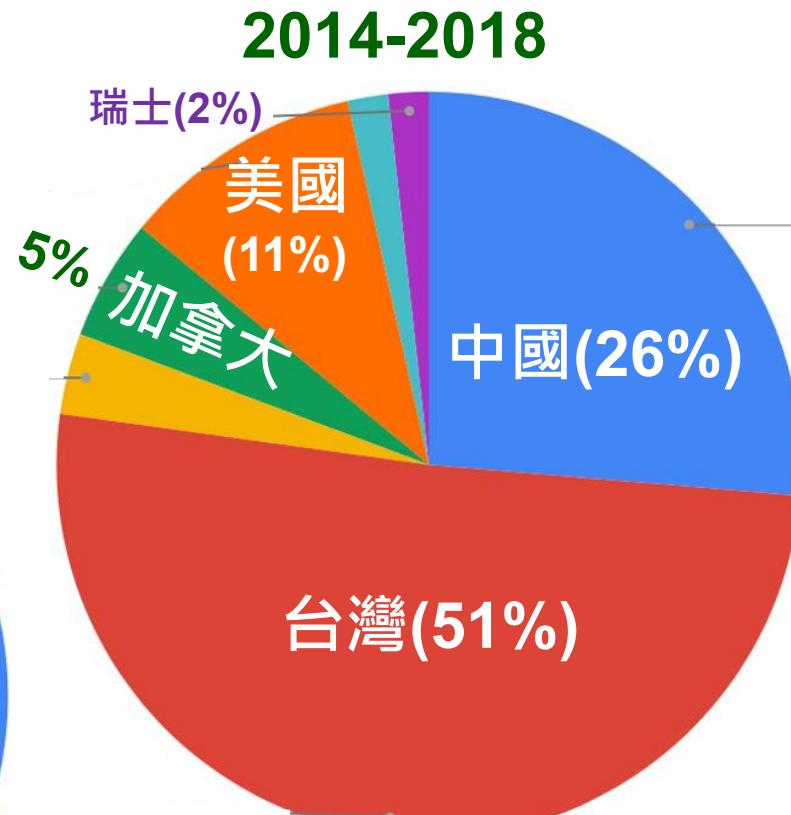
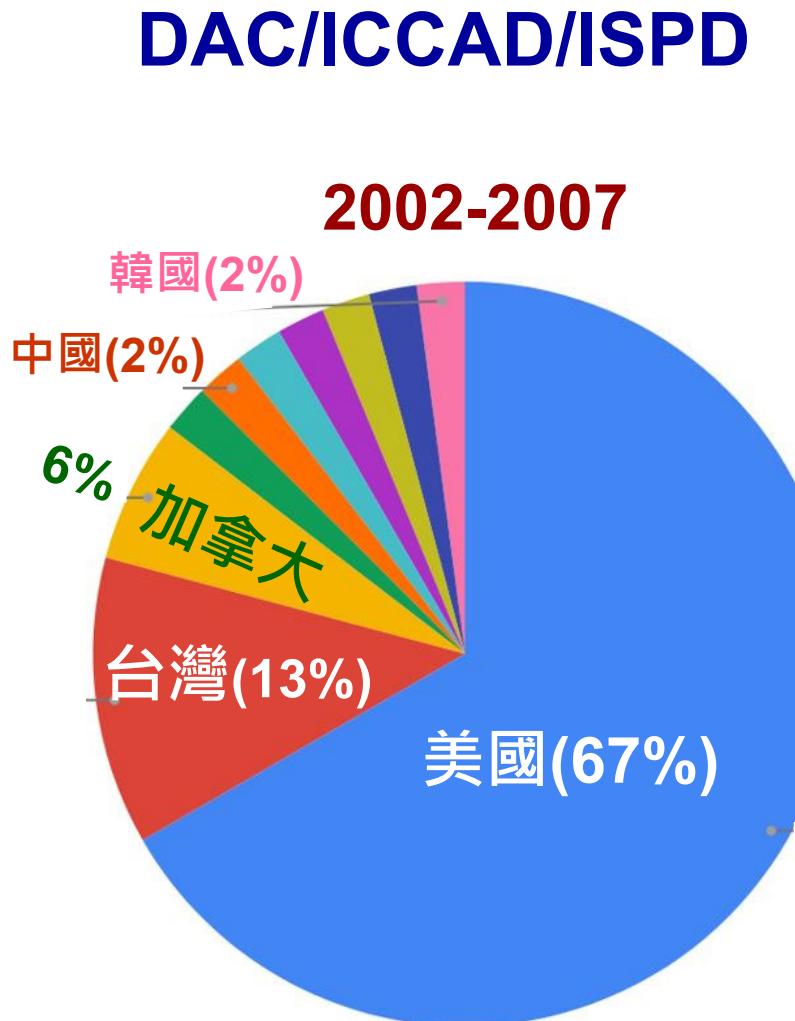
12/2004: “Double DAC/ICCAD publications in 3 years!”

	2002 (147#)	2003 (152)	2004 (163)	2005 (154)	2006 (201)	2007 (153)	2008 (147)	2009 (148)	2010 (148)	2011 (154)	2012 (166)	2013 (150)	2014 (174)	2015 (164)	2016 (152)	2017 (160)	2018 (168)
1st	USA (103)	USA (116)	USA (120)	USA (114)	USA (125)	USA (98)	USA (94)	USA (80)	USA (84)	USA (82)	USA (97)	USA (76)	USA (73)	USA (82)	USA (78)	USA (79)	USA (78)
2nd	Korea Germany (7)	Canada (6)	Korea (10)	Taiwan (8)	Taiwan (12)	Taiwan (12)	Taiwan (15)	Taiwan (15)	Taiwan (15)	Taiwan (19)	Taiwan (18)	Taiwan (20)	China + HK (14)	Germany (14)	China + HK (39)	China + HK (19)	
3rd	Korea Germany (6)	Italy (5)	Germany (5)	China + HK (5)	Canada (8)	Germany (8)	China + HK (10)	China + HK (7)	Korea (10)	Germany (11)	China + HK (10)	Germany (17)	Germany (11)	China + HK (13)	Korea (15)	Germany (18)	
4th	Belgium (5)	Japan Canada Italy (4)	Taiwan Korea France (4)	Korea Canada Germany Spain (4)	China + HK (7)	China + HK (6)	Germany (9)	Germany (6)	China + HK (9)	China + HK (8)	Germany (9)	China + HK (17)	Taiwan (10)	Taiwan (10)	Taiwan (14)	Taiwan (16)	
5th	Switzerland (4)	Korea Germany Israel India (4)	Taiwan Japan (3)	Korea Canada Germany Spain (4)	Germany (5)	Canada (5)	Korea Singapore (4)	Canada (4)	Germany (8)	Korea (7)	Singapore (8)	Switzerland (5)	Korea (7)	Korea (6)	Germany (11)	Korea (11)	
6th	Canada France (3)	Taiwan (3)	Japan (3)	Netherlands (4)	Singapore (4)	Singapore (4)	Singapore (3)	Israel Switzerland (6)	Switzerland (4)	France (4)	Korea (5)	Singapore, Spain, Switzerland (4)	Switzerland (4)	India (10)	Spain (5)		
7th				Israel (3)	Korea (3)	Switzerland (3)	Belgium (2)	Israel Switzerland (4)	Canada (5)	Italy (4)	Singapore (3)	Singapore (4)	UK (3)	Canada Singapore (4)	Switzerland (4)		

EE Times
(5/15/2013)

Taiwan: Microelectronics expertise widens': “Taiwan's success so far has been in large part due to electronic design automation (EDA) expertise, where it has only been outperformed by the U.S. for the last five years.”

全球EDA三大競賽獲勝隊伍統計



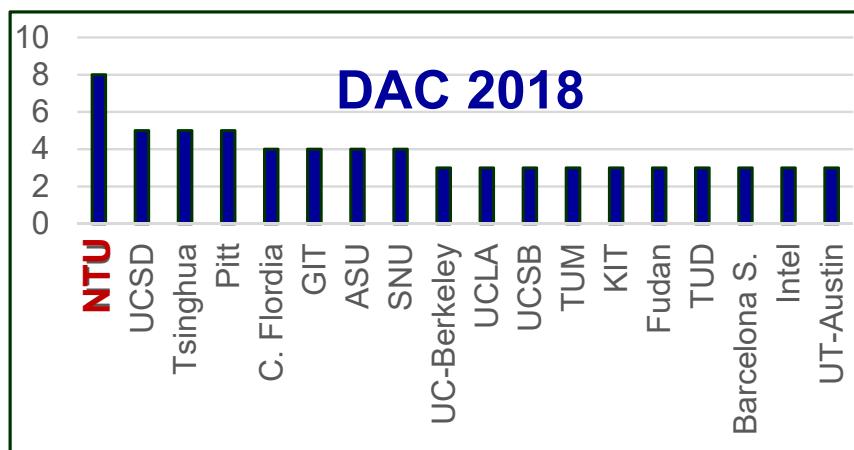
資料來源



DESIGN
AUTOMATION
CONFERENCE
UC San Diego

NTU: World's #1 EDA Record

- NTU ranks **#1** worldwide for DAC+ ICCAD publications every year since 2007 & int'l EDA competitions



EE|Times

C. Johnson: "**The Best and Brightest Worldwide**" (4/6/2015): "The best engineering minds on the planet compete each year in the ACM's ISPD design contest, which was won this year by the National Taiwan University."



The New York Times

Pound for Pound, Taiwan Is the Most Important Place in the World

Its excellence in the computer chip market puts it at the center of the battle for global technological supremacy.



By Ruchir Sharma **Dec. 14, 2020**

Mr. Sharma is the chief global strategist at Morgan Stanley Investment Management and the author of "The Ten Rules of Successful Nations."

Dec. 14, 2020, 9:47 a.m. ET

全球第一的研究紀錄

- **Hardware & Architecture** 領域四萬名學者近五年論文引用數
 - Microsoft Academic Search; 2010—2011 (現無此統計)
- **近30年最頂尖 EDA 會議和期刊 DAC+ICCAD+TCAD 論文數**
 - 102 Hardware & Architecture 會議排名: DAC: #1, ICCAD: #3 (Microsoft Academic Search)
- **ACM/IEEE EDA 研發競賽冠軍數 (6 次) 和獲獎數 (25)**

Top authors in Hardware & Architecture

Rank	Author	Publications	Citations	G-Index	H-Index
1	Yao-wen Chang (張謙文) National Taiwan University	184	1154	27	18
2	Josep Torrellas University of Illinois Urbana Champaign	211	2983	48	31
3	Robert Brayton University of California Berkeley	463	8133	—	—

Taiwan: Microelectronics expertise widens' (5/15/2013): **(Yao-Wen) Chang** is typical at NTU, a microelectronics pioneer in EDA

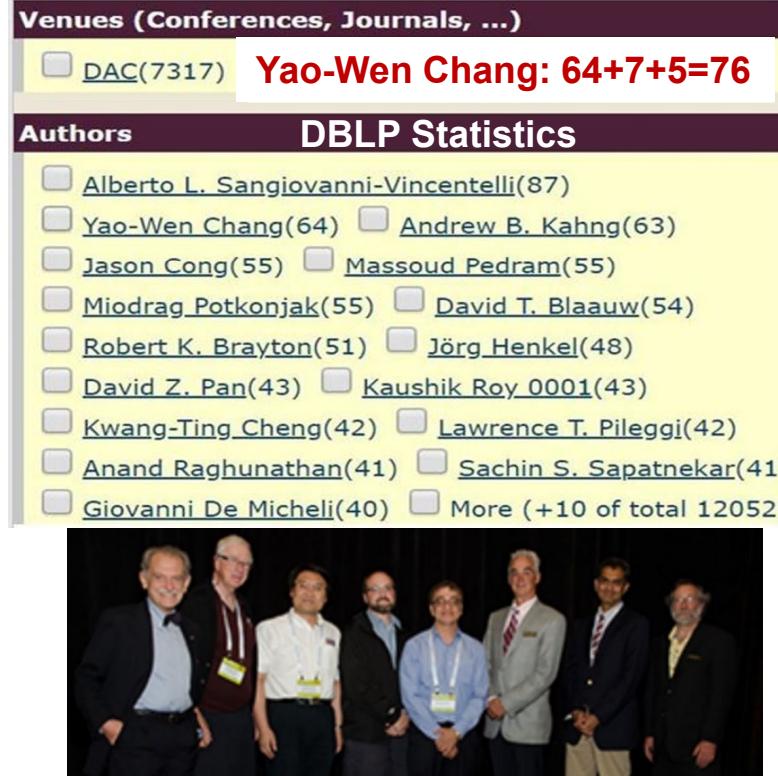


The Best and Brightest Worldwide (4/6/2015): “**The best engineering minds on the planet** compete each year in the ACM's ISPD design contest, which was **won** this year **by** the **National Taiwan University**.”

ISPD: Semiconductors aim for 8-nm nodes (4/6/2012): “**The winner was team from National Taiwan University led by Professor Yao-Wen Chang.**”

最頂尖會議DAC紀錄: 4個 50th DAC研究貢獻獎

- 58年史上第二多產 (76篇), 近30年全球第一
 - ICCAD: 3rd (72 篇) ; TCAD: 4th (80 篇)
- 2017 年最佳論文獎 (約 700篇文件;不分領域台灣首篇), 6 次最佳論文獎提名 (提名率: 1%)
- 其他會議期刊: 9 次最佳論文獎, ICCAD Memorial Award (2007), 21 次最佳論文獎提名 (TCAD: 2次, ICCAD: 5次, ISPD: 5次)





NTUplace4: 3-time Champions @ 2012 DAC & 2013 ICCAD & 2015 ISPD Contests

Routability Contest Prizes Award

June 8 2012 / 4:25 pm by Paul McLellan

Officially the contest is the DAC 2012 routability placement contest where the primary measurement criteria are how small the routing was and the secondary criterion was runtime. The algorithms were tested (basically ASIC designs) with realistic process rules (metal layers, via sizes, etc).

ACM Student Research Contest @ DAC 2012

Graduate Category

1st Place (Gold):

Student: Shao-Yun Fang, EE, NTU (Advisor: Prof. Yao-Wen Chang)
Paper Title: Lithography Optimization for Sub-22 Nanometer Technologies



And the winner (\$1200) was NTUplace4 from National Taiwan University. Meng-Kai Hsu, Yao-Wen Chang.

The contest was administrated and judged by Natarajan Viswanathan of IBM corporation. The sponsors were CEDA, TSMC, Cadence and SigDA.

[#video](http://www2.dac.com/events/videoarchive.aspx?confid=139&filter=keynote&id=139-120--0)

NTUplace3 & 4 as Commercial Placers



Product News

SpringSoft presents IC place-and-route tools

AnneFrancoise PE

3/15/2010 03:00 PM EDT

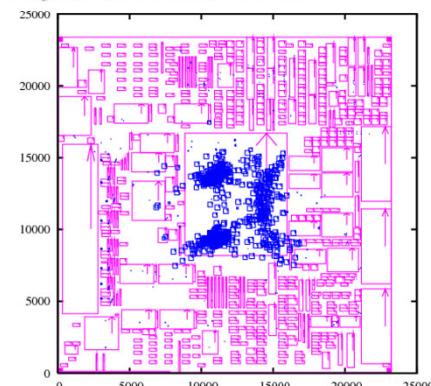
PARIS — Taiwan Semiconductor Manufacturing Company (Taiwan) announced a new platform with the integrated Laker Custom Digital

Laker Custom Row to achieve incremental iterations to pack th

Peter Clarke

8/3/2012 10:27 AM EDT

It utilizes stacking and R&D teams from Springsoft, Ciranova and Magma and overlap removal as thereby offer a higher level of automation in custom implementation tools.



NTUplace3 (2008) =>
Custom Digital Placer

NTUplace4 (2015) => Maxeda



C. Johnson: "The Best and Brightest Worldwide" (4/6/2015): "The best engineering minds on the planet compete each year in the ACM's ISPD design contest, which was won this year by the National Taiwan University."



MEDIATEK

聯發科技

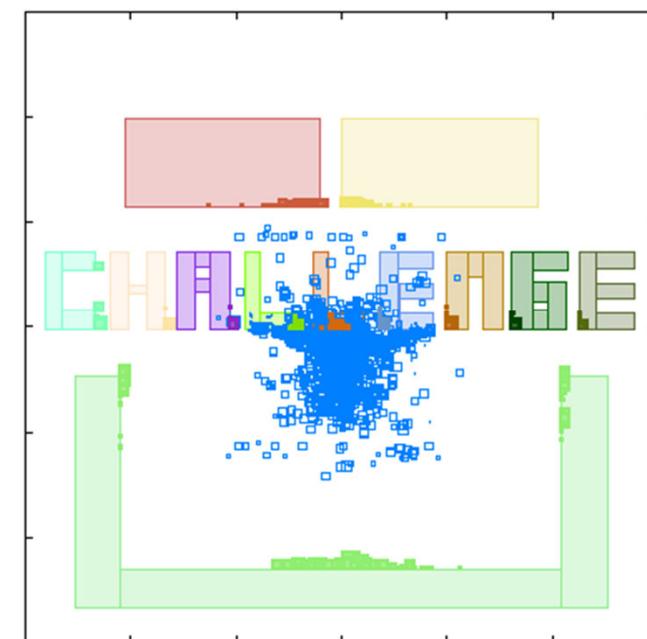
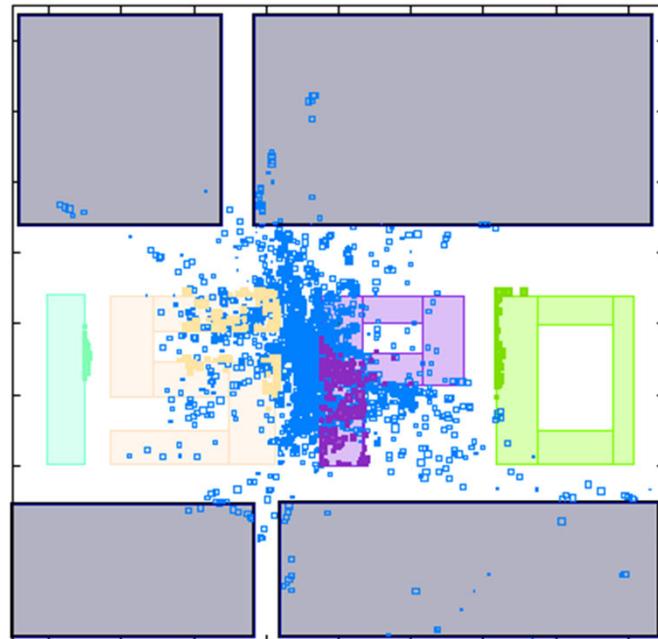
Raydium

FARADAY
TECHNOLOGY CORPORATION

REALTEK

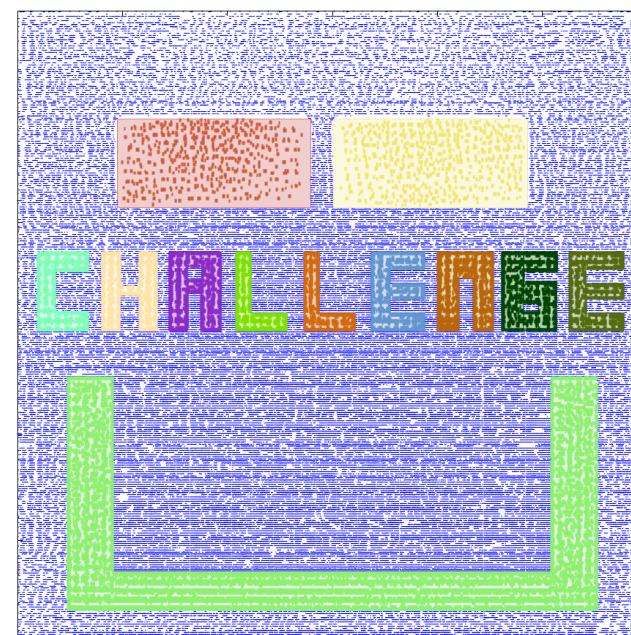
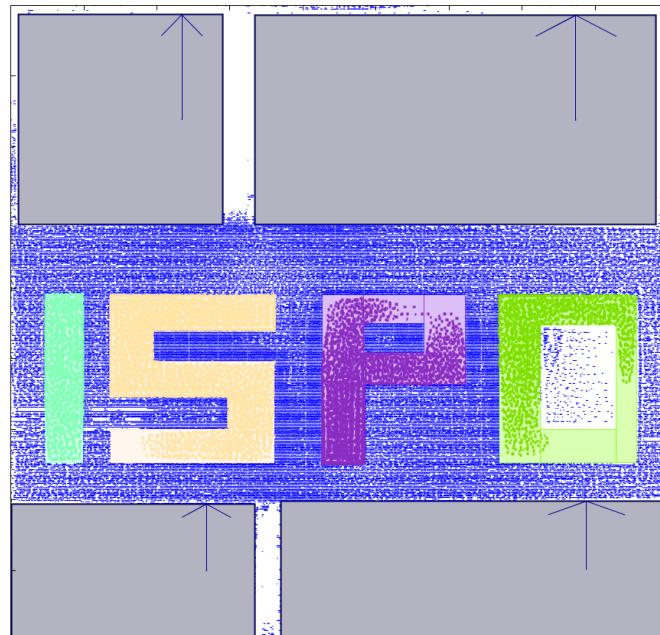
NTUplace4 on ISPD'15 Contest Benchmarks

- Circuit: mgc_des_perf_a
 - #Cell: 108k #Net: 115k
 - #Fence region: 4
- Circuit: mgc_des_perf_b
 - #Cell: 113k #Net: 113k
 - #Fence region: 12



NTUplace4 on ISPD'15 Contest Benchmarks

- Circuit: mgc_des_perf_a
 - #Cell: 108k #Net: 115k
 - #Fence region: 4
- Circuit: mgc_des_perf_b
 - #Cell: 113k #Net: 113k
 - #Fence region: 12



You Can Be the Next Winner!!

網站導覽 | 新生 | 在校學生 | 國際生 | 教職員 | 訪客 | 校友

回首站 | 聯絡我們 | 站內搜尋 :

English



學術庫 | 圖書館 | 博物館群 | 課程 | 招生 | 推廣教育 | 行事曆 | 捐款

認識臺大 學術單位 研究發展 行政組織 常見詢問 服務資源

臺大電機研發團隊勇奪 2015 ACM ISPD 冠軍

臺大電子與電機研究所於電子設計自動化領域再度創下世界紀錄！今年於美國加州蒙特利市舉辦的「ACM ISPD 細部可繞度導向擺置研發競賽」最終結果，由臺大電機系與電子所張耀文教授（電機資訊學院副院長）和電子所博士生黃朝琴、碩士生陳思鐸、楊勝為、林柏喬和電機所碩士生張晉豪與研究助理李昕穎所共同研發的積體電路擺置器 NTUpPlace4dr 獲得了第一名的榮耀！...more



EE|Times

C. Johnson: "The Best and Brightest Worldwide" (4/6/2015): "**The best engineering minds on the planet compete each year in the ACM's ISPD design contest, which was won this year by the National Taiwan University.**"

You Can Be the Next Winner!!

The screenshot shows the homepage of National Taiwan University (NTU). At the top, there's a large banner with the university's name in Chinese and English, along with its logo. Below the banner, there are several navigation links and search fields. On the left side, there's a sidebar with various links like '創校84年 校慶活動' (84th Anniversary Activities), '校長遴選專區' (President Selection Special Zone), '臺大電子報 NTU ePaper', '近期活動' (Recent Activities), '藝文中心' (Arts and Culture Center), '體育活動' (Sports Activities), '臺大演講網' (NTU Lecture Network), '臺大開放式課程' (NTU Open Courses), and links for '竹北分部產學合作' (Industry-Academic Cooperation), '外語學習課程' (Foreign Language Learning Courses), and '臺大華語 (華語學習)' (NTU Chinese Language Learning).

In the center, there's a main content area with a photo of three people (two men and one woman) standing in front of bookshelves. Below the photo, there's a caption: "左起電子所博士生徐孟楷同學、張耀文教授、電子所博士生方劭雲同學。 (101.11.05)" (From left to right: NTU PhD student Xu Mengkai, Professor Chang Yaowen, and NTU PhD student Fang Shaoyun. (November 5, 2012)).

Below the photo, there's a section titled "電子所張耀文教授團隊獲頂尖國際會議 ACM/IEEE DAC 美賽雙料冠軍" (The Electronic Engineering Department team led by Professor Chang Yaowen won the dual champion of the ACM/IEEE DAC competition). The text describes their success in the Design Automation Conference (DAC) and the ACM SIGDA Student Research Competition (SRC).

On the right side, there's a sidebar titled "最新消息" (Latest News) which lists recent achievements, and another sidebar titled "校園公告" (Campus Announcements) with links to various campus news sections.

Dual Champions at the 2012 DAC Contests

You Can Be the Next Winner!!

The screenshot shows the official website of National Taiwan University (NTU). At the top, there's a navigation bar with links for新生 (Freshman), 學生 (Student), 國際生 (International Student), 教職員 (Faculty/Staff), 訪客 (Guest), 校友 (Alumni), and 校歌 (School Song). There's also a search bar with placeholder text "請輸入關鍵字" (Please enter keywords) and a "Go!" button. The main header features the university's name in Chinese characters (臺灣大學) and English (National Taiwan University) with a large watermark of the university's bell logo.

The main menu includes 認識臺大 (About NTU), 學術單位 (Academic Units), 研究發展 (Research & Development), 行政組織 (Administrative Organization), 常見詢答 (FAQ), 服務資源 (Service Resources), and English. Below the menu, there are links for 圖書館 (Library), 博物館群 (Museum Group), 課程 (Courses), 招生 (Admissions), 推廣教育 (Promotion Education), 行事曆 (Calendar), 捐款 (Donation), 網路書院 (Online Library), INFO, myNTU, 活動快報 (Activity Bulletin), 校園焦點 (Campus Focus), and 最新消息 (Latest News).

On the left sidebar, there are four links: 畢業典禮 (Graduation Ceremony), NTU Space, NTU NEWSLETTER, and 臺大電子報 (NTU ePaper). On the right sidebar, there's a list of news items:

- 第4屆全球集思論壇
- 開創移民服務多贏局面 臺灣大學與移民署簽署策略聯盟
- 臺大公共論壇《民主對話 vs. 民粹對立》
- 2012QS公布亞洲地區大學排名臺大排行20
- 獸醫教育的未來發展座談
- 莎士比亞在臺大 論壇登場
- 【誠徵寫手】書寫生命、記錄校史：臺大學生日記365天
- 2012校史館特展：跨世代座標記憶~故去者

A central image shows four people (three men and one woman) standing in front of bookshelves, each holding a framed plaque or award. Below the image is the caption: NTUgs 團隊成員：左起何冠賢同學、張耀文所長、陳昱臻同學、許博雅同學。 (101.06.05)

Champion at the 2012 ISPD Contest

You Can Be the Next Winner!!

學術典藏 | 圖書館 | 博物館群 | 課程 | 招生 | 推廣教育 | 行事曆 | 捐款

認識臺大 學術單位 研究發展 行政組織 常見詢問 服務資源

臺大電機團隊獲2019年ACM ISPD國際細部繞線研發競賽第二名

本校電機團隊於電子設計自動化最重要的國際研發競賽再度獲得佳績！今年於美國加州舊金山市舉辦的「國際積體電路實體設計會議」公布為期四個多月的「ISPD初始細部繞線研發競賽」最終結果，由電機系與電子所張耀文教授和電機系大四學生張家銘、張振嘉、劉維凱以及電子所碩士生徐晨皓所共同研發的初始細部繞線器NTUidRoute獲得了第二名的榮耀！
...more



★ 最新消息

校長遴選相關業務精進檢討報告

活動

臺大其他粉絲團

活動快報

養鶯劇集《白噪音White Noise》

「勞健保及勞退金業務宣導」研習課程

校園推廣

NTU Highlights

臺大電子報

畢業

2nd Place at the 2019 ISPD Contest

國際行政經歷

- 首位非美國歐洲的 IEEE CEDA 總裁 & 候任總裁

- ExCom, IEEE Council on EDA (CEDA), 2012起
- CEDA Vice President
(Conference & TA), 2014-17
- CEDA President-elect, 2018-19
- Chair, CEDA Strategy Com., 2018起
- **CEDA President, 2020-21**

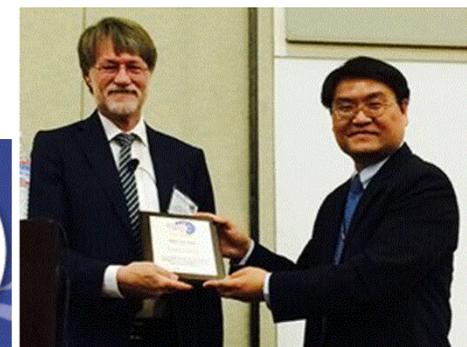


- 首位非美歐日的頂尖會議主席

(102 HW & Architecture 會議排名: ICCAD: #3, ISPD: #4)

- Chair, Program/Conference/Executive Committee, IEEE/ACM **ICCAD**, 2013/14/15
- Chair, Program/Conference/Steering Committee, ACM **ISPD**, 2010/11/12
- Program Committee Chair, IEEE FPT, IEEE/ACM ASP-DAC, etc.

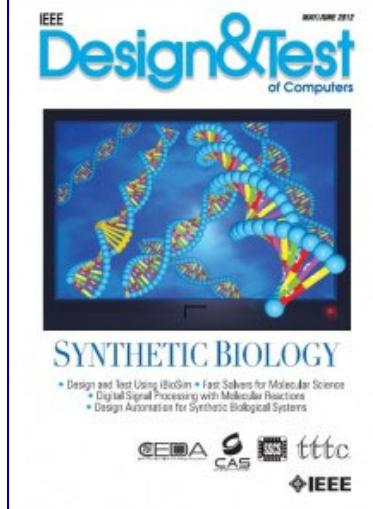
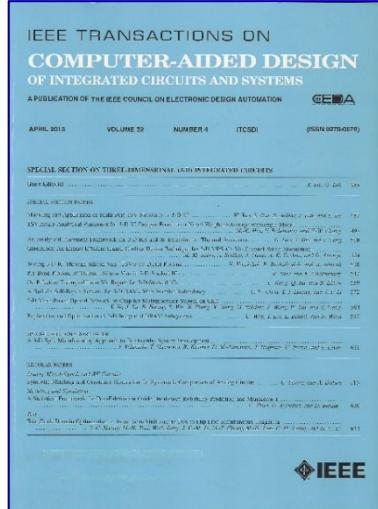
Two Great Keynotes at Iccad



Peter van Staa - Robert Bosch GmbH

頂尖國際期刊副編輯/編輯

- IEEE Trans. on Computer-Aided Design (TCAD), 2008-13
 - EDA 最頂尖期刊 (創刊28 年後台灣的第一位 AE)
- IEEE Trans. on VLSI Systems (TVLSI), 2015起
- IEEE Design & Test of Computers (D&T), 2012-14, 2016起 (interview editor)



An Interview With Professor Chenming Hu, Father of 3D Transistors

Yao-Wen Chang
National Taiwan University

9/2017 D&T

September 2016. In this interview, Prof. Hu shared with our D&T readers the motivations and preparation for his work on 3D transistors, the technology needs for semiconductors, his insightful tips on innovation, and his inspiring suggestions to readers.

Before this interview, the Editor prepared over 20 questions and also called for questions from experts and readers. We received many responses from the individuals who proposed the question. As a result, nearly 19 questions and their answers are compiled in this special section. We hope that our DAT readers will enjoy this interview. Thank you!

Dr. Chenming Hu has been a 3D Transistor pioneer, developing the FinFET in 1995 and was the first to propose FinFET in 2001 production, calling it the most radical idea that he had, which noted in over 50 years. By 2015 all top servers, computers, Android, and iOS devices used FinFET. Dr. Chenming Hu received the National Technology and Innovation Medal from President Obama in the White House in 2016. The DAT interview editor, Yao-Wen Chang, interviewed him "Microelectronics Visionary" when presenting him the 2009 Nishizawa Medal for "achievements in the field of microelectronics, especially in high-density and higher-performance integrated circuits." The 2011 Asian American Engineer of the Year Award was presented to Dr. Chenming Hu for his work in designing IC products with cumulative sales of many hundreds of billions of dollars. The 2013 Kadhim Award noted his "tremendous career of

Prof. Chenming Hu and the interviewer, Prof. Yao-Wen Chang (photo taken on 22 September 2016, in the DAT office, National Taiwan University, Taipei, Taiwan).

Digital Object Identifier 10.1109/MDAT.2017.272911
Date of publication: 26 July 2017; date of current version: 13 September 2017.

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Copublished by the IEEE CEDA, IEEE CAS, IEEE SISD, and TTS.

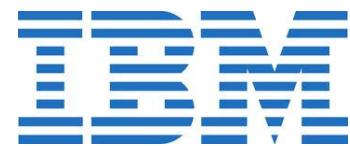
Prof. Chenming Hu: “During my undergraduate study at NTU, the solid training on mathematics and physics was critical for my research career. Most importantly, the self-confidence and positive attitude built up then has supported me to face challenges and explore new things.”

大綱

實驗室概況

業界計畫實例

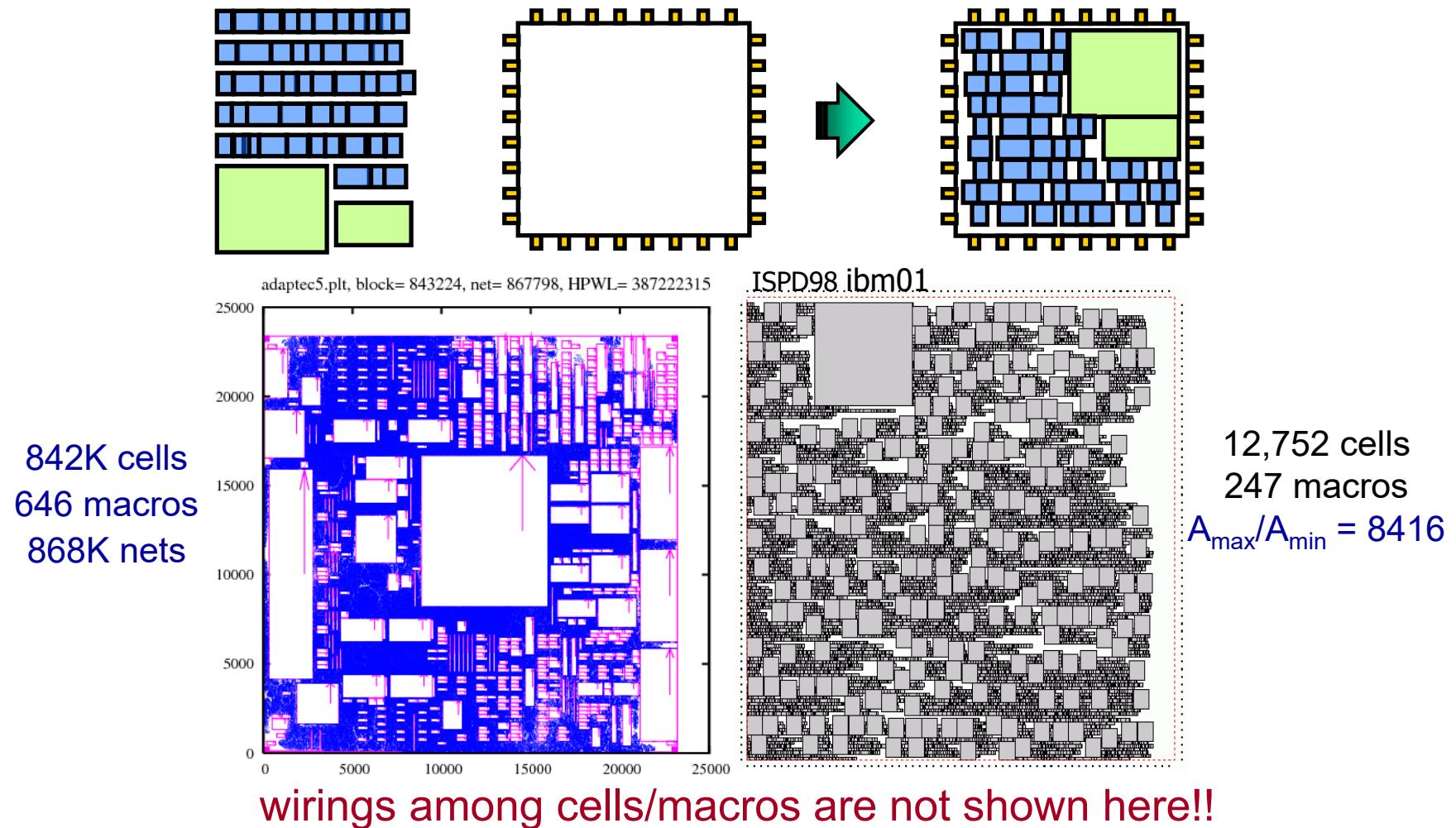
IBM, Maxeda, MediaTek & RealTek: Placement



Maxeda

VLSI Placement

- Place objects into a die s.t. no objects overlap with each other & some cost metric (e.g., wirelength) is optimized



Demo: MP-Tree Placer (1/2)

- Stage 1: Macro placement



Circuit: adaptec5

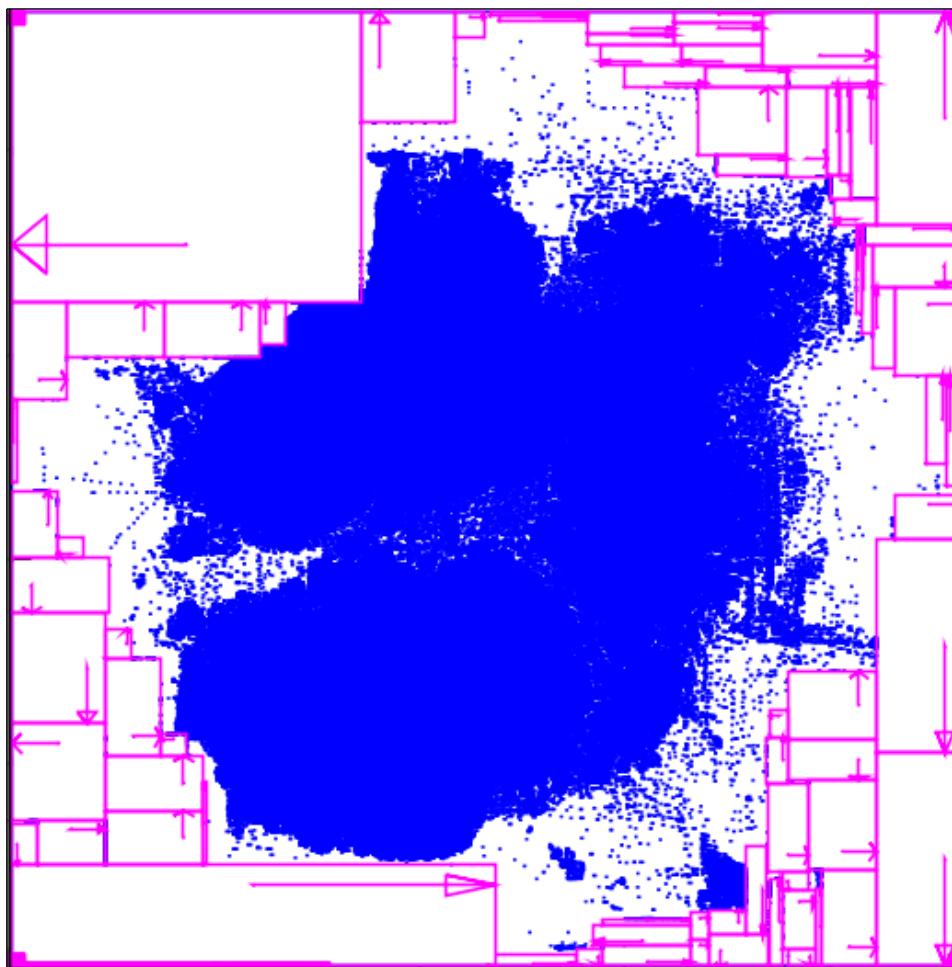
#Cell: 842k

#Net: 867k

#Macro: 76

Demo: MP-Tree Placer (2/2)

- Stage 2: Standard-cell placement



Circuit: adaptec5

#Cell: 842k

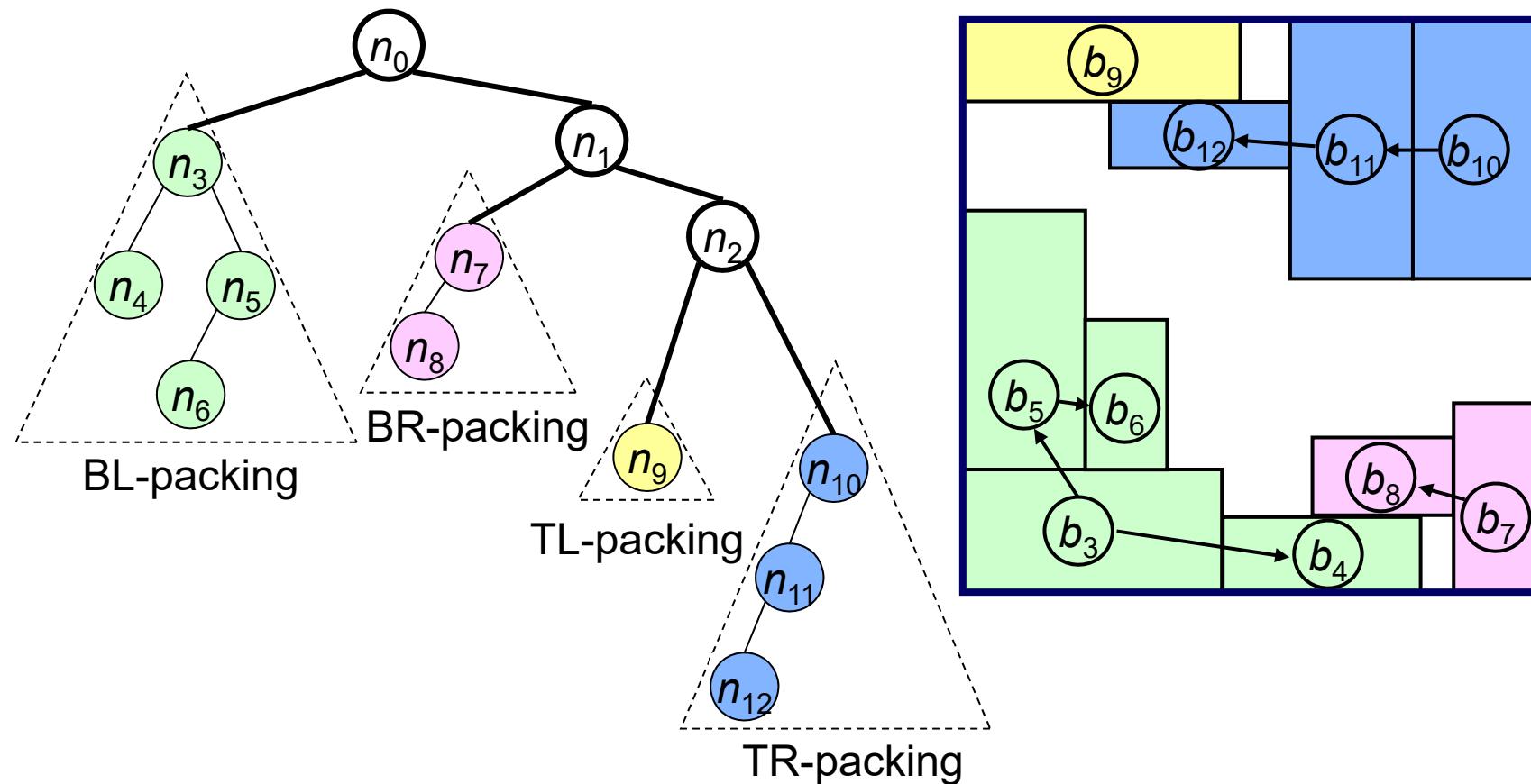
#Net: 867k

#Macro: 76

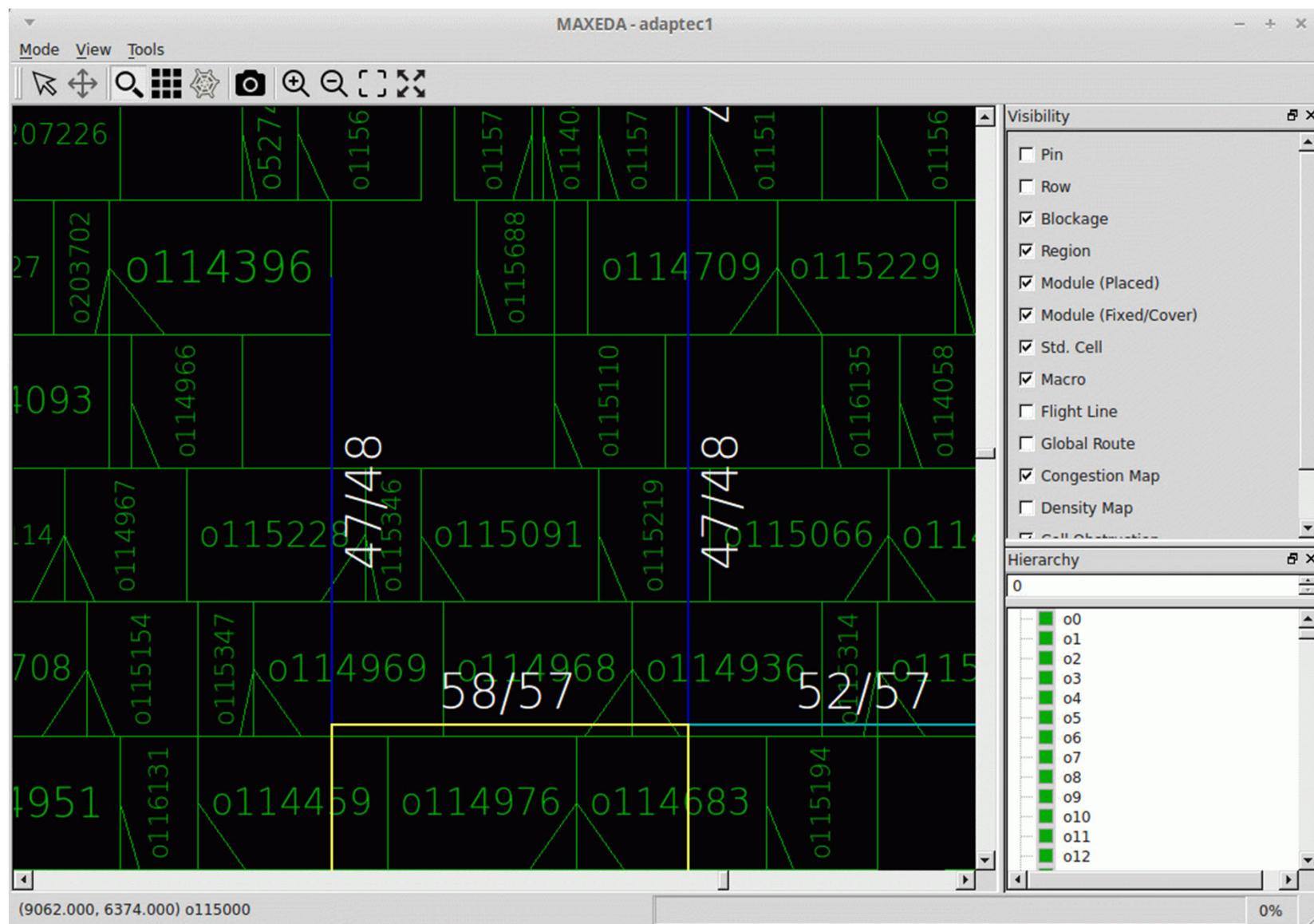
HPWL: 3.27e6

MP-tree Macro Placement Example

- Use four packing subtrees to handle a rectangular chip
- Applies to a placement region with any number of corners

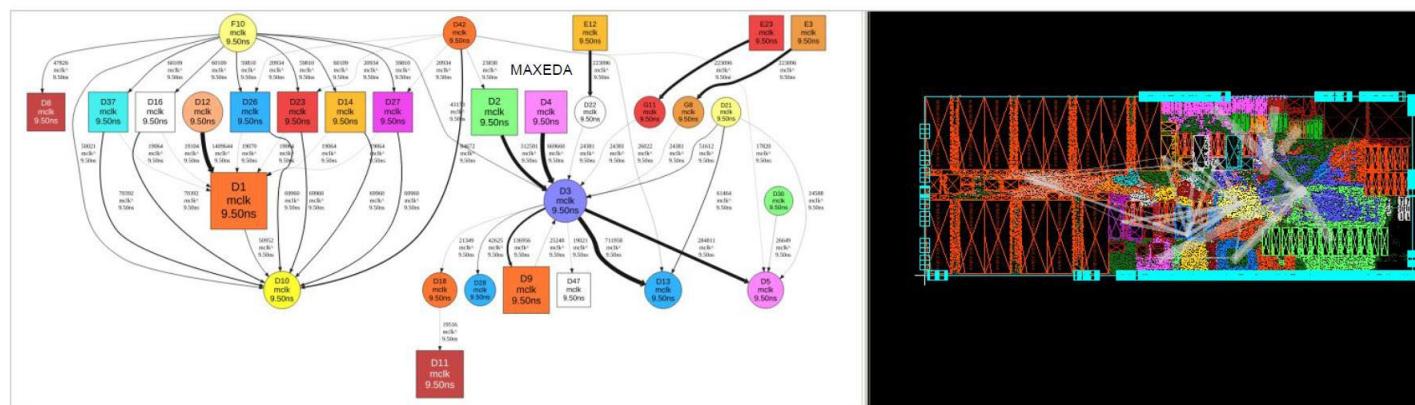
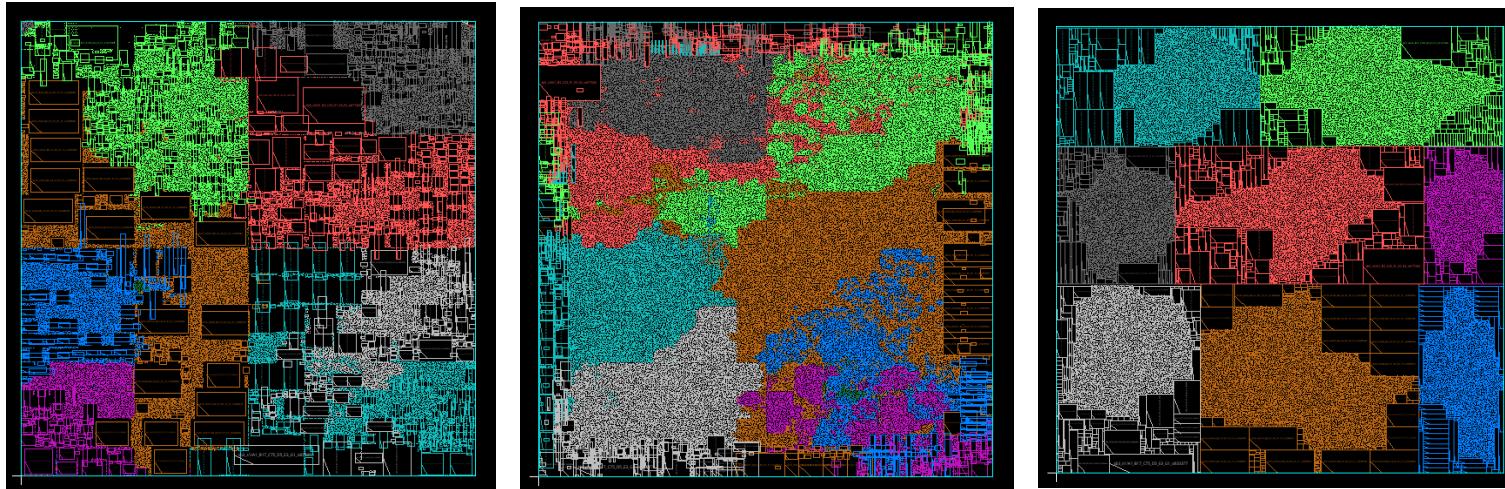


MaxPlace: Best Macro Placer “on the Planet”



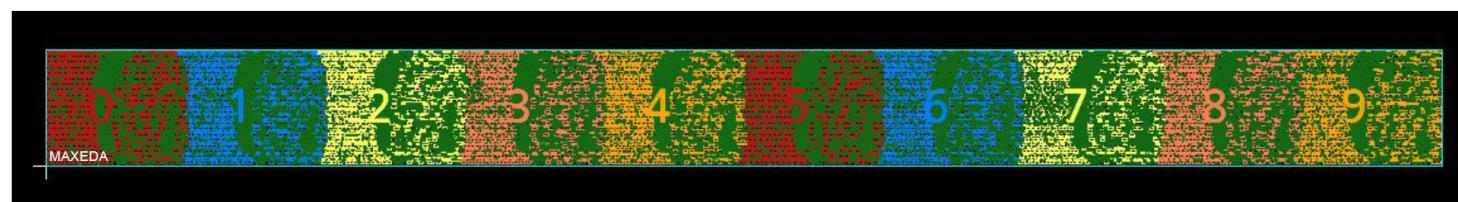
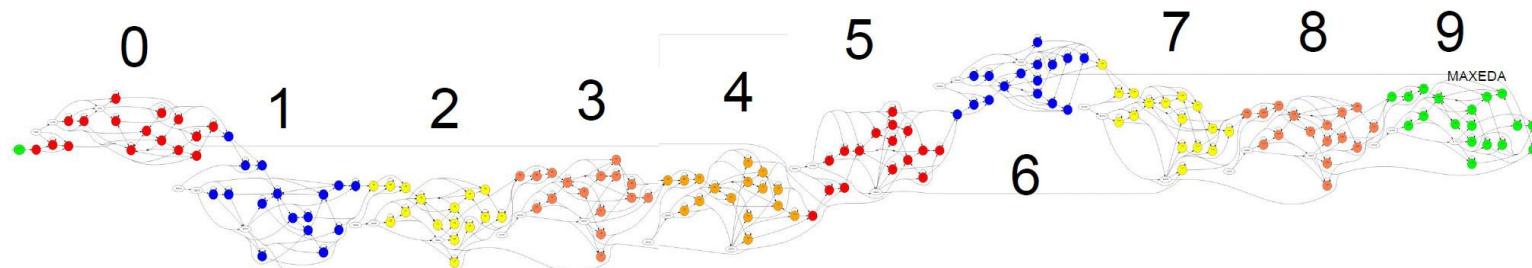
Macro Placement w. Dataflow Analysis

- Multiple-domain mixed-size placement

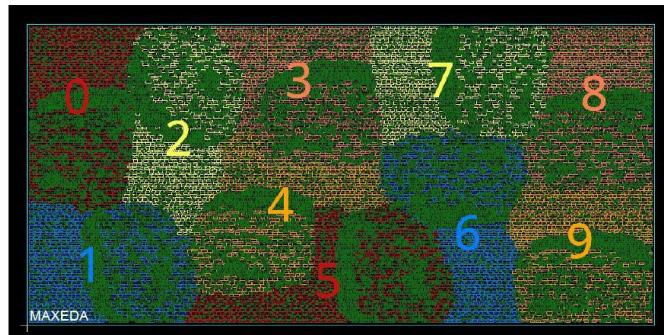


Placement for Display Driver Chips

- Thin-outline placement for display applications



Wirelength: 9.38071e+08



Wirelength:
9.61361e+08



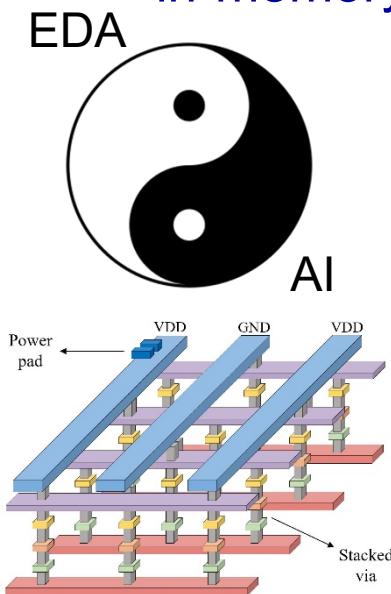
AI for EDA & EDA for AI

- **AI technologies reshape EDA**

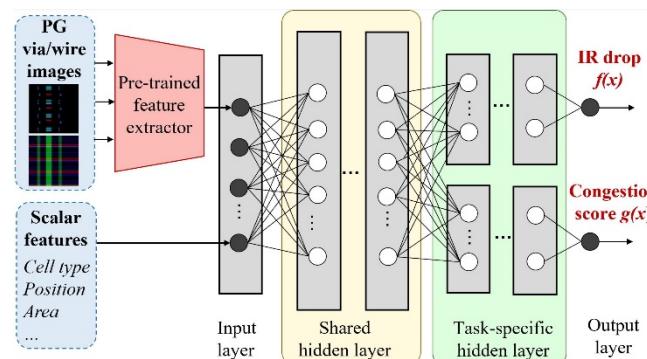
- Enhance EDA techniques with machine learning

- **EDA helps AI system designs**

- Redefine the architecture and way of computing, e.g., neuromorphic and in-memory computing.



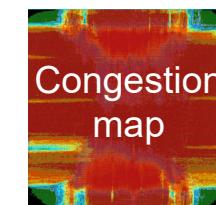
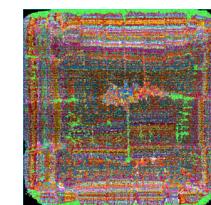
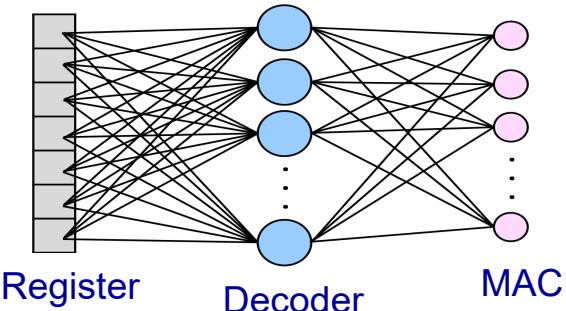
AI for EDA



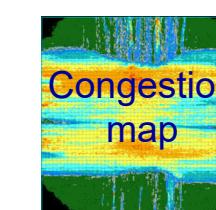
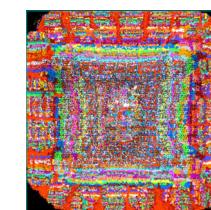
ML for IR-drop optimization

EDA for AI (chip design)

kernel structure of a CNN



Placement by “leading” industry tool

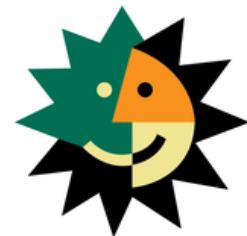


Placement by NTU/MAXEDA tool

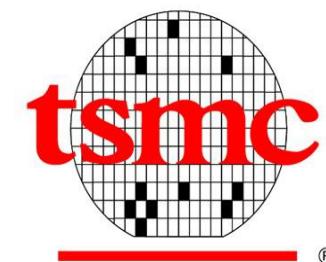
ASE, AnaGlobe & TSMC:

3D Heterogeneous Integration &

Chip/Package/Board Design

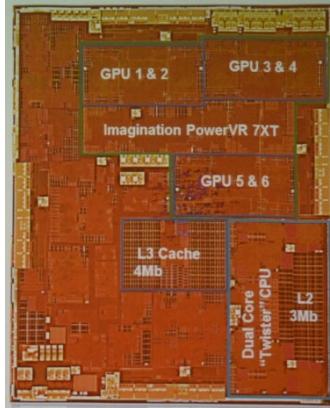
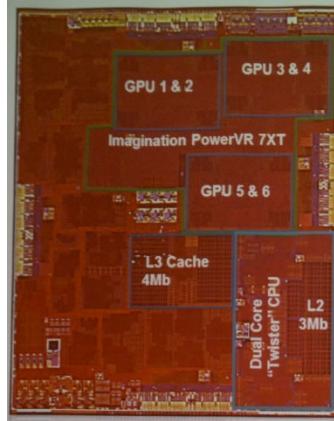


ASE GROUP



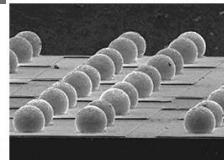
Chip, Package, and Board

Apple A9 chip for iPhone 6s
(1.85GHz; 5B+ transistors)

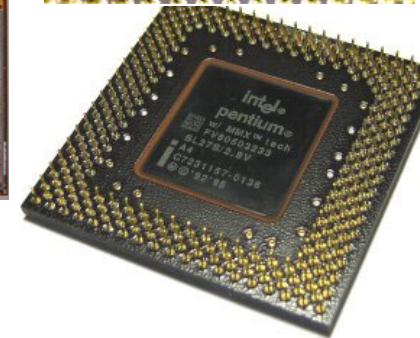


圖二、IC 與載板的連接方式

A 覆晶載板(Flip Chip, FC)



覆晶載板



裸載板(Wire Bound, WB)

打線載板

印刷電路板

來源：南電，康和整理，2010/Q

packages



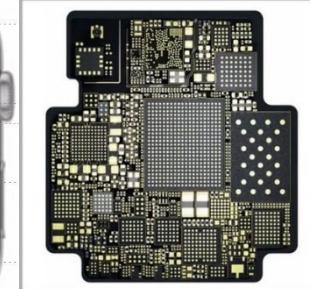
packages



iPhone 11 Pro Max board

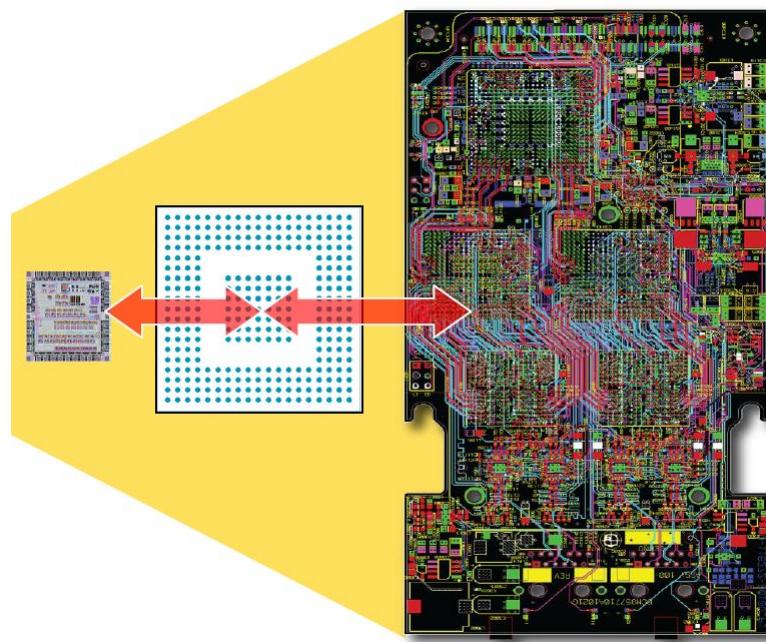
boards

Apple watch
board



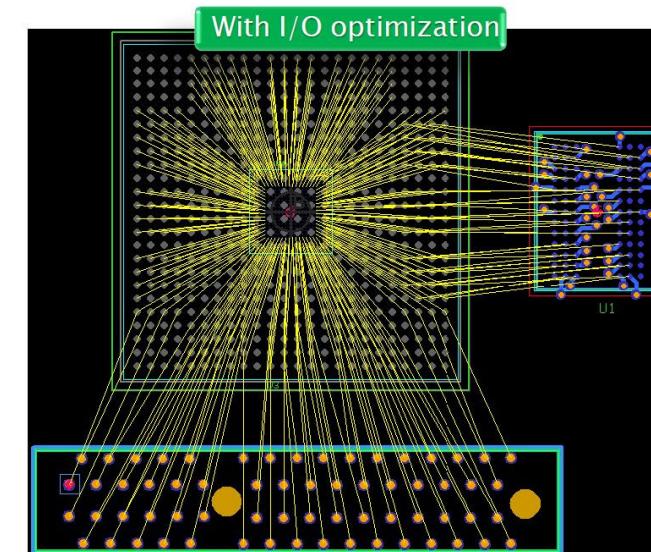
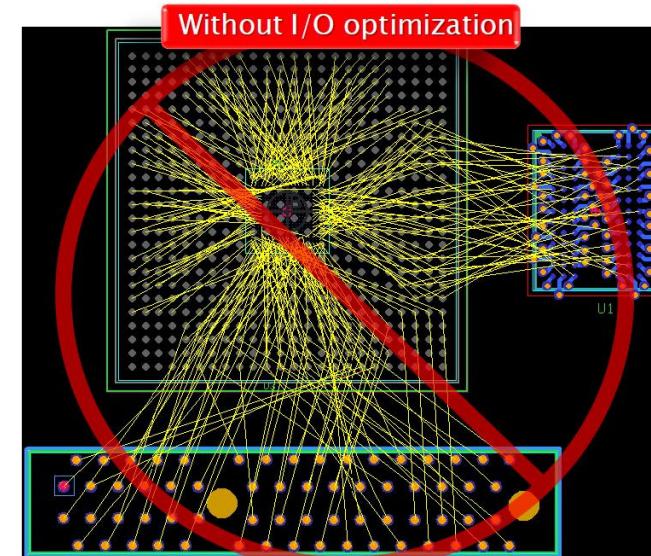
Effects of Chip-Package-Board Co-Design

Without co-design



John F. Park, ICCAD'10

With co-design



HI (InFO Package) for TSMC's Success

- Dr. Morris Chang (2016): InFO is key for TSMC to beat Samsung for Apple's chip orders
 - 財經新報: 《台積電藉 InFO 晶圓級封裝技術 獨拿 A10 處理器產能訂單》

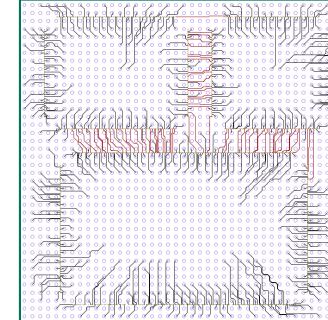
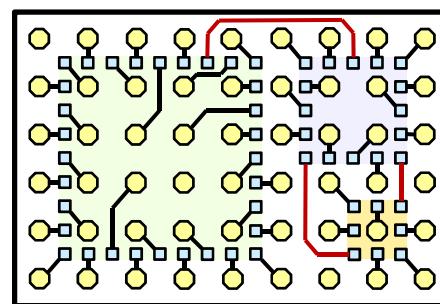
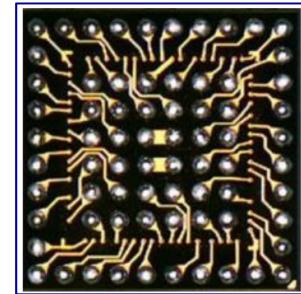
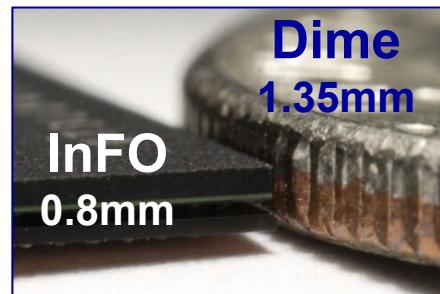
天下雜誌 一個「小媳婦部門」為何能讓台積電擊敗三星、獨吃蘋果？
2018年04月22日

財經新報 台積電藉 InFO 晶圓級封裝技術 獨拿 A10 處理器產能訂單
作者 Atkinson | 發布日期 2016年04月14日

FOCUS TAIWAN

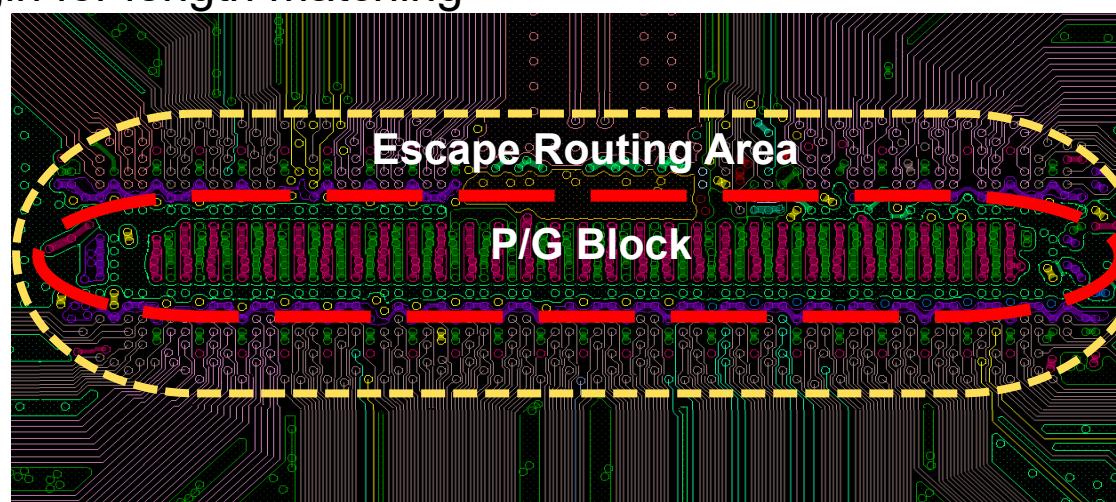
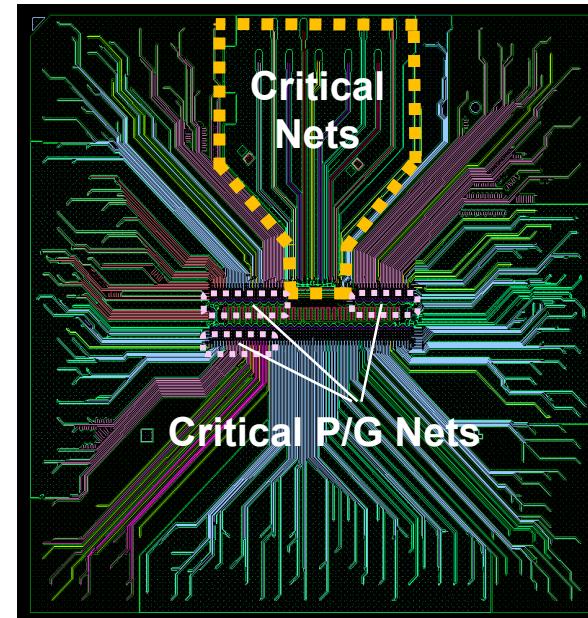
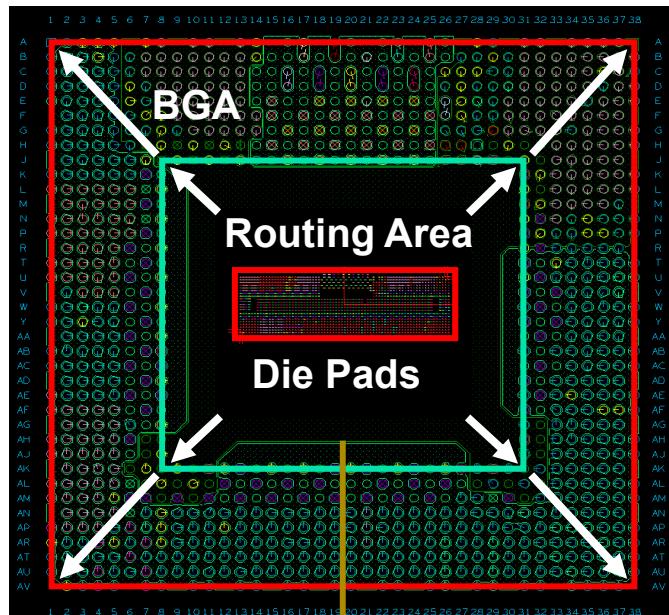
05/30/2020

TSMC's IC packaging, testing plant to become operational in mid-2021

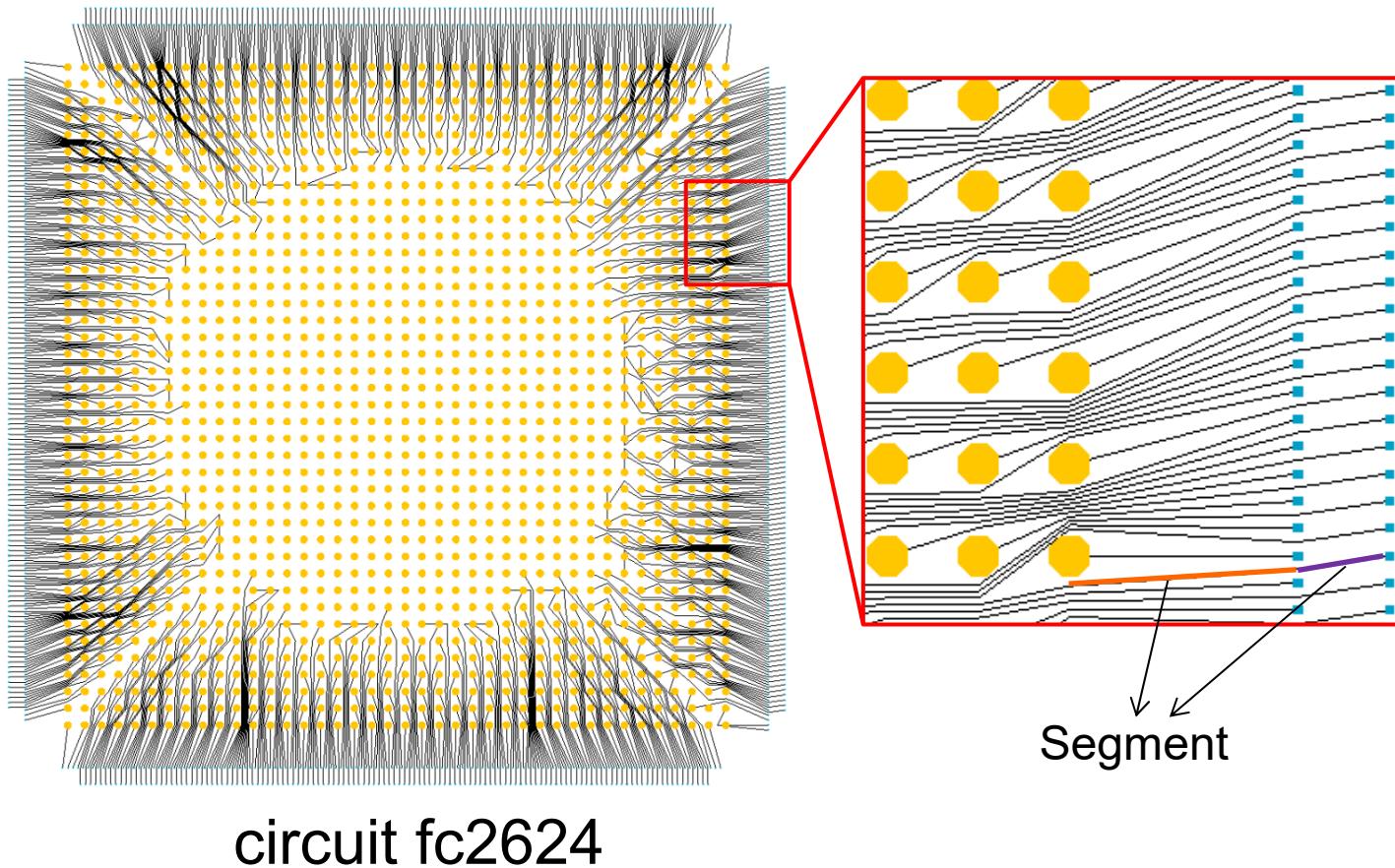


First published InFO package router [Lin et al., ICCAD'16]
US Patent 9,928,334, 2018 (with AnaGlobe)

Sample Circuits

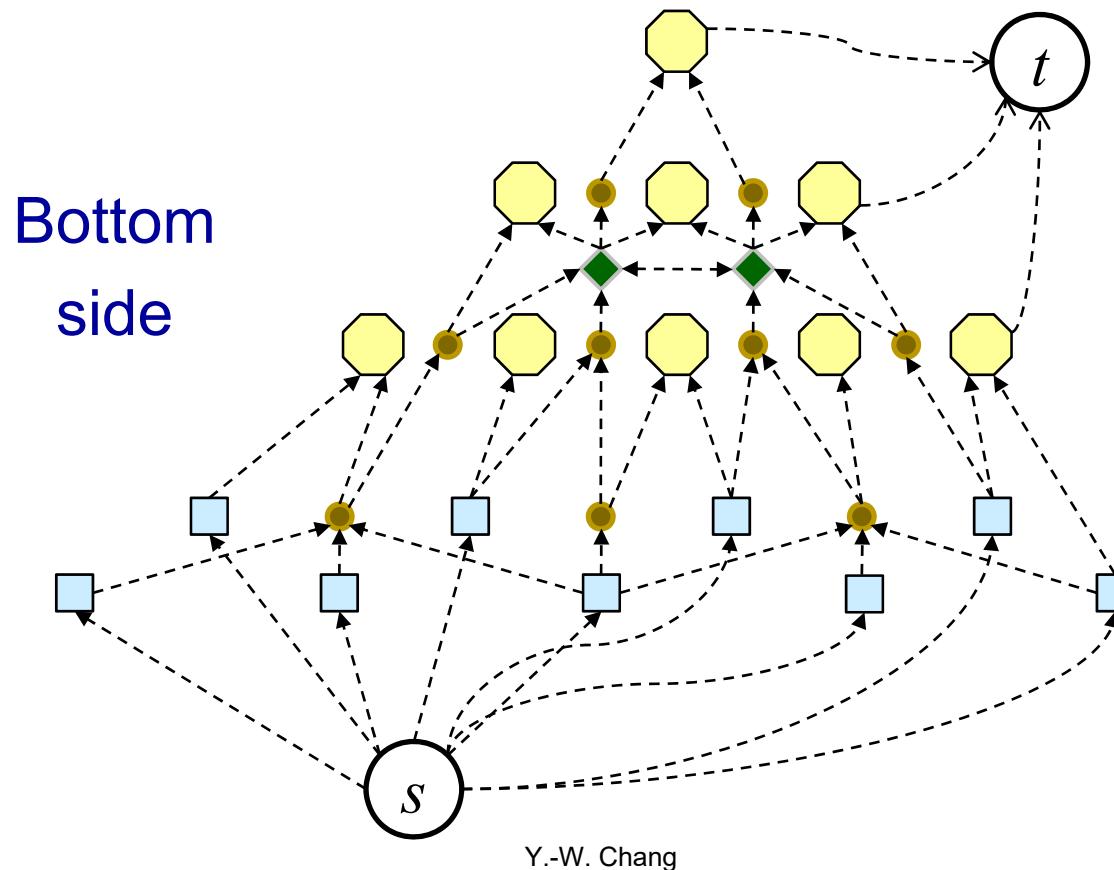


Flip-Chip / InFO-Package Routing



Flow Network Based Design

- Construct tile and intermediate nodes
- Construct flow edges from outside to inside
- Connect pads to super-source and super-sink

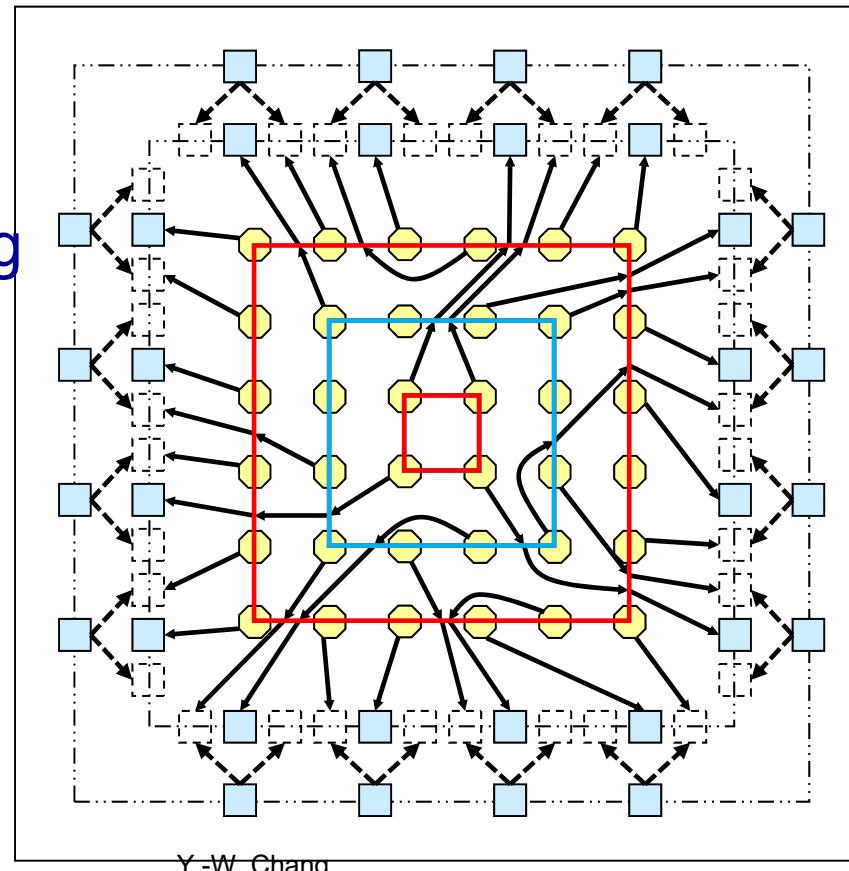


Dynamic Programming Based Design

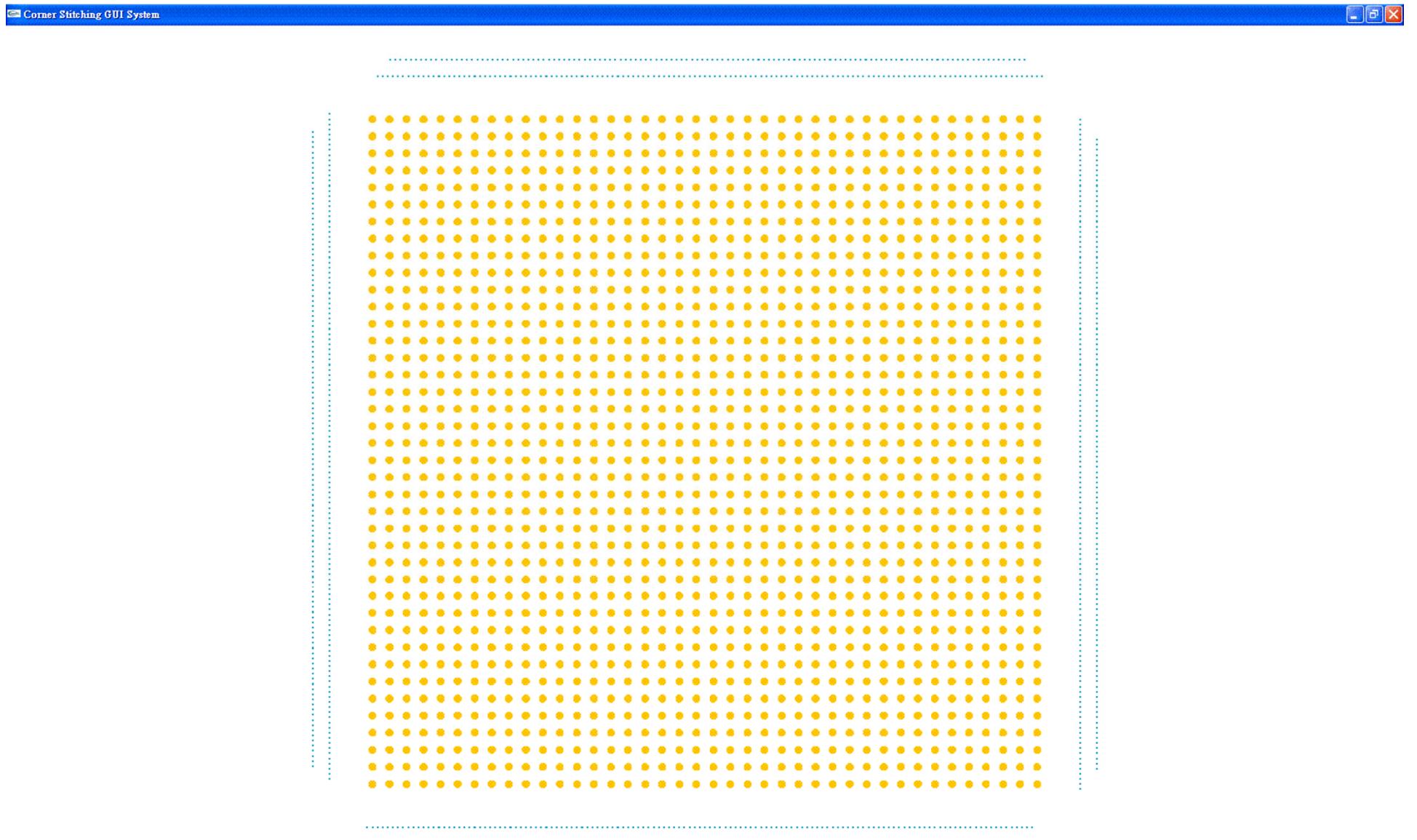
- Decompose chip into rings of pads and route from inner rings to outer rings
- Keep applying dynamic programming (LCS & MPSC) between two adjacent rings (**red ring** and **blue ring**)

— current ring
— preceding ring

Achieve over
100X speedups
over ILP



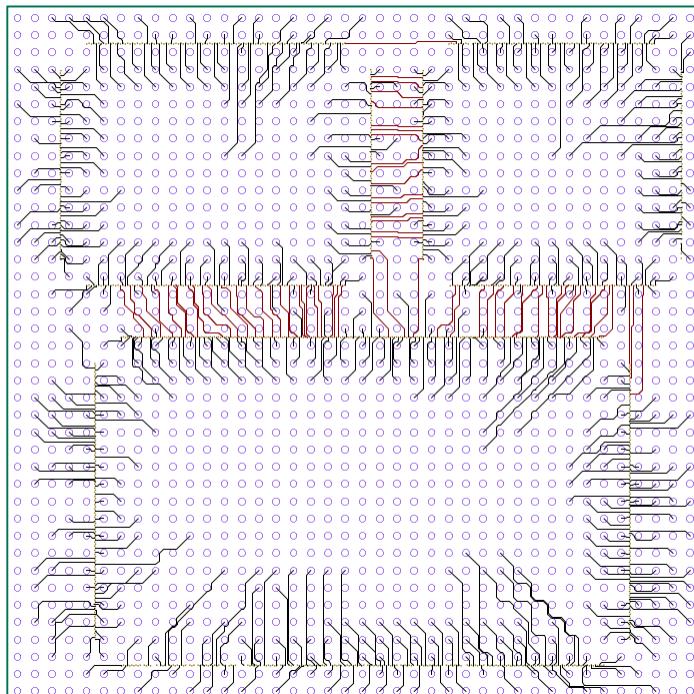
Demo



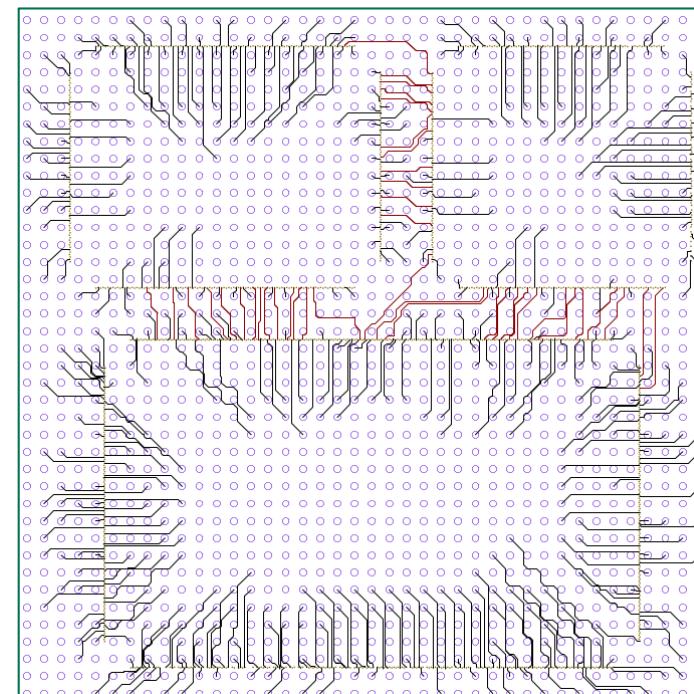
First InFO Package Router: Circuit info3

ICCAD 2016

- : Pre-assignment net
- : Free-assignment net



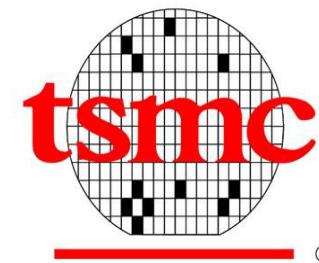
Layer 1



Layer 2

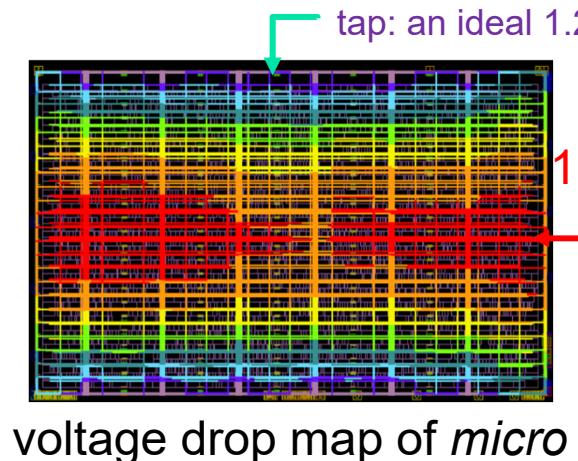
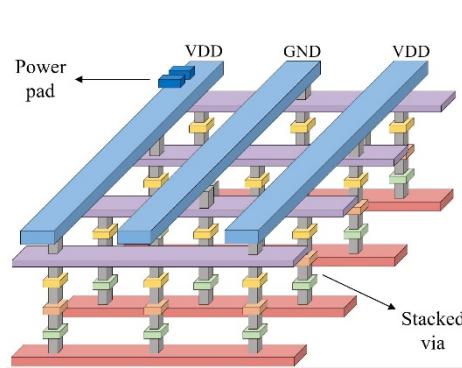
Synopsys & TSMC: Machine Learning for Power Integrity & Manufacturability, Multiple Patterning, e-Beam, EUV, DSA, Nanowire

SYNOPSYS®

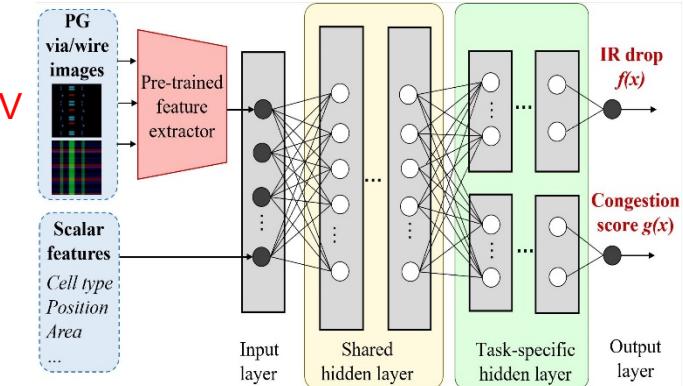


ML-Based Power Integrity Optimization

- Interconnect resistance constituting the power dissipation network causes voltage drop in the network
- Effects of IR drop
 - Reducing circuit speed
 - Causing functional failures due to the reduced noise margin



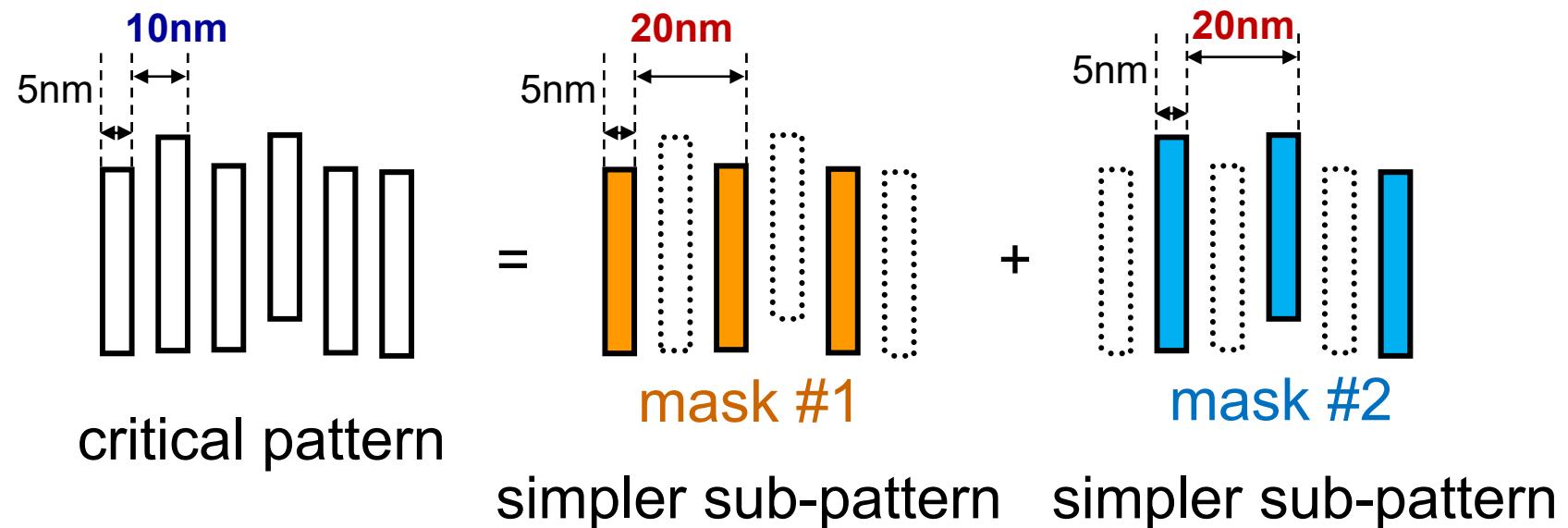
SYNOPSYS®



ML for IR-drop optimization

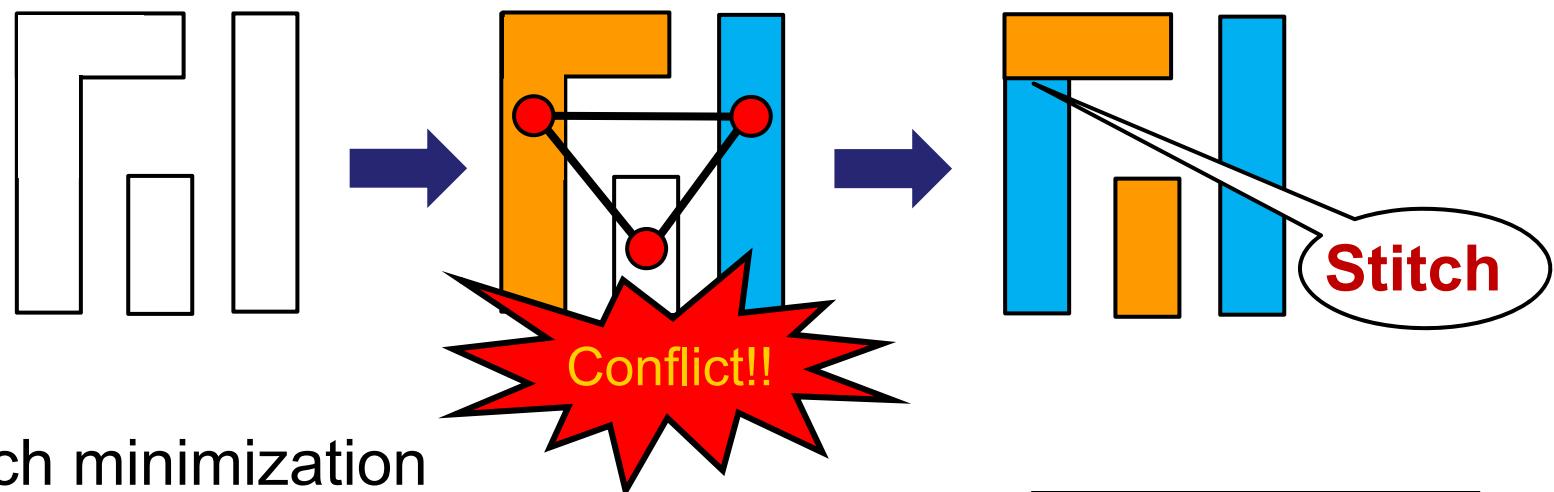
Double Patterning & More

- The major lithography technique used for 20nm node and beyond
- Decompose the critical pattern into two simpler sub-patterns and use **two masks** to form each sub-pattern

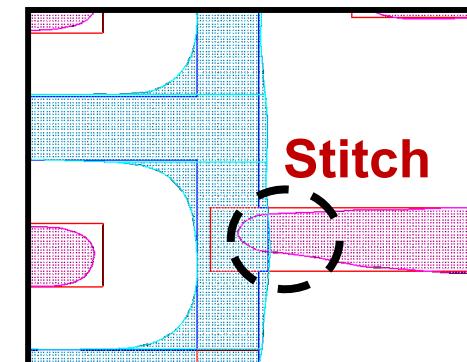


Two Challenges

- Layout decomposition
 - Decomposition for complex 2D patterns is not always feasible
 - Some conflicts can be resolved with stitch insertion



- Stitch minimization
 - Stitches may result in significant printability degradation and thus cause yield problems



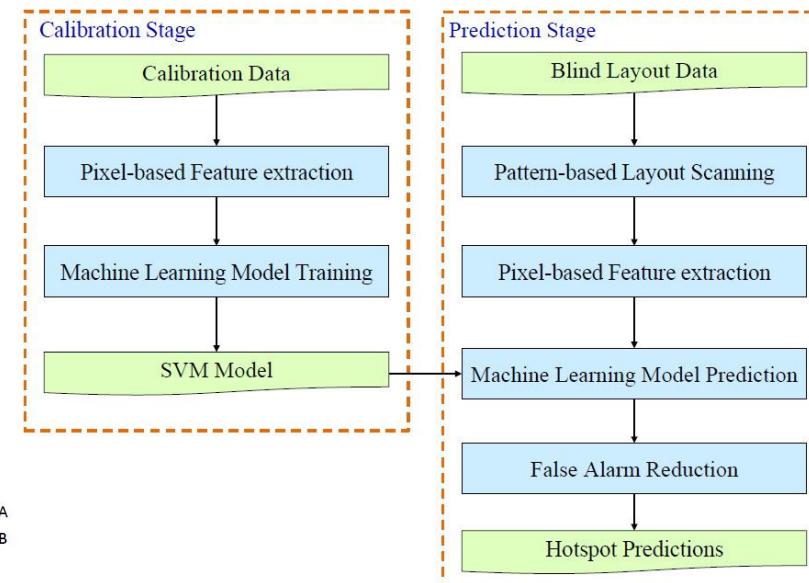
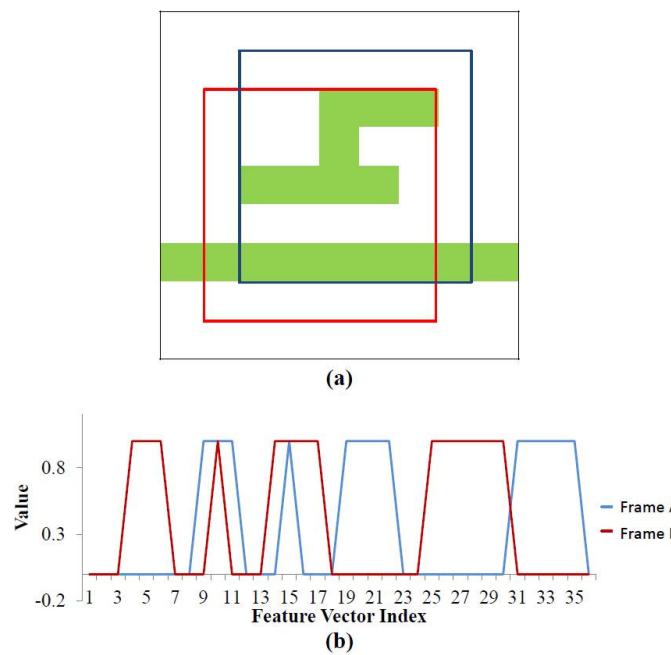
Machine-Learning-Based Hotspot Detection

Hotspot Detection with Machine Learning Based on Pixel-based Feature Extraction

Abstract—The complexity of physical verification increases rapidly with fast shrinking technology nodes. Considering only DRC constraints or lithography models cannot capture the side physical effects in the fabrication process well. Thus, it is desirable to consider a more general physical verification problem with various types of hotspots. In this paper, we apply machine learning which is based on pixel-based feature extraction to deal with the generalized hotspot detection problem. We further propose a two-dimensional discrete Fourier transformation-based pixel extraction method, a pattern-based layout scanning approach, and two false alarm reduction approaches. Experimental results based on the 2012 CAD Contest @ ICCAD benchmarks show the effectiveness of our work.

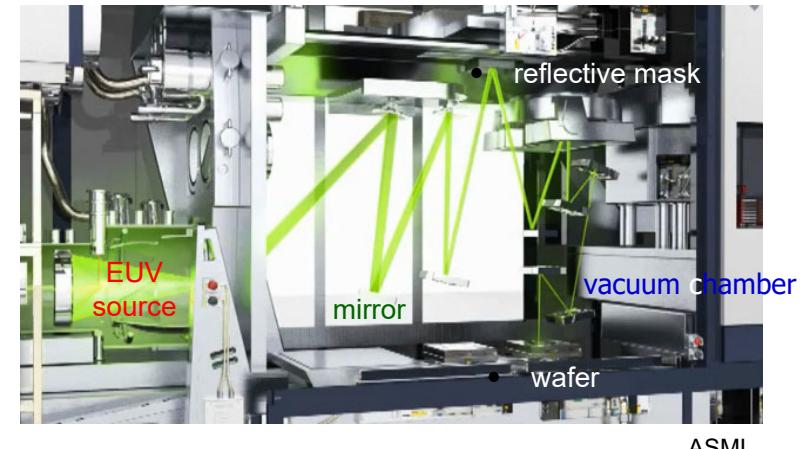
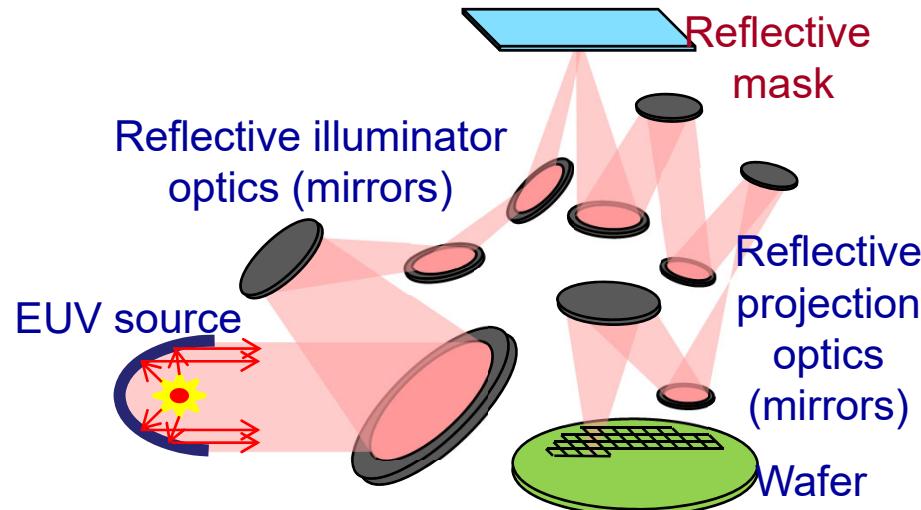
however, these methods lack the capability to find out undefined or unknown problematic patterns.

Machine learning-based methods use machine learning models in the artificial intelligence domain. By giving the calibration data, a machine learning model is trained to find out the relationships among the training features and make decisions to the new testing data based on these relationships. Previous works [2], [3], [4], [5], [11], [14] use state-of-the-art learning models such as artificial neural networks (ANN) and support vector machines (SVM). Machine learning-based hotspot detection methods can deal with never-seen-before patterns better compared with pattern matching-based approaches; however, most of the machine learning-based methods suffer from low accuracy and high false-alarm rate. In addition, the performance extremely

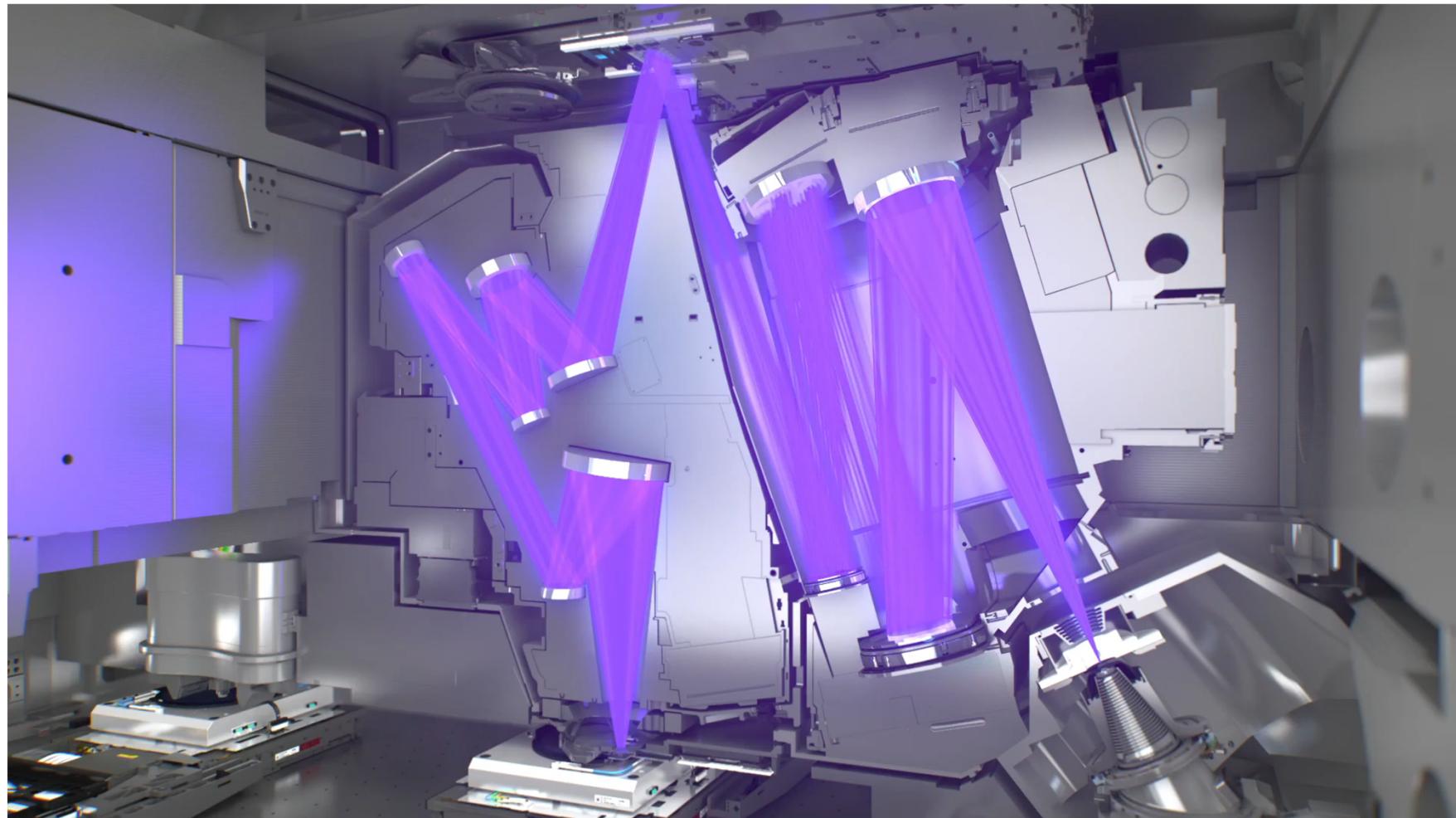


Extreme Ultraviolet Lithography (EUVL)

- EUVL is the most invested new-generation lithography technology
 - Its wavelength (λ) is only 13.5 nm
 - Reflective optical components and masks are used
 - TSMC adopted EUV for 7nm production in 2018, also for 3nm & beyond
- Rayleigh criterion for resolution: $R = k_1 \lambda / NA$
 - k_1 : resolution constant (≥ 0.25); NA : numerical aperture ($0.33 \rightarrow 0.55$)



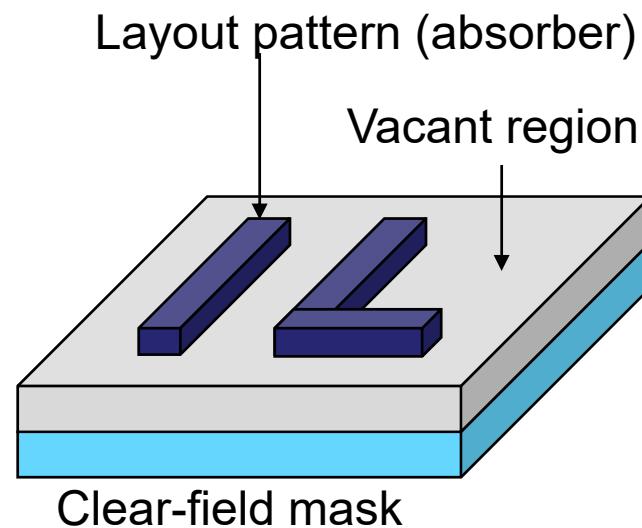
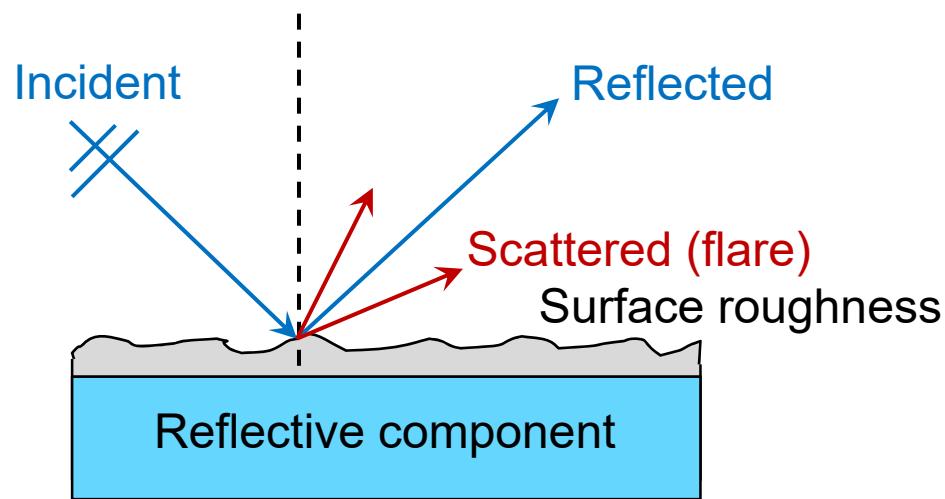
ASML EUV Patterning System



<https://www.youtube.com/watch?v=skUCP2f4HIM>

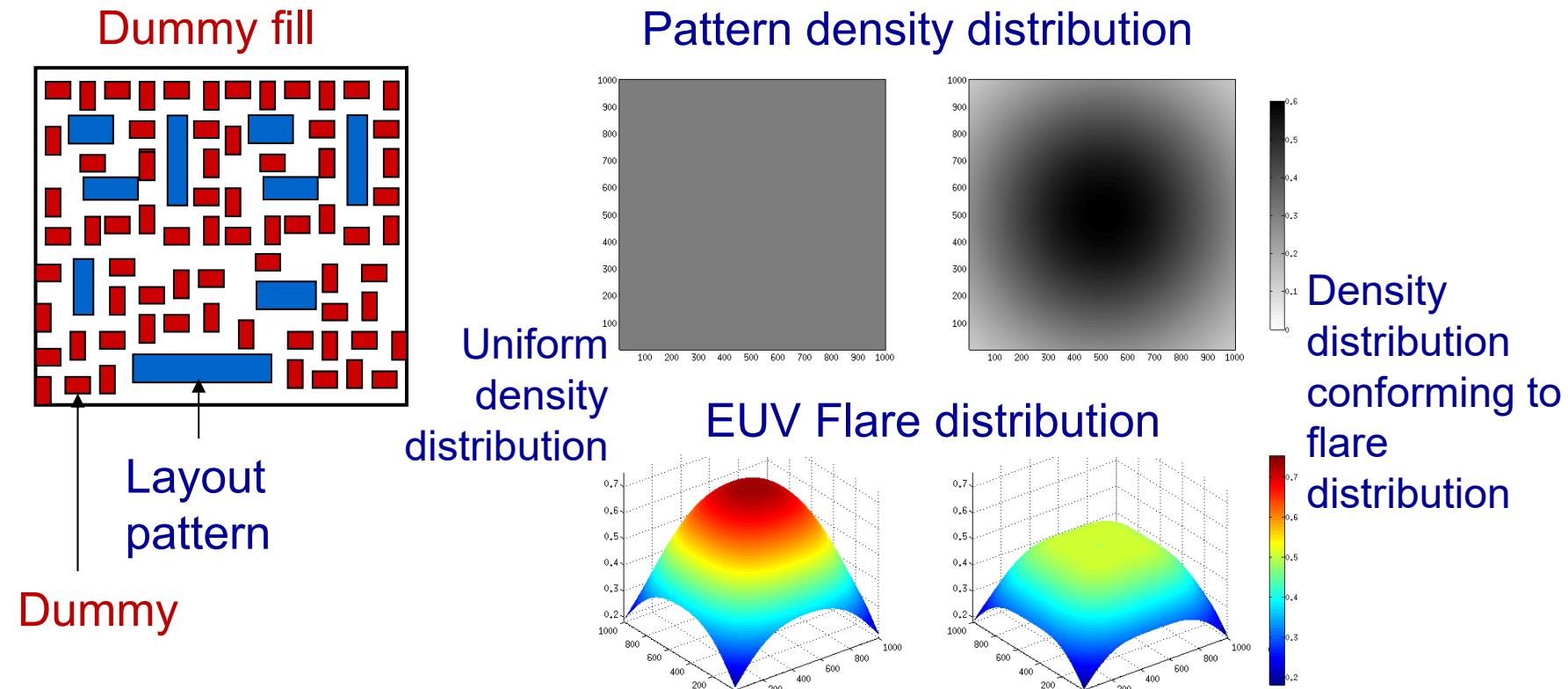
EUV Flare Effect

- Reflective masks are used
- **Flare**: scattered light due to the surface roughness of the optical system
- **Clear field mask**: layout patterns are formed by absorbers
- Flare will be distributed from vacant regions and reduce image contrast (and thus pattern quality)



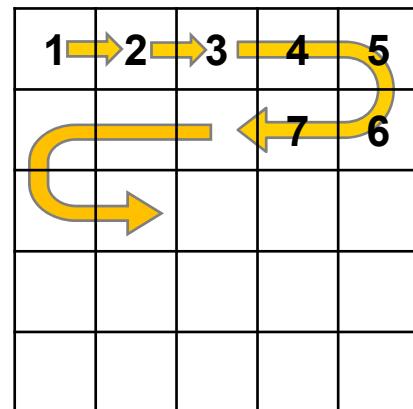
Flare Mitigation with Dummification

- Flare can be mitigated with dummification (dummy fill)
 - Existing dummy fill algorithms are for CMP optimization to maximize layout uniformity
 - Need to consider global flare distribution for flare mitigation

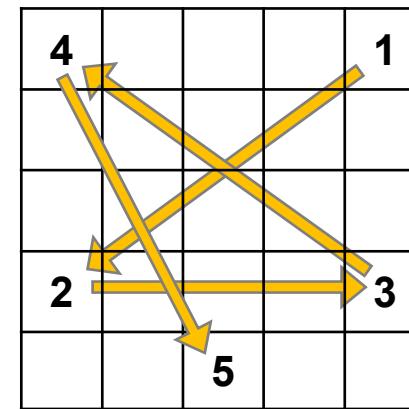


Subfield Scheduling in EBL

- **Contiguously sequential writing:** writing proceeds in the order from one subfield to the next adjacent subfield
 - High voltage beams with contiguously sequential writing cause resist heating effects and critical dimension (CD) distortion
- **Subfield scheduling:** writing proceeds in a non-contiguously sequential way to avoid successive writing [Babin et al., SPIE'03; Fang et al., ISPD'12, TCAD'14]



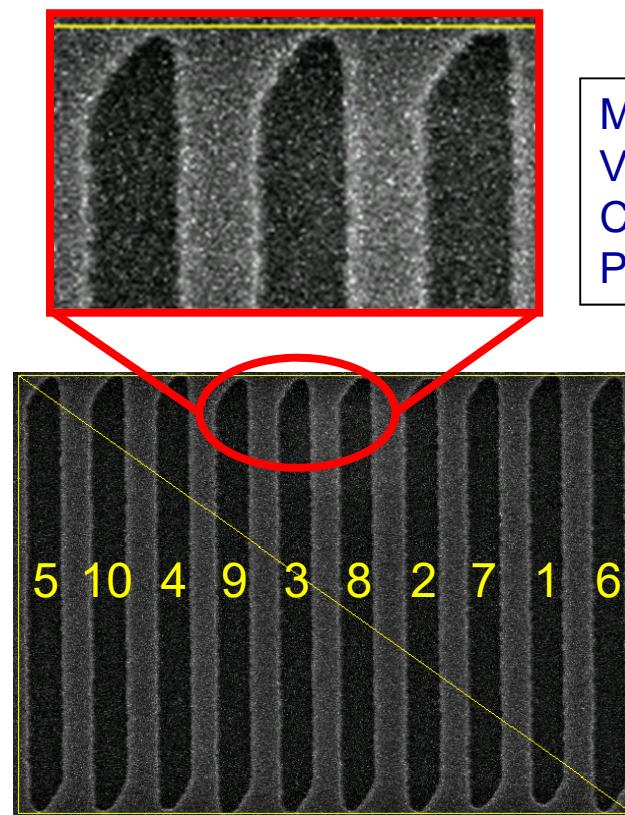
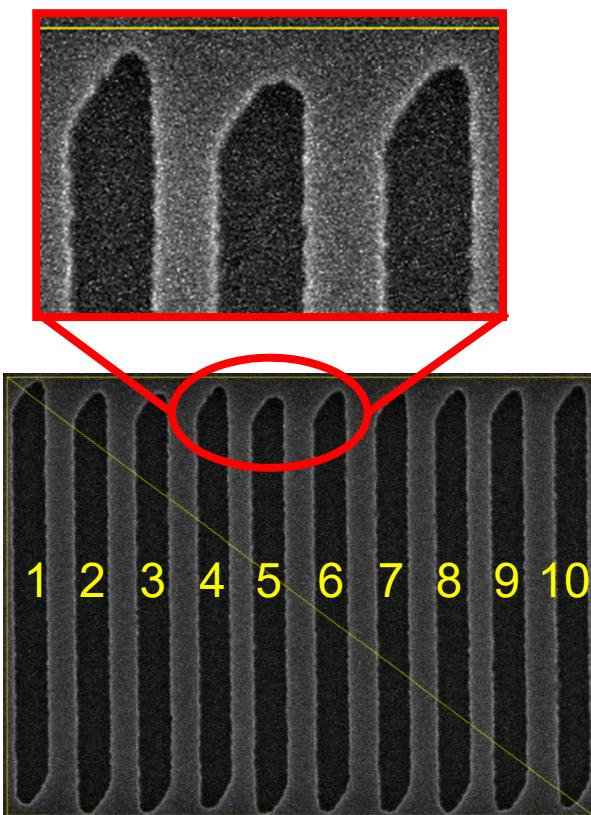
Contiguously
sequential writing



Subfield scheduling
(non-contiguously-sequential writing)

Effect of Subfield Scheduling

- Line-end roughness is improved (smaller) with subfield scheduling (non-contiguously-sequential writing)



Machine: ELS7500
Voltage: 50keV
Current: 600pA
Photoresist: ZEP520A

EE Times on Our EBL Scheduling



News & Analysis

ISPD: Semiconductors aim for 8-nm node

R. Colin Johnson

4/6/2012 04:35 PM EDT

To solve e-beam's throughput problems, Lin described efforts to use massively parallel e-beams at KLA-Tencor Corp. (Milpitas, Calif.) and Mapper Lithography BV (Delft, the Netherlands), allowing thousands of simultaneous beams to speed throughput, albeit only if reliability, uniformity and accuracy can be improved.

One of the best paper nominees at this year's ISPD was from professor Yao-Wen Chang's group at National Taiwan University, which addressed the overheating problems of massive e-beam writing processes, achieved by reordering the writing sequence to better control dimensional distortions.

AnaGlobe & Synopsys: Analog Layout



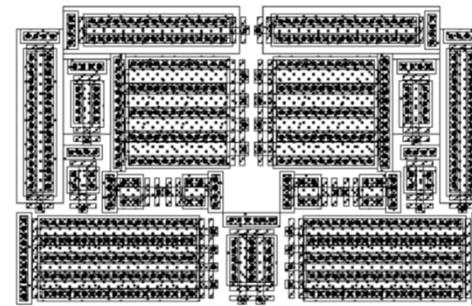
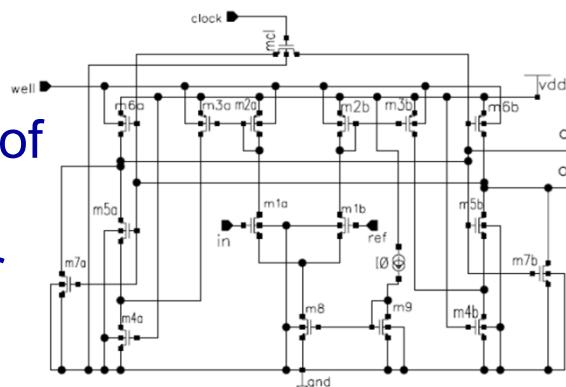
SYNOPSYS®

Analog Circuit Placement

- Devices need to be placed properly to reduce parasitic mismatches and circuit sensitivities to thermal gradients or process variations for better electrical effects and higher performance

Symmetry constraint	Proximity constraint
Preplaced constraint	Variant constraint
Fixed-boundary constraint	Boundary constraint
Minimum separation constraint	Regularity constraint

Schematic of the CMOS comparator



Placement with symmetry constraint

Basic Analog Placement Constraints (1/2)

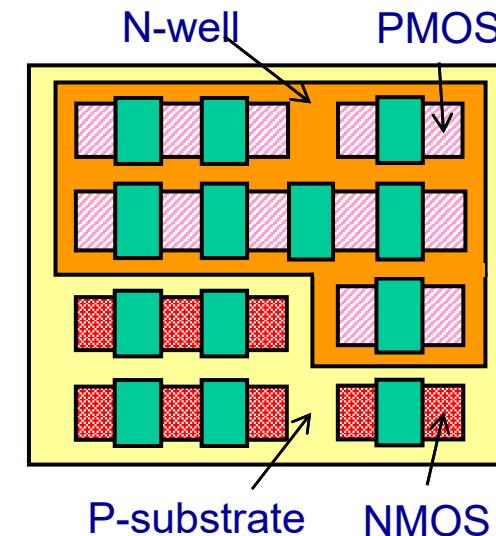
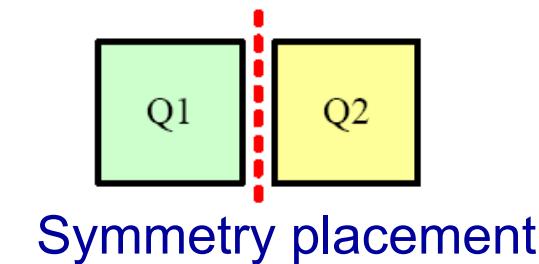
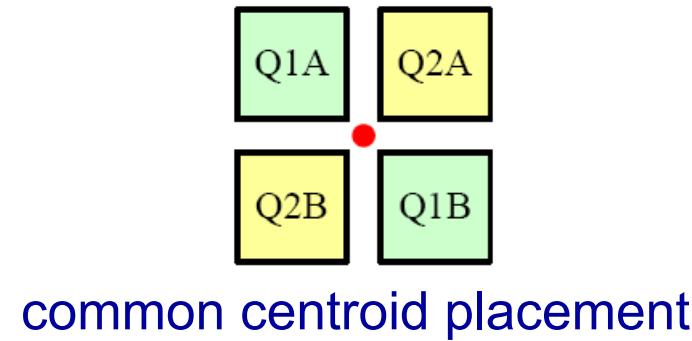
- Device matching/symmetry
 - Reduce mismatches which may cause higher offset voltages or degrade power-supply rejection ratio
 - Inter-digitized or common centroid placement: current mirrors, differential pairs, ratioed devices
 - Mirrored placement w.r.t. the vertical or horizontal symmetry axis: differential circuits

- Device proximity

- Place matched devices together or closely to reduce the impact of local variations during fabrication

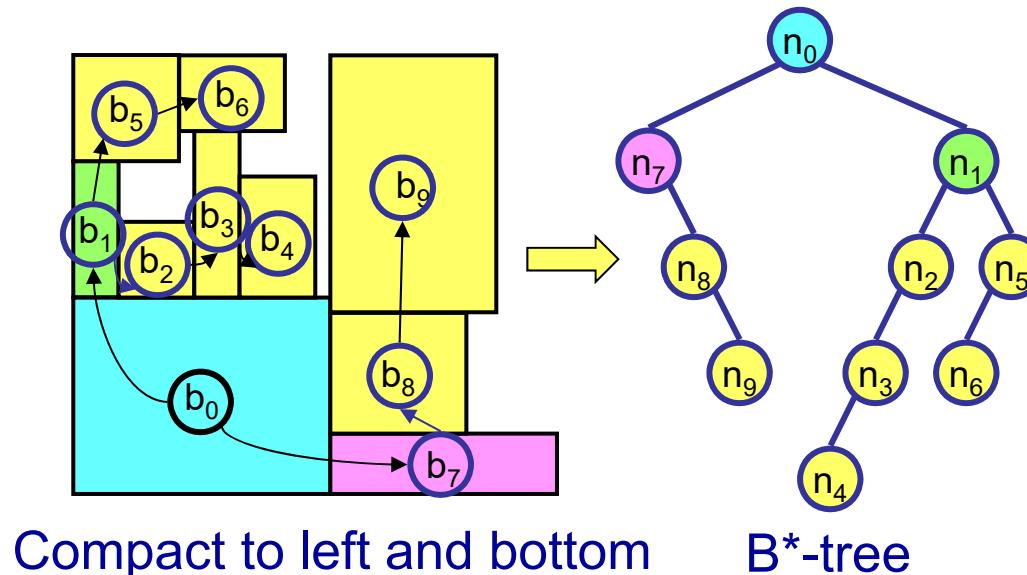
Device-proximity
placement

Y.-W. Chang



B*-Trees for Analog Placement

- Chang *et al.*, “B*-tree: A new representation for non-slicing floorplans,” DAC-2K.
 - Left child: the lowest, adjacent block on the right ($x_j = x_i + w_i$).
 - Right child: the first block above, with the same x -coordinate ($x_j = x_i$).

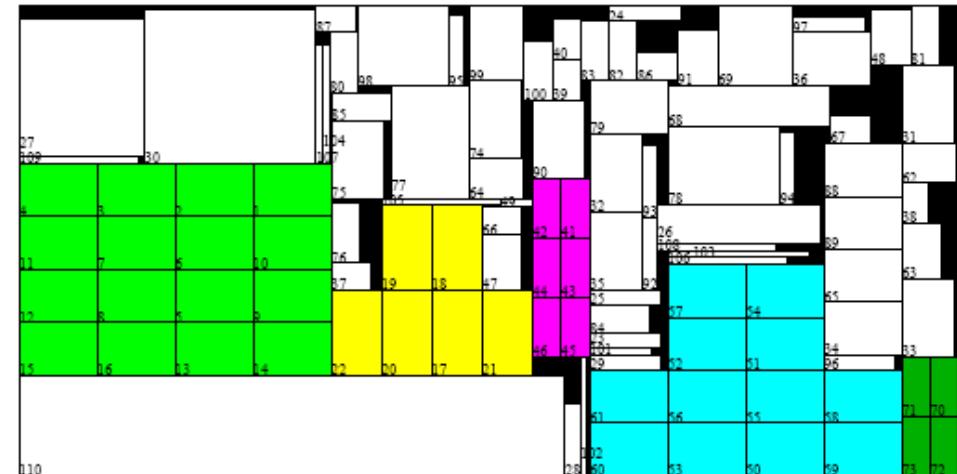


Analog Placement Examples

Circuit	biasynth_2p4g
# of Mod.	65
# of Sym. Mod.	8 + 5 + 12
Area utilization	95.53%
Runtime	22 sec



Circuit	Inamixbias_2p4g
# of Mod.	110
# of Sym. Mod.	16 + 6 + 6 + 12 + 4
Area utilization	94.59%
Runtime	43 sec



1st Linear-Time Algorithm for All the 10 Constraints

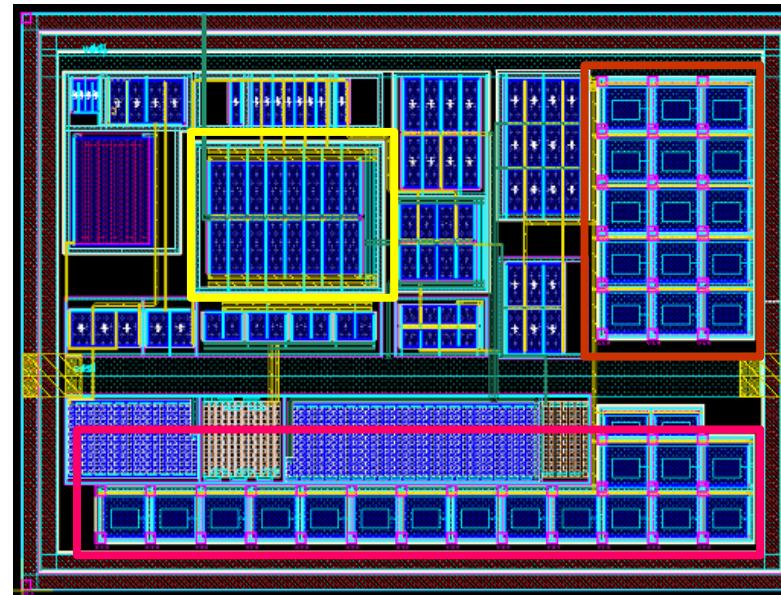
- Wu, Ou, Chang: “QB-trees: **Towards an optimal** topological representation and its applications to analog layout designs,” DAC-16.

Table 1: Comparisons of the time complexity of constraint handling and packing by tree- and SP-based representations. (“NA”: not available. Here, n is the number of modules, and k is the number of given constraints).

Work	Representation	Symmetry	Proximity	Preplaced	Fixed-boundary	Min sep.	Max sep.	Range	Boundary	Close-to-boundary	Variant
YWY00 [20]	slicing tree	NA	NA	NA	NA	NA	NA	$O(n)$	NA	NA	NA
NTN+04 [14]	SP with clustering	NA	$O(n^2)$	NA	NA	NA	NA	NA	NA	NA	NA
LCL08 [11]	HB*-tree with clustering	NA	$O(n)$	NA	NA	NA	NA	NA	NA	NA	NA
LCL09 [12]	ASF-B*-tree	$O(n)$	NA	NA	NA	NA	NA	NA	NA	NA	NA
LLH+10 [9]	ASF-B*-tree	$O(n)$	NA	NA	NA	NA	NA	NA	$O(n)$	NA	NA
TYC06 [16]	SP w/ dummy nodes	$O(n^2k)$	NA	$O(n^2k)$	NA	$O(n^2k)$	$O(n^2k)$	$O(n^2k)$	NA	$O(n^2)$	
MXT+11 [13]	C-CBL and SP w/ dummy nodes	$O(n^2k)$	NA	$O(n^2k)$	NA	$O(n^2k)$	$O(n^2k)$	$O(n^2k)$	NA	$O(n^2)$	
TCH+11 [18]	B*-tree with corner stitching	$O(n)$	$O(n)$	$O(nk)$	$O(nk)$	$O(nk)$	NA	NA	$O(n)$	NA	$O(n)$
This work	QB-tree	$O(n)$	$O(n)$	$O(n)$	$O(n)$	$O(n)$	$O(n+k)$	$O(n)$	$O(n)$	$O(n)$	$O(n)$

Preplaced
modules

changeable
aspect ratio



symmetry

[Source: Springsoft
& Po-Hung Lin]



Thank You!!

ywchang@ntu.edu.tw
<http://cc.ee.ntu.edu.tw/~ywchang>