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| FPGA device selected: |  |
| Total Number of occupied Slices: | 15822 |
| Total Number of Slice Flip Flops: |  |
| Total Number of Slice LUTs: | 63288 |
| Cortex-M0 Number of occupied Slices: | 1211 |
| Cortex-M0 Number of Slice Flip Flops: | 830 |
| Cortex-M0 Number of Slice LUTs: | 3175 |
| Bridge Number of occupied Slices: |  |
| Bridge Number of Slice Flip Flops: |  |
| Bridge Number of Slice LUTs: |  |
| Best possible clock frequency: | 62.379MHz |