Zihao (Harry) Liu

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EDUCATION

University of Edinburgh — **Edinburgh, United Kingdom**
Master's Degree in High Performance Computing — *Sep. 2023 – Sep. 2024*

- Member of TeamEPCC - Participating in the International Supercomputing Conference (ISC) Student Cluster Competition (SCC), holding in Germany at May 2024.

University of Bristol — **Bristol, United Kingdom**
Bachelor's Degree in Electrical and Electronic Engineering — *Sep. 2019 – Jun. 2023*

- **Grade:** Second Class Honours (First Division) – 68%.

Shenzhen College of International Education — **Shenzhen, China**
GCE A-Level — *Aug. 2017 – Jun. 2019*

- **Grade:** Computer Science (A*), Mathematics (A*), Physics (A*). Economics (A).

WORK EXPERIENCES

Arm — **Manchester, United Kingdom**
Hardware Engineering Intern — *Jul. 2023 – Present*

- Interned in the System Memory Management Unit (SMMU) Design Team.
- Worked on the autogeneration of RTL designs and UVM testbenches using Python. The work tackles inconsistency in register values in large designs, also aimed to automate repeated, error-prone and time-consuming coding tasks.
- Optimized existing autogeneration flow and developed new reusable features that generated over 100,000 lines of UVM testbench using less than 300 lines of scripts, also generated multiple design blocks within the RTL.
- Worked with both design (register host blocks) and verification (functional coverages) aspects of SystemVerilog.
- Rewritten part of existing flow using OOP for better readability and reusability.

Huawei Technologies Research & Development (UK) Ltd — **Cambridge, United Kingdom**
Research Intern — *Feb. 2023 – Jun. 2023*

- Constructed automated Continuous Integration (CI) using Jenkins from zero to one for the Turing CPU team.
- Enabled efficient allocation of computation resources for testing by creating cluster of machines using Kubernetes.
- Developed various Docker images based on different test environments and deployed them in Kubernetes cluster.
- Developed CI job scripts (Jenkinsfile) for various pipelines, including merge request pipelines, nightly regression pipelines, and test report generation pipelines. Worked with various plugins in Jenkins to employ additional features to pipeline that supports the work of developers.
- Developed aggregated test report generation script using Python and Pandas. Exported report in the form of Excel by processing SAIL, LLVM testsuite log files. Used matplotlib for regression statistics visualization.

PROJECT EXPERIENCES

AHB Bridge in SoC (VHDL) — **University of Bristol**
Group Leader — *Sep. 2022 – Oct. 2022*

- Constructed a microprocessor-based System-on-Chip and replaced the Leon3 processor with the Arm Cortex-M0 in a System-on-Chip, designed and implemented a bridge between the Cortex-M0 and the rest of the SoC infrastructure to establish compatible communication.
- Worked with professionally written VHDL and Verilog code and used advanced concepts such as VHDL records and generate statements, and tested the implementation efficiency by co-simulating Verilog and VHDL using Xilinx ISE.
- Received high appraisal on the performance of our group's microprocessor design by **exceeding the best achievable clock frequency** stated by the professor in place & route.

Peak Detector (VHDL) — **University of Bristol**
Group Leader — *Apr. 2021 – Jun. 2021*

- Familiarized with FPGA design in VHDL and produced a Peak Byte Detector Program that detects peak values in hexadecimal input series.
- Implemented two-phase handshake protocols using logic gates to achieve robustness and validity of data from the generator to the processor; constructed ASM charts and FSM for designing state transition codes in the project.

SKILLS & INTERESTS

Skills: English (Fluent), Chinese (Native), Python (Proficient), C (Intermediate), Linux, Bash, SystemVerilog, OOP.