CSL718 Architecture of High Performance Computers
Assignment 3
Implement Tomasulo's Algorithm

This assignment requires you to modify the in-order pipeline in Tejas to implement Tomasulo's approach to out-of-order pipelining.

Tomasulo's Approach

Base your design on the text-book description of the Tomasulo algorithm. ("Computer Architecture: A Quantitative Approach" by Hennessy and Patterson, Fifth Edition, Page 191, Figure 3.14). The features we are looking for include:

1. Issue Bound Operand Fetch
2. Reservation Stations
3. Common Data Bus (must be a ported structure)
4. Reorder Buffer, to enable control flow speculation and precise exceptions

Submission Details

- This assignment can be done in groups of two students each. You are required to submit the source code, a report and test cases that validate the code.
- You are required to modify the in-order pipeline in Tejas. Contain your changes within the package `src/simulator/pipeline/multi_issue_inorder`. Do **NOT** borrow code from other packages.
- You will have to demonstrate that your implementation is functionally correct. To do this, employ the framework provided in `src/simulator/pipeline/PipelineTests.java`.
- Your pipeline structures must be configurable – it must be possible to vary the fetch width, number of FUs of each type, ROB size etc.

- Vary the reservation station and reorder buffer sizes, and comment on the optimal size of each.
- Vary the number of ports in the CDB. Comment on the optimal number.

Another document explaining some relevant details of Tejas will be released shortly.

Deadlines

- Deadline 1 : 23:55 hrs, 28th March, 2015 - Design Document. By this point, you are expected to have understood the scheme to be implemented by you, and the software architecture of Tejas. The document must explain your understanding of the existing source, what new code must be added, and where.
- Deadline 2 : 23:55 hrs, 13th April, 2015 - Progress Report. By this point, it is expected that the coding is completed, and you are working on validation. Code (may not be functional at this point) must be submitted.
- Deadline 3 : 23:55 hrs, 20th April, 2015 - Progress Report. Functional code expected.
- Deadline 4 : 23:55 hrs, 25th April, 2015 - Final Submission. Inclusive of test cases, experimentation results.