Advanced Architecture Coursework

Scalar Processor Harry Waugh

Processor Architecture Unstruction Memory Increment Cycles > I Fetch Unit Increment Cycles V Decode Unit Increment Cycles Register File Execute Unit Main Memory

Instruction Set (MIPS Subset)

- Arithmetic ops: Add, Addi, Sub, Subi, Mul
- Logical ops: And, Or, Srl, Sll
- Data Transfer: Li, Lw, La, Sw, Mv
- Branch: Beq, Blt, J
- System: Exit

Benchmarks

- GCD
- Factorial
- Sum N Natural Numbers
- Bubble sort
- More coming soon...