Selenium coated CMOS passive pixel array for medical imaging

Shaikh Hasibul Majid*[a], Amir H. Goldan[a], Bahman Hadji[a], George Belev[c], Safa Kasap[b], Karim S. Karim[a]

[a]Dept of Electrical and Computer Engineering, University of Waterloo, ON, Canada N2L 3G1;
[b]Dept of Electrical and Computer Engineering, University of Saskatchewan, SK, Canada S7N 5A9;
[c]Canadian Light Source, Saskatoon, SK, Canada

ABSTRACT

Digital imaging systems for medical applications use amorphous silicon thin-film transistor (TFT) technology due to its ability to be manufactured over large areas. However, TFT technology is far inferior to crystalline silicon CMOS technology in terms of the speed, stability, noise susceptibility, and feature size. This work investigates the feasibility of integrating an imaging array fabricated in CMOS technology with an a-Se detector. The design of a CMOS passive pixel sensor (PPS) array is presented, in addition to how an 8×8 PPS array is integrated with the 75 micron thick stabilized amorphous selenium detector. A non-linear increase in the dark current of 200 pA, 500 pA and 2 nA is observed with 0.27, 0.67 and 1.33 V/micron electric field respectively, which shows a successful integration of selenium layer with the CMOS array. Results also show that the integrated Selenium-CMOS PPS array has good responsivity to optical light and X-rays, leaving the door open for further research on implementing CMOS imaging architectures going forward. Demonstrating that the PPS chips using CMOS technology can use a-Se as a detector is thus the first step in a promising path of research, which should yield substantial and exciting results for the field. Though area may still prove challenging, larger CMOS wafers can be manufactured and tiled to allow for a large enough size for certain diagnostic imaging applications and potentially even large area applications like digital mammography.

Keywords: Amorphous selenium, direct conversion X-ray imager, Medical imaging, CMOS array

1. INTRODUCTION

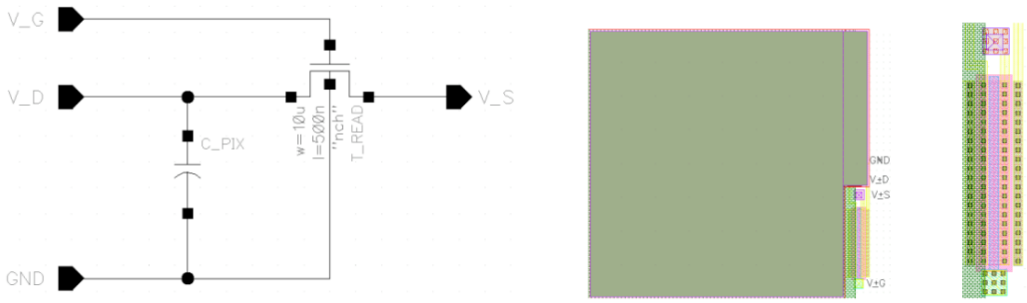
Direct detection flat panel imagers for x-ray imaging using amorphous selenium as its photoconductor layer in combination with amorphous silicon thin film transistor (TFT) PPS arrays demonstrate high image quality at a lower dark current because of the high resistivity of selenium, offer large area imaging at a relatively lower cost because of the availability of silicon and simplicity in fabricating PPS arrays. However, performance in the image lag due to the slower charge carrier of amorphous selenium (s-Se) and slower response of amorphous silicon (a-Si) make these devices unsuitable of faster imaging devices such as tomography. A novel approach to overcome the 'slowness' of these detectors is to use CMOS PPS arrays instead of using amorphous Si PPS arrays. In terms of the speed, CMOS arrays perform much faster response than the Si arrays, which motivated us to initiate an investigation to build such devices. The most attractive feature of these devices is that they can be fabricated without such a high level of design complexity, hence provides us with an easier fabrication process and a better success rate in building those devices.

2. CMOS PPS ARRAY DESIGN

In this work the PPS architecture was chosen for the array due to its simplicity. The CMOS chip was designed and laid out using Cadence Design System's electronic design automation software suite and fabricated in the 0.18 μm process through CMC Microsystems. Based on the wafer space granted by CMC, the 8×8 array of 40 μm pixel pitch. The 0.3 mm thick CMOS die has an area of 1.0 mm × 2.8 mm, which allowed us to incorporate the 320 μm × 320 μm active pixel area along with plenty of space for the bond pads. A bottom up process was used to create a single cell that was instantiated repeatedly to create the overall block. Screenshot of the cadence schematic of the cell is shown in figure 1(A).

*hasibul.majid@uwaterloo.ca; phone 1 519 888-4567 x.33799; uwaterloo.ca

Medical Imaging 2011: Physics of Medical Imaging, edited by Norbert J. Pelc, Ehsan Samei, Robert M. Nishikawa,
Proc. of SPIE Vol. 7961, 79614L · © 2011 SPIE · CCC code: 1605-7422/11/$18 · doi: 10.1117/12.877684



(A) (B)

Figure 1: A) Schematic diagram of a single PPS pixel cell using Cadence; B) Layout of a single CMOS PPS pixel

The cell contains the PPS read transistor as well as the pixel capacitor. The four pins V_G, V_S, V_D and GND are the read line connected to the gate of the PPS transistor, the data line connected to the source of the transistor, the pixel detector node on top of which the detector will be coated and the ground respectively. Layout of the single pixel cell is shown in figure 1(B). Channel length and the channel widths are 10 μm and 5 μm respectively. The drain contact of the transistor was connected to the top metal layer of the CMOS process, which is the 6th layer and known as *metal6* layer. This layer, which also made up the top electrode of the pixel capacitor, was exposed by forgoing the top layer protective oxide over this area to allow for the amorphous selenium detector to be deposited on top and accumulate charge on the node. The shaded grey area represents the active area of the pixel that collects charge generated by photons striking the detector. The calculated pixel fill factor is 99.1% in this design.

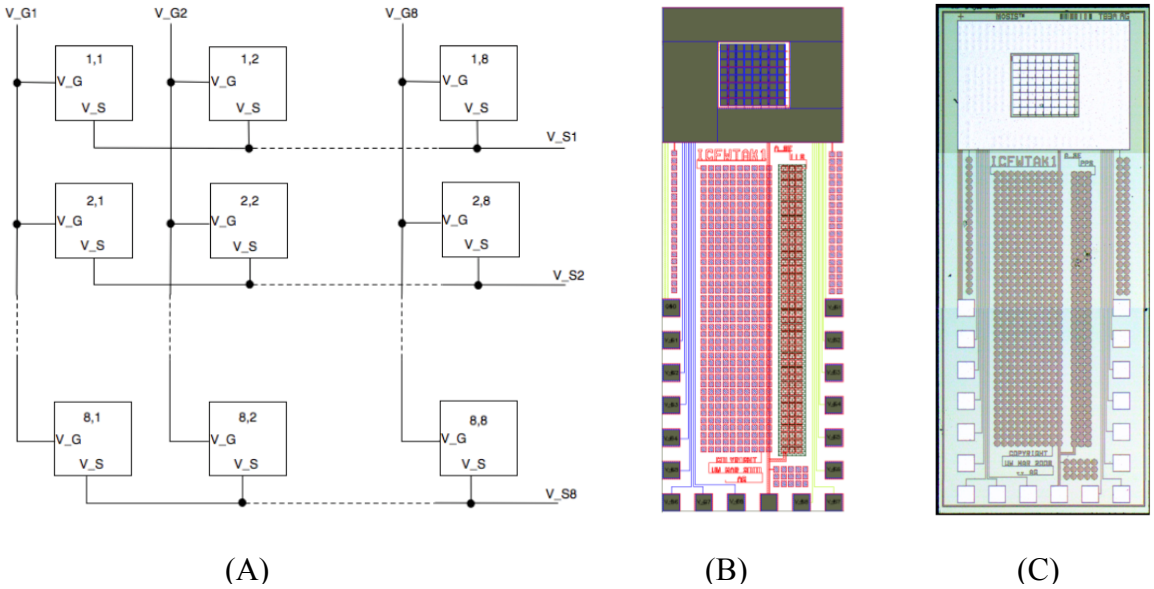
The pixel capacitor was made using the capacitor top metal (CTM) layer of the CMOS process with the area of 30 μm × 30 μm. The CTM layer is a special layer exclusively meant for making Metal-Insulator-Metal (MIM) capacitors integrated in the process. The CTM layer was connected to the *metal6* layer by placing several vias in an array throughout the area while *metal5* layer was laid out over the entire pixel area. The *metal4*, *metal3*, *metal2* and *metal1* layers were only laid out around the perimeter of the pixel as guard rings and connected to each layer above through vias. The *metal1* layer was then routed on the right side to the pixel's ground pin, causing the pixel capacitor between the

Figure 2: Cross section of a pixel on the CMOS die showing the formation of pixel capacitance

CTM and the *metal5* layer through the interlayer dielectric (ILD) separating the two. Figure 2 shows a cross section of a pixel showing formation of the capacitor. The pixel capacitor was desired to have a value of 1 pF.

The single PPS cell was then instantiated 64 times, in eight rows and eight columns to form the 8×8 array. The V_G nodes of every cell in a row were connected to each other while the V_S nodes of every cell in a row were connected to each other, such that the array had eight *read* line inputs – V_G1 through V_G8 – and eight *data* line outputs – V_S1

through V_S8. The array also had 64 V_D inputs, which would be where each pixel accumulates charge on its pixel



(A) (B) (C)

Figure 3: (A) 8 X 8 PPS array interconnection; (B) Full layout of PPS chip; (C) Micrograph of the die

capacitor at the drain of the PPS transistor and corresponding to each individual cell's V_D pin. Figure 3(A) shows the arrangement of the 8×8 array's interconnections. The top-level layout of the chip is shown in figure 3(B), where the bond pads and the active pixel area is clearly illustrated. Figure 3(C) illustrates the micrograph of the fabricated die.

3. INTEGRATION OF THE PHOTODETECTOR

In the present work a layer of amorphous selenium was used as the photodetector layer of the device. For last few decades amorphous selenium has been used as the photodetector layer for direct detection imagers [i]. However, the structure of a-Se, left to it without being stabilized, is prone to crystallization over time, causing its performance as a detector to degrade until it loses its photogenerative properties completely [ii]. Extensive research has been done in the study of alloying a-Se to prevent this unwanted crystallization, while also improving its charge transport characteristics to prevent trapping of the generated EHPs (thus increasing carrier lifetime) [iii]. It has since become established that alloying a-Se with a small amount of arsenic (As), typically in the range from 0.2% to 0.7% (w/w) makes the structure stable creating more defects for the charge carriers. In order to improve the charge collection efficiency the alloy is doped with a few parts per million of chlorine (Cl), typically in the range between 10 to 40 ppm.

Evaporation technique was used to deposit selenium on the active pixel area. The technique used to make these devices are described somewhere else [iv]. The fabrication of the a-Se detector on top of the CMOS PPS chips was done at the Electronic Materials and Devices Research Centre at the University of Saskatchewan. The deposition of the a-Se detector was done in two layers. The composition of the alloyed selenium used for the first layer of evaporation was 0.3% As and 2.5 ppm Cl, known to be stable composition with good charge transport properties. The substrate temperature was kept at 60°C while the boat temperature for evaporating the alloy was 295°C. Deposition was done for 22 minutes to deposit a layer of a-Se from this alloy that was 67 µm to 68 µm thick. The second layer used a slightly different alloy composition, at 2% As and doped with an Alkali metal as opposed to Cl. This alloy was evaporated for four minutes while the substrate was kept at 60°C and the boat was kept at 310°C, resulting in a layer of about 8 µm to 9 µm being deposited on top of the previous layer. This gave a total thickness for the a-Se detector of about 75 µm. The use of the higher As-rich alloy for the much thinner top layer trades off charge transport in exchange for higher resistivity at the surface, which keeps the leakage current of the a-Se detector low. The top contact was made by depositing chromium (Cr) using evaporation method.

4. DESIGN AND ASSEMBLY OF PPS READOUT AND INTEGRATION OF THE DETECTOR CHIP

A printed circuit board (PCB) was designed and fabricated in order to allow for the driving stimulus for the PPS array

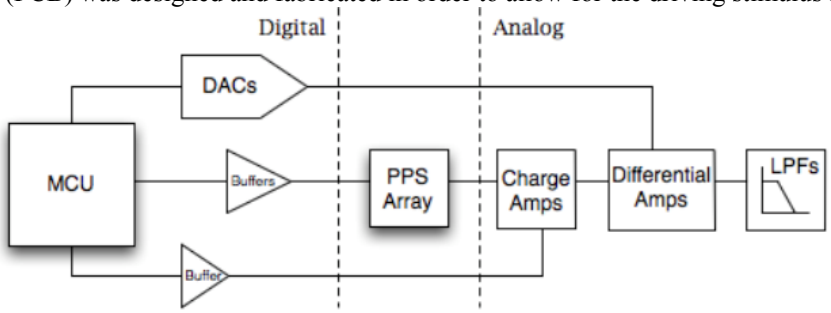


Figure 4: Block diagram of the PPS array tester

and to capture its output with readout circuitry. This section outlines the parts used in the design and how they were integrated together on the PCB. CadSoft's EAGLE software was used for the schematic design and board layout. The design process involved outlining the requirements of the test system, selecting the components that were required and creating an EAGLE library to use them, and, following schematic entry, doing the PCB layout and sending it to fabrication. The design used surface mount (SMD) components almost exclusively to allow for a clean and compact layout. Figure 4 shows a generalized top-level block diagram of the PCB to illustrate the major components and how they interact with each other. Digital parts on the PCB required positive voltages of 1.8 V and 5 V, while analog parts required differential voltages of +/-5 V to allow for signals to swing above and below zero volts. Thus, a DC input to the board of +/-9 V would suffice to allow for the required voltages, utilizing large decoupling capacitors of 220 μF.

A MC68HC908MR32 microcontroller (MCU) was used to govern the operation of the chip by providing the input signals from the device. The microcontroller (MCU) uses an 8 MHz system clock, two separate timer modules comprising of six channels together, and a serial-peripheral interface (SPI) module for easy interfacing. The software for the MCU was written in assembly language. Two buffering chips were used in between the MCU and the targets it was used to drive. The buffers were necessary to protect the MCU from sinking too much current through its output pins. The buffers would also allow for shifting of the high logic level from the MCU's 5 V level to the PPS array's 1.8 V level. The MCU was also responsible for programming eight digital-to-analog converters (DACs) on the PCB through its SPI module. Each DAC would output an independent voltage based on the digital word written to it by the MCU. The use of these voltages, one per line, was to cancel out the deterministic noise injected into the system at the output of the charge amplifier, by feeding the pair of signals into a differential instrumentation amplifier. The DACs used were Maxim MAX5170 chips in 16-pin QSOP packages, which used the 5 V digital rail. The purpose of the charge amplifier is to provide a stable output voltage after readout based on the charge that is accumulated on the pixel capacitor during integration. The charge amplifier chip used was Burr Brown's ACF2101 in a 24-pin SOIC surface mount package, each of which contains two charge amplifiers. The chip requires a dual power supply of +/-5 V, and thus made use of the 5V and -5V analog voltage rails. The output of the charge amplifier has the signal riding on a deterministic noise voltage, due to the fact that when the reset signal is deasserted and the switch across the charge amplifier is opened, an amount of charge is injected onto the feedback capacitor in a phenomenon referred to as charge injection. Thus, through the use of a differential amplifier stage, this constant level can be eliminated by connecting the charge amp output to its positive input and a DAC outputting the measured charge injection level to its negative input. So if the DAC level is calibrated correctly, the gain of the differential amplifier optimally amplifies only the signal part of the charge amplifier output. The differential amplifier used was Analog Devices's AD8228 instrumentation amplifier, which provides two fixed gain settings, 10 or 100. The final stage of the analog signal processing was a low-pass filter designed to eliminate high-frequency noise on the signal. This was done with an active RC filter consisting of an opamp with a resistor and capacitor across its negative feedback path to set the cutoff frequency and a resistor at its input to set the filter gain. The opamp used was the Analog Devices AD8655 chip.

The selenium coated detector chip had to be placed on a specially designed printed circuit board (PCB) substrate, or daughterboard, such that it could be held in place while being wirebonded and to allow for easy integration with the

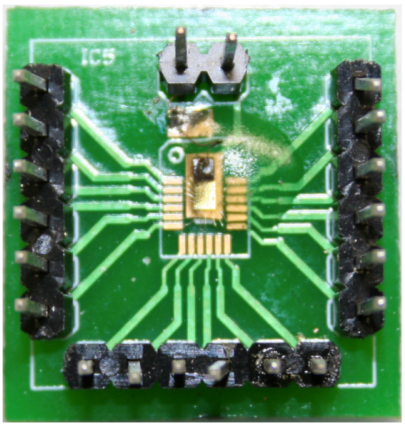


Figure 5: Test daughterboard with wirebonded and encapsulated PPS chip

testing environment. The daughterboard is shown in figure 5 and was designed and fabricated alongside the test PCB.

5. RESULTS

5.1 Validation of the CMOS chip: In order to validate the CMOS chips tests were conducted before pursuing any further experiments. The current versus voltage (I-V) test was performed using an Agilent 4156C Semiconductor Parameter Analyzer (SPA) in conjunction with an Agilent 16442A test fixture. Figure 6 shows the I_D-V_{GS} curve

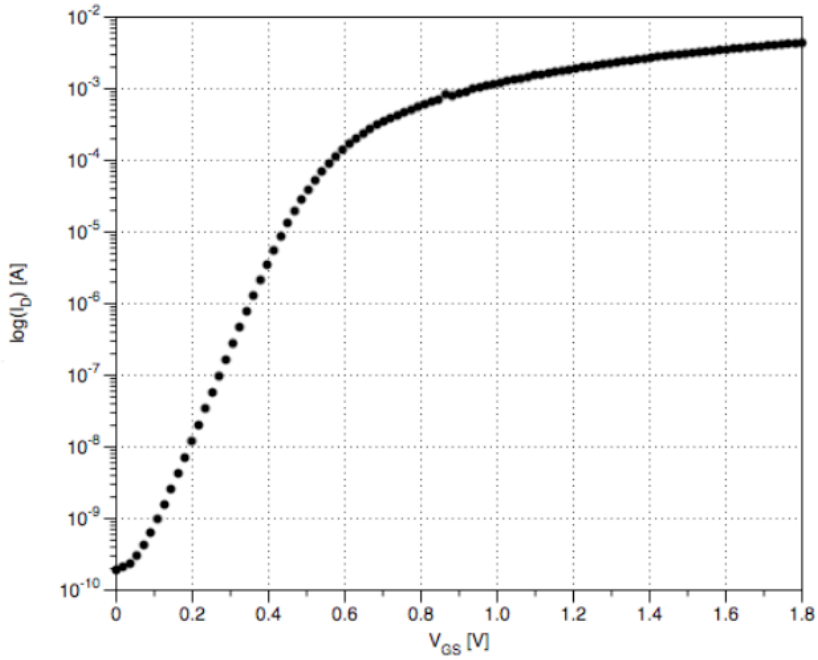


Figure 6: I_D vs V_{GS} curve with I_D plotted logarithmically to show the sub-threshold leakage in the NMOS transistor

where the I_D is plotted in logarithmic scale to show the sub-threshold leakage of the transistor. Figure 7 shows

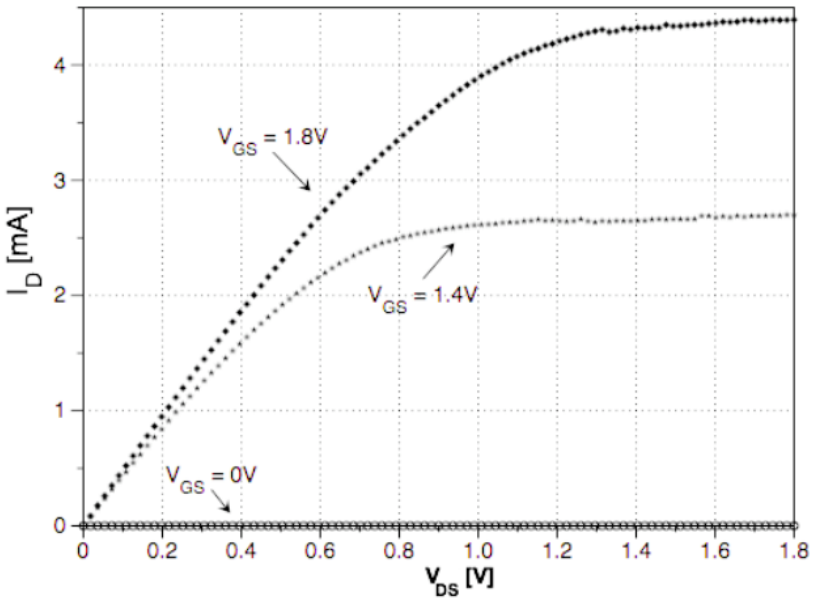


Figure 7: I_D vs V_{DS} graph for an on-pixel transistor in the array with varying V_{GS} values

the I_D-V_{DS} curves at three different V_{GS}, valued at 0, 1.4 and 1.8 volts. These graphs correspond to the proper operation of an NMOS transistor in 0.18 micron CMOS technology with a threshold voltage (V_t) of about 0.5 V.

5.2 Electric field bias in the dark: A positive dc voltage was applied at the top electrode of the detector while keeping the detector assembly in the dark environment in order to test the photodetector layer. The associated current is known as dark current (I_{DARK}). The applied electric field was kept low so that a larger amount of dark current might not damage the whole device. Initially the detector was relaxed at a zero electric field. A test sequence was programmed in the SPA so that it can measure the dark current with the respective applied voltages. Table 1 shows the sequence of the testes at different electric field biases and their descriptions, while figure 8 illustrates the setup of the test.

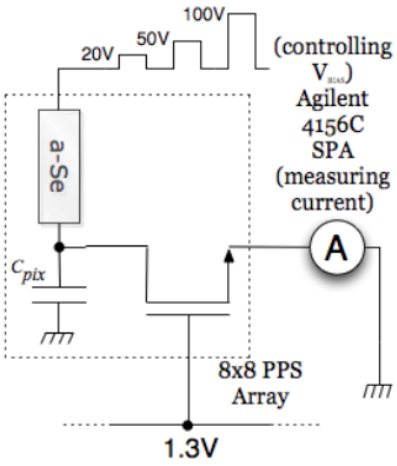


Table 1: Electric field bias test sequence

Sequence Number	Test Description	V_{bias}	Duration
1	0.27 V/µm Electric Field Bias	20 V	1 hour
2	Relaxation Period	0 V	1 hour
3	0.67 V/µm Electric Field Bias	50 V	1 hour
4	Relaxation Period	0 V	1 hour
5	1.33 V/µm Electric Field Bias	100 V	1 hour

Figure 8: Dark current measurement setup

The results of the test are shown in figure 9, with current versus time plotted on a log-log scale. It can be seen that as the electric field bias increases, the dark current through the detector increases such that the settled dark current is about 2

nA, 500 pA, and 200 pA for 1.33 V/µm, 0.67 V/µm, and 0.27 V/µm respectively. The transient behaviour of the a-Se is

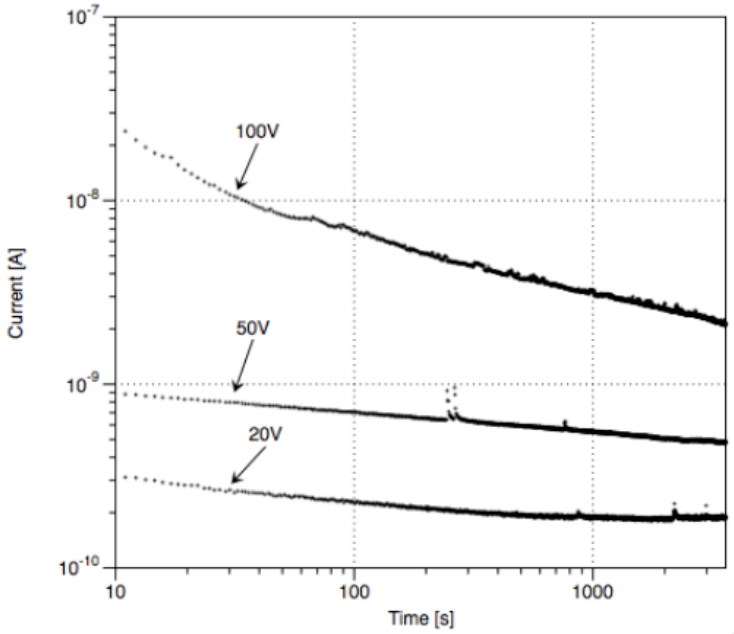
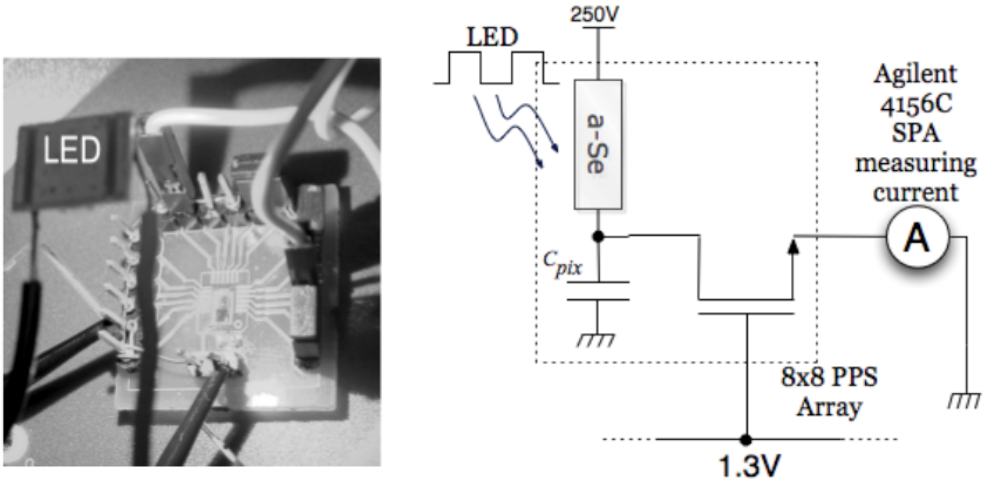


Figure 9: Dark current at three different electric fields

also apparent, as the current is still decaying at the end of hour long measurements. It should be noted that the current being measured henceforth was read through the PPS transistors on the CMOS array, indicating proper integrated operation of the a-Se detector and the CMOS array at the selenium-silicon interface.

5.3 Optical measurements: In order to test the photoresponsivity of the detector high power LEDs with three different wavelengths were used. Wavelengths of the blue, green and red LEDs were 465 nm, 530 nm and 636 nm respectively. Selenium's photoresponsivity extends to the optical wavelengths, gradually decreasing as the wavelength approaches red light and beyond.

The sample was allowed to relax for upwards of 16 hours between tests and the electric field bias was set to 3.33 V/um



(A) (B)

Figure 10: (A) LED positioned above the detector inside a test fixture; (B) Photocurrent test setup

(250 V) using the Canberra high-voltage power supply. Figure 10 (A) shows the setup of the sample and the LED inside the test fixture. The tests were run as transient current measurements just like the previous section; however, to illustrate

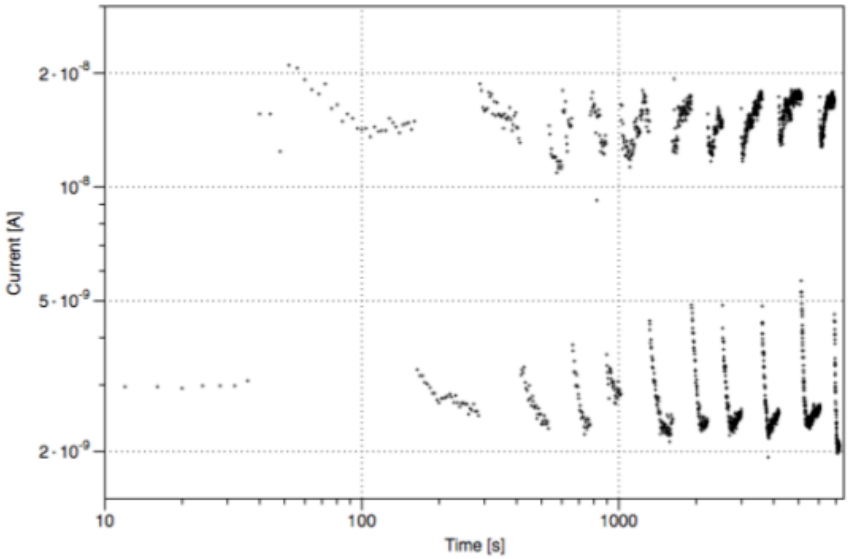


Figure 11: Photoresponse with 465 nm wavelength at 3.33 V/micron electric field

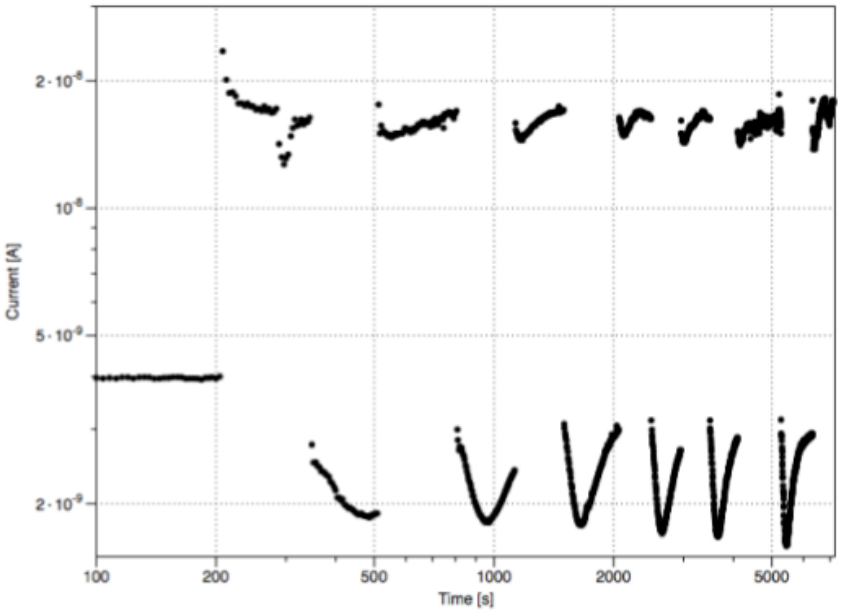


Figure 12: Photoresponse with 530 nm wavelength at 3.33 V/micron electric field

the photoresponsivity of the detector, the LED power supply was turned on and off periodically throughout the test to highlight the difference in current in the detector in dark versus light conditions. The on/off timing was two minutes initially and increased to five, ten, and fifteen minutes as time went on in the test in order to show up nicely on the logarithmically displayed transient graph. Figure 10 (B) shows the setup of the test. Figures 11, 12, and 13 show the sample's response to LEDs emitting blue, green, and red light respectively, plotted on a log-log scale of current versus time. It is apparent from the graphs that the responsivity of selenium is better to blue and green light than red light. The

on-current level for the former two wavelengths is about 20 nA as opposed to the off-current level of about 2 nA, a one order of magnitude difference. With red light, the on level is about 8 nA. The responsivity of selenium has been shown

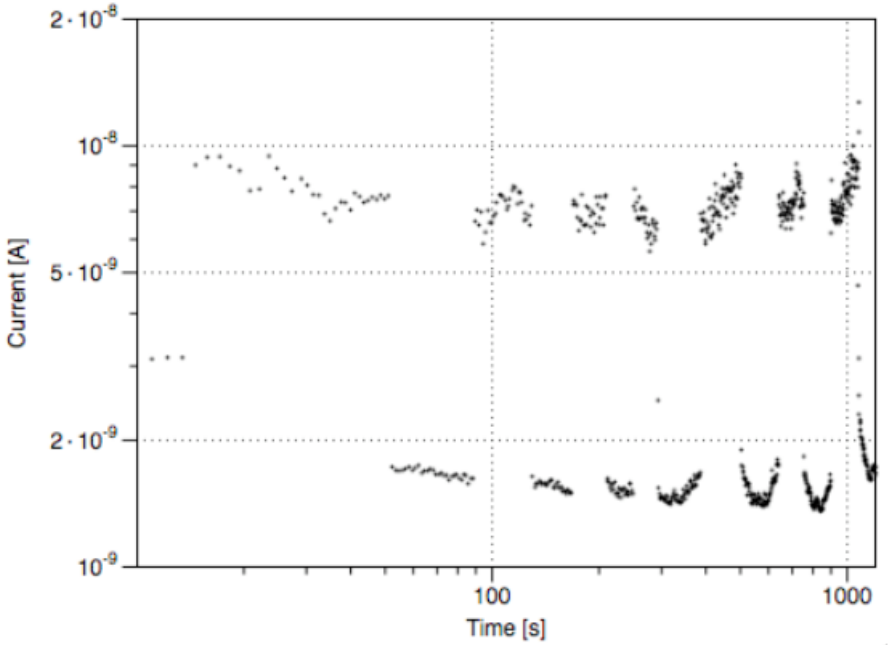


Figure 13: Photoresponse with 636 nm wavelength at 3.33 V/micron electric field

to be poorer with increasing wavelengths in literature as early as 1960 [5(19)], with a drop off that begins around the 500 nm green wavelength.

5.4 X-ray measurements: A similar sets of experiments were conducted to test the detector under the influence of X-ray. A 40 kV_P X-ray energy beam was used with 2 mA of tube current. Durations of the X-ray pulses were 30 seconds initially, increasing to one minute, then two minutes and finally five minutes. Figure 14 shows the test results.

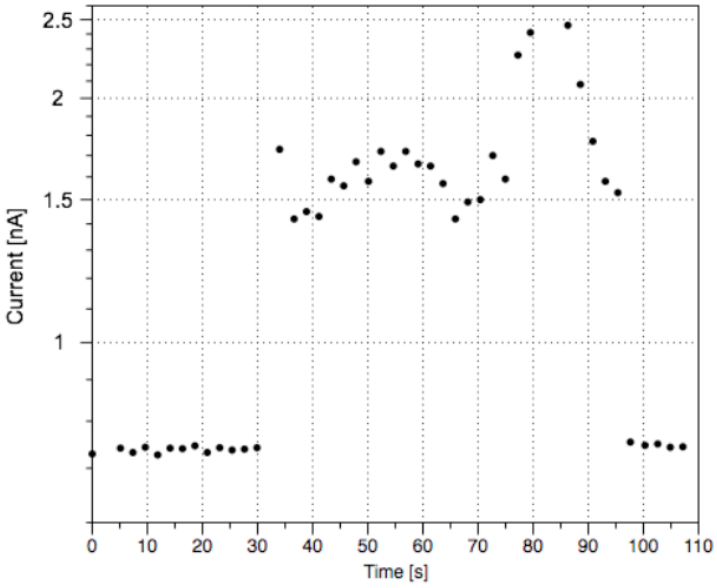


Figure 14: Transient response to single one-minute pulse from a 40 kV_P X-ray beam

The difference between the current levels through the detector when the X-ray source is on and when it is off is about 1 nA consistently based on the pulsed test. This clearly shows responsivity to X-rays. To quantify the photocurrent more clearly as was done with the optical tests, another test was run after the detector was allowed to relax again, with the X-ray System being pulsed on (again, 40 kVp at 2 mA of tube current) and being left on to measure the current, which would also allow for analysis of the linearity. The average relaxed dark current level before X-ray excitation was 0.74 nA, and the the average current that was generated during the minute that the X-ray beam was on was 1.77 nA, giving a photocurrent due to X-rays generated by the detector of 1.03 nA. The response of the detector while the X-ray beam was

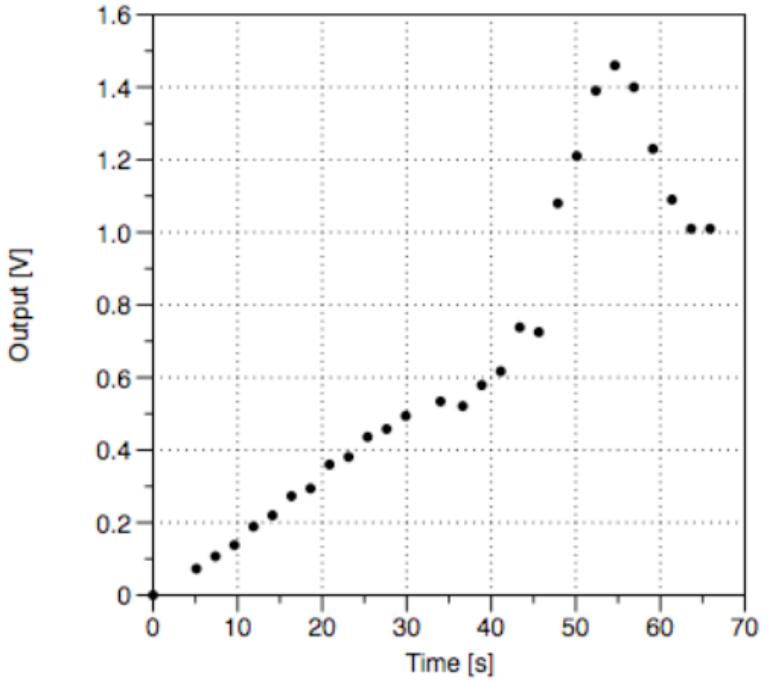


Figure 15: Selenium-CMOS detector linearity test under the influence of a 40 kV_P X-ray beam

on is shown represented as voltage accumulated on a 100 nF capacitor in figure 15 to show the detector's linearity. The dosimeter placed inside the X-ray machine during the X-ray test read dose rates varying from 205 mR/s to 220 mR/s (being on the higher near the end of the minute mark) with a total integrated dose after the test of 13.71 R. Variation in the dose rate has affected the linear characteristics towards the end of the test.

6. SUMMARY

A passive pixel sensor (PPS) array in 0.18 µm CMOS technology was fabricated in order to serve as the basis for taking the first step towards a CMOS-based medical imaging system which would be able to provide faster readout, higher resolution, and lower noise sensitivity than traditional amorphous silicon thin-film transistor digital imaging systems. Amorphous selenium was deposited on top of the active array area to provide an integrated Selenium- CMOS detector. A printed circuit board was designed to facilitate the testing of the array. The results of the PPS array were promising with optical wavelengths and X-rays from the signal current generated versus the dark current, showing very good linearity as well. Testing the array using the printed circuit board readout system showed that the output of the pixels from the array varied across it due to shadowing from the bias contact and varying charge collection efficiency across the array, confirming the operation of the array as an image sensor.

REFERENCE

[i] M.J. Yaffe and J.A. Rowlands, "X-ray Detectors for Digital Radiography", Phys. Med. Biol., Vol.42, 1–39, 1997

[ii] S.O. Kasap and J.A. Rowlands, "X-ray Photoconductors and Stabilized a-Se for Direct Conversion Digital Flat-panel X-ray Image Detectors", Journal of Materials Science: Materials in Electronics, Vol. 11, 179-198, 2000

[iii] J.C. Schottmiller, "Relationships in Selenium-alloy Films", J. Vac. Sci. Technol., Vol. 12, No. 4, 807-810, Jul 1975

[iv] Shaikh H. Majid, "Excess Noise of Amorphous Selenium Used in X-ray Detectors", PhD Thesis, University of Saskatchewan, 2009