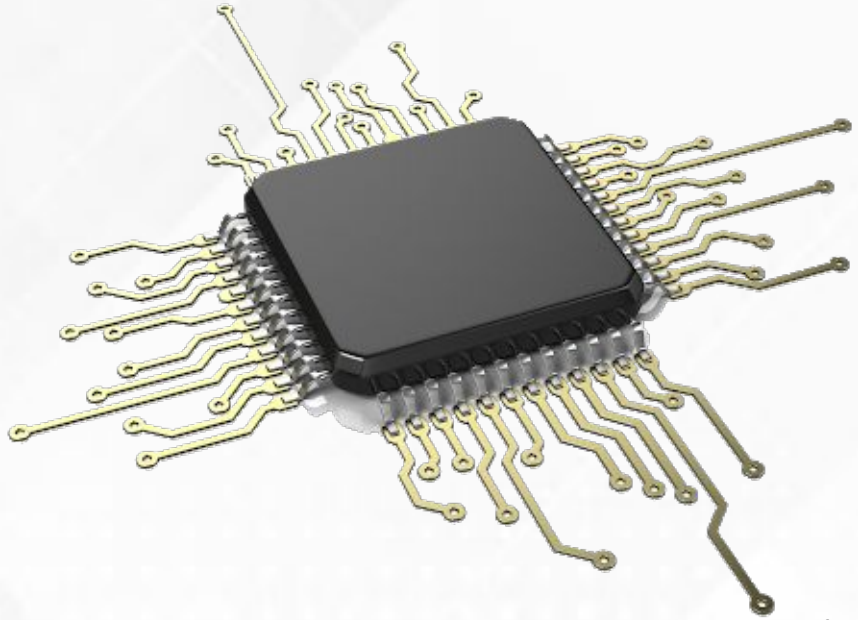
Computer Organization & Architecture
(COA)
GTU # 3140707

Dedicated Faculty, Committed Education
Darshan
Institute of Engineering & Technology

Unit-8

Input-Output Organization



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Outline

- Asynchronous Data Transfer
- Modes Of Transfer
- Priority Interrupt
- DMA
- Input-Output Processor (IOP)
- Questions asked in GTU exam

Asynchronous Data Transfer

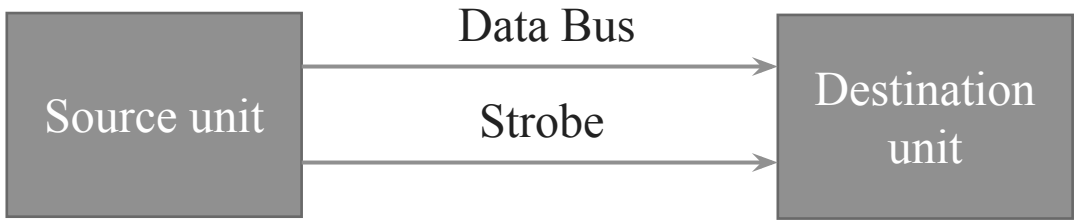
Section - 1

Asynchronous Data Transfer

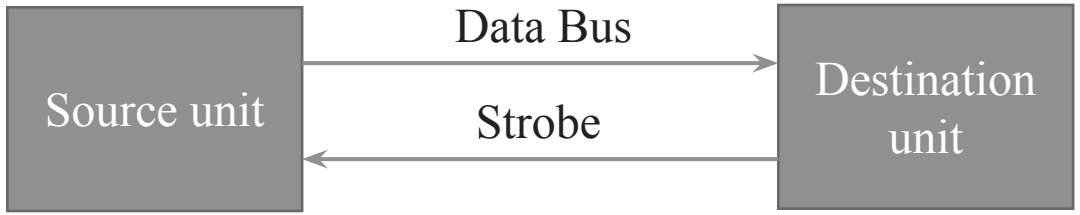
- Asynchronous data transfer between two independent units requires that control signals be transmitted between the communicating units to indicate the time at which data is being transmitted.
- Two ways of achieving
  1. Strobe
  2. Handshaking

Strobe Method

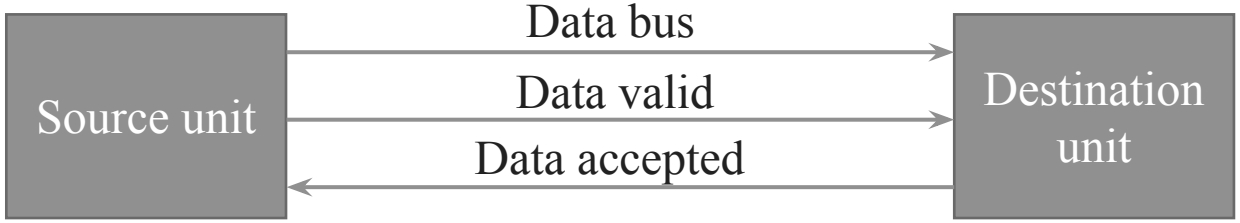
1.1 Source initiated Strobe

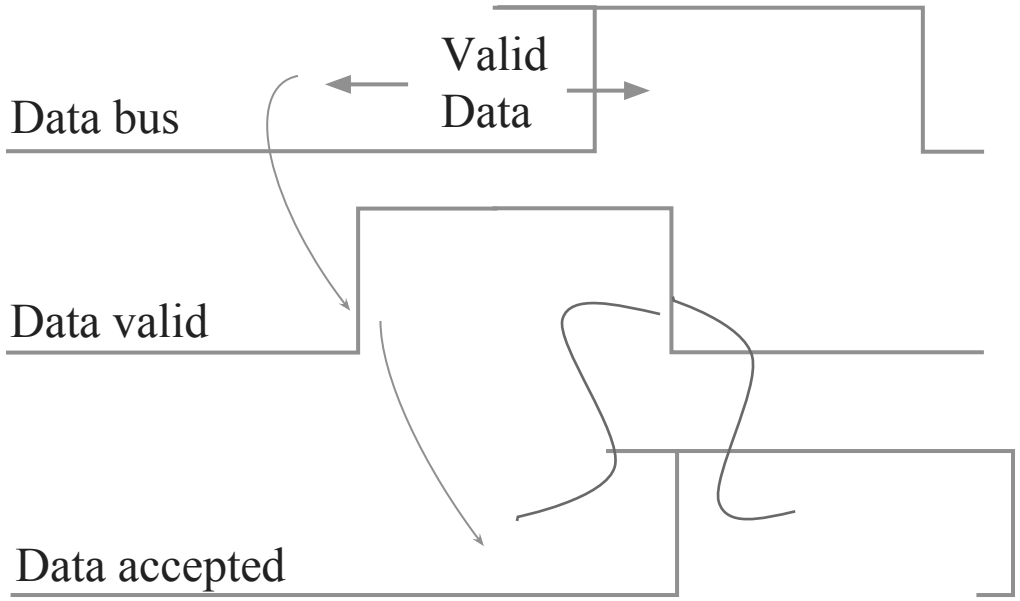


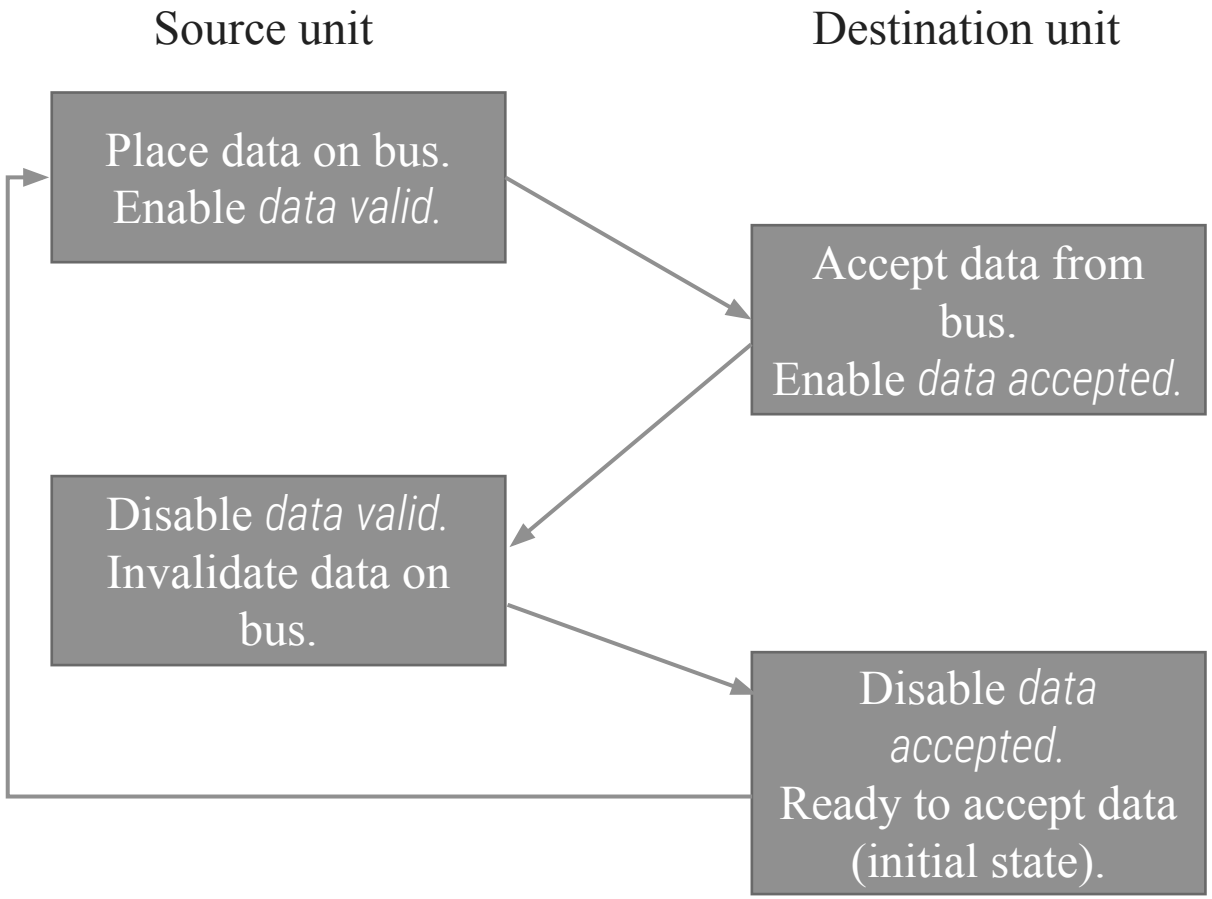
1.2 Destination initiated Strobe



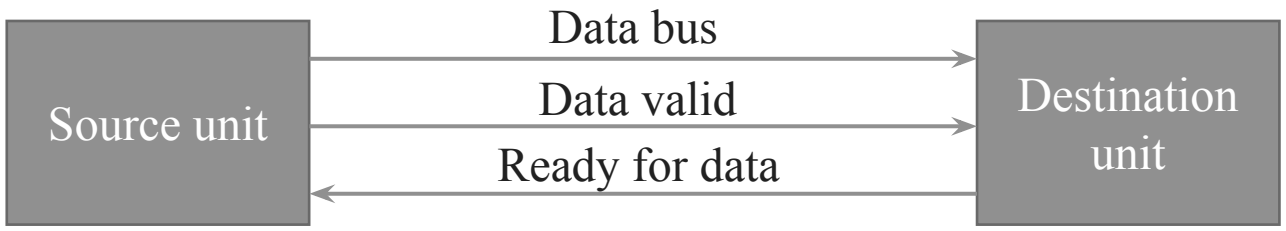
2.1 Source initiated Handshake

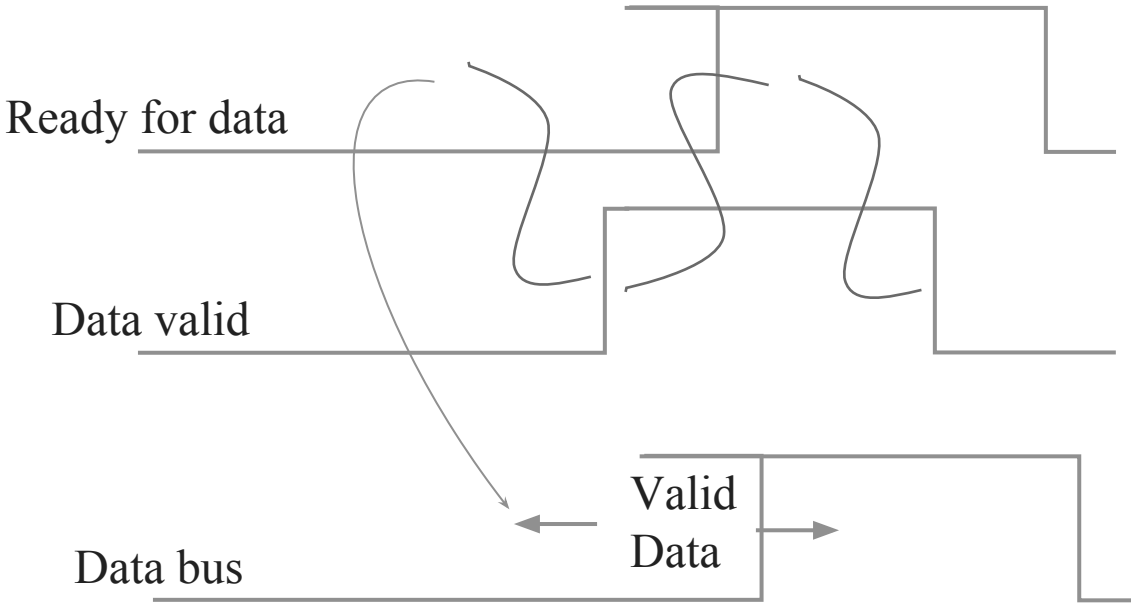


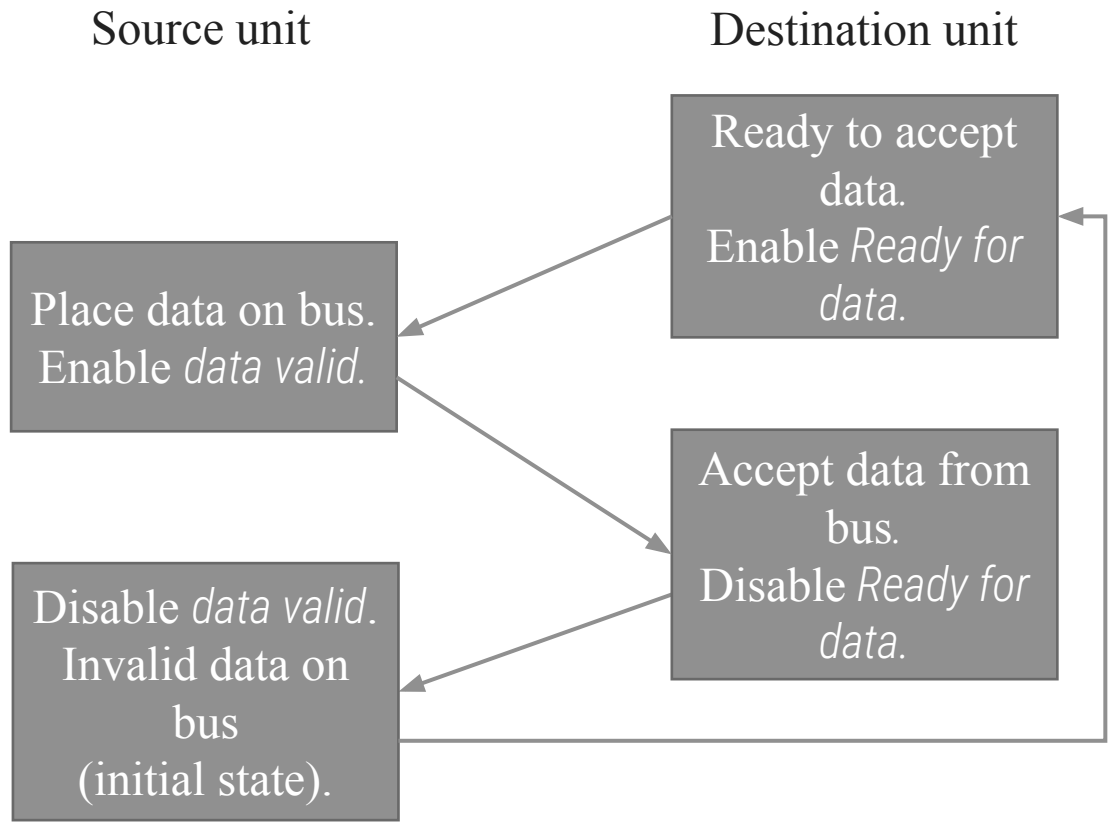




2.2 Destination initiated Handshake

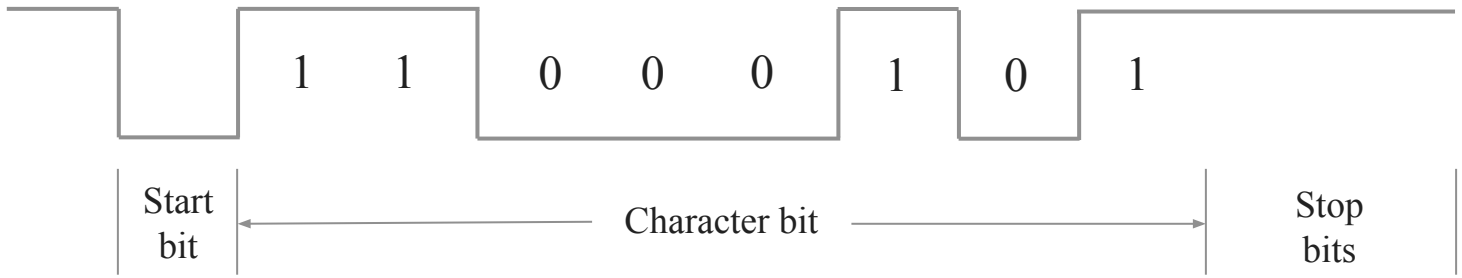






Asynchronous Serial Transfer

- Rules for transmission
  1. When a character is not being sent, the line is kept in the 1-state.
  2. The initiation of a character transmission is detected from the start bit, which is always 0.
  3. The character bits always follow the start bit.
  4. After the last bit of the character is transmitted, a stop bit is detected when the line returns to the 1-state for at least one bit time.



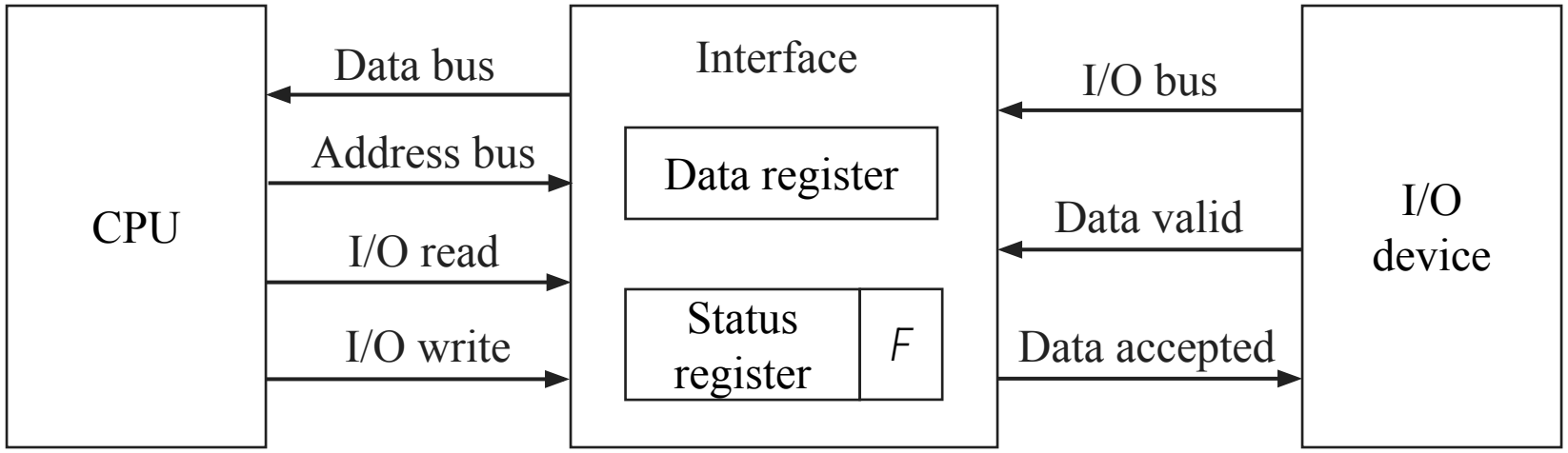
Modes Of Transfer

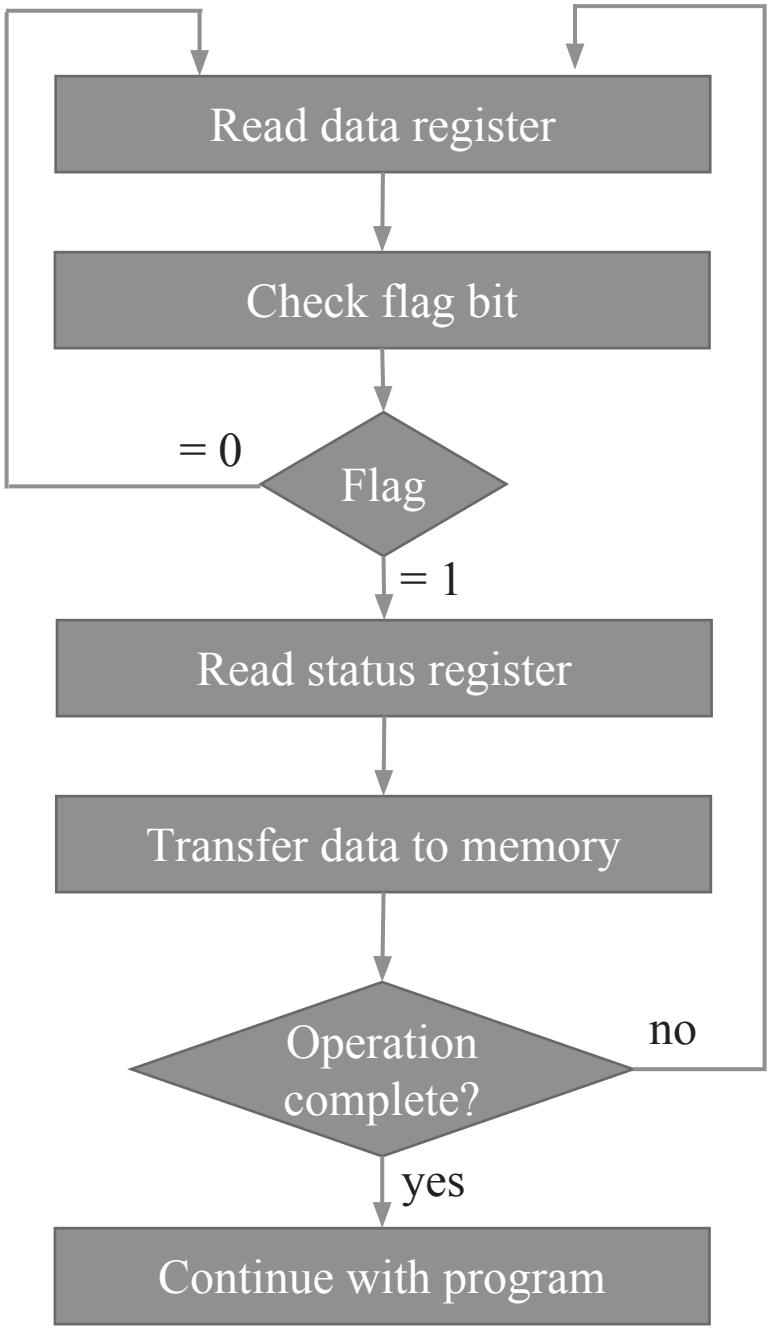
Section - 2

Modes of Transfer

- Data transfer between the central computer and I/O devices may be handled in a variety of modes.
- Some modes use the CPU as an intermediate path; others transfer the data directly to and from the memory unit.
- Data transfer to and from peripherals may be handled in one of three possible modes:
  1. Programmed I/O
  2. Interrupt-initiated I/O
  3. Direct memory access (DMA)

Programmed I/O





Interrupt-initiated I/O

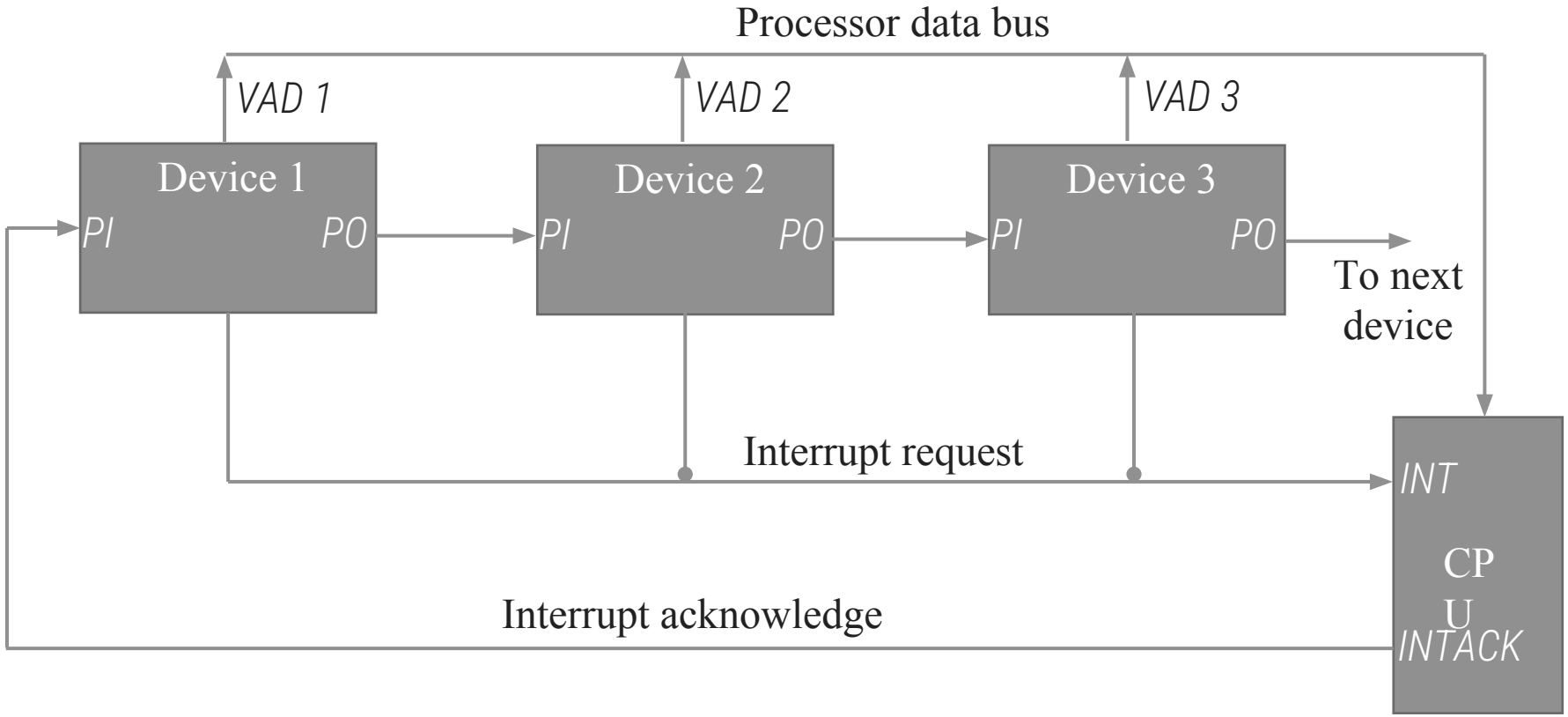
- An alternative to the CPU constantly monitoring the flag is to let the interface inform the computer when it is ready to transfer data.
- While the CPU is running a program, it does not check the flag.
- However, when the flag is set, the computer is momentarily interrupted from proceeding with current program and is informed of the fact that the flag has been set.
- The CPU deviates from what it is doing to take care of the input or output transfer.
- After the transfer is completed, the computer returns to the previous program to continue what it was doing before the interrupt.

Priority Interrupt

Section - 3

Priority Interrupt (Daisy-Chaining Technique)

- Determines which interrupt is to be served first when two or more requests are made simultaneously
- Also determines which interrupts are permitted to interrupt the computer while another is being serviced.
- Higher priority interrupts can make requests while servicing a lower priority interrupt.

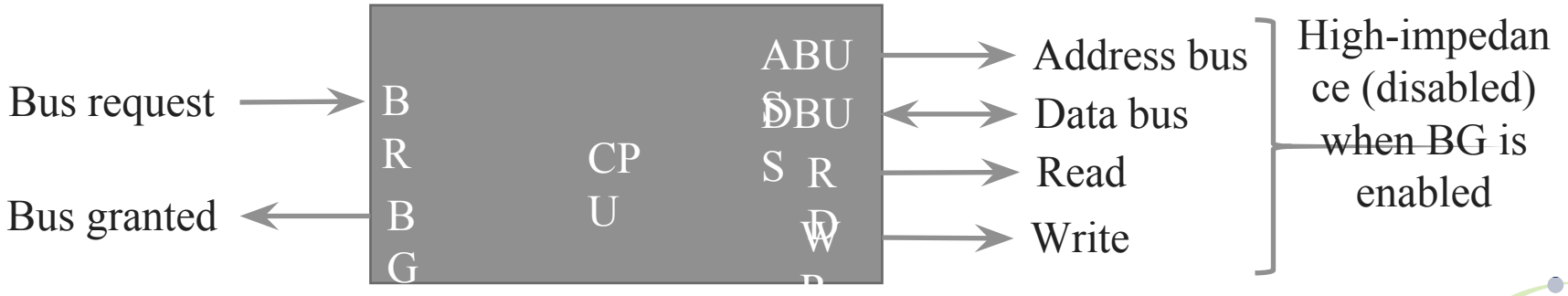


DMA (Direct Memory Access)

Section - 4

DMA (Direct Memory Access)

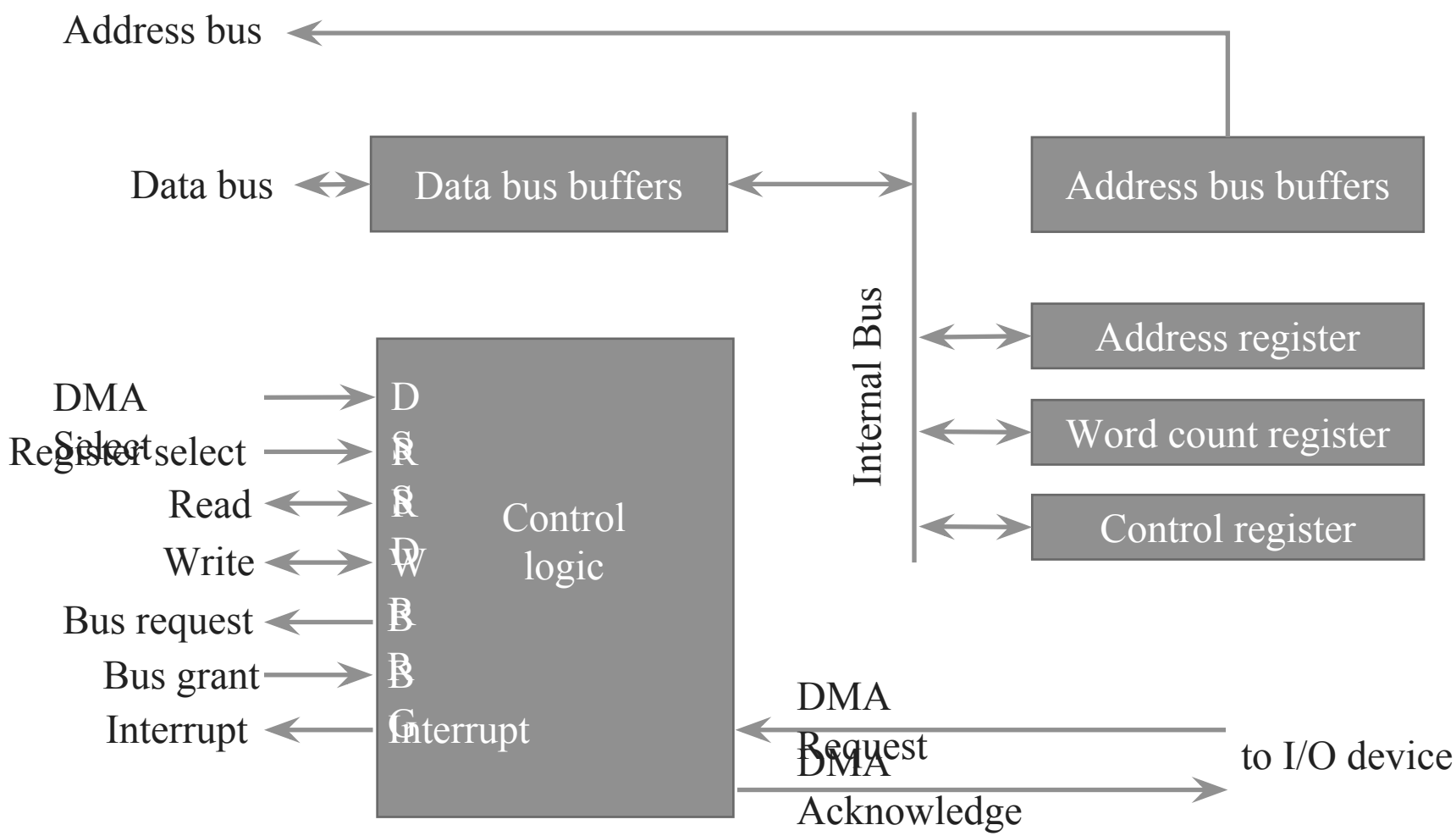
- The transfer of data between a fast storage device such as magnetic disk and memory is often limited by the speed of the CPU.
- Removing the CPU from the path and letting the peripheral device manage the memory buses directly would improve the speed of transfer.
- This transfer technique is called direct memory access (DMA).
- During DMA, CPU is idle and has no control of the memory buses.
- A DMA controller takes over the buses to manage the transfer directly between the I/O device and memory.



DMA Controller

DMA Controller

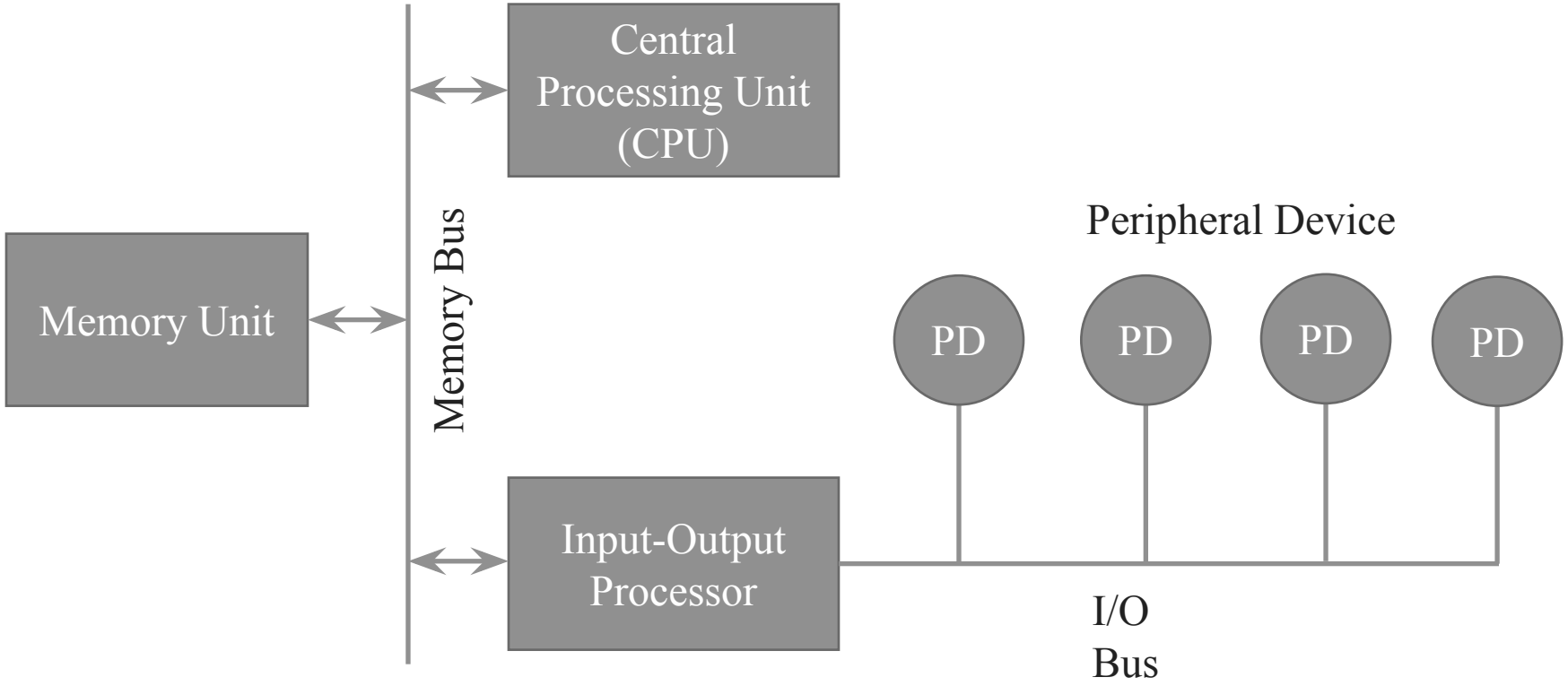
- DMA controller - Interface which allows I/O transfer directly between Memory and Device, freeing CPU for other tasks
- CPU initializes DMA Controller by sending memory address and the block size (number of words).



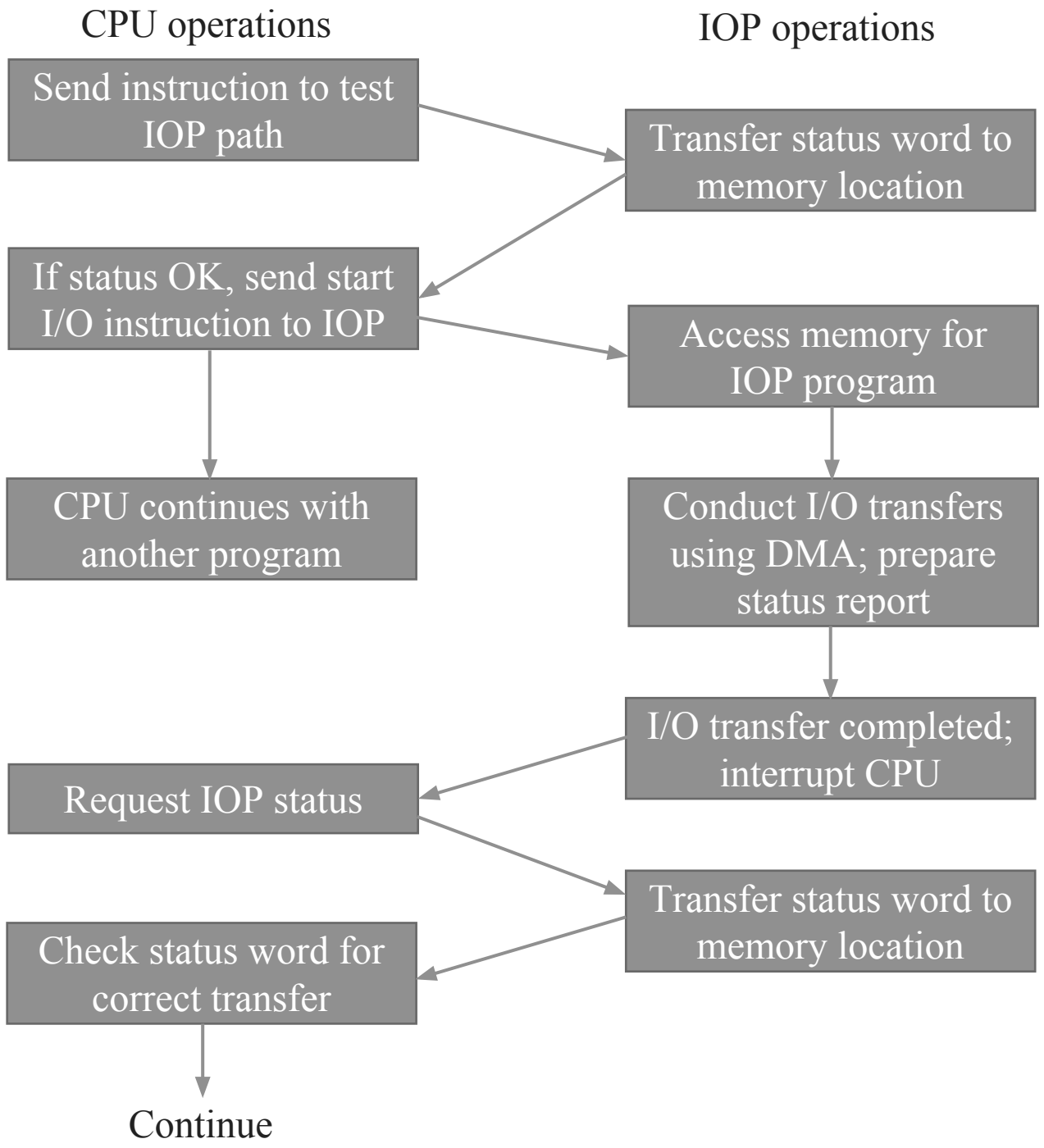
Input-Output Processor (IOP)

Section - 5

Input-Output Processor (IOP)



CPU – IOP Communication



Questions asked in GTU exam

Section - 6

Questions asked in GTU exam

1. Explain daisy chain priority interrupt.
2. Explain the DMA operation.
3. What is the use of IOP? Explain its communication with CPU.
4. Explain asynchronous data transfer using timing diagrams.
5. Differentiate isolated I/O and memory mapped I/O.
6. Differentiate Programmed I/O and Interrupt initiated I/O.
7. What are the advantages of Serial Data Transmission of data?
8. Briefly explain source initiated transfer using handshaking.
9. Enlist possible modes of data transfer to and from peripherals.