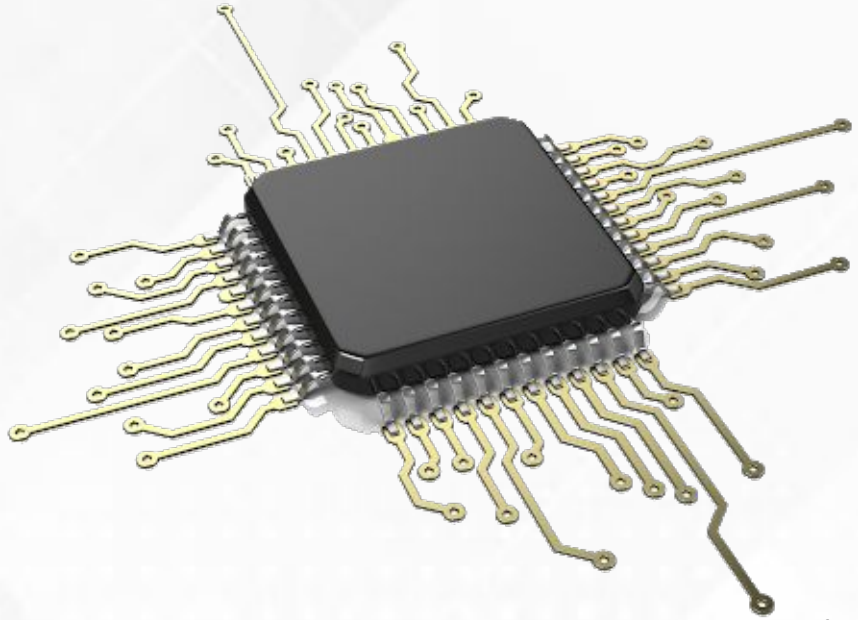
Computer Organization & Architecture
(COA)
GTU # 3140707

Dedicated Faculty, Committed Education
Darshan
Institute of Engineering & Technology

Unit-10
Multiprocessors



Prof. Krunal D. Vyas
Computer Engineering Department
Darshan Institute of Engineering & Technology,
Rajkot
krunal.vyas@darshan.ac.in
9601901005

Outline

- Tightly coupled V/S Loosely coupled
- Interconnection Structures
- Cache Coherence
- Shared Memory Architecture
- Questions asked in GTU exam

Tightly coupled V/S Loosely coupled

Section - 1

Tightly coupled V/S Loosely coupled

Tightly Coupled System	Loosely Coupled System
Tasks and/or processors communicate in a highly synchronized fashion.	Tasks or processors do not communicate in a synchronized fashion.
Communicates through a common shared memory.	Communicates by message passing packets.
Shared memory system.	Distributed memory system.
Overhead for data exchange is lower comparatively.	Overhead for data exchange is higher comparatively.

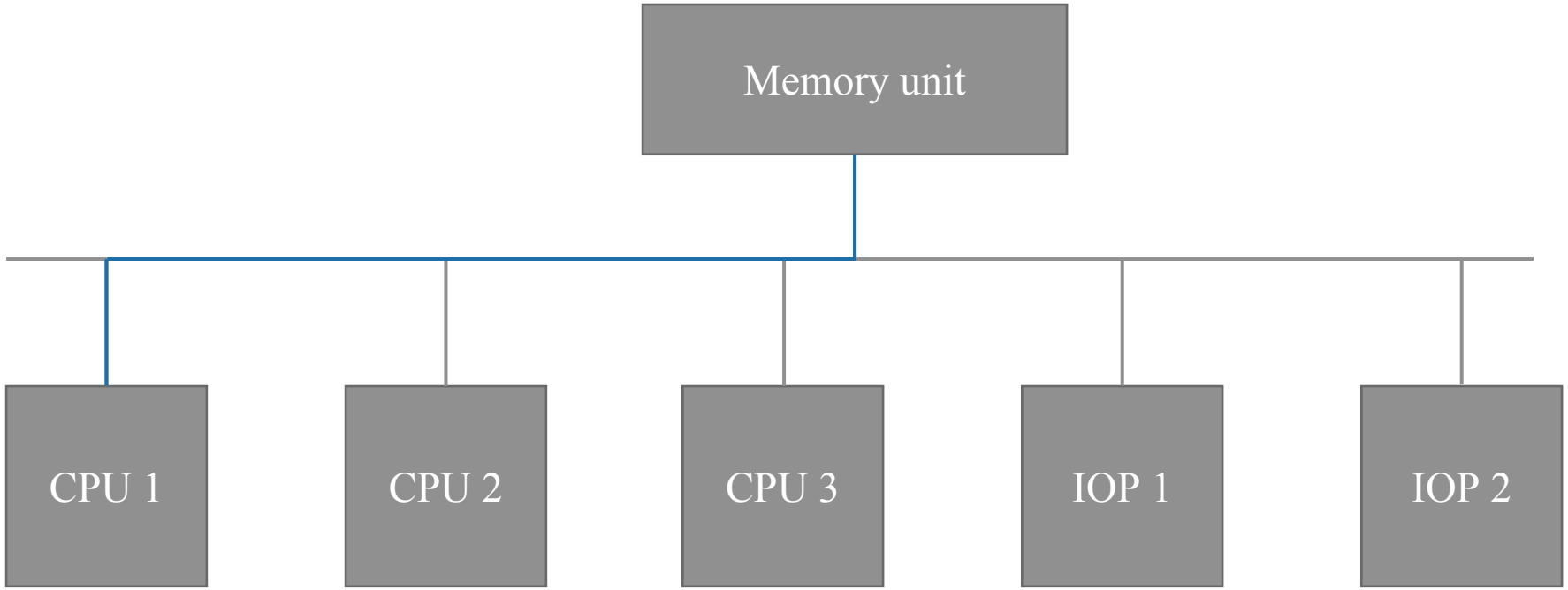
Interconnection Structures

Section - 2

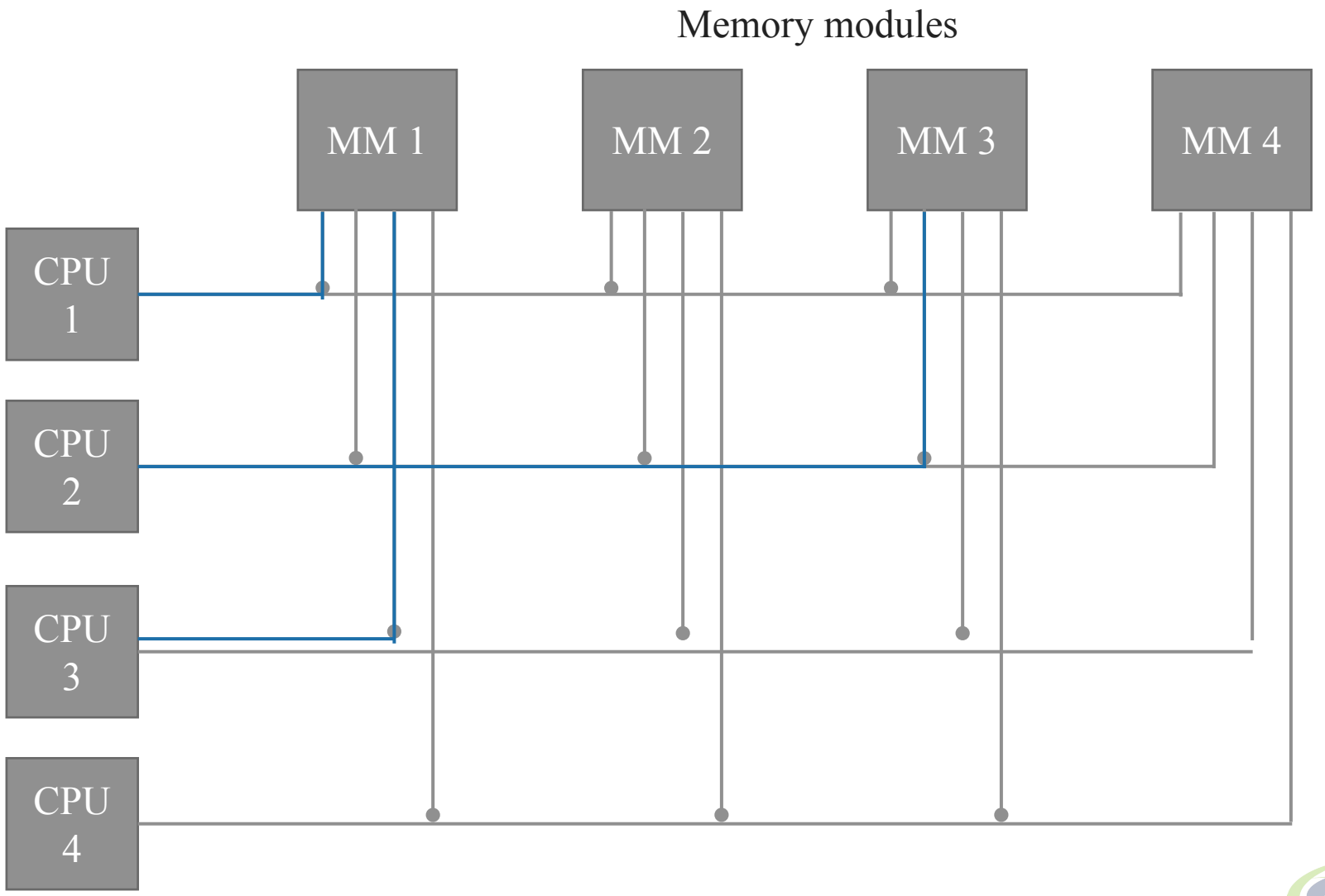
Interconnection Structures

1. Time-shared common bus
2. Multiport memory
3. Crossbar switch
4. Multistage switching network
5. Hypercube system

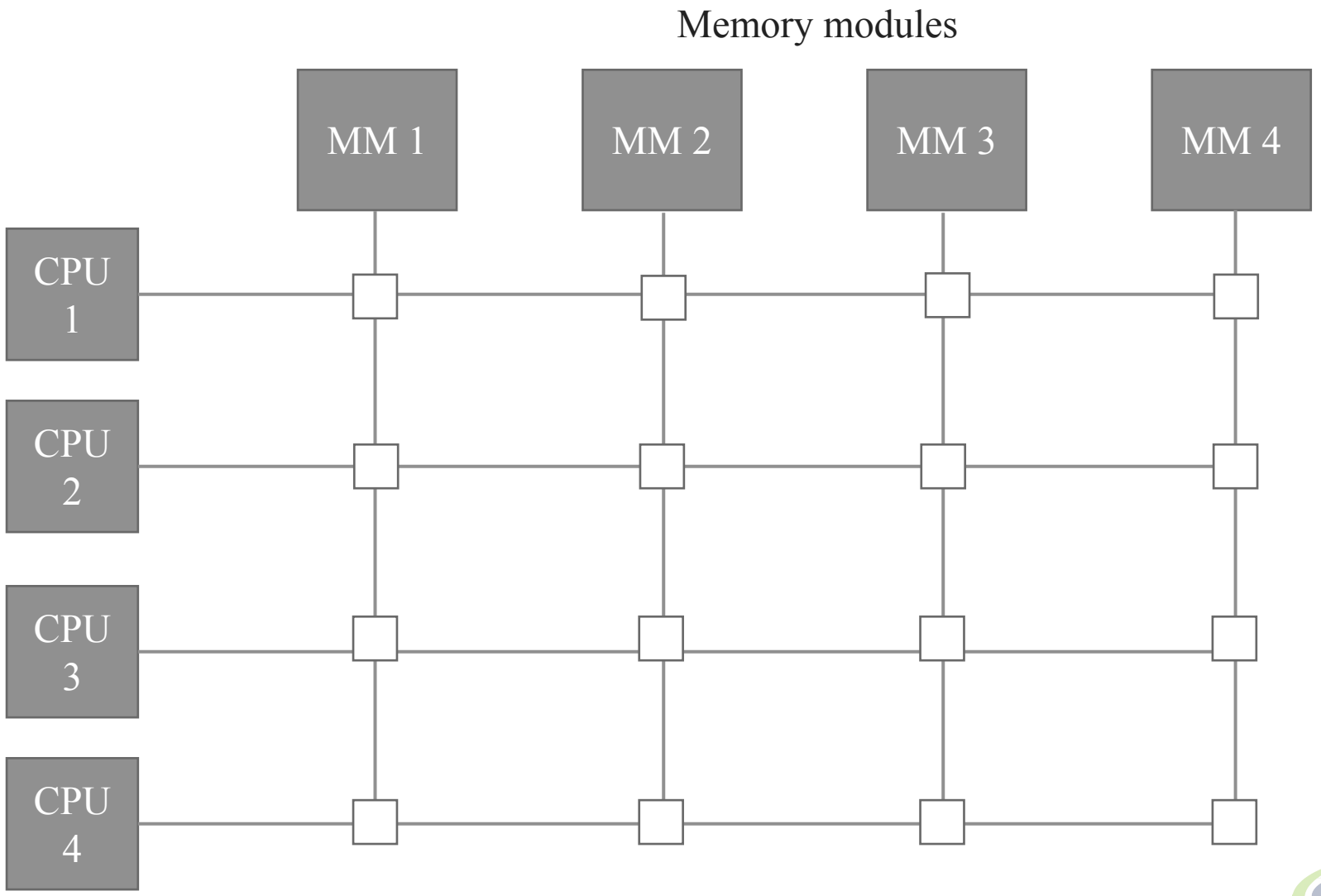
1. Time-shared common bus



2. Multiport Memory

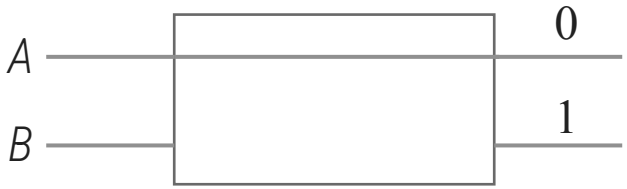


3. Crossbar switch

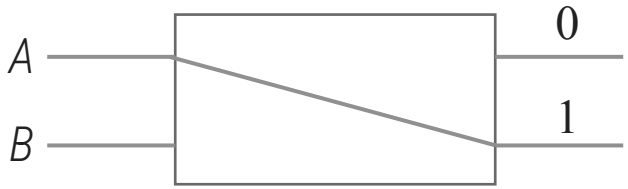


4. Multistage switching network

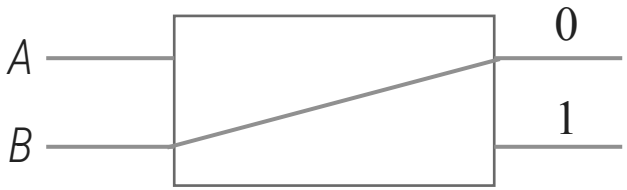
Operation of 2 X 2 interchange switch



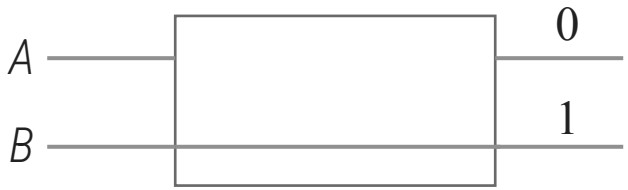
A connected to 0



A connected to 1

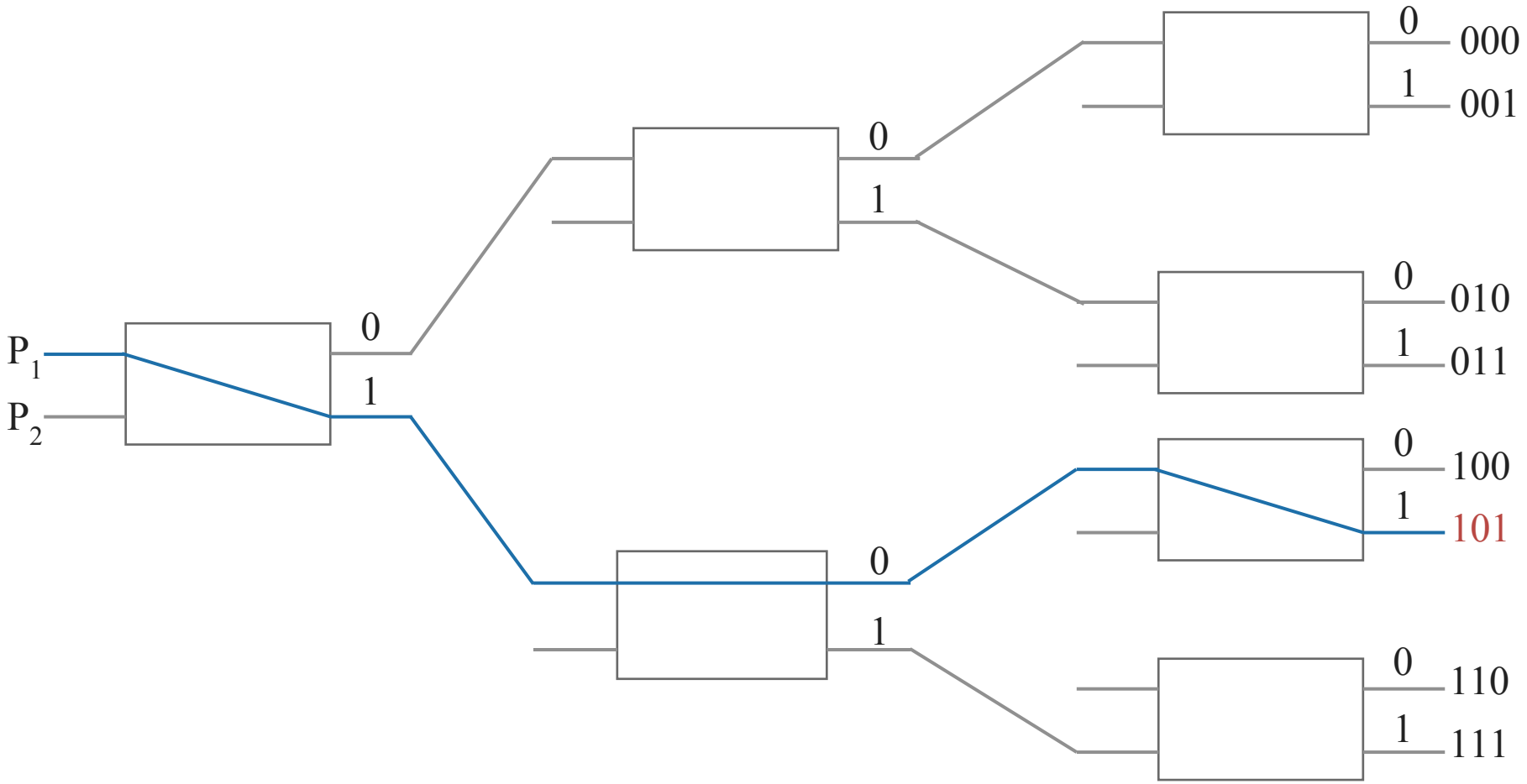


B connected to 0



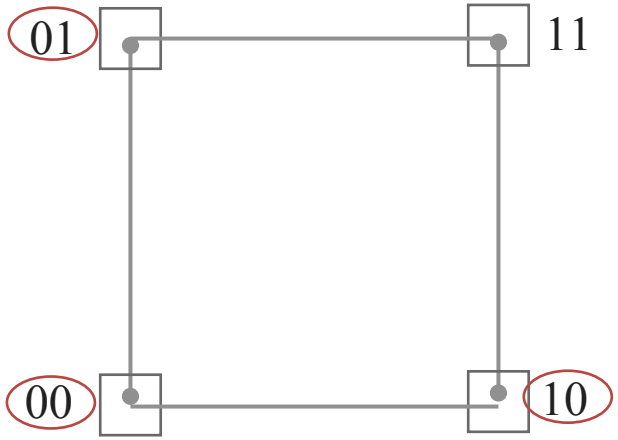
B connected to 1

4. Multistage switching network

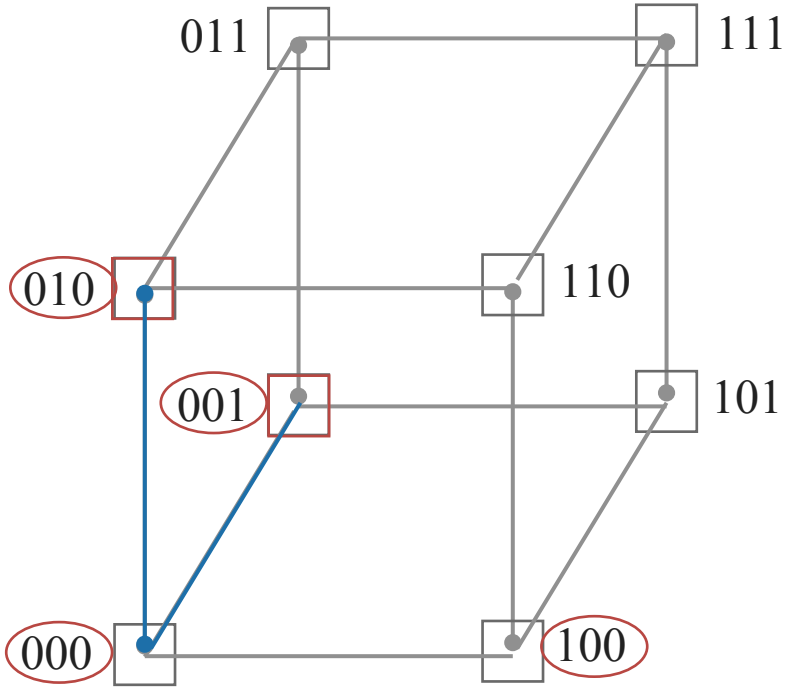


5. Hypercube Interconnection

One-cube



Two-cube



Three-cube

010 x-or 001 =
011

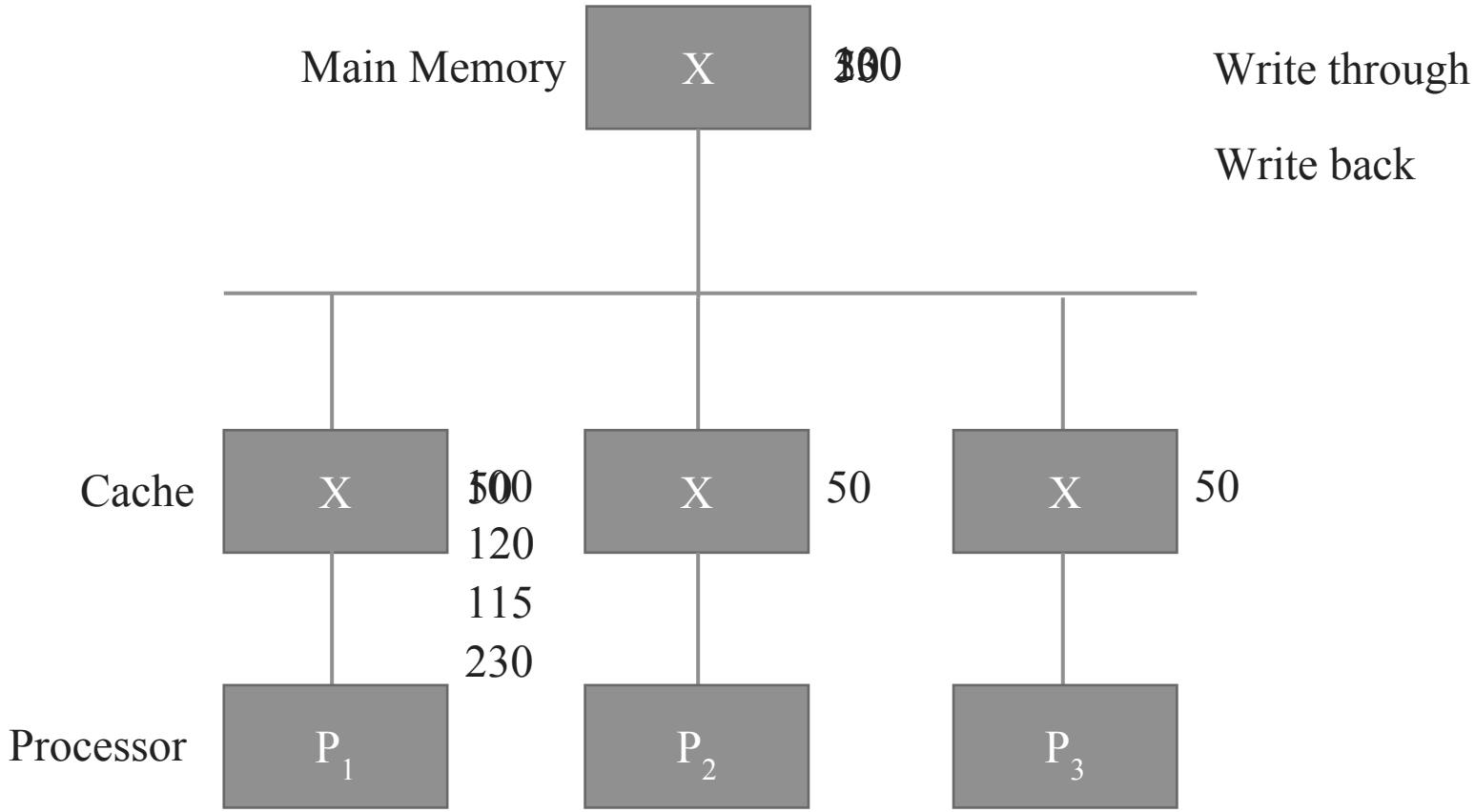
Dynamic Arbitration Algorithm

- Time Slice: The time slice algorithm allocates a fixed-length time slice of bus time that is offered sequentially to each processor, in round-robin fashion.
- Polling: In a bus system that uses polling, the bus grant signal is replaced by a set of lines called poll lines which are connected to all units.
- LRU: The Least Recently Used (LRU) algorithm gives the highest priority to the requesting device that has not used the bus for the longest interval.
- FIFO: In first-come, first-serve scheme, requests are served in the order received.
- Rotating daisy-chain: The rotating daisy-chain procedure is a dynamic extension of the daisy-chain algorithm. In this scheme there is no central bus-controller, and the priority line is connected from the priority-out of the last device back to the priority-in of the first device in a closed loop.

Cache Coherence

Section - 3

Cache Coherence Problem



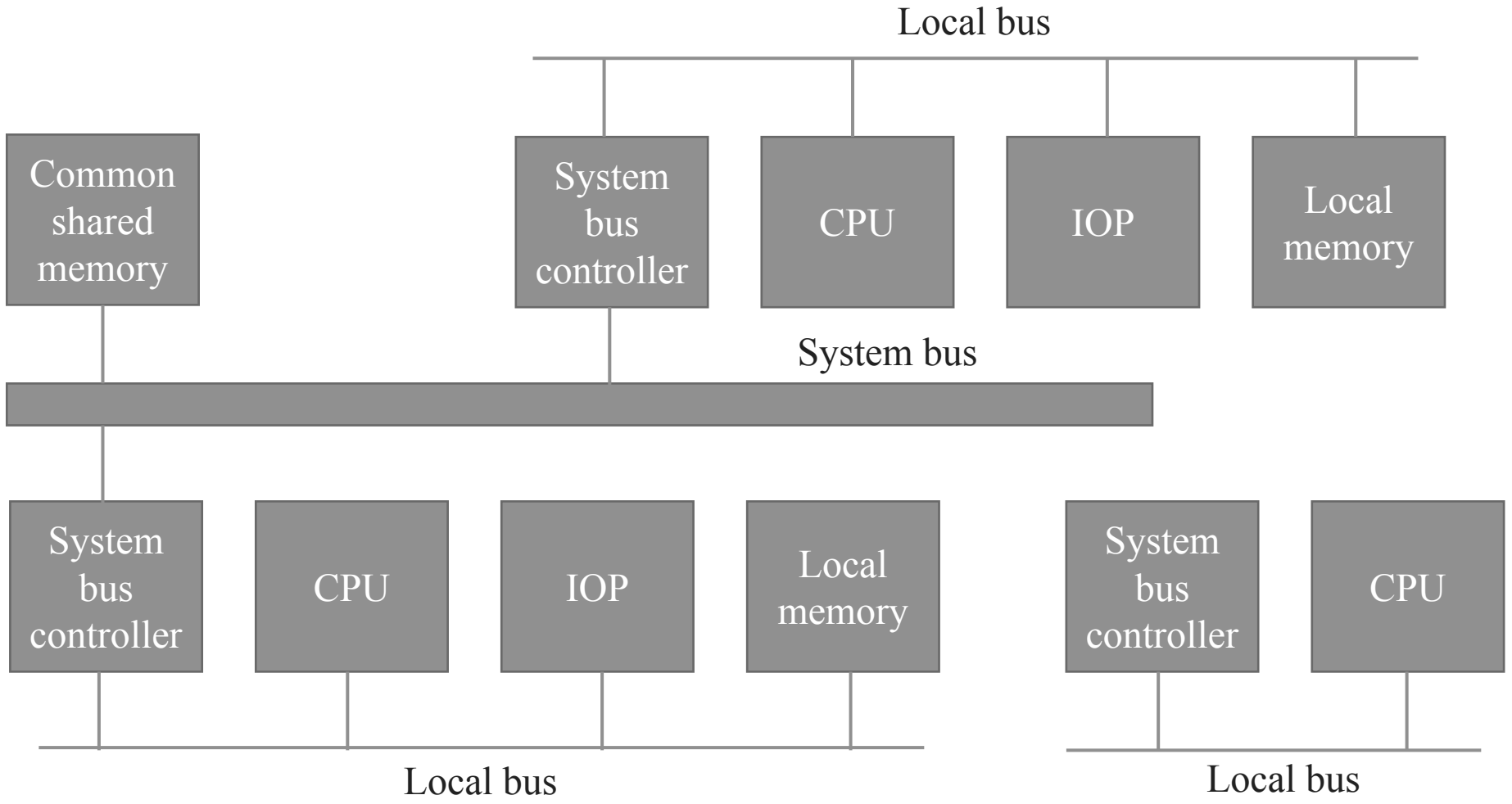
Cache Coherence Solution

- Write Update
- Write Invalidate
- Software approaches
  - Compiler based cache coherence mechanism
- Hardware approaches
  - Directory protocols
  - Snoopy protocols

Shared Memory Architecture

Section - 4

Shared Memory Architecture



Questions asked in GTU exam

Section - 5

Questions asked in GTU exam

1. Draw and explain shared memory architecture of multiprocessor system
2. Explain Inter-process communication
3. Explain any two interconnection structures that make it possible to form a multiprocessor system with diagram.
4. Differentiate tightly coupled and loosely coupled systems.
5. Give the features of a multiprocessor system.
6. What is cache coherence?