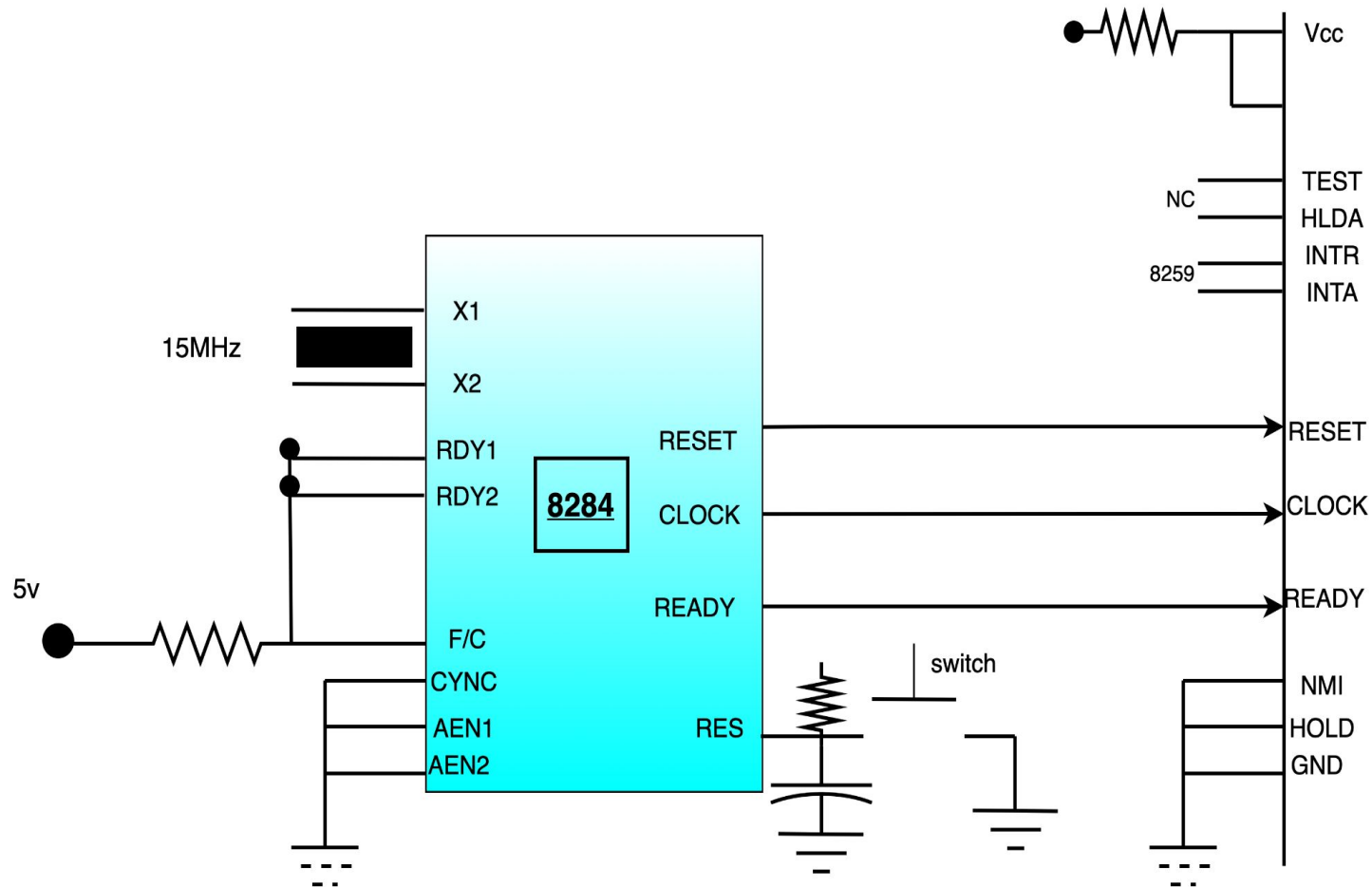


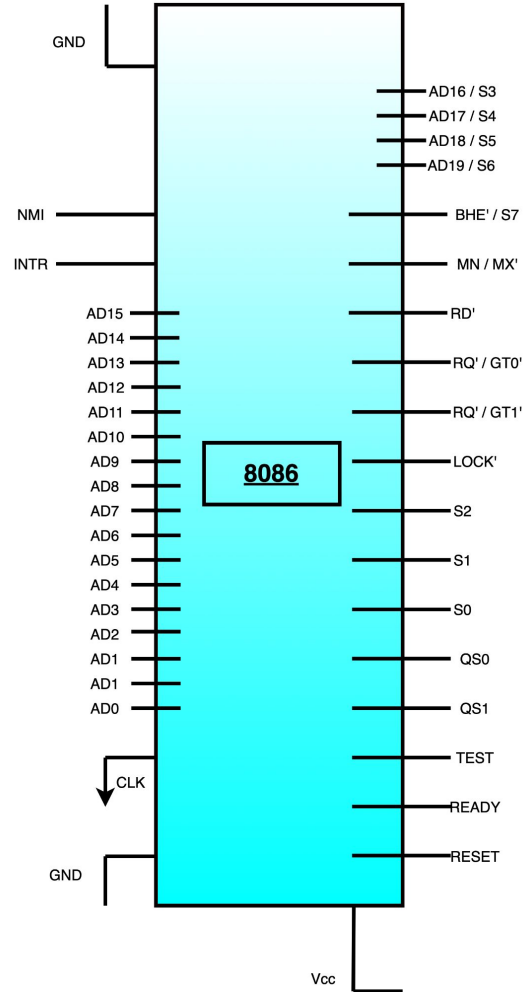
Hardware Design

8284

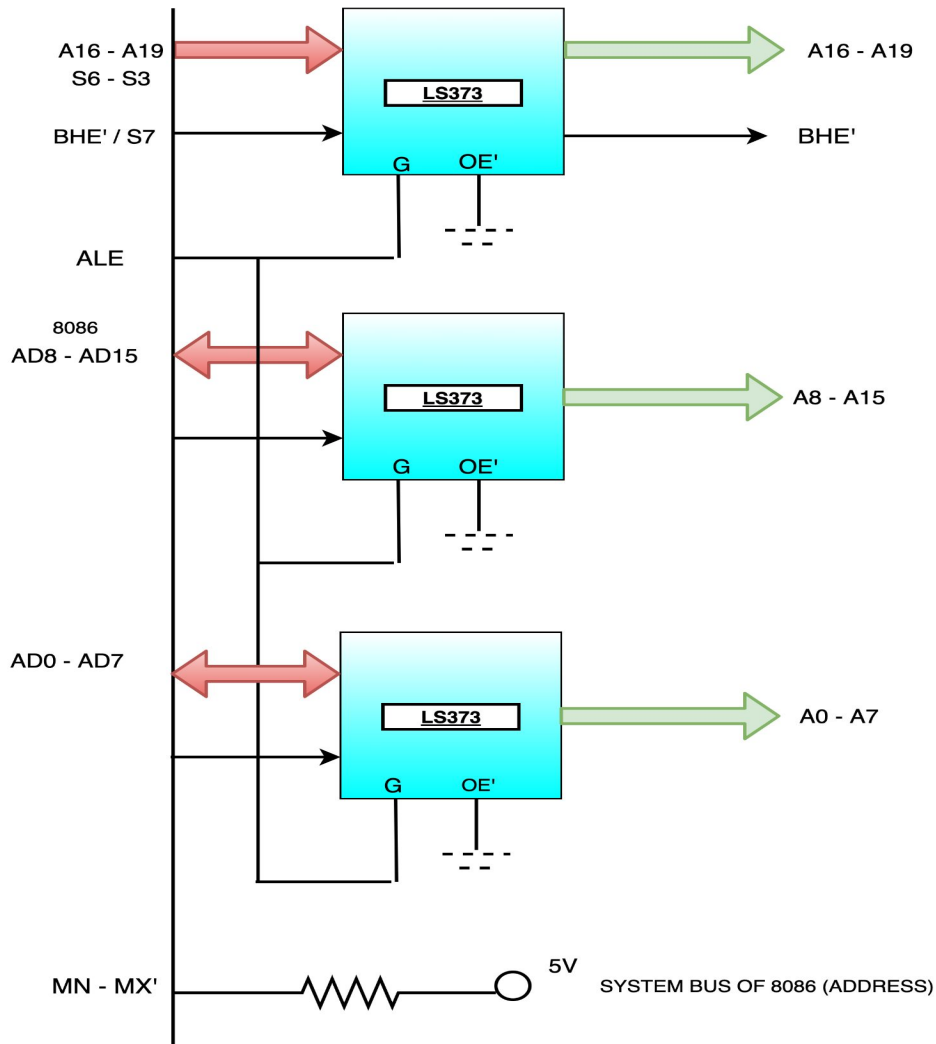


8086 INPUTS

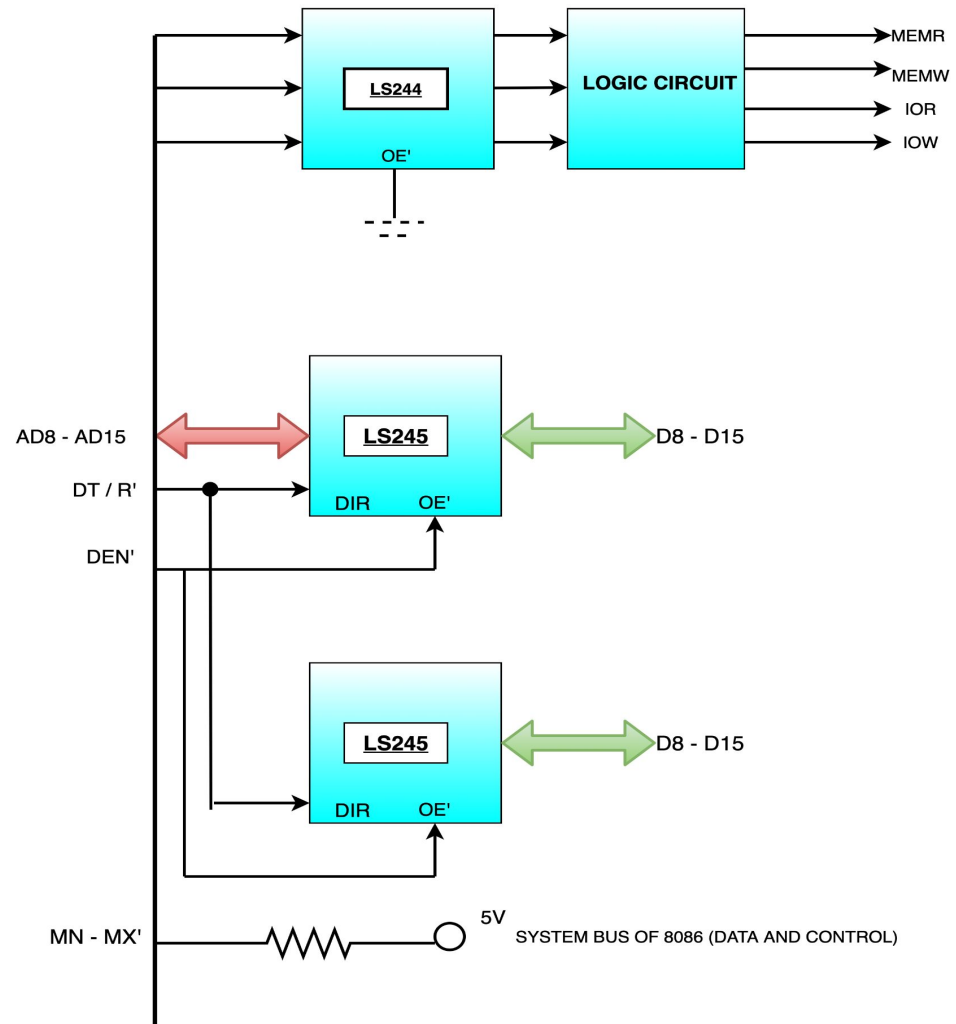
8086

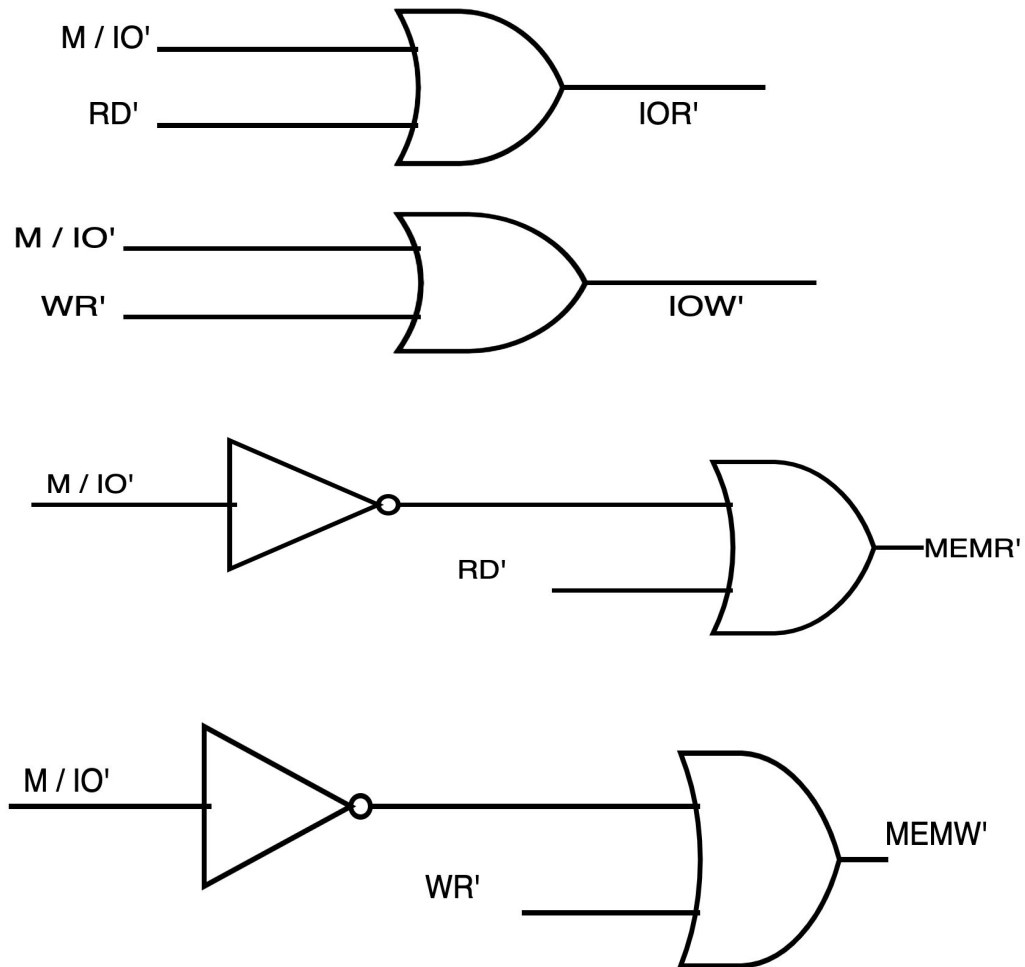


SYSTEM BUS OF 8086 (ADDRESS)



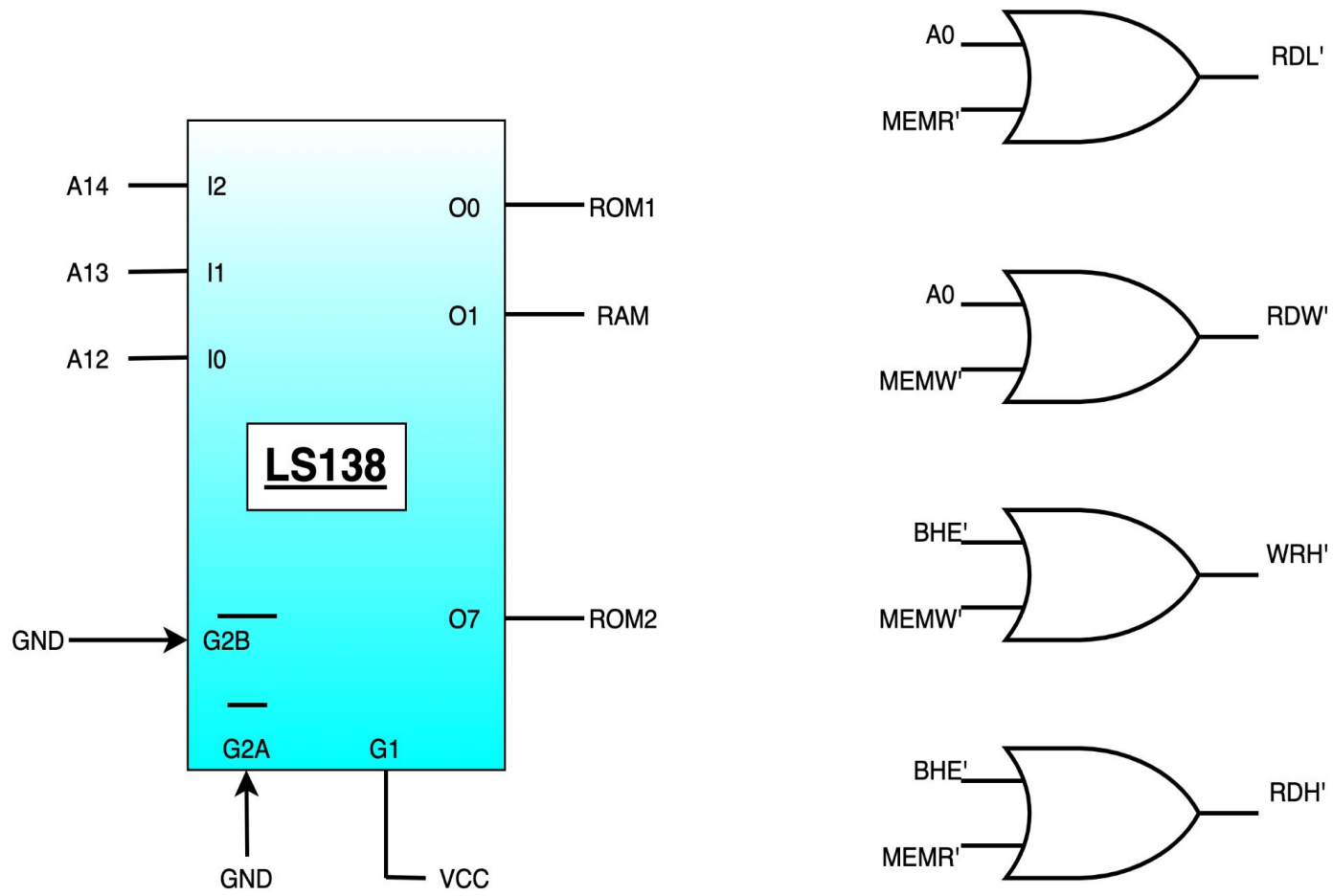
SYSTEM BUS OF 8086 (DATA + CONTROL)



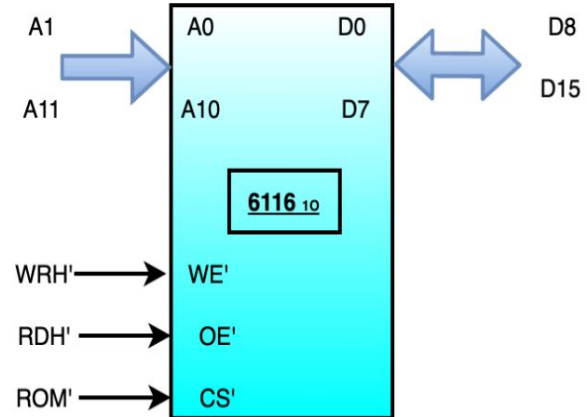
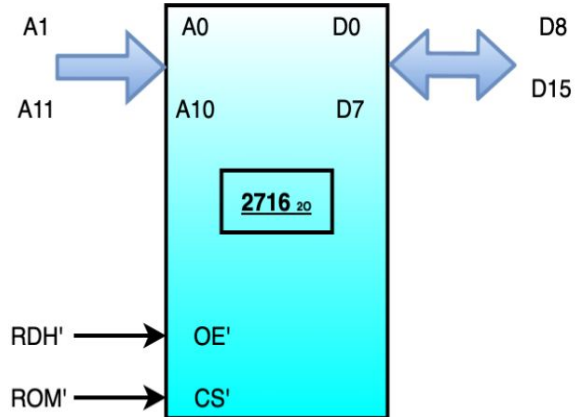
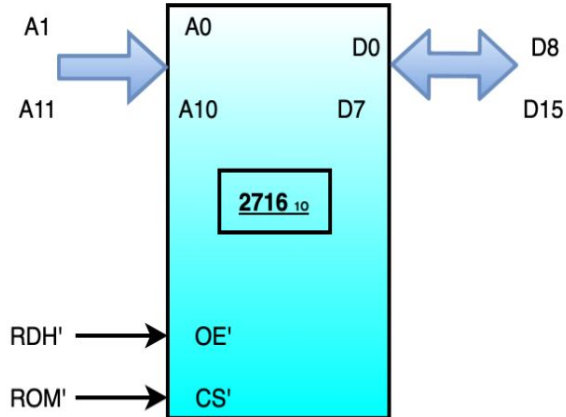
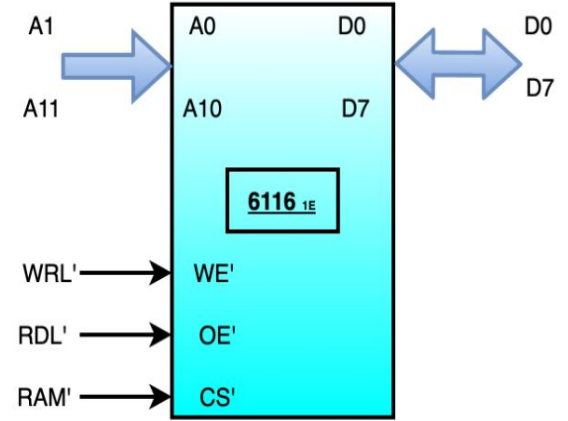
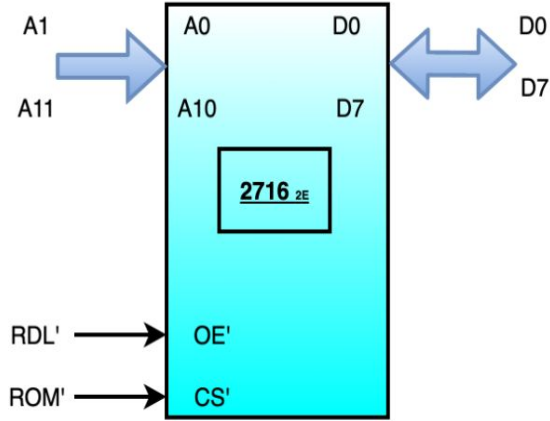
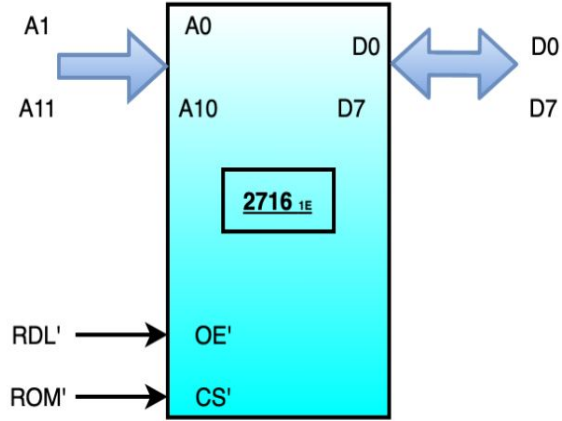


M / IO'	RD'	WR'	BUS CYCLE
1	0	1	MEMR'
1	1	0	MEMW'
0	0	1	IOR'
0	1	0	IOW'

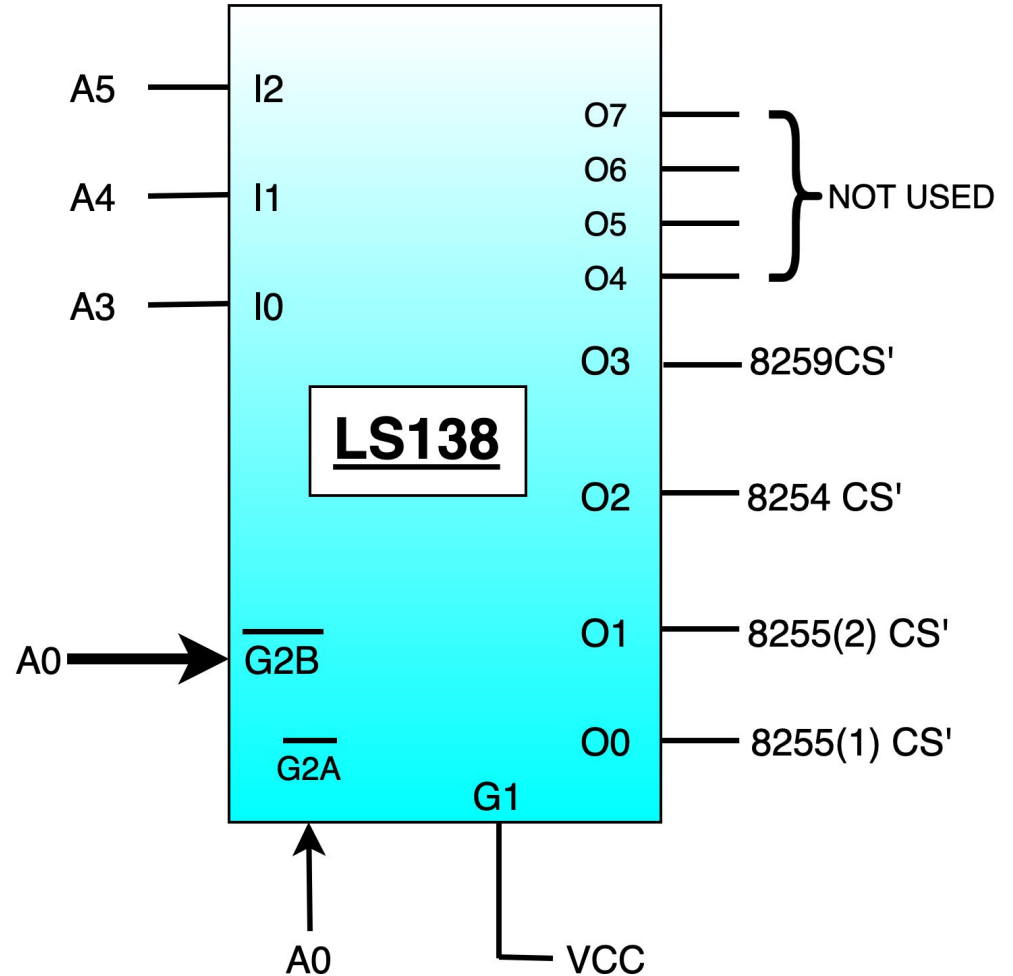
MEMORY DECODER



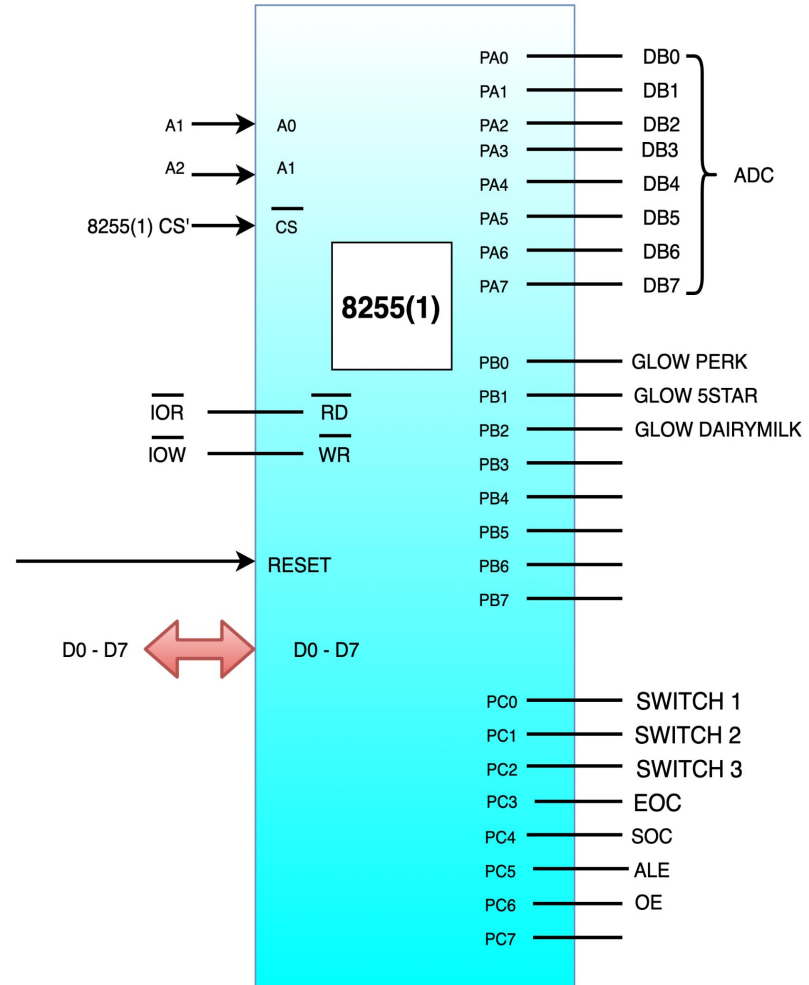
MEMORY INTERFACING



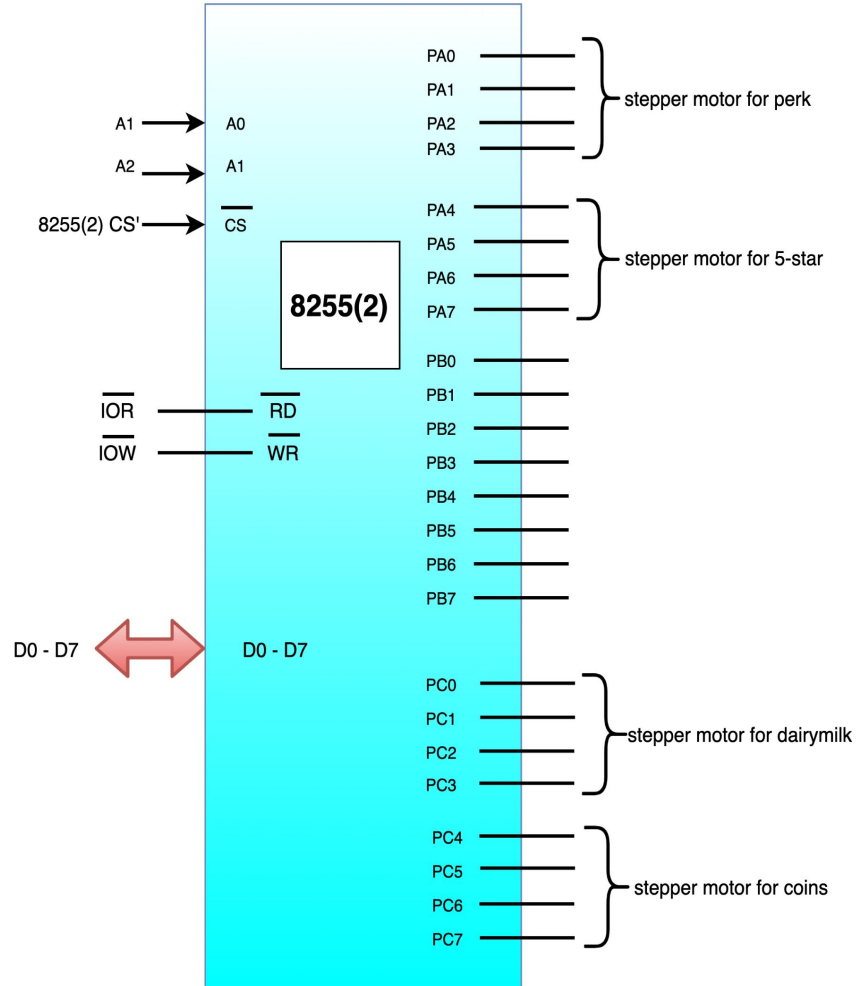
I/O DECODER



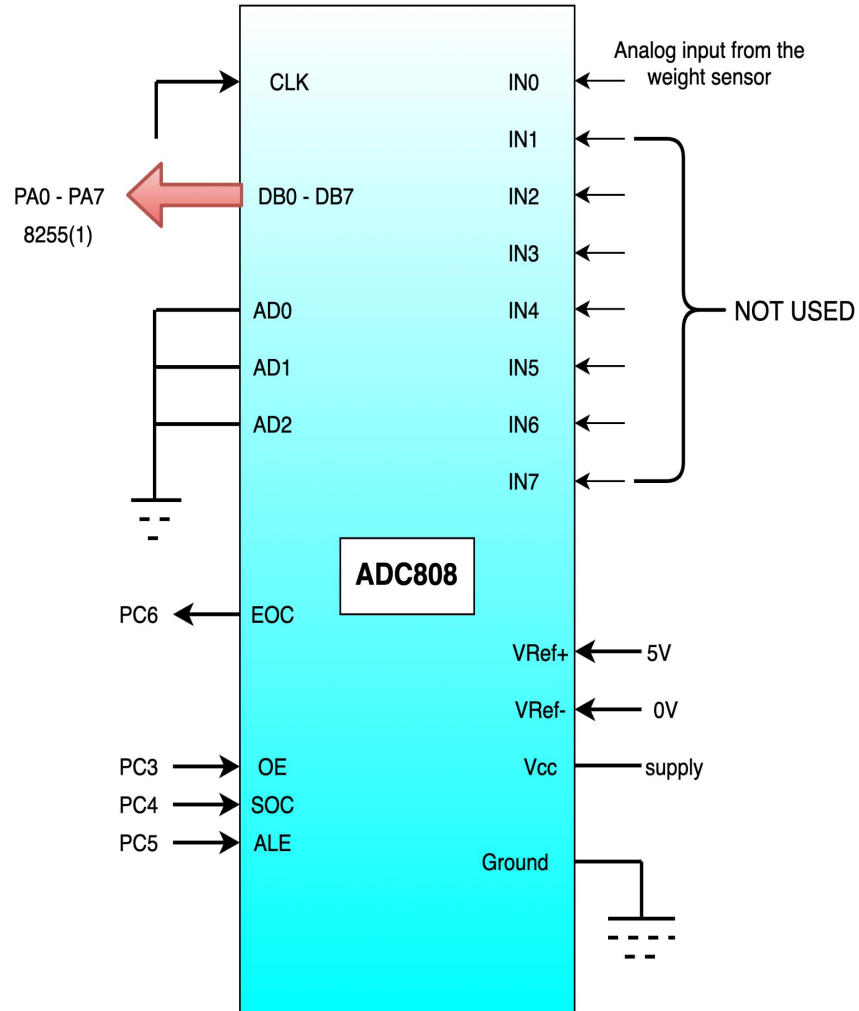
8255 (1)



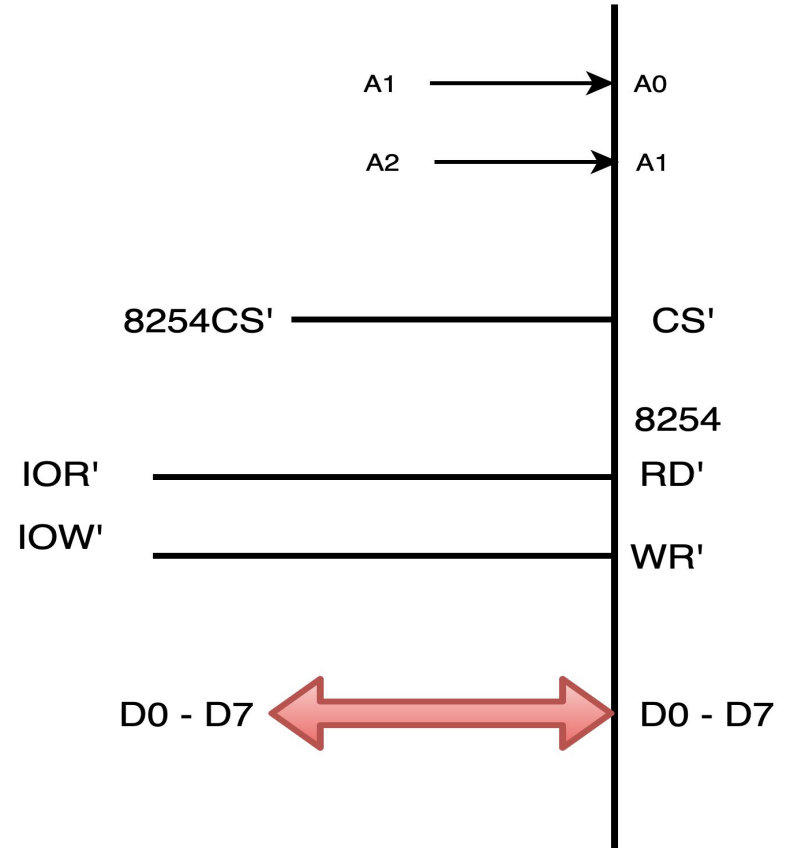
8255 (2)



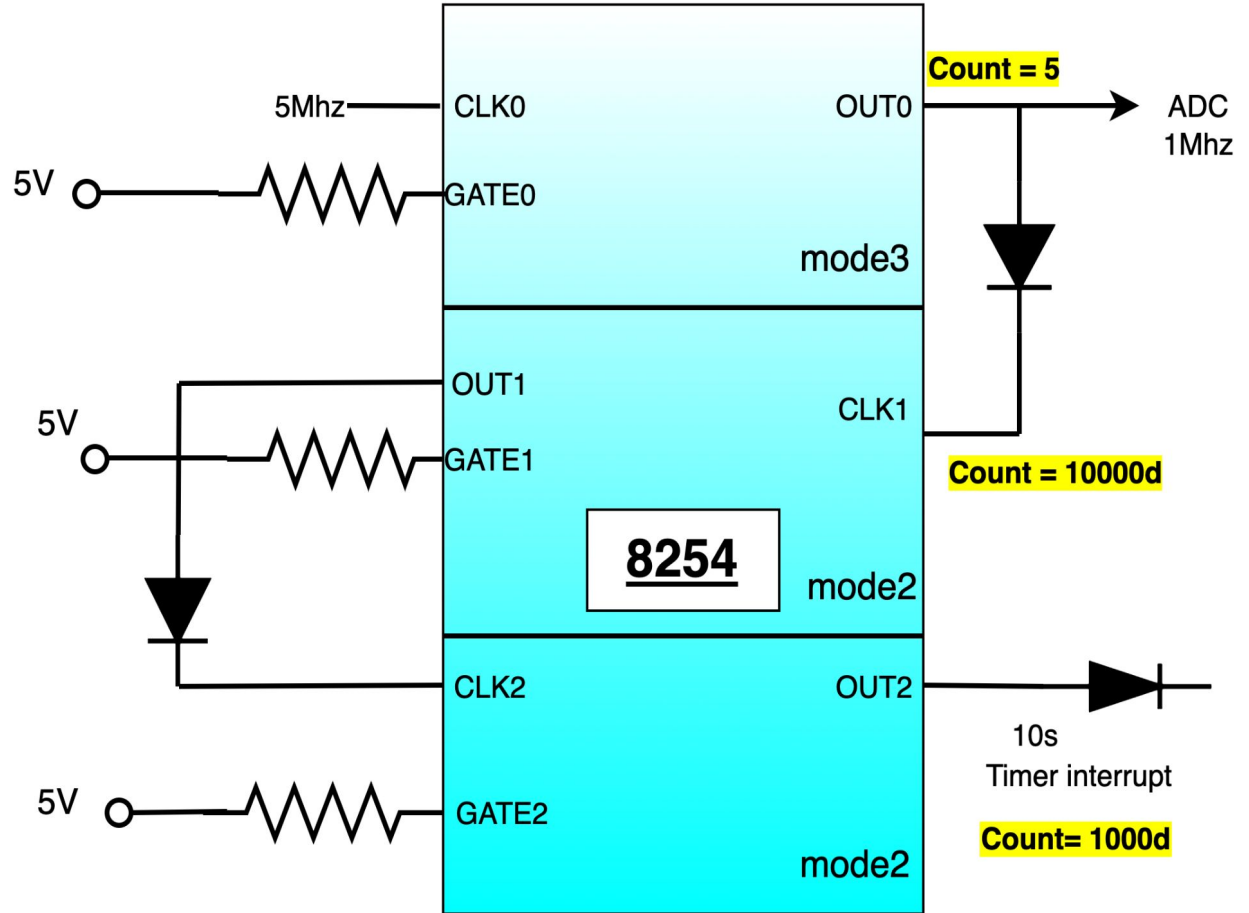
ADC808



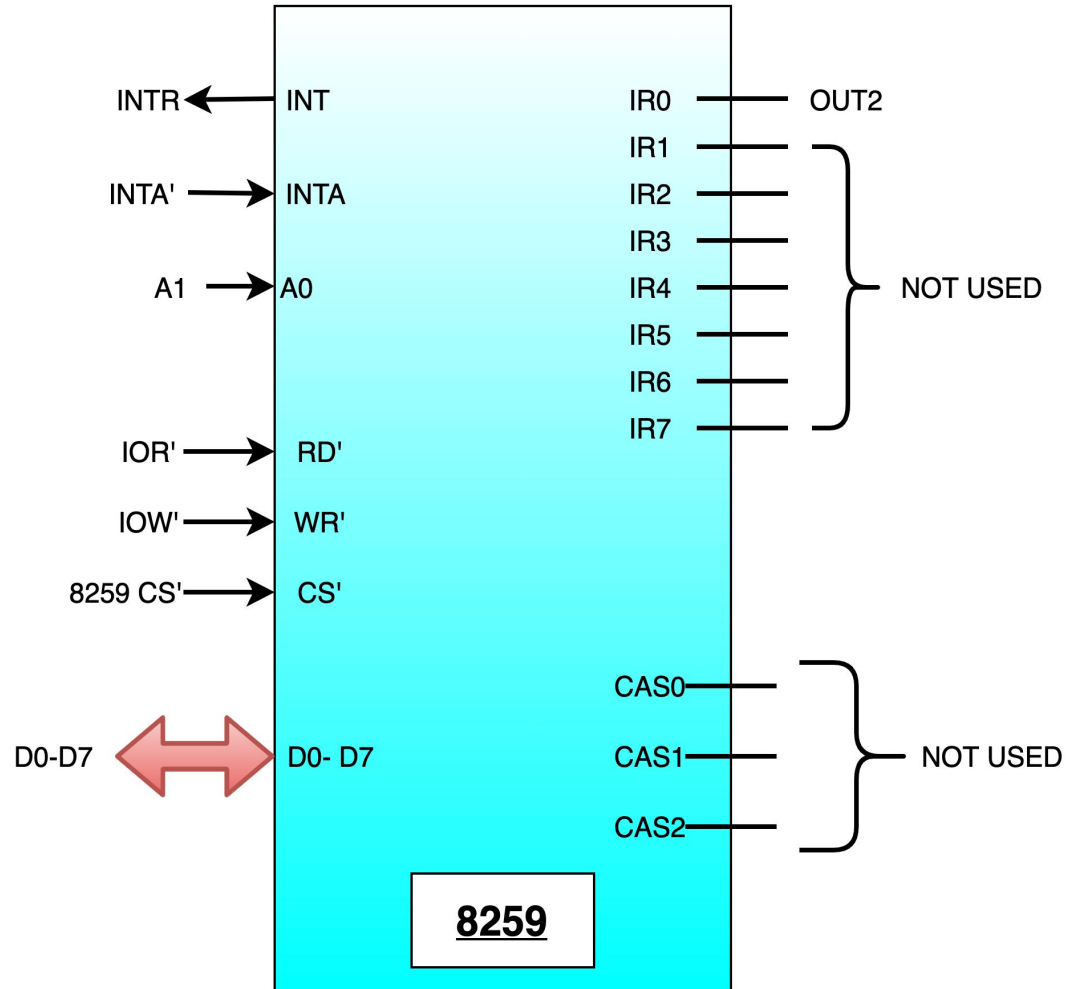
8254 INTERFACE TO THE PROCESSOR



8254



8259



STEPPER MOTOR

