DIGITAL DESIGN (EEE F215)
Assignment

GROUP 6

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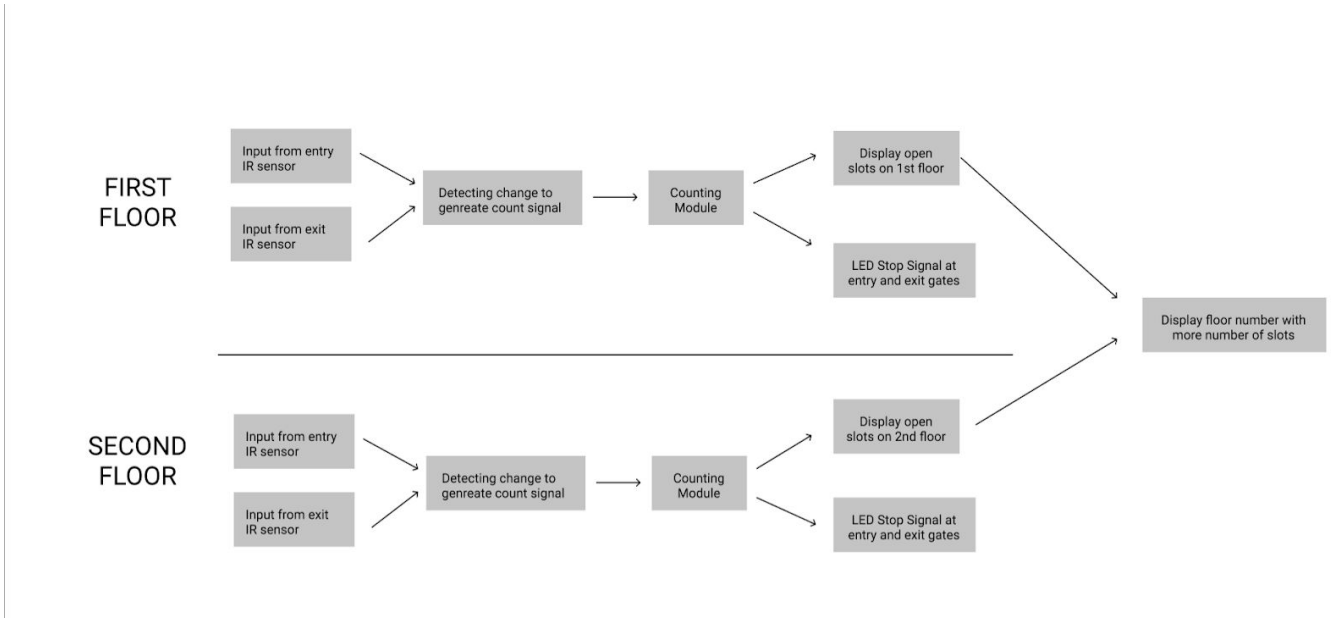
Design Question

Design a display for a parking structure employed in a mall, that displays the number of open parking slots in each floor of the
building so that customers may be directed to that particular floor. Each parking slot is made up of a IR sensor that senses if a car
is parked in the slot or not. Minimum number of floors in the parking structure is 2.

Top Level Block Diagram



Assumptions made w.r.t the design problem

At a time, one car is either entering or exiting the parking lot. Simultaneous entry and exit is not considered. To make the user aware about this, we have added a separate LED at each entry and exit. Whenever the LED at the entry is red, it means that a car is currently exiting the lot. So the car at the entry must wait till the other car has exited and then will be allowed to enter. The LED functions as a STOP signal.

1. Separate floors have their separate displays independent of each other. Each floor has 2 IR sensors : one at the entry and one at exit.
2. When a car crosses a sensor its value changes from 0 to 1. Once it has passed through the entry/ exit gate, the sensor's value falls back to 0.
3. Number of parking slots on each floor is 100. There are 2 floors total.
4. A synchronous clock signal is used with frequency 1 Hz, and it is assumed that the cars are entering / exiting such that the IR sensor changes when the clock signal is low. (From 0-1-0 of the IR sensor, only one rising edge of the clock is assumed)
5. Each floor has 2 seven segment displays for displaying the number of remaining parking slots.

6. A separate seven segment display shows the floor number which has more number of parking slots. The user can then choose accordingly.

Additional Functionality :

1. Adding the extra display showing the floor number with more number of open slots.
2. STOP signal at entry and exit gates

Annotations to explain our design :

S (exit)	R (entry)	Q	Q’	Change in Display
0	0	Q	Q’	No change
0	1	0	1	Slots decrease
1	0	1	0	Slots increase
1	1	-	-	Forbidden Case

For all counters 2 control pins are used :

Count	Load	Function
0	0	No change
1	0	Count Up
1	1	Count Down
1	0	Loading condition(not required in our design)

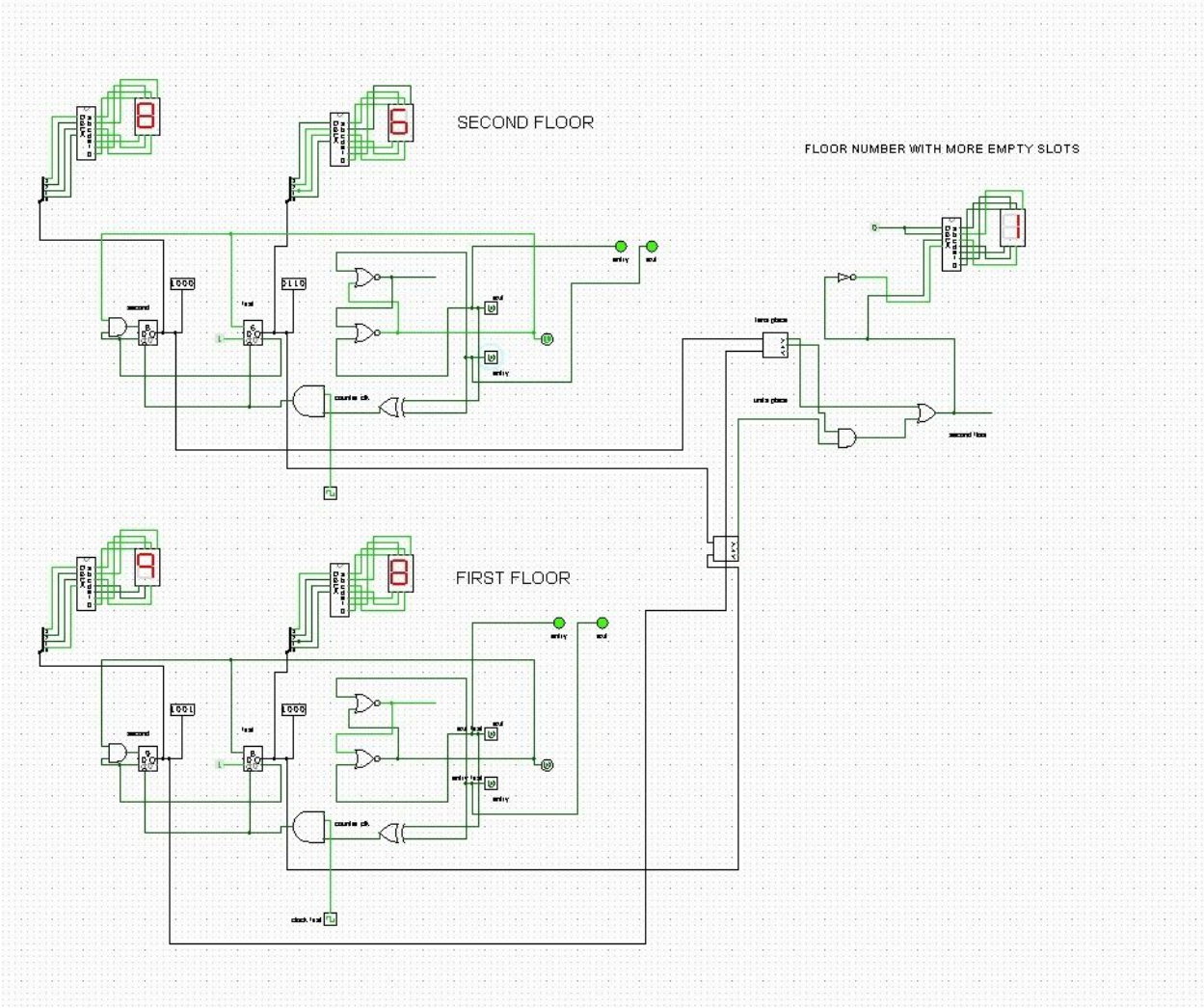
For the first decade counter (count=1) always. Our load signal is Q’, so that when cards enter (R=1,S=0), more slots are occupied and we count down the number of free slots. Thus load =1 in this case.

For the 2nd counter, it should count only when the 1st counter reaches either its maximum or minimum value (carry=1). Thus the load of the second counter is (Q’ AND Carry).

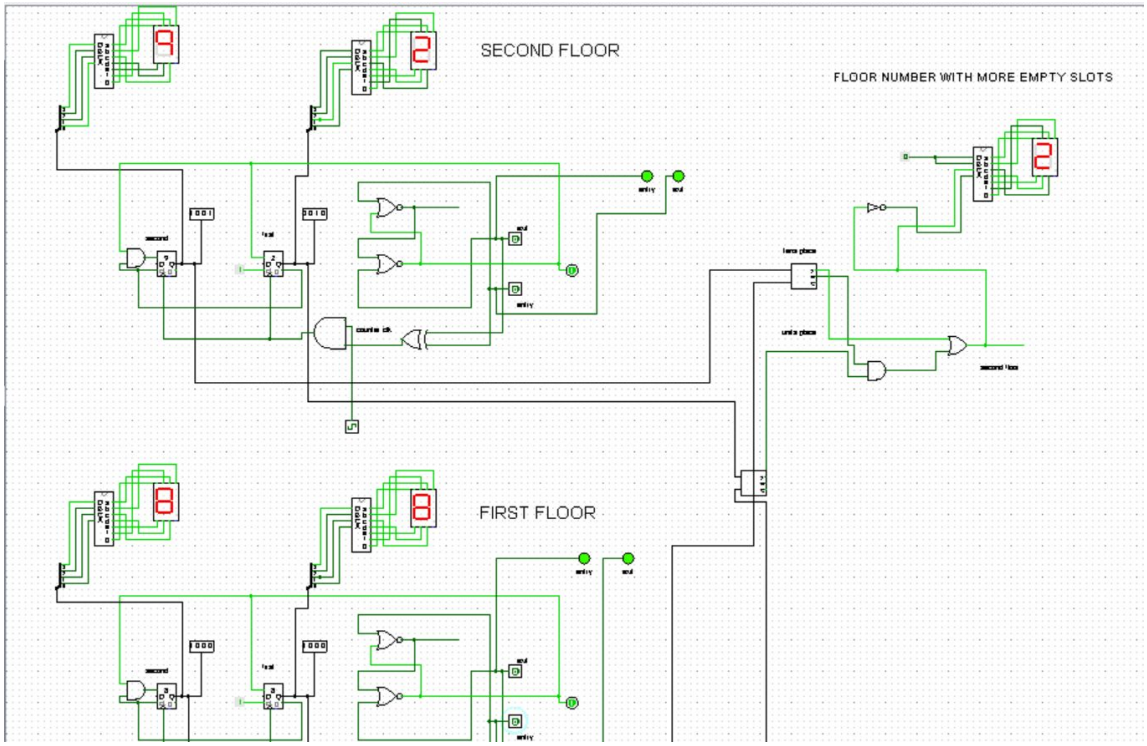
As no 2 cars simultaneously enter and exit, our clock pulse only works when either of entry or exit is 1. So (entry XOR exit) is used and it is passed through an AND gate with the clock.Thus effective clock of counter is (clk AND (entry XOR exit)).

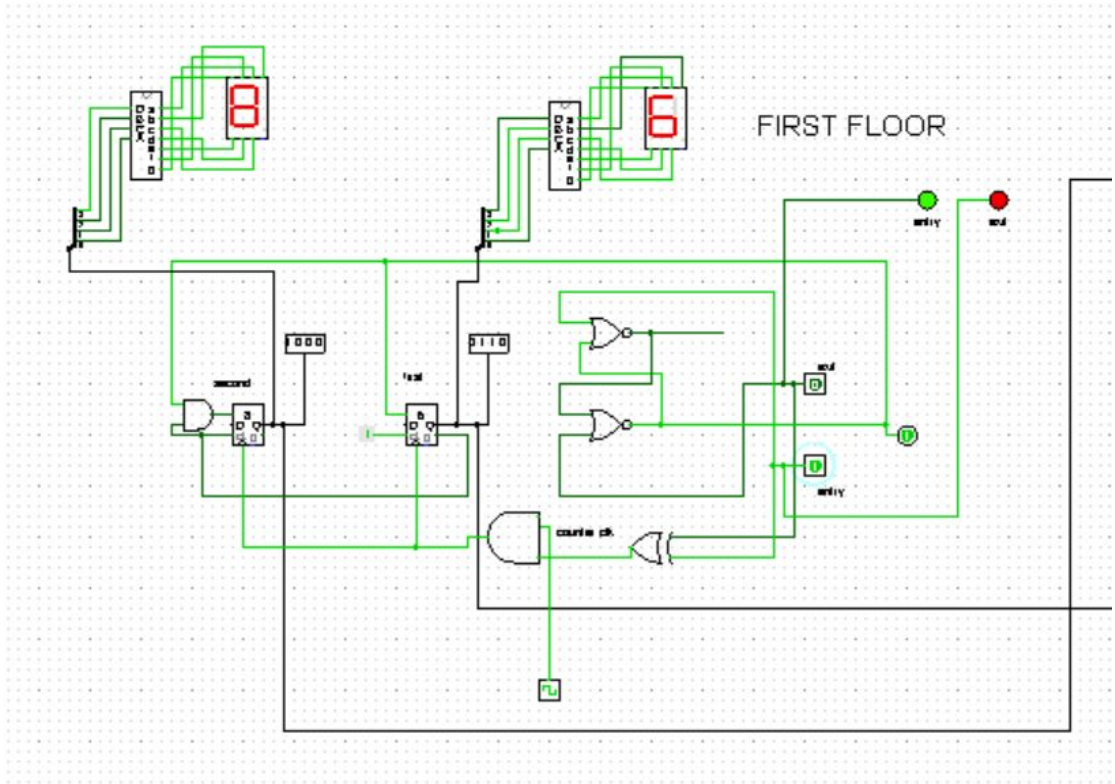
Sample I/P and O/P :

clock first	entry first	exit first	first tens	first units
0	0	0	0	0
0	1	0	0	0
0	0	0	0	0
1	0	0	0	0
0	0	0	0	0
1	0	0	0	0
0	0	0	0	0
1	0	0	0	0
0	0	0	0	0
1	0	0	0	0
0	0	0	0	0
0	1	0	0	0
1	1	0	9	9
0	1	0	9	9
0	0	0	9	9
1	0	0	9	9
0	0	0	9	9
1	0	0	9	9
0	0	0	9	9
0	1	0	9	9
1	1	0	9	8
0	1	0	9	8
1	1	0	9	7
0	1	0	9	7
1	1	0	9	6
0	1	0	9	6
0	0	0	9	6
1	0	0	9	6
0	0	0	9	6
0	0	1	9	6
1	0	1	9	7
0	0	1	9	7
1	0	1	9	8
0	0	1	9	8
0	0	0	9	8
1	0	0	9	8
0	0	0	9	8
1	0	0	9	8



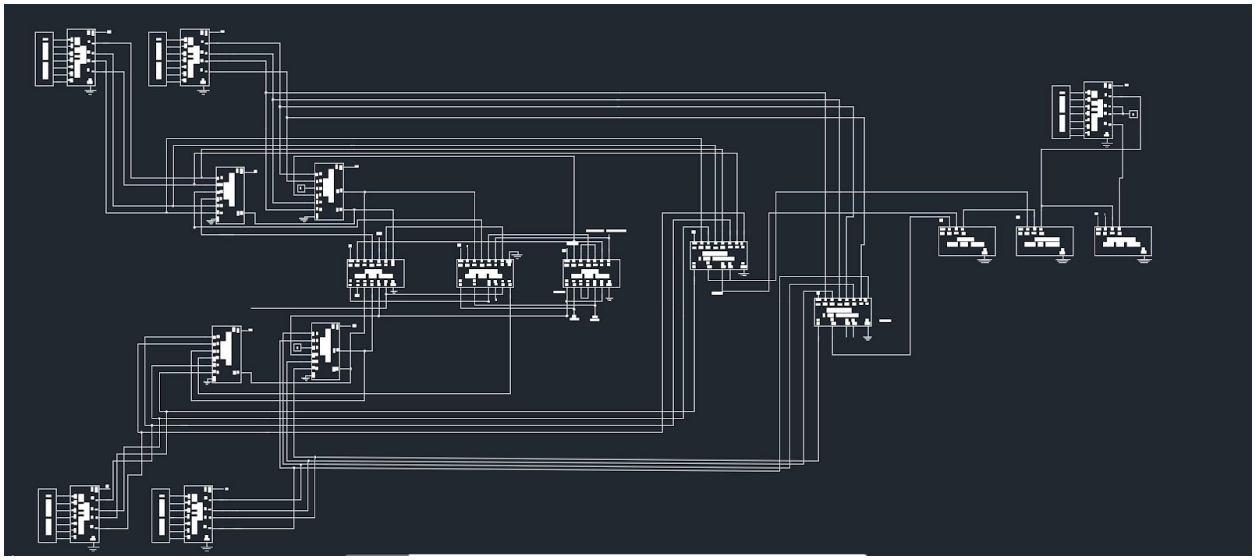
Circuit Output for the above Logging Table



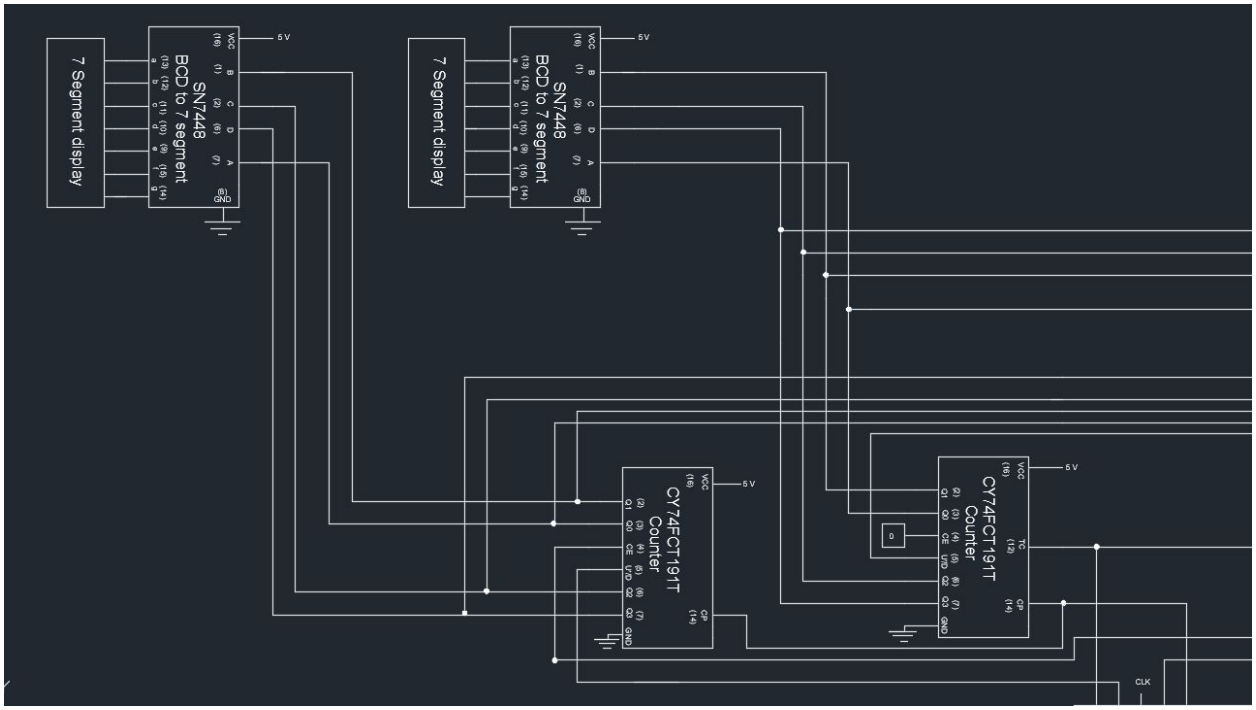


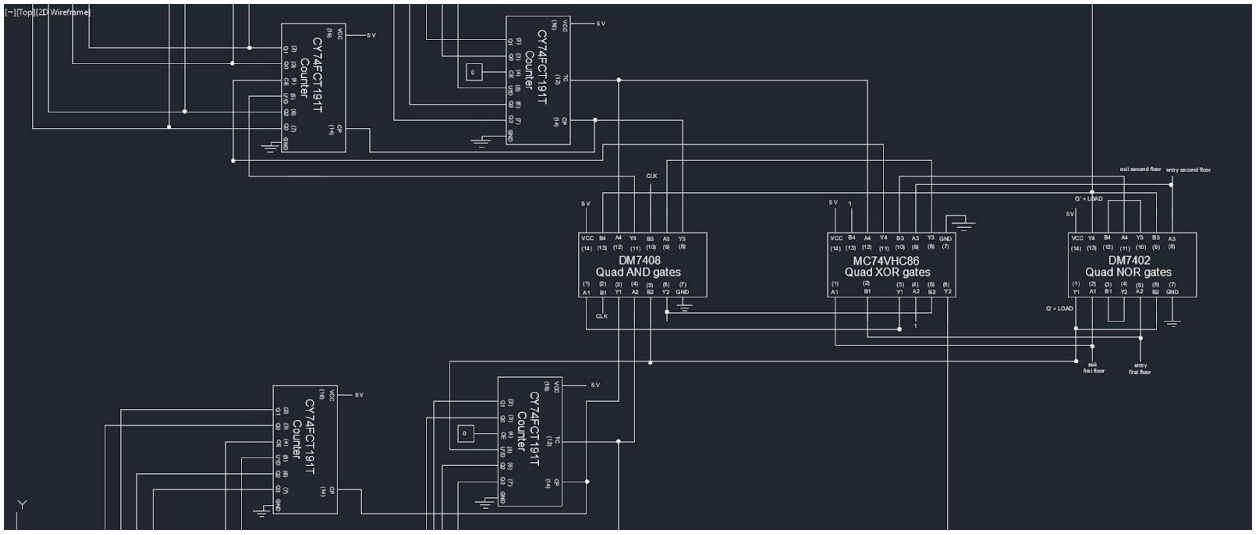
LED for exit is on while entry is ongoing

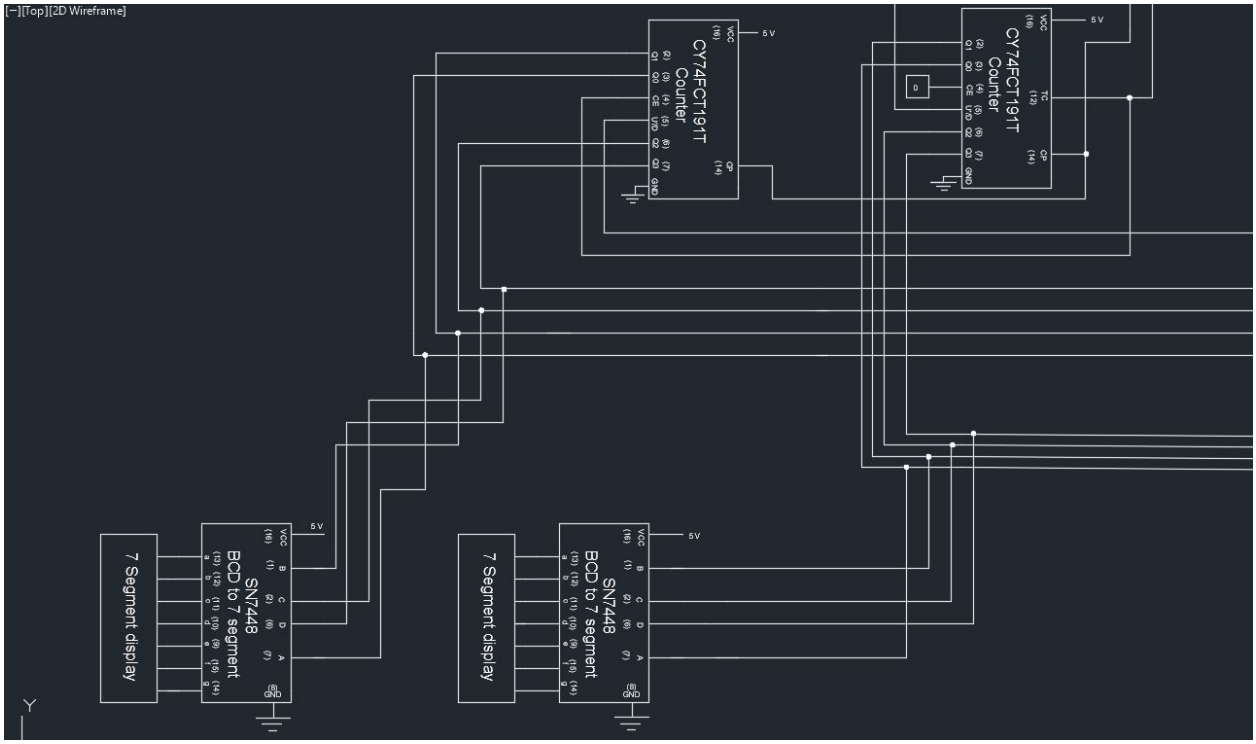
Pin Out Diagram

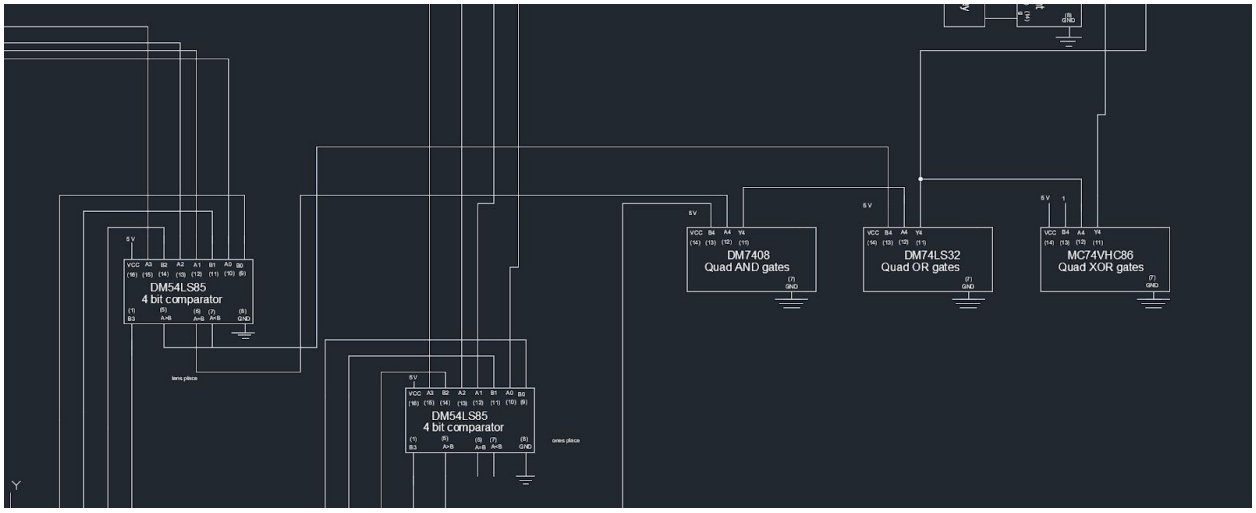


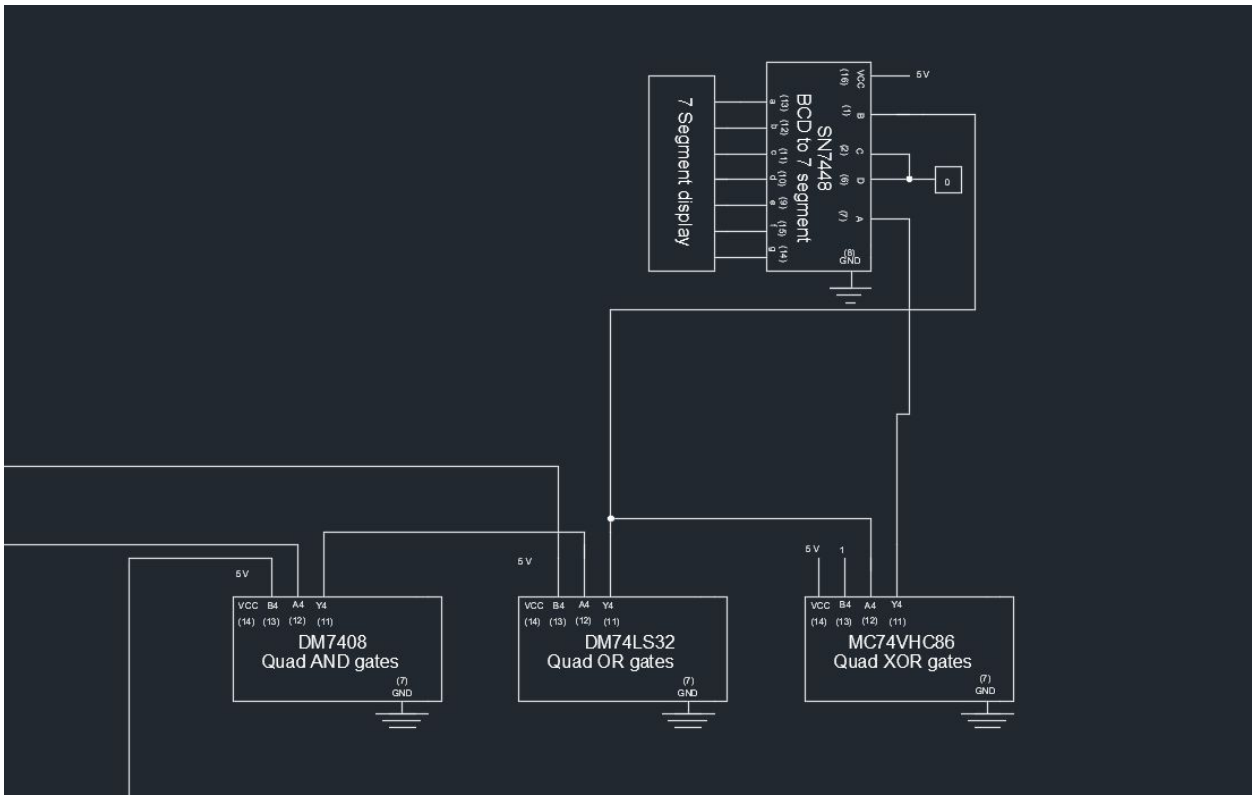
(AutoCAD file attached in zip file)




[−][Top][2D Wireframe]
CY74FCT191T
Counter
DM7408
Quad AND gates
MC74VHC86
Quad XOR gates
DM7402
Quad NOR gates
CLK
5 V
exit second floor
entry second floor
Q' = LOAD
exit first floor
entry first floor


[−][Top][2D Wireframe]
CY74FCT191T
Counter
SN7448
BCD to 7 segment
7 Segment display
5 V





Appendix

ICs required for the design:

1. SN7448 - BCD to seven segment decoder (qty-5)
2. DM7402 - Quad 2 input NOR gates (qty - 1) (for SR latch)
3. DM54LS85 - 4-Bit Magnitude Comparators (qty -2)
4. CY74FCT191T - 4-Bit Up/Down Binary Counter (qty - 4)
5. MC74VHC86 - Quad 2-Input XOR Gate (qty - 2)
6. DM7408 - Quad 2-Input AND Gates (qty - 2)
7. DM74LS32 - Quad 2-Input OR Gate (qty -1)

Bill of Materials

Sr. No.	IC Number	Description	Quantity	Price (per unit) in INR	Amount in INR
1.	SN7448	BCD to 7 segment decoder	5	40	200
2.	DM7402	Quad 2 input NOR gates	1	25	25
3.	DM54LS85	4-Bit Magnitude Comparators	2	200	400
4.	CY74FCT191T	4-Bit Up/Down Binary Counter	4	100	400
5.	MC74VHC86	Quad 2-Input XOR Gate	2	15	30
6.	DM7408	Quad 2-Input AND Gates	2	20	40
7.	DM74LS32	Quad 2-Input OR Gate	1	15	15
		TOTAL	**17**	**415**	**1110**