

# MC74VHC86

## Quad 2-Input XOR Gate

The MC74VHC86 is an advanced high speed CMOS 2-input Exclusive-OR gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7 V, allowing the interface of 5 V systems to 3 V systems.

### Features

- High Speed:  $t_{PD} = 4.8 \text{ ns}$  (Typ) at  $V_{CC} = 5 \text{ V}$
- Low Power Dissipation:  $I_{CC} = 2 \mu\text{A}$  (Max) at  $T_A = 25^\circ\text{C}$
- High Noise Immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2 V to 5.5 V Operating Range
- Low Noise:  $V_{OLP} = 0.8 \text{ V}$  (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: Human Body Model (HBM) > 2000 V; Machine Model > 200 V
- Chip Complexity: 56 FETs or 14 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

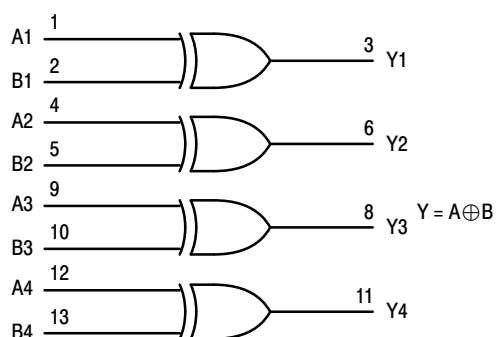


Figure 1. Logic Diagram

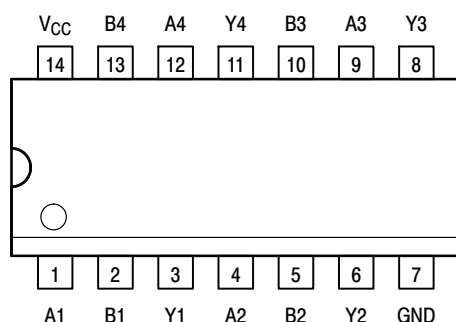


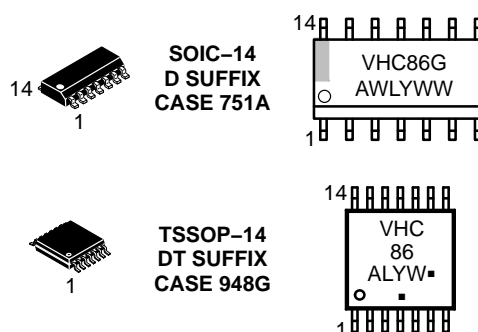
Figure 2. Pinout: 14-Lead Packages (Top View)



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### MARKING DIAGRAMS



A = Assembly Location  
WL, L = Wafer Lot  
Y, YY = Year  
WW, W = Work Week  
G or ■ = Pb-Free Package  
(Note: Microdot may be in either location)

### FUNCTION TABLE

| Inputs |   | Output |
|--------|---|--------|
| A      | B | Y      |
| L      | L | L      |
| L      | H | H      |
| H      | L | H      |
| H      | H | L      |

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

# MC74VHC86

## MAXIMUM RATINGS

| Symbol    | Parameter   | Value                 | Unit |
|-----------|---|-----------------------|------|
| $V_{CC}$  | DC Supply Voltage   | −0.5 to +7.0          | V    |
| $V_{in}$  | DC Input Voltage  | −0.5 to +7.0          | V    |
| $V_{out}$ | DC Output Voltage   | −0.5 to $V_{CC}$ +0.5 | V    |
| $I_{IK}$  | Input Diode Current   | −20                   | mA   |
| $I_{OK}$  | Output Diode Current  | ±20                   | mA   |
| $I_{out}$ | DC Output Current, per Pin                                      | ±25                   | mA   |
| $I_{CC}$  | DC Supply Current, $V_{CC}$ and GND Pins                        | ±50                   | mA   |
| $P_D$     | Power Dissipation in Still Air, SOIC Package†<br>TSSOP Package† | 500<br>450            | mW   |
| $T_{stg}$ | Storage Temperature   | −65 to +150           | °C   |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating SOIC Package: −7 mW/°C from 65° to 125°C  
TSSOP Package: −6.1 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

| Symbol     | Parameter  | Min    | Max       | Unit |
|------------|--|--------|-----------|------|
| $V_{CC}$   | DC Supply Voltage  | 2.0    | 5.5       | V    |
| $V_{in}$   | DC Input Voltage   | 0      | 5.5       | V    |
| $V_{out}$  | DC Output Voltage  | 0      | $V_{CC}$  | V    |
| $T_A$      | Operating Temperature, All Package Types   | −55    | +125      | °C   |
| $t_r, t_f$ | Input Rise and Fall Time<br>$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$<br>$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$ | 0<br>0 | 100<br>20 | ns/V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# MC74VHC86

## DC ELECTRICAL CHARACTERISTICS

| Symbol          | Parameter                 | Test Conditions  | V <sub>CC</sub><br>V | T <sub>A</sub> = 25°C         |                   |                               | T <sub>A</sub> = -55°C to +125°C |                               | Unit |
|-----------------|---------------------------|--|----------------------|-------------------------------|-------------------|-------------------------------|----------------------------------|-------------------------------|------|
|                 |                           |  |                      | Min                           | Typ               | Max                           | Min                              | Max                           |      |
| V <sub>IH</sub> | High-Level Input Voltage  |  | 2.0<br>3.0 to 5.5    | 1.50<br>V <sub>CC</sub> × 0.7 |                   |                               | 1.50<br>V <sub>CC</sub> × 0.7    |                               | V    |
| V <sub>IL</sub> | Low-Level Input Voltage   |  | 2.0<br>3.0 to 5.5    |                               |                   | 0.50<br>V <sub>CC</sub> × 0.3 |                                  | 0.50<br>V <sub>CC</sub> × 0.3 | V    |
| V <sub>OH</sub> | High-Level Output Voltage | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br>I <sub>OH</sub> = -50 μA                           | 2.0<br>3.0<br>4.5    | 1.9<br>2.9<br>4.4             | 2.0<br>3.0<br>4.5 |                               | 1.9<br>2.9<br>4.4                |                               | V    |
|                 |                           | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br>I <sub>OH</sub> = -4 mA<br>I <sub>OH</sub> = -8 mA | 3.0<br>4.5           | 2.58<br>3.94                  |                   |                               | 2.48<br>3.80                     |                               |      |
| V <sub>OL</sub> | Low-Level Output Voltage  | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br>I <sub>OL</sub> = 50 μA                            | 2.0<br>3.0<br>4.5    |                               | 0<br>0<br>0       | 0.1<br>0.1<br>0.1             |                                  | 0.1<br>0.1<br>0.1             | V    |
|                 |                           | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br>I <sub>OL</sub> = 4 mA<br>I <sub>OL</sub> = 8 mA   | 3.0<br>4.5           |                               |                   | 0.36<br>0.36                  |                                  | 0.44<br>0.44                  |      |
| I <sub>in</sub> | Input Leakage Current     | V <sub>in</sub> = 5.5 V or GND   | 0 to 5.5             |                               |                   | ±0.1                          |                                  | ±1.0                          | μA   |
| I <sub>CC</sub> | Quiescent Supply Current  | V <sub>in</sub> = V <sub>CC</sub> or GND   | 5.5                  |                               |                   | 2.0                           |                                  | 20.0                          | μA   |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3.0ns)

| Symbol                                 | Parameter                      | Test Conditions  | T <sub>A</sub> = 25°C |            |              | T <sub>A</sub> = -55°C to +125°C |              | Unit |
|--|--------------------------------|--|-----------------------|------------|--------------|----------------------------------|--------------|------|
|  |                                |  | Min                   | Typ        | Max          | Min                              | Max          |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Propagation Delay, A or B to Y | V <sub>CC</sub> = 3.3 ± 0.3 V C <sub>L</sub> = 15 pF<br>C <sub>L</sub> = 50 pF |                       | 7.0<br>9.5 | 11.0<br>14.5 | 1.0<br>1.0                       | 13.0<br>16.5 | ns   |
|  |                                | V <sub>CC</sub> = 5.0 ± 0.5 V C <sub>L</sub> = 15 pF<br>C <sub>L</sub> = 50 pF |                       | 4.8<br>6.3 | 6.8<br>8.8   | 1.0<br>1.0                       | 8.0<br>10.0  |      |
| C <sub>in</sub>                        | Input Capacitance              |  |                       | 4          | 10           |                                  | 10           | pF   |

|                 |   |   |    |
|-----------------|---|---|----|
| C <sub>PD</sub> | Power Dissipation Capacitance (Note 1.) | Typical @ 25°C, V <sub>CC</sub> = 5.0 V | pF |
|                 |   | 18                                      |    |

1. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>/4 (per gate). C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

## NOISE CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3.0ns, C<sub>L</sub> = 50 pF, V<sub>CC</sub> = 5.0 V, Measured in SOIC Package)

| Symbol           | Characteristic                               | T <sub>A</sub> = 25°C |      | Unit |
|------------------|--|-----------------------|------|------|
|                  |  | Typ                   | Max  |      |
| V <sub>OLP</sub> | Quiet Output Maximum Dynamic V <sub>OL</sub> | 0.3                   | 0.8  | V    |
| V <sub>OLV</sub> | Quiet Output Minimum Dynamic V <sub>OL</sub> | -0.3                  | -0.8 | V    |
| V <sub>IHD</sub> | Minimum High Level Dynamic Input Voltage     |                       | 3.5  | V    |
| V <sub>ILD</sub> | Maximum Low Level Dynamic Input Voltage      |                       | 1.5  | V    |

# MC74VHC86

## ORDERING INFORMATION

| Device          | Package               | Shipping†          |
|-----------------|-----------------------|--------------------|
| MC74VHC86DR2G   | SOIC-14<br>(Pb-Free)  | 2500 / Tape & Reel |
| MC74VHC86DTG    | TSSOP-14<br>(Pb-Free) | 96 Units / Rail    |
| MC74VHC86DTR2G  | TSSOP-14<br>(Pb-Free) | 2500 / Tape & Reel |
| NLVVHC86ADTR2G* | TSSOP-14<br>(Pb-Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

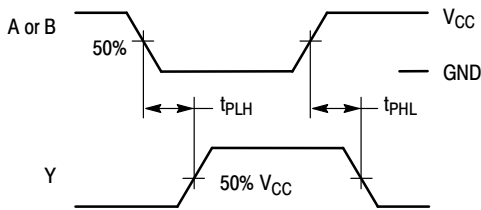
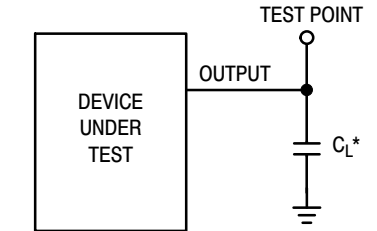


Figure 3. Switching Waveforms



\*Includes all probe and jig capacitance

Figure 4. Test Circuit

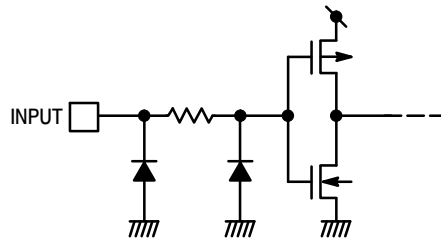
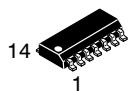


Figure 5. Input Equivalent Circuit

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

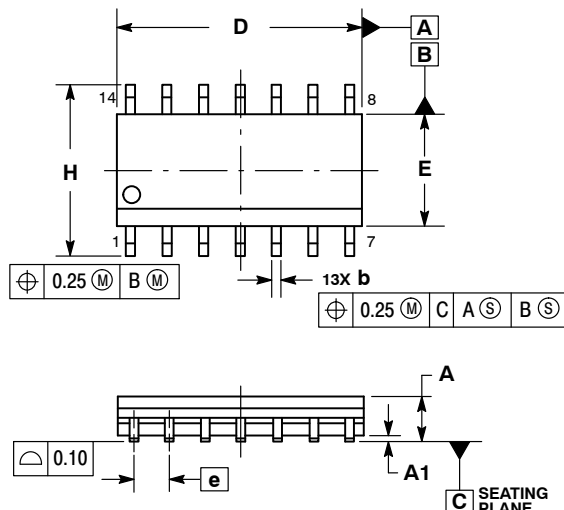
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SOIC-14 NB  
CASE 751A-03  
ISSUE L

DATE 03 FEB 2016

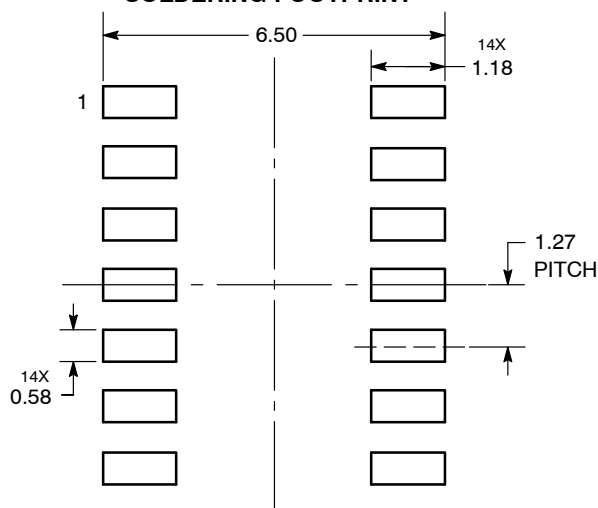


## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 1.35        | 1.75 | 0.054     | 0.068 |
| A1  | 0.10        | 0.25 | 0.004     | 0.010 |
| A3  | 0.19        | 0.25 | 0.008     | 0.010 |
| b   | 0.35        | 0.49 | 0.014     | 0.019 |
| D   | 8.55        | 8.75 | 0.337     | 0.344 |
| E   | 3.80        | 4.00 | 0.150     | 0.157 |
| e   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 5.80        | 6.20 | 0.228     | 0.244 |
| h   | 0.25        | 0.50 | 0.010     | 0.019 |
| L   | 0.40        | 1.25 | 0.016     | 0.049 |
| M   | 0°          | 7°   | 0°        | 7°    |

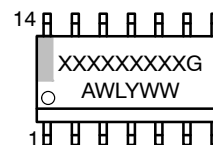
## SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

STYLES ON PAGE 2

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**SOIC-14**  
**CASE 751A-03**  
**ISSUE L**

**DATE 03 FEB 2016**

**STYLE 1:**  
PIN 1. COMMON CATHODE  
2. ANODE/CATHODE  
3. ANODE/CATHODE  
4. NO CONNECTION  
5. ANODE/CATHODE  
6. NO CONNECTION  
7. ANODE/CATHODE  
8. ANODE/CATHODE  
9. ANODE/CATHODE  
10. NO CONNECTION  
11. ANODE/CATHODE  
12. ANODE/CATHODE  
13. NO CONNECTION  
14. COMMON ANODE

**STYLE 2:**  
CANCELLED

**STYLE 3:**  
PIN 1. NO CONNECTION  
2. ANODE  
3. ANODE  
4. NO CONNECTION  
5. ANODE  
6. NO CONNECTION  
7. ANODE  
8. ANODE  
9. ANODE  
10. NO CONNECTION  
11. ANODE  
12. ANODE  
13. NO CONNECTION  
14. COMMON CATHODE

**STYLE 4:**  
PIN 1. NO CONNECTION  
2. CATHODE  
3. CATHODE  
4. NO CONNECTION  
5. CATHODE  
6. NO CONNECTION  
7. CATHODE  
8. CATHODE  
9. CATHODE  
10. NO CONNECTION  
11. CATHODE  
12. CATHODE  
13. NO CONNECTION  
14. COMMON ANODE


**STYLE 5:**  
PIN 1. COMMON CATHODE  
2. ANODE/CATHODE  
3. ANODE/CATHODE  
4. ANODE/CATHODE  
5. ANODE/CATHODE  
6. NO CONNECTION  
7. COMMON ANODE  
8. COMMON CATHODE  
9. ANODE/CATHODE  
10. ANODE/CATHODE  
11. ANODE/CATHODE  
12. ANODE/CATHODE  
13. NO CONNECTION  
14. COMMON ANODE

**STYLE 6:**  
PIN 1. CATHODE  
2. CATHODE  
3. CATHODE  
4. CATHODE  
5. CATHODE  
6. CATHODE  
7. CATHODE  
8. ANODE  
9. ANODE  
10. ANODE  
11. ANODE  
12. ANODE  
13. ANODE  
14. ANODE

**STYLE 7:**  
PIN 1. ANODE/CATHODE  
2. COMMON ANODE  
3. COMMON CATHODE  
4. ANODE/CATHODE  
5. ANODE/CATHODE  
6. ANODE/CATHODE  
7. ANODE/CATHODE  
8. ANODE/CATHODE  
9. ANODE/CATHODE  
10. ANODE/CATHODE  
11. COMMON CATHODE  
12. COMMON ANODE  
13. ANODE/CATHODE  
14. ANODE/CATHODE

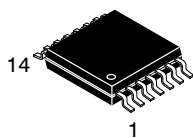
**STYLE 8:**  
PIN 1. COMMON CATHODE  
2. ANODE/CATHODE  
3. ANODE/CATHODE  
4. NO CONNECTION  
5. ANODE/CATHODE  
6. ANODE/CATHODE  
7. COMMON ANODE  
8. COMMON ANODE  
9. ANODE/CATHODE  
10. ANODE/CATHODE  
11. NO CONNECTION  
12. ANODE/CATHODE  
13. ANODE/CATHODE  
14. COMMON CATHODE

|                         |                    |   |
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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

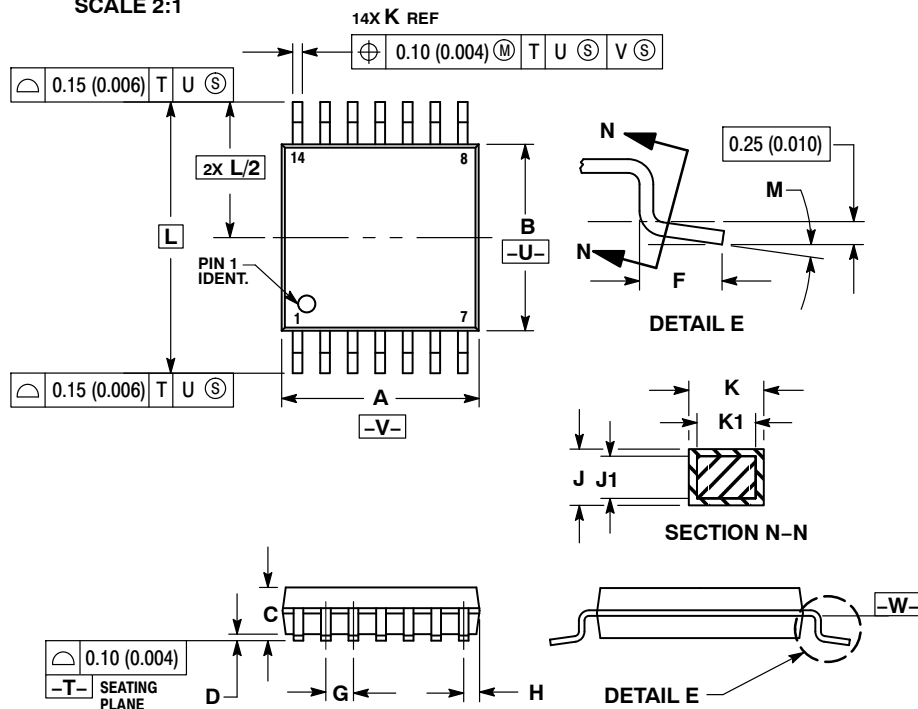
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SCALE 2:1

## TSSOP-14 WB CASE 948G ISSUE C

DATE 17 FEB 2016

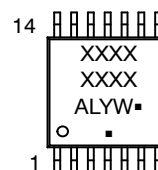


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.50        | 0.60 | 0.020     | 0.024 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

### GENERIC MARKING DIAGRAM\*

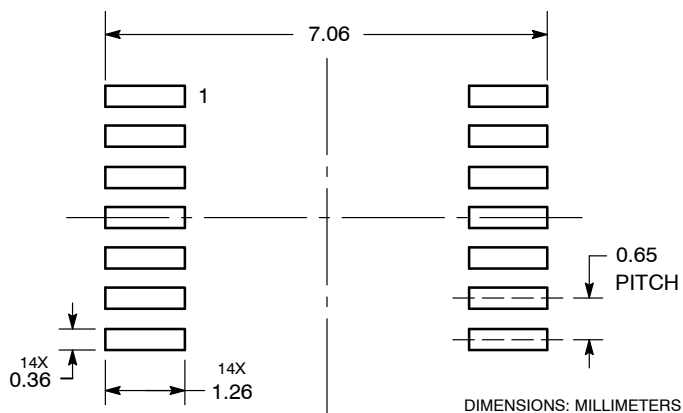


- A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

### SOLDERING FOOTPRINT




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