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INTERNATIONAL  
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AKURDI PUNE

**D.Y. PATIL INTERNATIONAL UNIVERSITY**

**B.TECH CSE FY SEM-2**

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**SUBJECT: DIGITAL LOGIC AND DESIGN**

**BATCH: A1**

### **EXPERIMENT-4 (A)**

#### **Aim:**

Implementation of 4x1 multiplexer.

#### **Requirements:**

- AND gate
- OR gate
- NOT gate
- MyDaQ

#### **Theory:**

Multiplexer is a device that has multiple inputs and a single line output. The select lines determine which input is connected to the output, and also to increase the amount of data that can be sent over a network within certain time. It is also called a data selector.

Multiplexers are classified into four types:

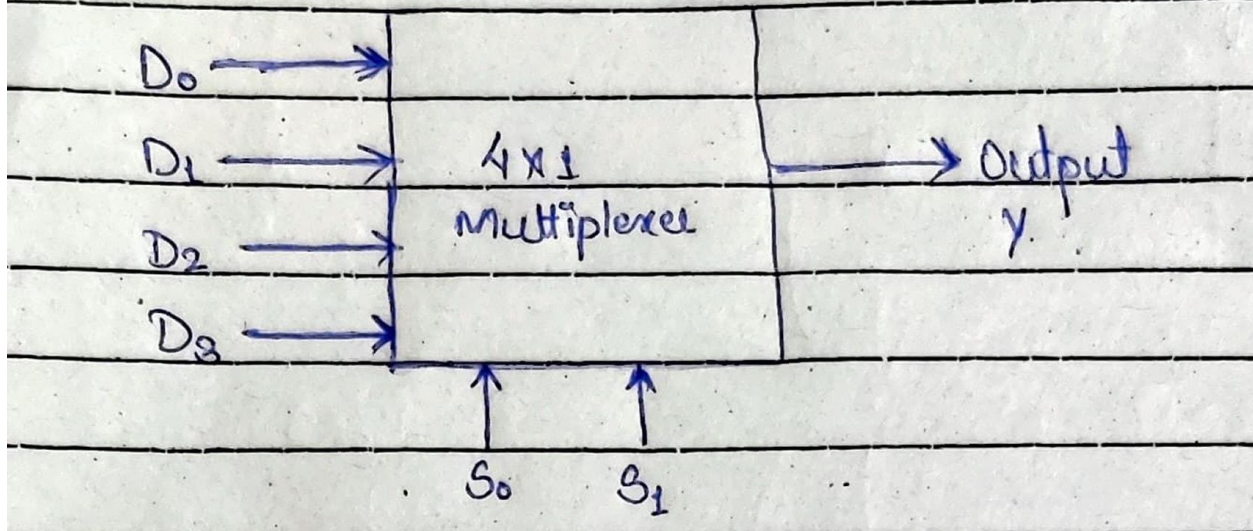
1. 2-1 Multiplexer (1 select line)
2. 4-1 Multiplexer (2 select lines)
3. 8-1 Multiplexer (3 select lines)
4. 16-1 multiplexer (4 select lines)

#### **4x1 Multiplexer:**

4x1 Multiplexer has four data inputs D0, D1, D2 & D3, two selection lines S0 & S1 and one output Y. The block diagram of 4x1 Multiplexer is shown in the following figure. One of these 4 inputs will be connected to the output based on the combination of inputs present at these two selection lines.

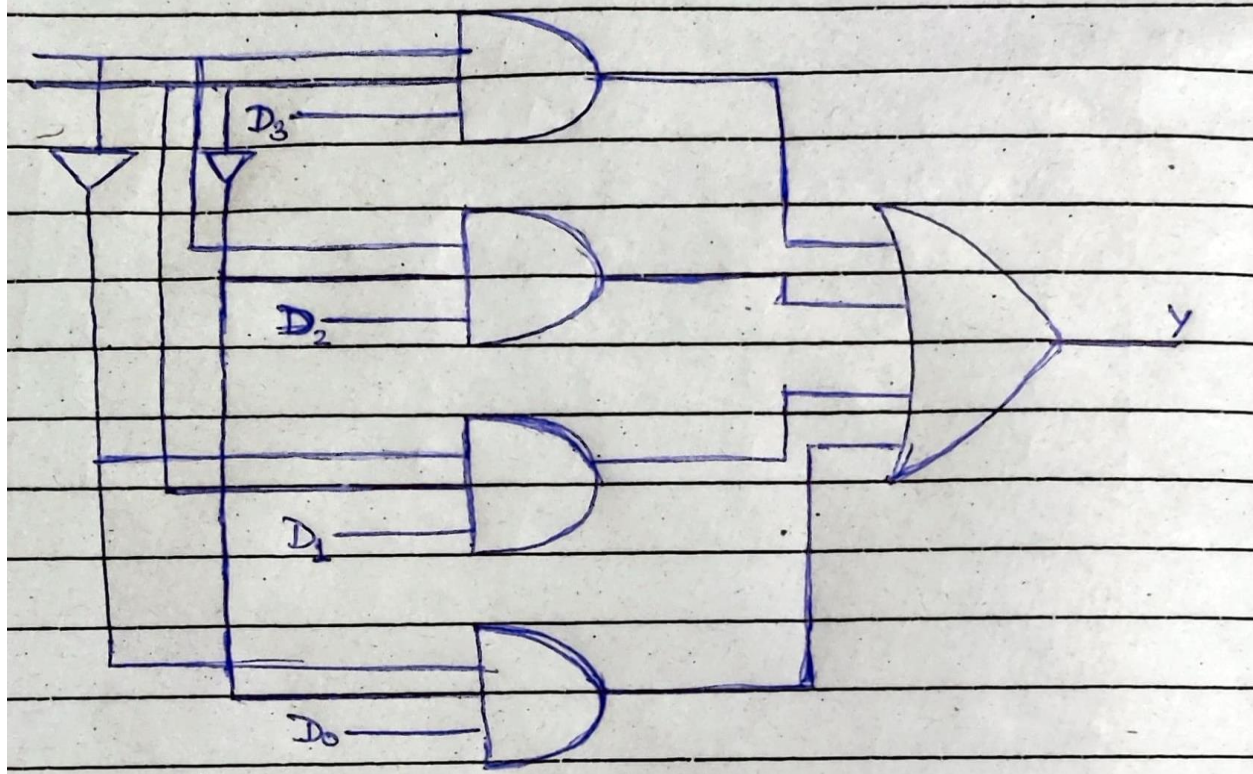
### Block Diagram of 4x1 Multiplexer:

#### Block Diagram of 4x1 Multiplexer:



### Circuit Diagram:

#### Circuit Diagram of 4x1 Multiplexer:



Truth Table:

Selection lines		output
$S_0$	$S_1$	$Y$
0	0	$D_0$
0	1	$D_1$
1	0	$D_2$
1	1	$D_3$

Mathematical Expression for 4x1 Multiplexer:

$$Y = S_1' S_0' D_0 + S_1' S_0 D_1 + S_1 S_0' D_2 + S_1 S_0 D_3$$

**Observation Table:**

Input Variables-  $E_a, S_1, S_0$

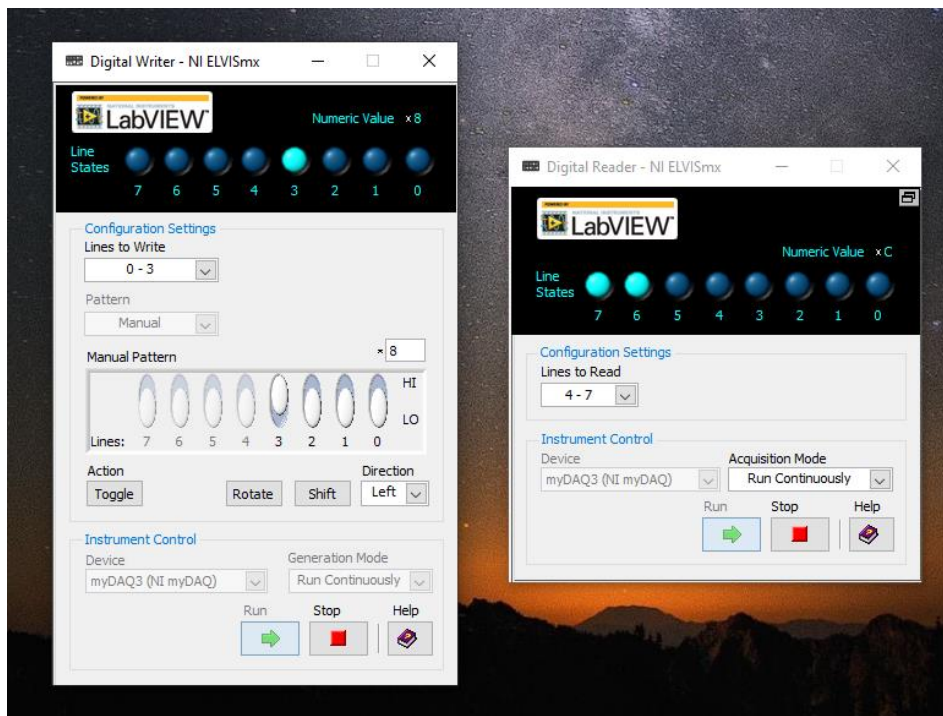
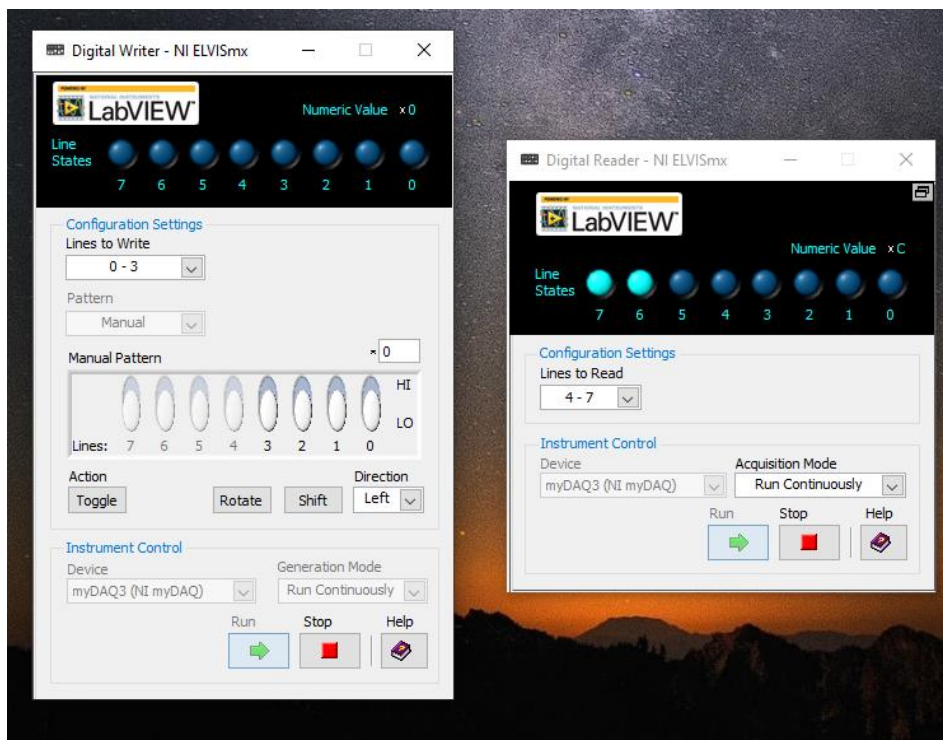
Output Variables-  $Y_a$

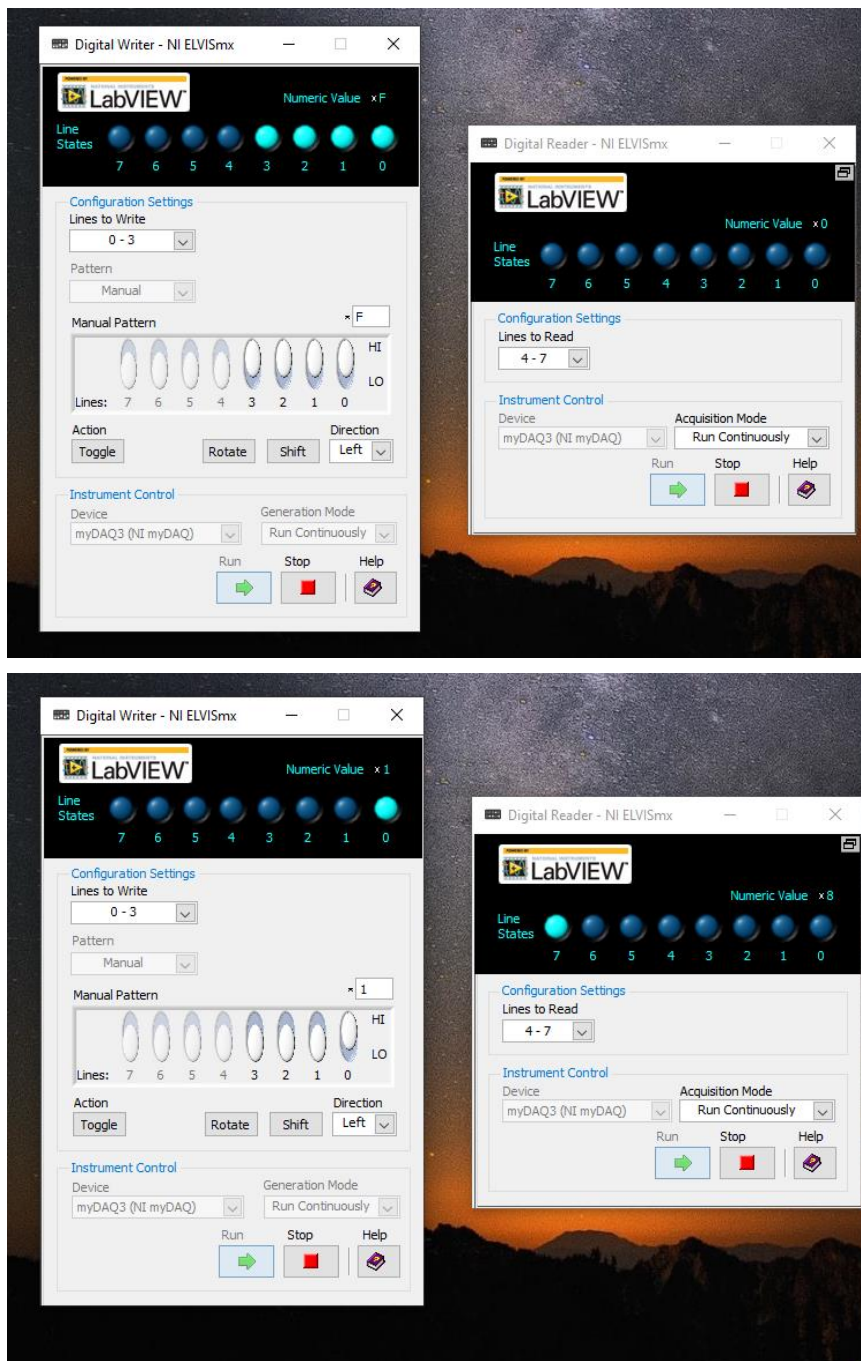
where,  $E_a, E_b$  represents the enable bits for the respective multiplexers and  $S_1, S_0$  are the select lines.  $Y_a, Y_b$  represents the output bits for the respective multiplexers.

Input			Output
$\overline{E_a}$	$S_1$	$S_0$	$Y_a$
D0	0	0	D0
D1	1	0	D1
D2	0	1	D2
D3	1	1	D3

**Output:**







**Result:** The implementation of 4x1 multiplexer is done.

## EXPERIMENT-4 (B)

### Aim:

Implementation of 1x4 demultiplexer.

### Requirements:

- NAND Gate
- NOT Gate

### Theory:

Describe the demultiplexers in brief and enlist the different demultiplexers. And also explain the 1x4 demultiplexer along with its block diagram.

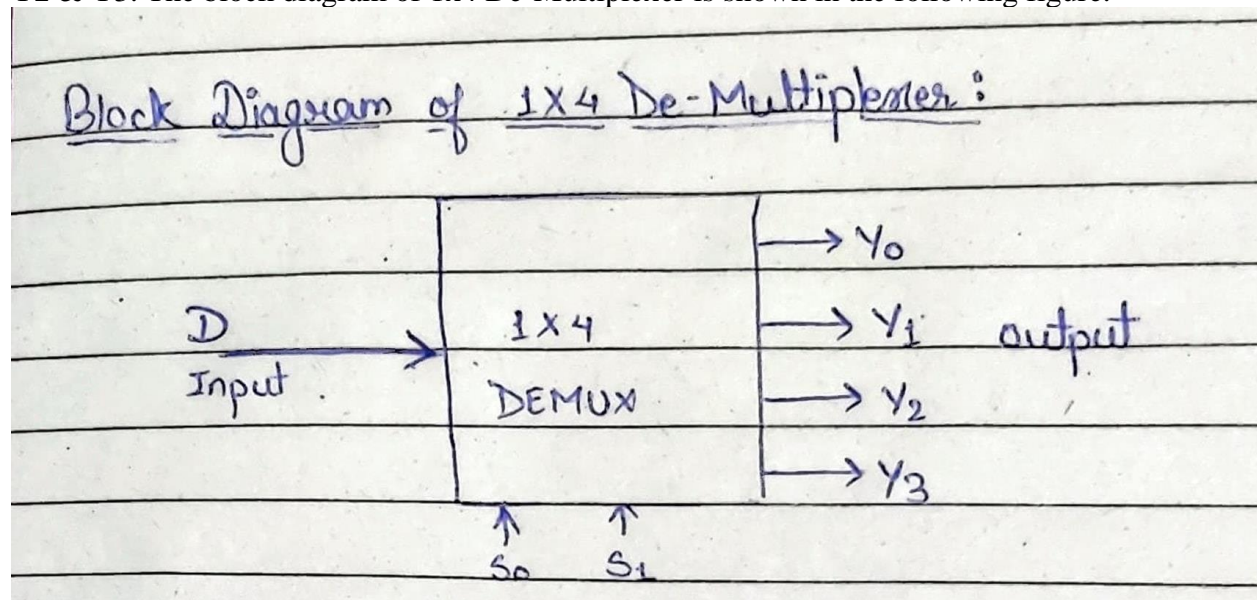
De-multiplexer De-multiplexer is also a device with one input and multiple output lines. It is used to send a signal to one of the many devices. The main difference between a multiplexer and a de-multiplexer is that a multiplexer takes two or more signals and encodes them on a wire, whereas a de-multiplexer does reverse to what the multiplexer does.

De-Multiplexer are classified into four types:

- 1) 1-2 demultiplexer (1 select line)
- 2) 1-4 demultiplexer (2 select lines)
- 3) 1-8 demultiplexer (3 select lines)
- 4) 1-16 demultiplexer (4 select lines)

### **1x4 De-multiplexer:**

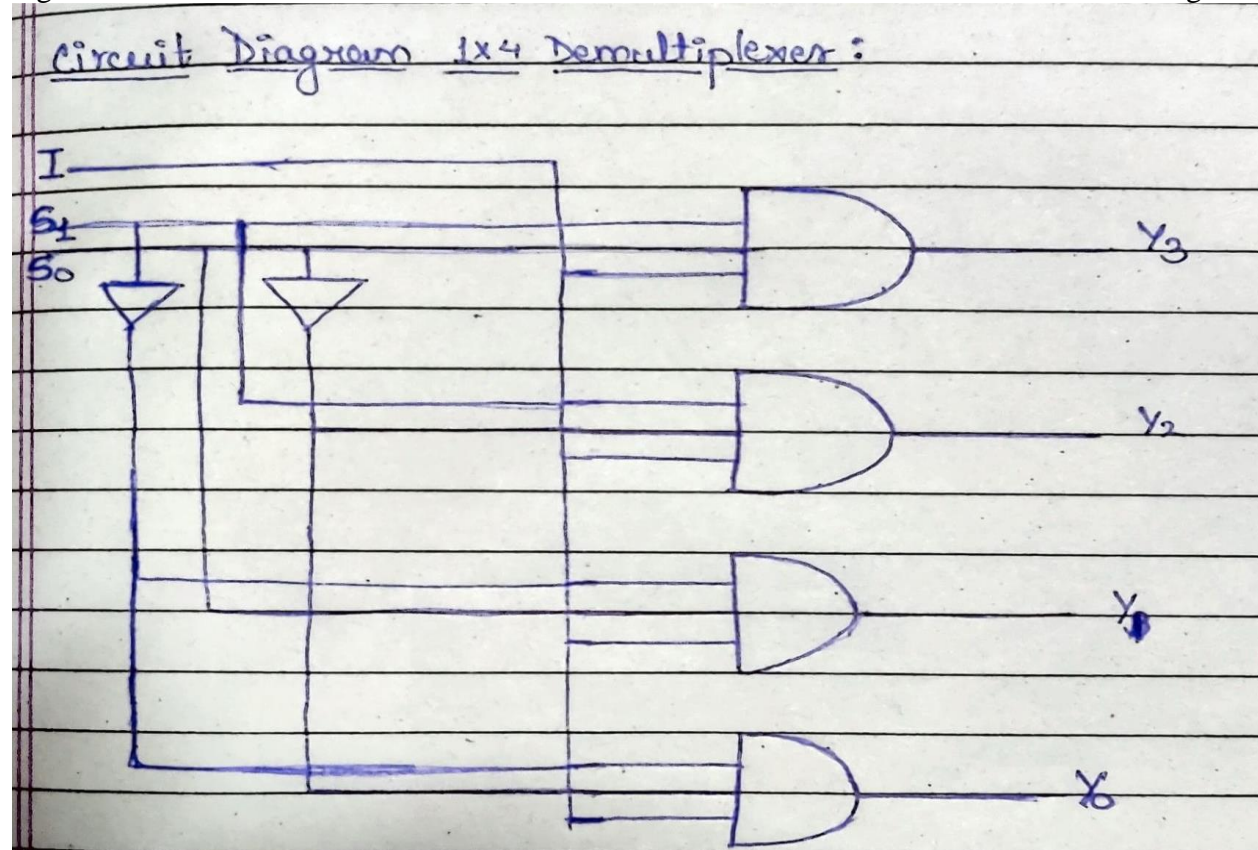
1x4 De-Multiplexer has one input Data(D), two selection lines, S0 & S1 and four outputs Y0, Y1, Y2 & Y3. The block diagram of 1x4 De-Multiplexer is shown in the following figure.





### Circuit Diagram:

Mention the mathematical equations used for the realization part along with its truth table and logic diagram.



Truth Table :

Selection Inputs		outputs			
S <sub>0</sub>	S <sub>1</sub>	Y <sub>3</sub>	Y <sub>2</sub>	Y <sub>1</sub>	Y <sub>0</sub>
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

### Mathematical Expression:

$$Y_3 = S_1 S_0 D$$

$$Y_2 = S_1 S_0' D$$

$$Y_1 = S_1' S_0 D$$

$$Y_0 = S_1' S_0' D$$

**Observation Table:**

Input Variables- G, B, A

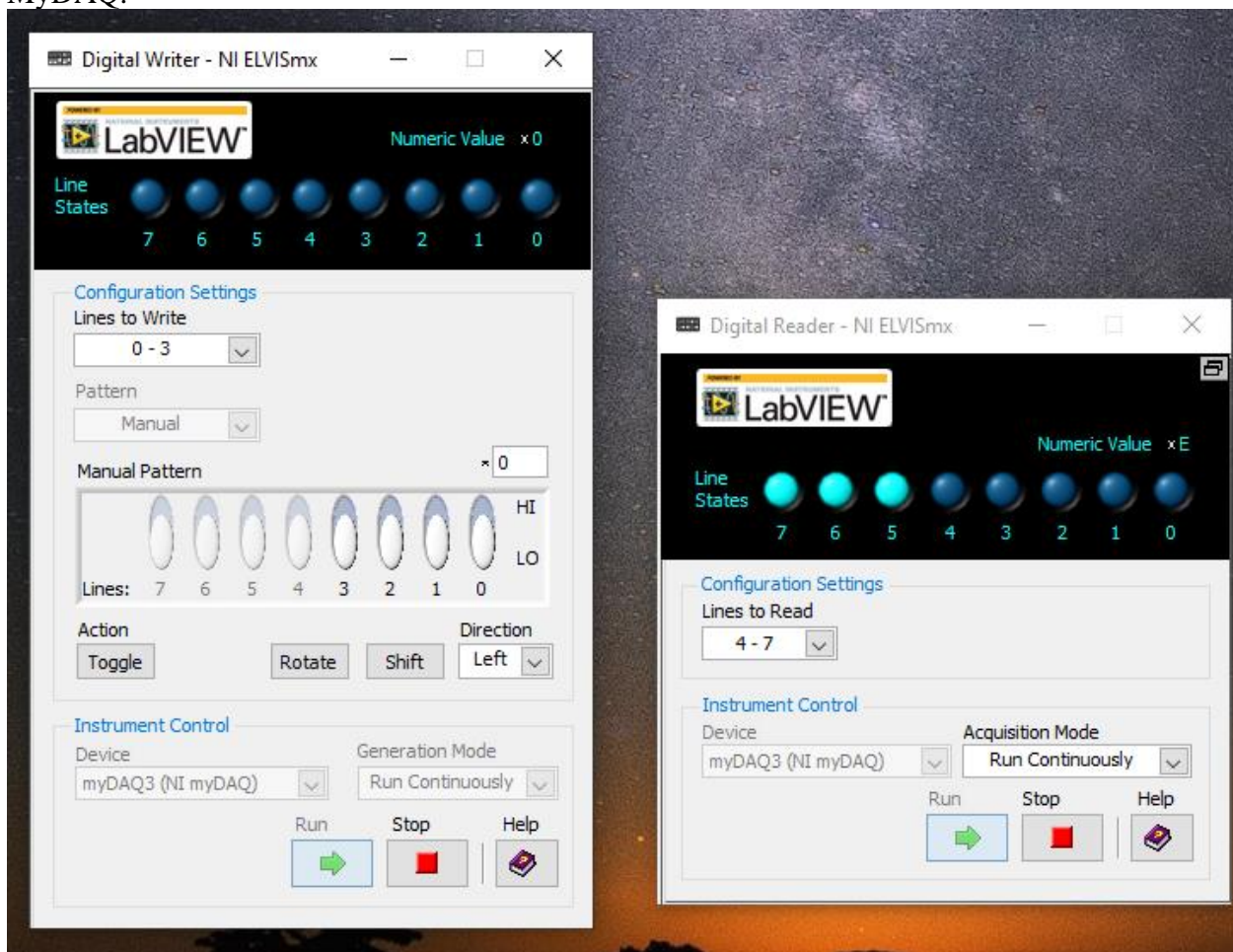
Output Variables-  $Y_0, Y_1, Y_2, Y_3$

where G, B, A represents the input bits for 1x4 demultiplexer,

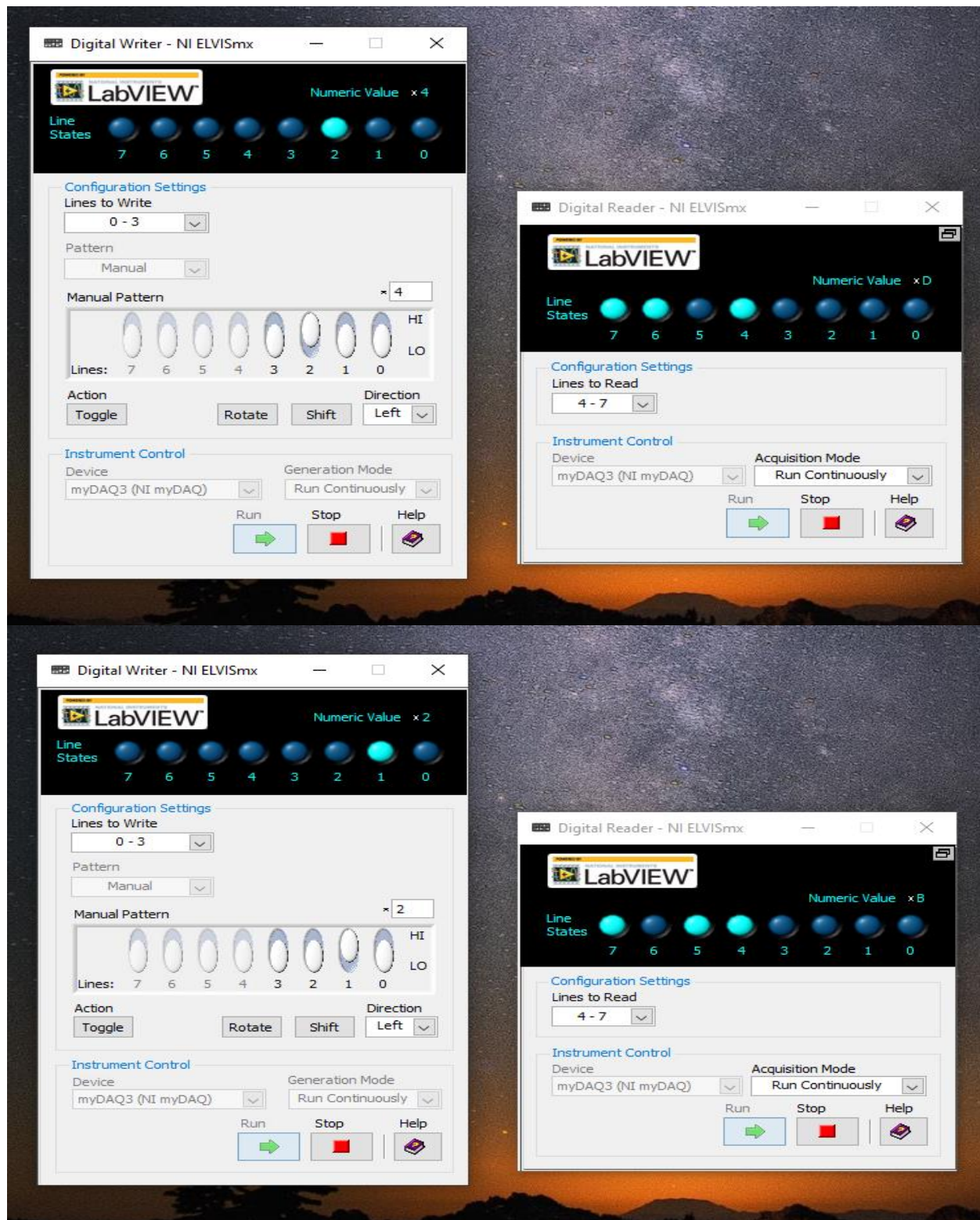
$Y_0, Y_1, Y_2, Y_3$  represents the output bits for 1x4 demultiplexer

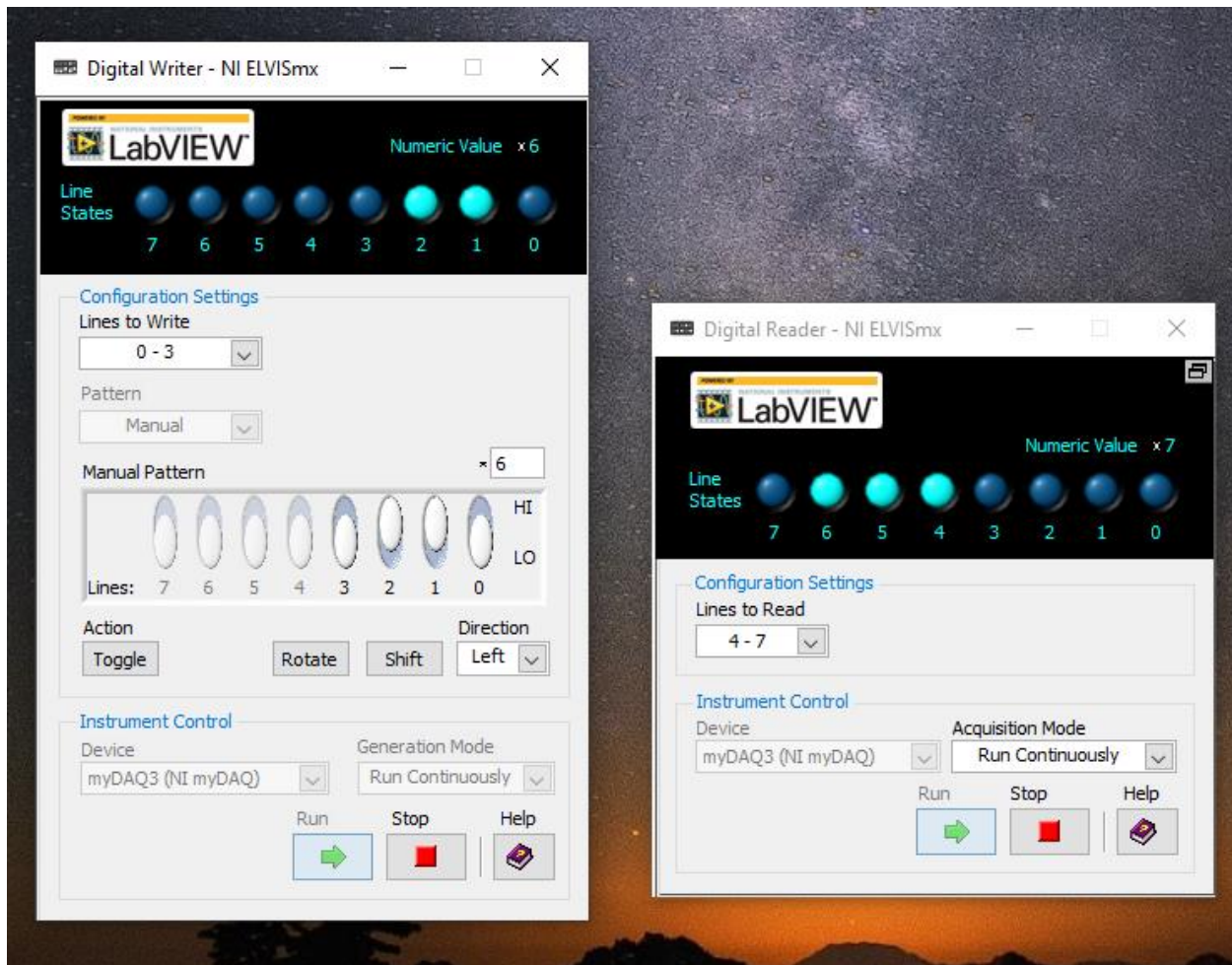
Input			Output			
G	B	A	$Y_0$	$Y_1$	$Y_2$	$Y_3$
D	0	0	D	0	0	0
D	1	0	0	D	0	0
D	0	1	0	0	D	0
D	1	1	0	0	0	D

**Output:** Attach the screenshots of the simulation of 1x4 demultiplexer which is performed on MyDAQ.









**Result:**

The implementation of 1x4 demultiplexer is done.