D.Y. PATIL INTERNATIONAL UNIVERSITY

B.TECH CSE FY SEM-2

A.Y. 2022-2023

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SUBJECT: DIGITAL LOGIC AND DESIGN

BATCH: A1

EXPERIMENT-6

Aim:

Verify the truth table of RS, JK, T and D flip-flops using NAND and NOR gates.

Requirements:

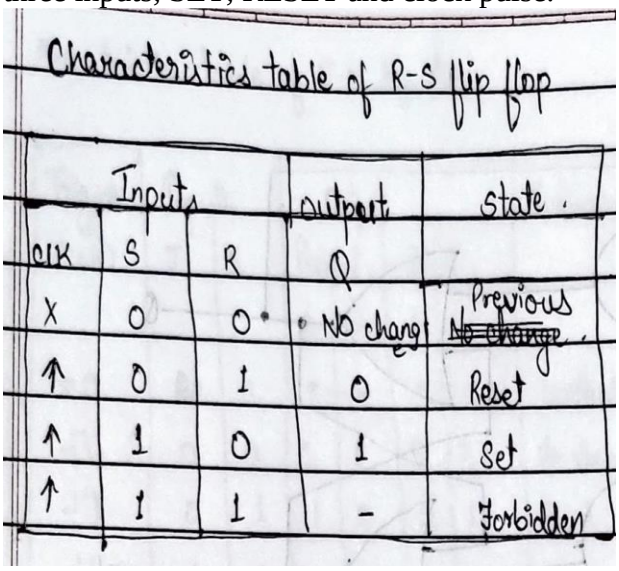
- NAND gate

Theory:

A flip flop is an electronic circuit with two stable states that can be used to store binary data. The stored data can be changed by applying varying inputs. Flip-flops and latches are fundamental building blocks of digital electronics systems used in computers, communications, and many other types of systems.

1. R-S flip flop

   The basic NAND gate RS flip flop circuit is used to store the data and thus provides feedback from both of its outputs again back to its inputs. The RS flip flop actually has three inputs, SET, RESET and clock pulse.



Characteristics table of R-S flip flop

Inputs			output	state
clk	S	R	Q	
X	0	0	No chang	Previous ~~No change~~
↑	0	1	0	Reset
↑	1	0	1	Set
↑	1	1	-	Forbidden

2. D flip flop

A D flip flop has a single data input. This type of flip flop is obtained from the SR flip flop by connecting the R input through an inverter, and the S input is connected directly to data input. The modified clocked SR flip-flop is known as D-flip-flop and is shown below. From the truth table of SR flip-flop we see that the output of the SR flip-flop is in unpredictable state when the inputs are same and high. In many practical applications, these input conditions are not required. These input conditions can be avoided by making them complement of each other.

Characteristics table of D flip flop

Input			output	
D	reset	clock	Q	Q'
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	1	0
1	1	0	0	1
1	1	1	0	1

3. J-K flip flop

In a RS flip-flop the input R=S=1 leads to an indeterminate output. The RS flip-flop circuit may be re-joined if both inputs are 1 than also the outputs are complement of each other as shown in characteristics table below.

Characteristics table of J-K flip flop.

Trigger (CLK)	Inputs		Output				Inference
	J	K	Present		Next		
			Q	Q'	Q	Q'	
0	0	x	-	-	-	-	Latched
⎍	0	0	0	1	0	1	No change
⎍	0	1	1	0	0	1	Reset
⎍	1	0	1	0	1	0	Set
⎍	1	1	0	1	1	0	Toggles

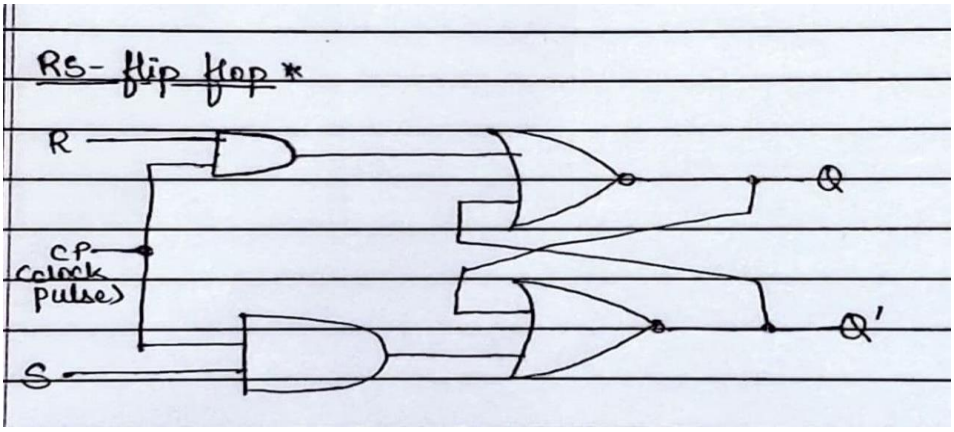
4. T flip flop

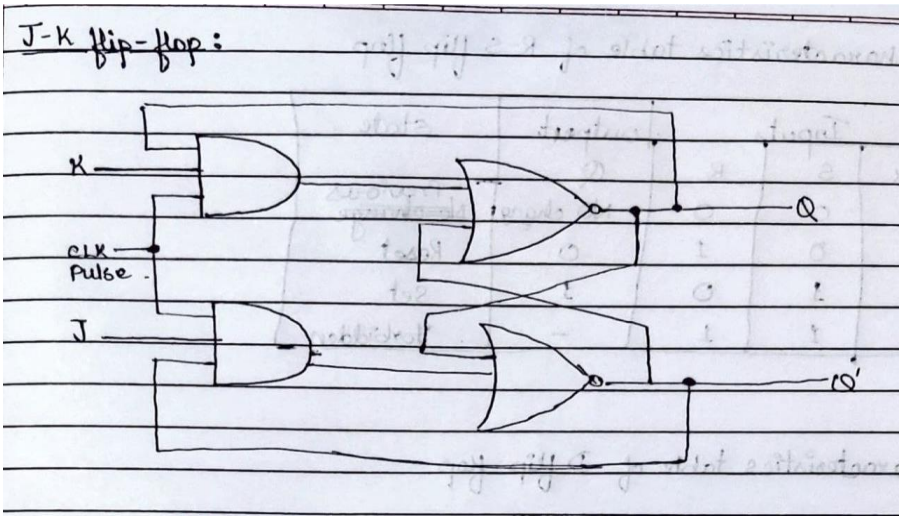
T flip-flop is known as toggle flip-flop. The T flip-flop is modification of the J-K flip-flop. Both the JK inputs of the JK flip – flop are held at logic 1 and the clock signal continuous to change as shown in table below.

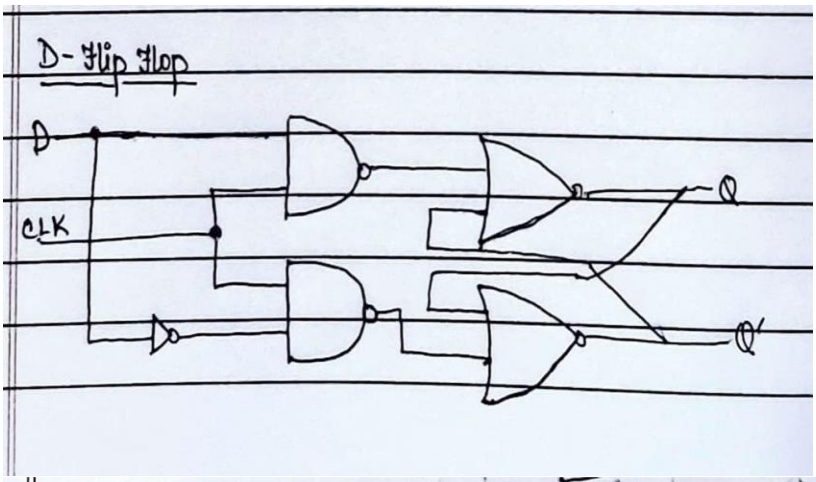
Characteristics table of T flip-flop

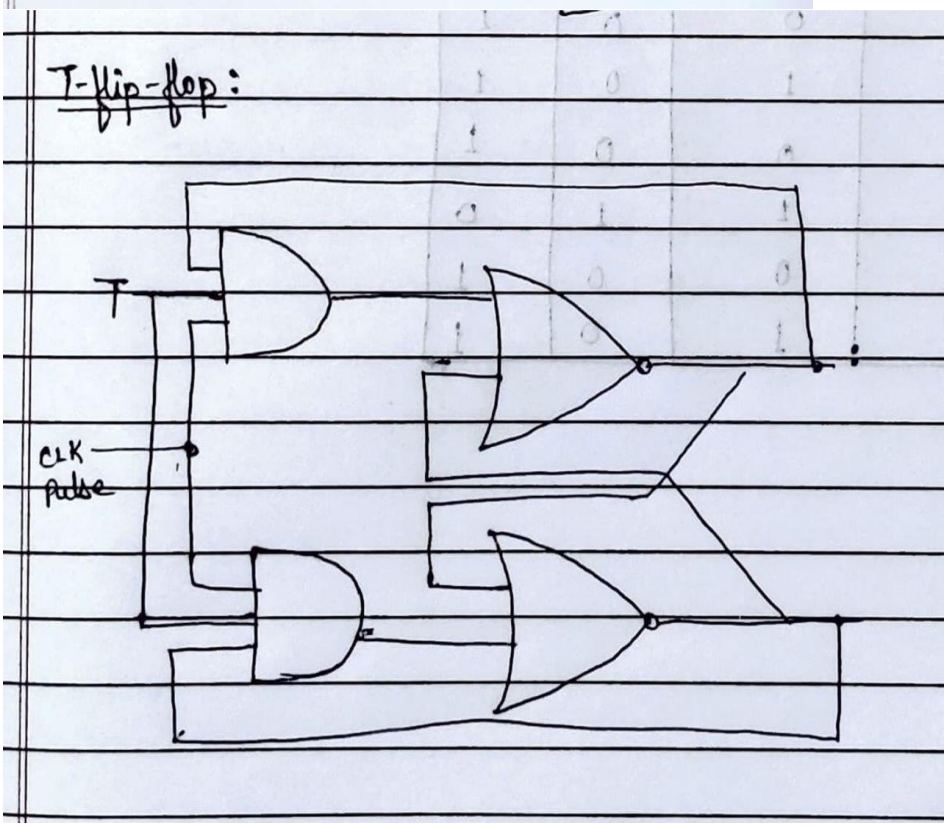
T	Clock	Q	Q'
0	↑	Q	Q'
1	↑	Q'	Q
X	↓	Q	Q'

Circuit Diagram:









Observation Table:

I. RS Flip Flop

Input				Output				Remarks
Sr. No.	Clock	S	R	Q (n-1)	Q'(n-1)	Q	Q'	
1.	0	0	0	X	X	0	1	No change
2.	1	0	1	0	1	0	1	Reset

3.	1	1	0	0	1	1	0	Set
4.	1	1	1	1	0	0	0	INVALID

II. JK Flip Flop

Input				**Output**				**Remarks**
Sr. No.	**Clock**	**J**	**K**	**Q (n-1)**	**Q'(n-1)**	**Q**	**Q'**	
1.	1	1	1	0	1	1	0	Toggle
2.	1	0	0	0	1	0	1	No Change
3.	1	0	1	0	1	0	1	Reset
4.	1	1	0	0	1	1	0	Set

III. D Flip Flop

Input			**Output**				**Remarks**
Sr. No.	**Clock**	**D**	**Q (n-1)**	**Q'(n-1)**	**Q**	**Q'**	
1.	0	0	X	X1	0	1	No Change
2.	1	0	0	1	0	1	Reset
3.	0	1	0	1	0	1	No Change
4.	1	1	0	1	1	0	Set

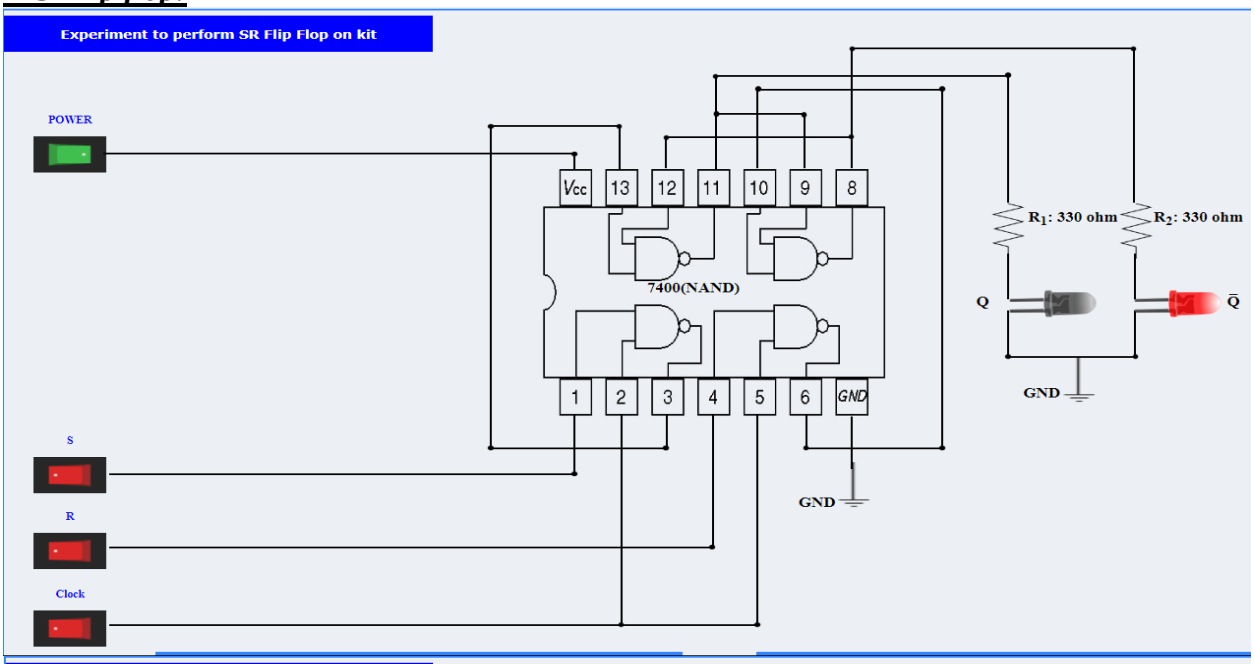
IV. T Flip Flop

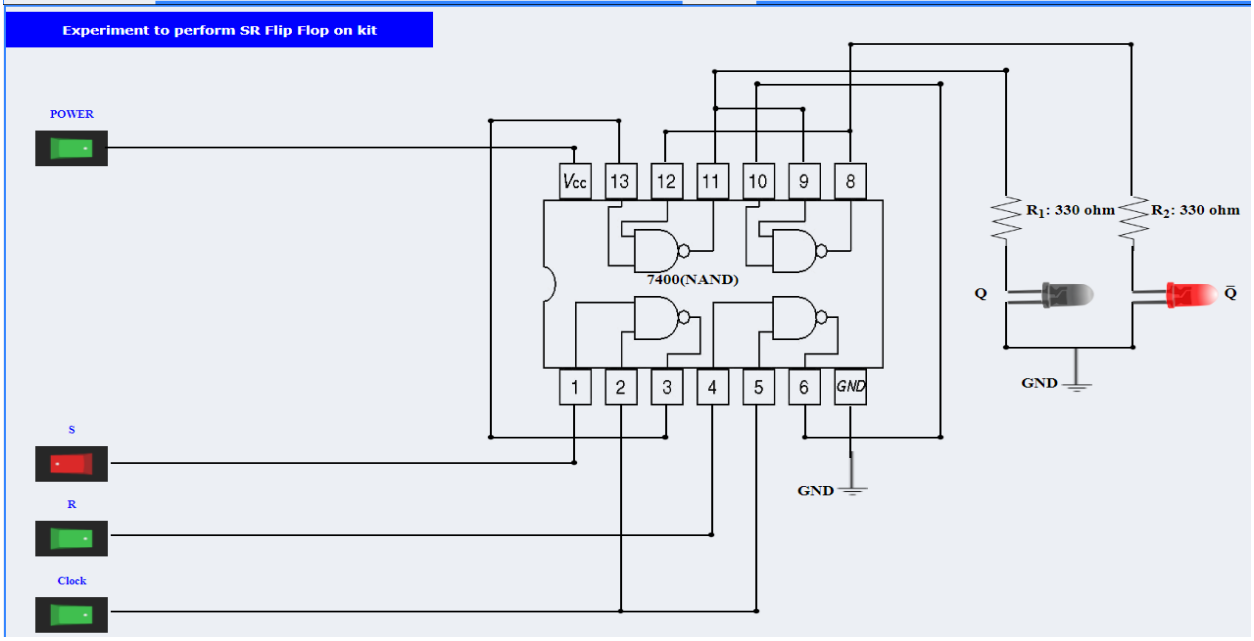
Input			**Output**				**Remarks**
Sr. No.	**Clock**	**T**	**Q (n-1)**	**Q'(n-1)**	**Q**	**Q'**	

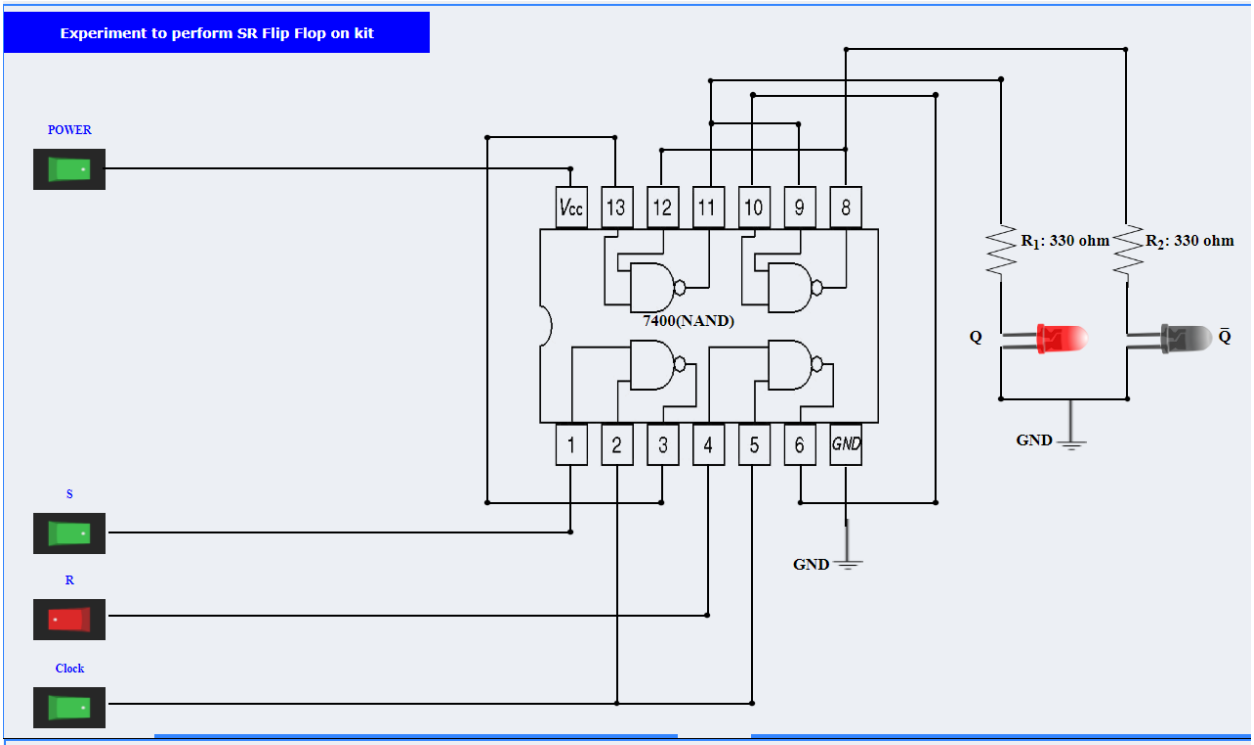
1.	1	0	X	X	0	1	No Change
2.	1	1	0	1	1	0	Toggle
3.	0	0	1	0	1	0	No change

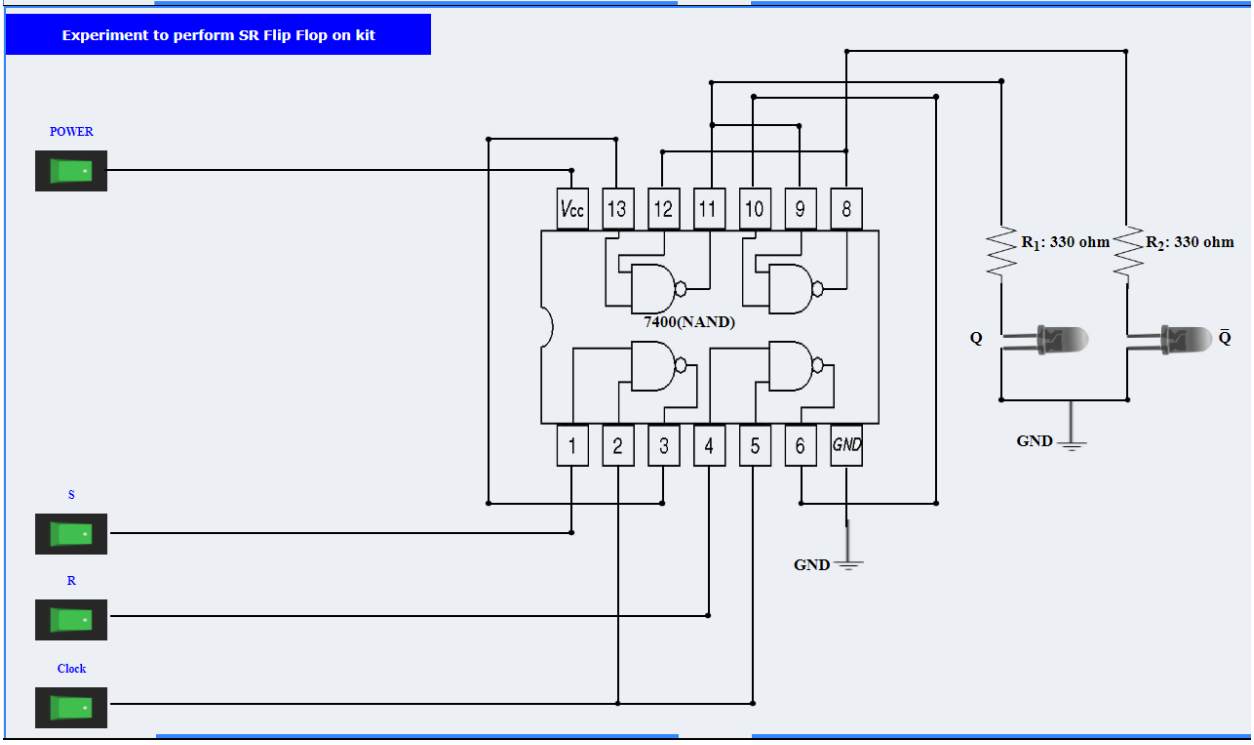
Output: Attach the screenshots of the simulation of all the flip flops with their respective timing diagrams as well as IC diagrams (circuit diagrams).

R-S Flip flop:

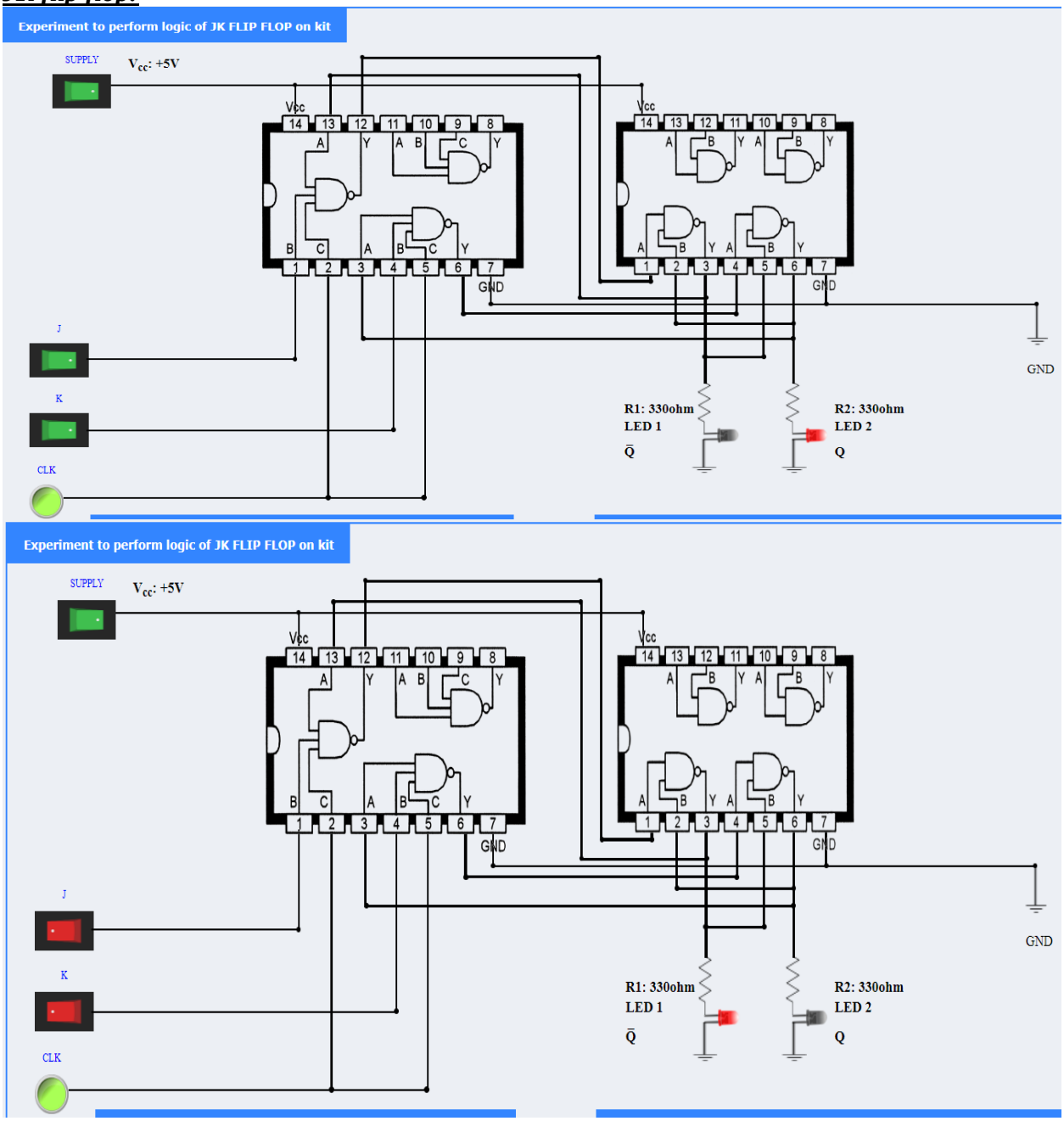


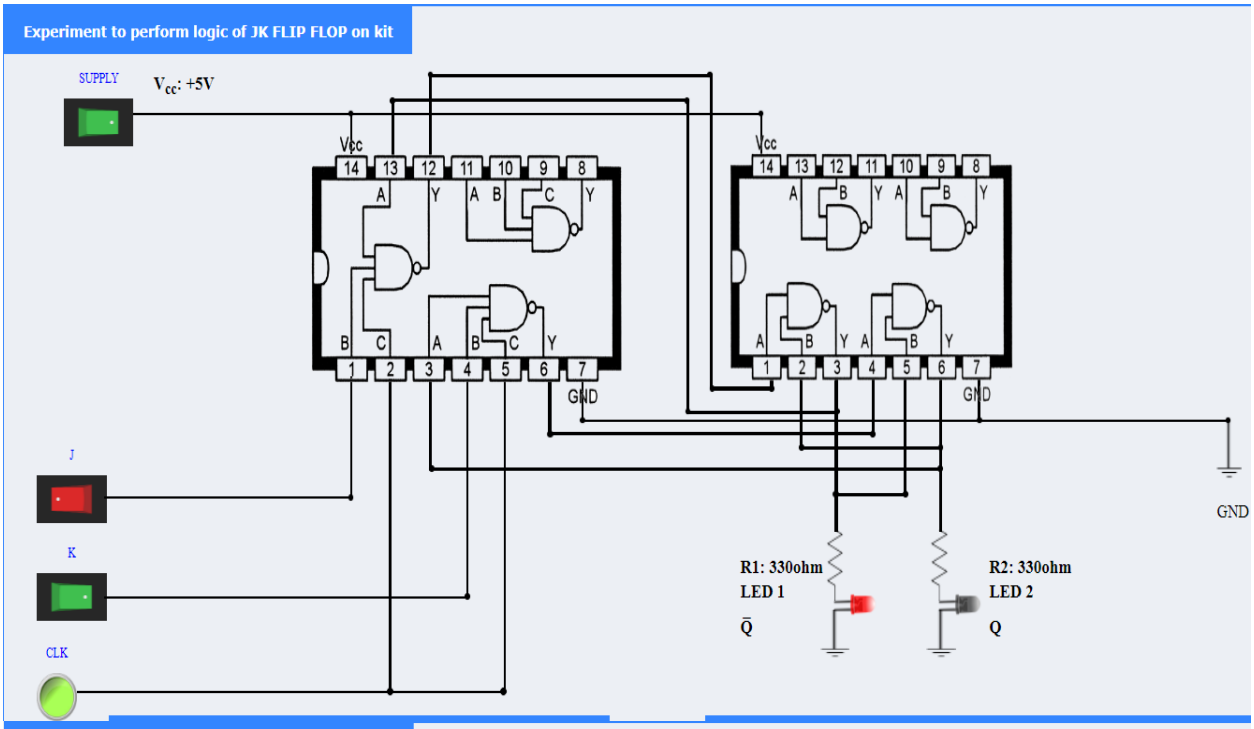


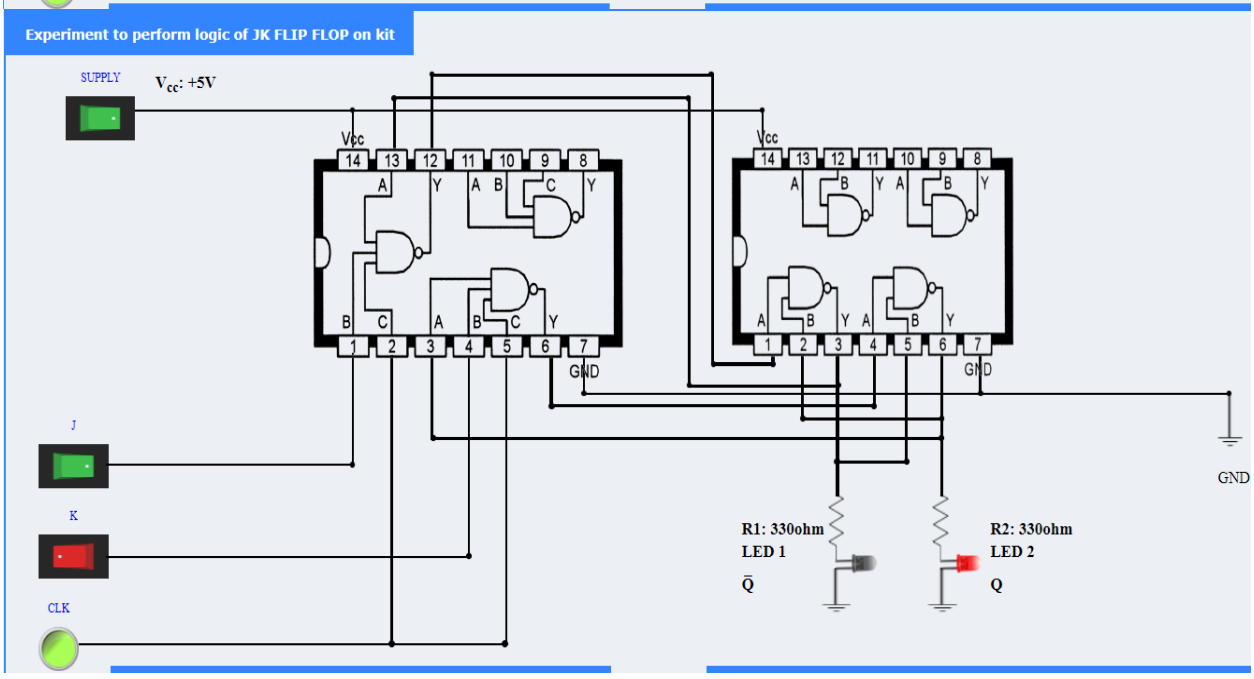

Experiment to perform SR Flip Flop on kit
POWER
S
R
Clock
Vcc
13
12
11
10
9
8
7400(NAND)
1
2
3
4
5
6
GND
GND
R1: 330 ohm
R2: 330 ohm
Q
Q̄
GND


Experiment to perform SR Flip Flop on kit
POWER
S
R
Clock
Vcc
13
12
11
10
9
8
7400(NAND)
1
2
3
4
5
6
GND
GND
R1: 330 ohm
R2: 330 ohm
Q
Q̄
GND

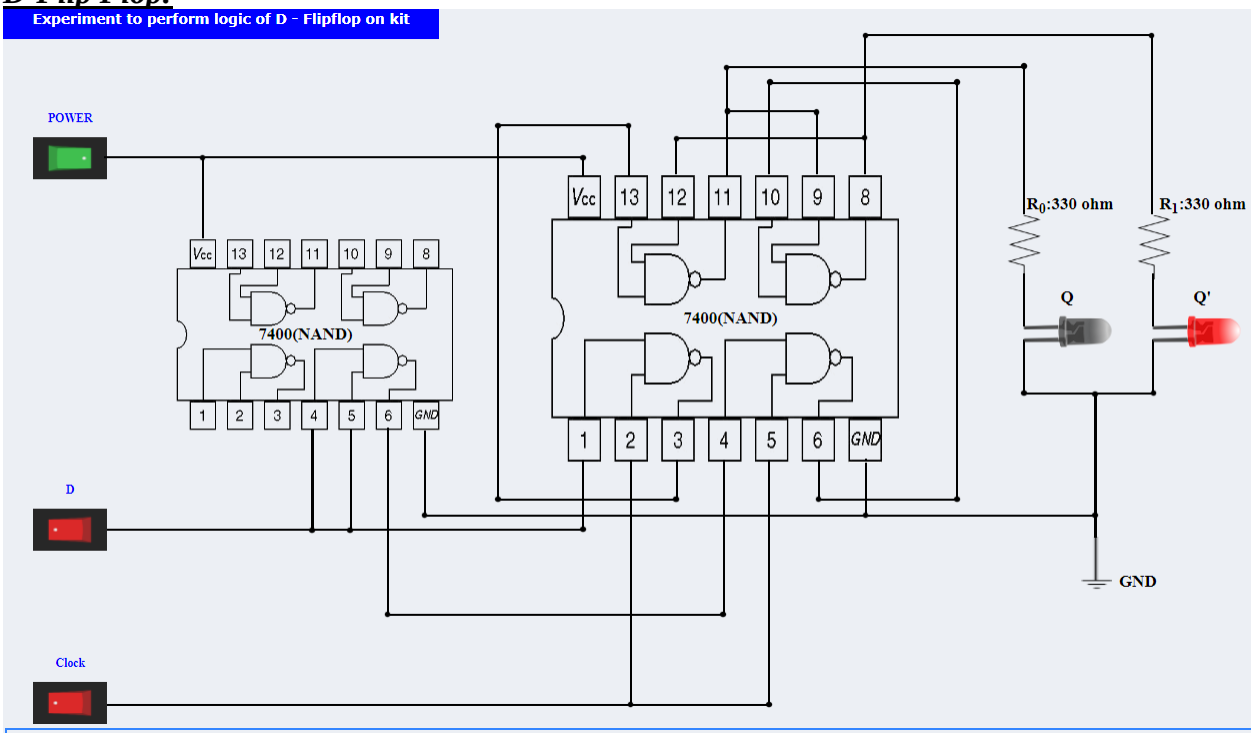
JK flip flop:

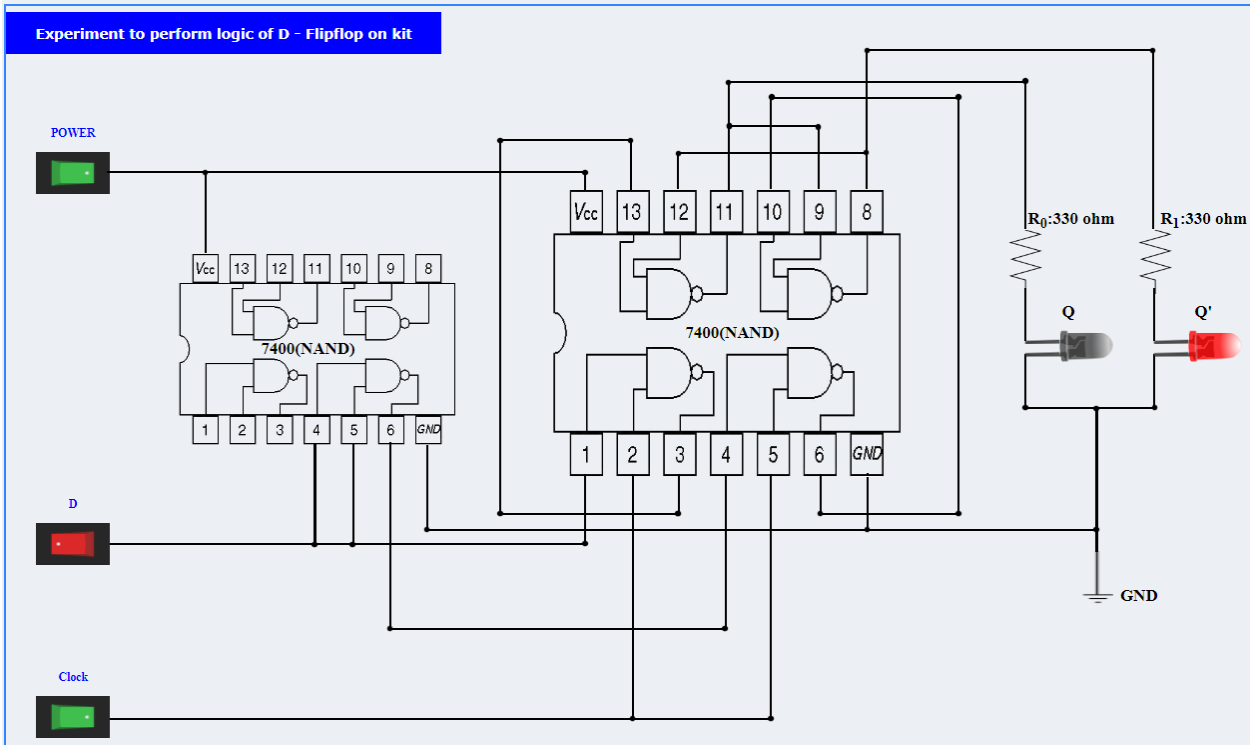

Experiment to perform logic of JK FLIP FLOP on kit
SUPPLY
Vcc: +5V
Vcc
GND
J
K
CLK
R1: 330ohm
LED 1
Q̄
R2: 330ohm
LED 2
Q
Experiment to perform logic of JK FLIP FLOP on kit
SUPPLY
Vcc: +5V
GND
J
K
CLK
R1: 330ohm
LED 1
Q̄
R2: 330ohm
LED 2
Q

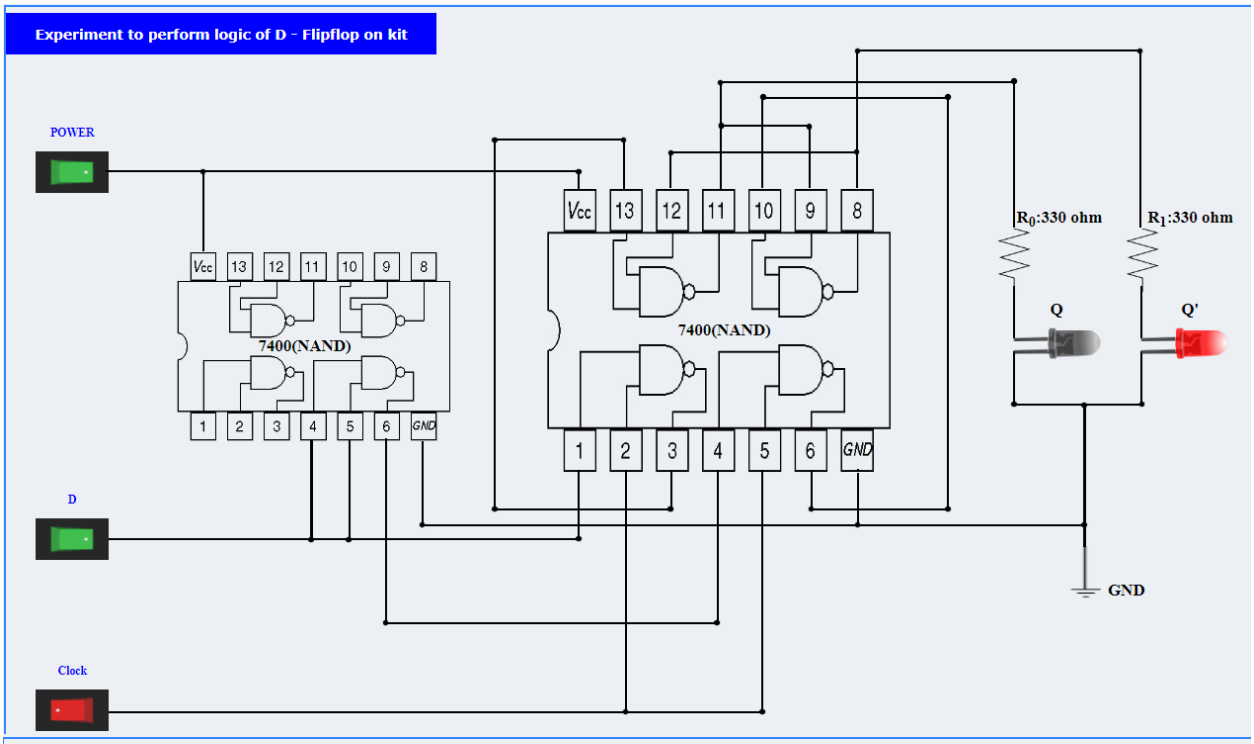

Experiment to perform logic of JK FLIP FLOP on kit
SUPPLY
Vcc: +5V
Vcc
GND
J
K
CLK
R1: 330ohm
LED 1
Q̄
R2: 330ohm
LED 2
Q

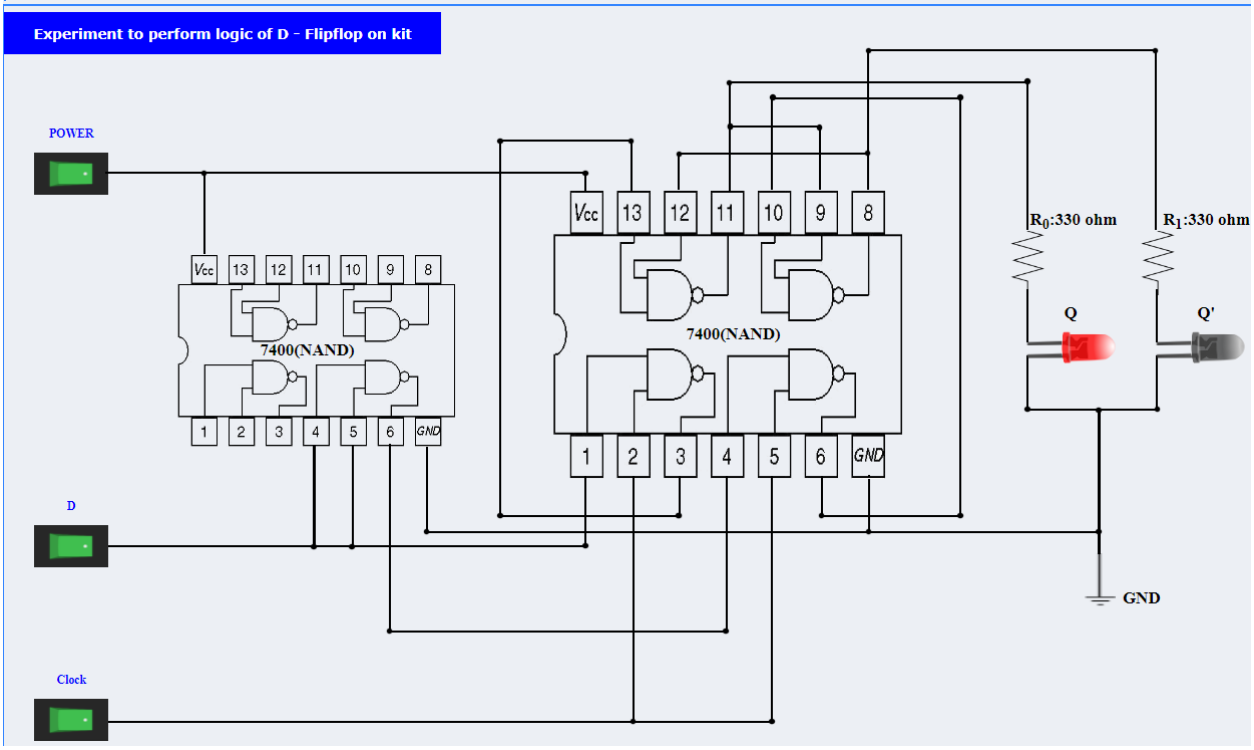

Experiment to perform logic of JK FLIP FLOP on kit
SUPPLY
Vcc: +5V
Vcc
GND
J
K
CLK
R1: 330ohm
LED 1
Q̄
R2: 330ohm
LED 2
Q

D-Flip Flop:


Experiment to perform logic of D - Flipflop on kit
POWER
D
Clock
Vcc 13 12 11 10 9 8
7400(NAND)
1 2 3 4 5 6 GND
R0:330 ohm
R1:330 ohm
Q
Q'
GND


Experiment to perform logic of D - Flipflop on kit
POWER
D
Clock
Vcc 13 12 11 10 9 8
7400(NAND)
1 2 3 4 5 6 GND
R0:330 ohm
R1:330 ohm
Q
Q'
GND





Result:

The respective truth tables of RS, JK, T and D flip-flops using NAND and NOR gates are verified.

Note: **The whole documentation is to be converted to pdf/word format before uploading it on the Moodle. Only the pdf/word format will be acceptable. The Submission has to be done on time. After the deadline no submission of the particular experiment will be acceptable.**