D.Y. PATIL INTERNATIONAL UNIVERSITY

B.TECH CSE FY SEM-2

A.Y. 2022-2023

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SUBJECT: DIGITAL LOGIC AND DESIGN

BATCH: A1

EXPERIMENT-7 (A)

Aim:

Design and verify the 4-Bit Serial In - Parallel Out Shift Register**.**

Requirements:

- Battery
- Switch
- Clock Pulse
- Led

Theory:

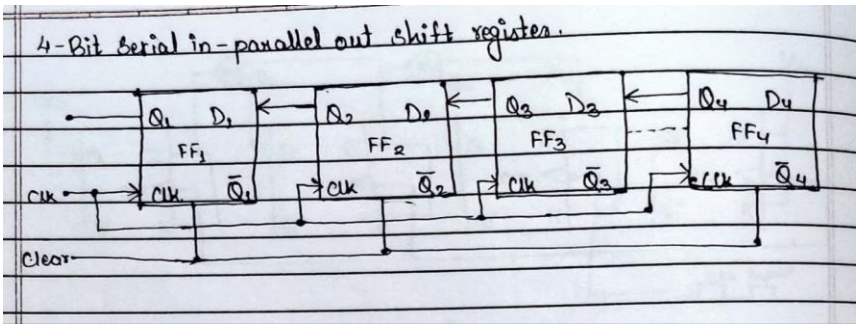
There are four types of shift registers based on applying inputs and accessing of outputs.

- Serial In – Serial Out Shift Register
- Serial In – Parallel Out Shift Register
- Parallel In – Serial Out Shift Register
- Parallel In – Parallel Out Shift Register

A serial-in, parallel- out shift register is similar to the serial-in, serial-out shift register in that it shifts data into internal storage elements and shifts data out at the serial out, pin. It is different in that it makes all the internal stages available as outputs.

The circuit having four D flip-flops contains a clear and clock signal to reset these four flip flops. The output from each flip-Flop is connected to the D input of the flip-flop at its right.

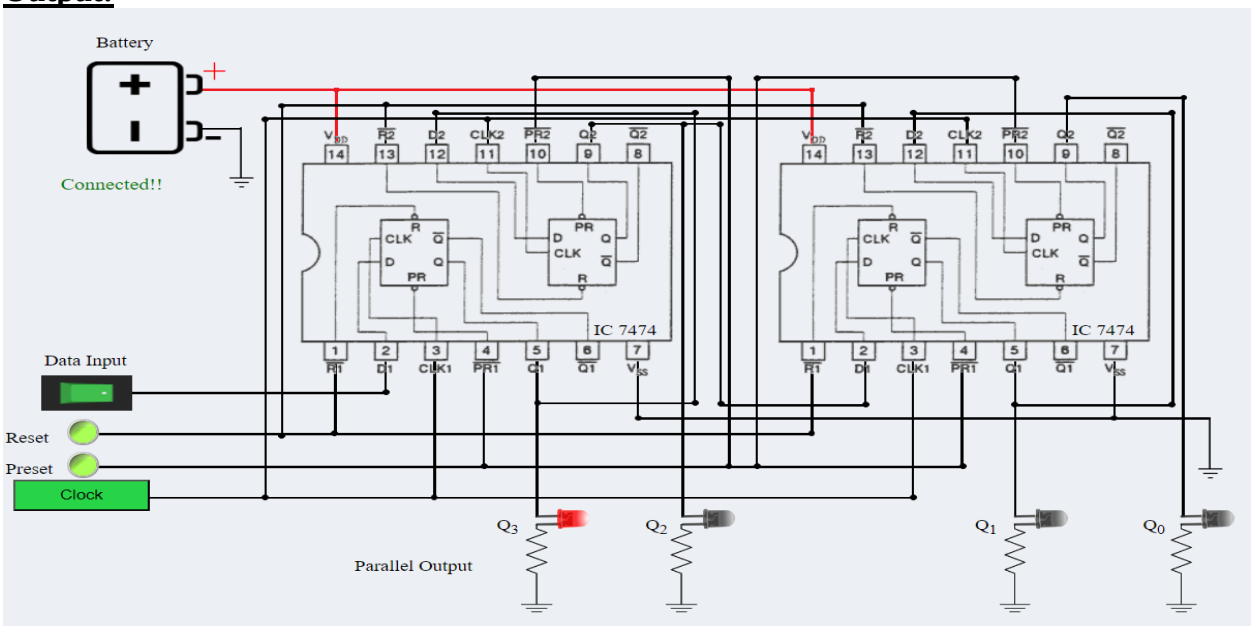
Circuit Diagram:

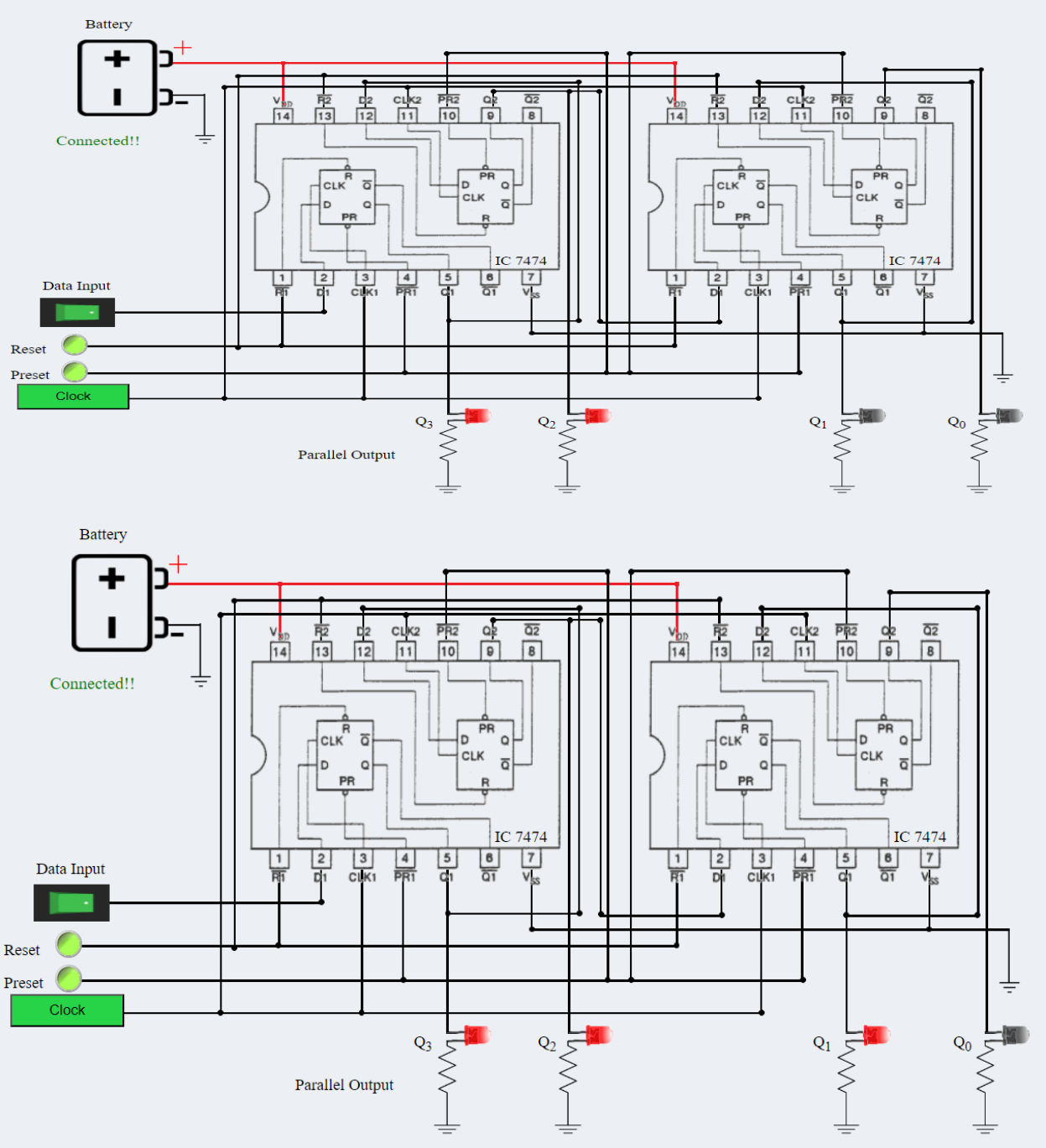


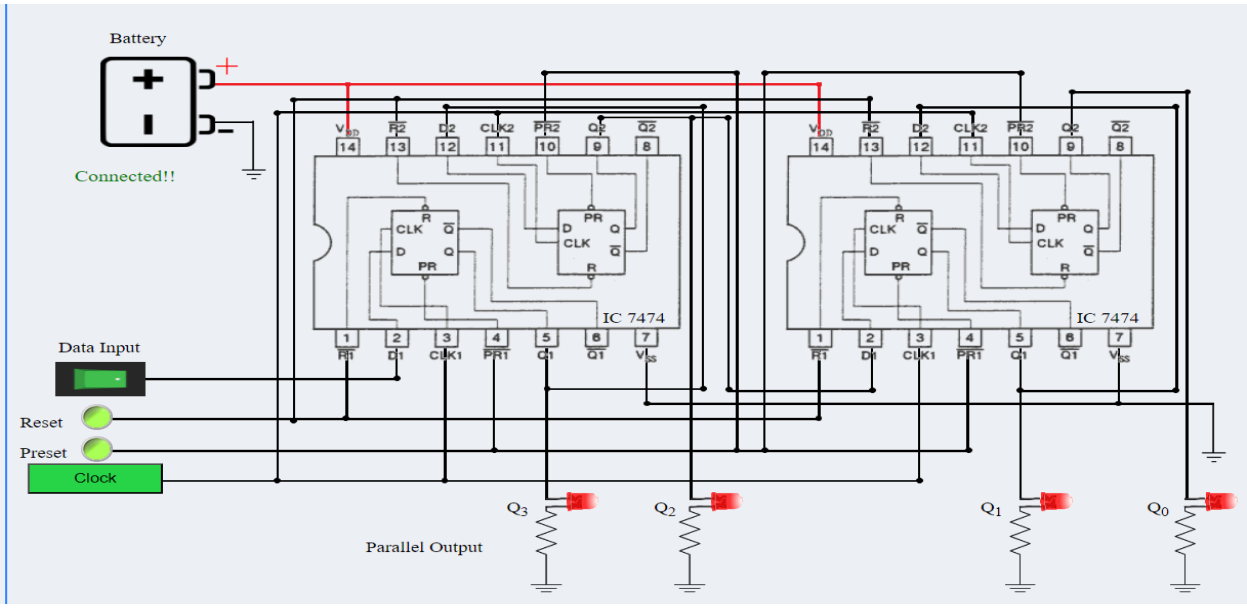
Observation Table:

Sr. No.	Clock	Data Input	Q3	Q2	Q1	Q0
1.	0	0	0	0	0	0
2.	1	1	1	0	0	0
3.	2	1	1	1	0	0
4.	3	1	1	1	1	0

Output:




Battery
Connected!!
IC 7474
IC 7474
Data Input
Reset
Preset
Clock
Q3
Q2
Q1
Q0
Parallel Output
Battery
Connected!!
IC 7474
IC 7474
Data Input
Reset
Preset
Clock
Q3
Q2
Q1
Q0
Parallel Output



Result:

The 4-Bit Serial In - Parallel Out Shift Register is designed and verified.

EXPERIMENT-7 (B)

Aim:

Design and verify the 4- Bit Synchronous and Asynchronous Counters using JK Flip Flop.

Requirements:

- Switch
- Synchronous parallel counter using J-K Flip flop
- Asynchronous parallel counter using J-K Flip flop

Theory:

Counters are broadly classified into:

1) Asynchronous counter
2) Synchronous counter

- **Asynchronous Counter**

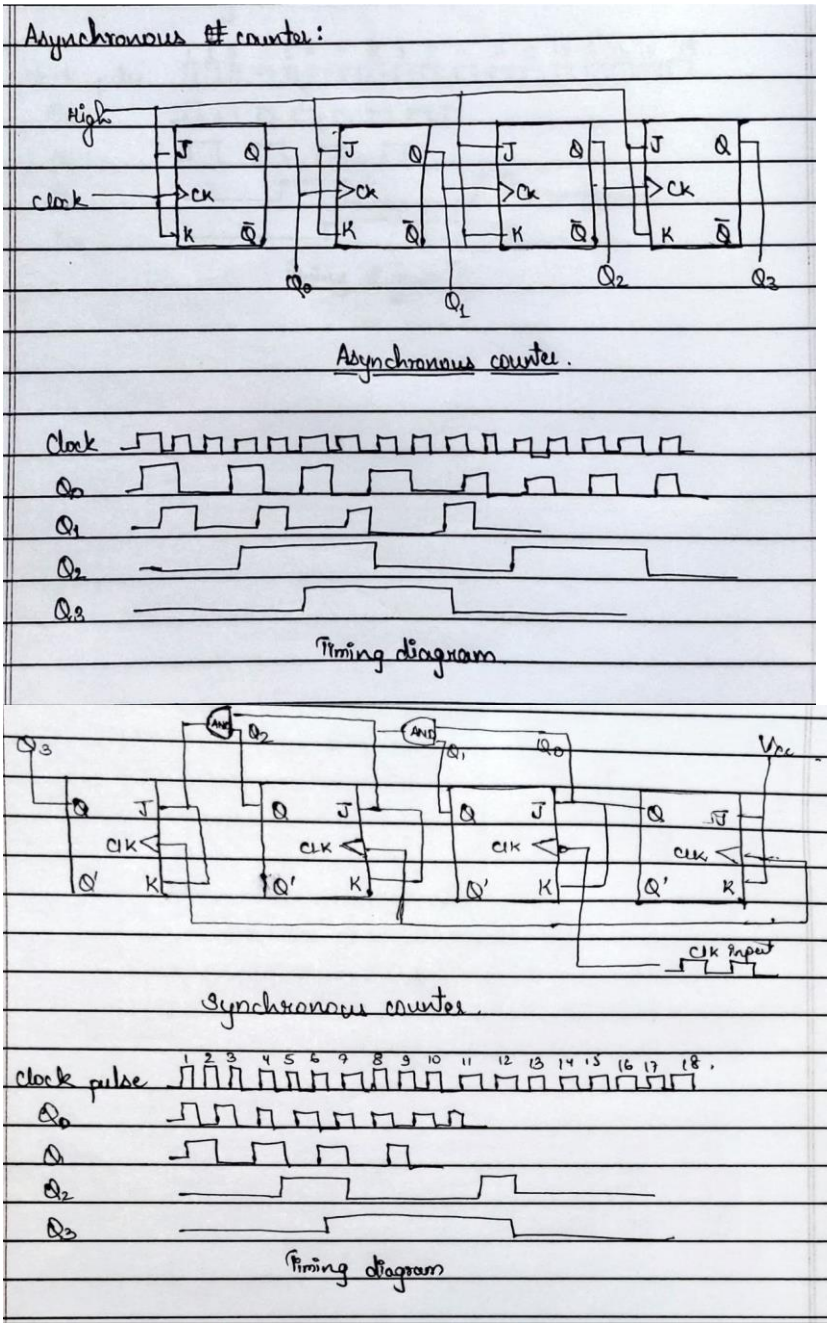
  In asynchronous counter we don't use universal clock, only first flip flop is driven by main clock and the clock input of rest of the following counters is driven by output of previous flip flops. We can understand it by following diagram-

It is evident from timing diagram that Q0 is changing as soon as the rising edge of clock pulse is encountered, Q1 is changing when rising edge of Q0 is encountered(because Q0 is like clock pulse for second flip flop) and so on. In this way ripples are generated through Q0,Q1,Q2,Q3 hence it is also called RIPPLE counter.

- **Synchronous Counter:**

  Unlike the asynchronous counter, synchronous counter has one global clock which drives each flip flop so output changes in parallel. The one advantage of synchronous counter over asynchronous counter is, it can operate on higher frequency than asynchronous counter as it does not have cumulative delay because of same clock is given to each flip flop. From circuit diagram we see that Q0 bit gives response to each falling edge of clock while Q1 is dependent on Q0, Q2 is dependent on Q1 and Q0 , Q3 is dependent on Q2,Q1 and Q0.

Circuit Diagram:



Observation Table:

I. Asynchronous Counter

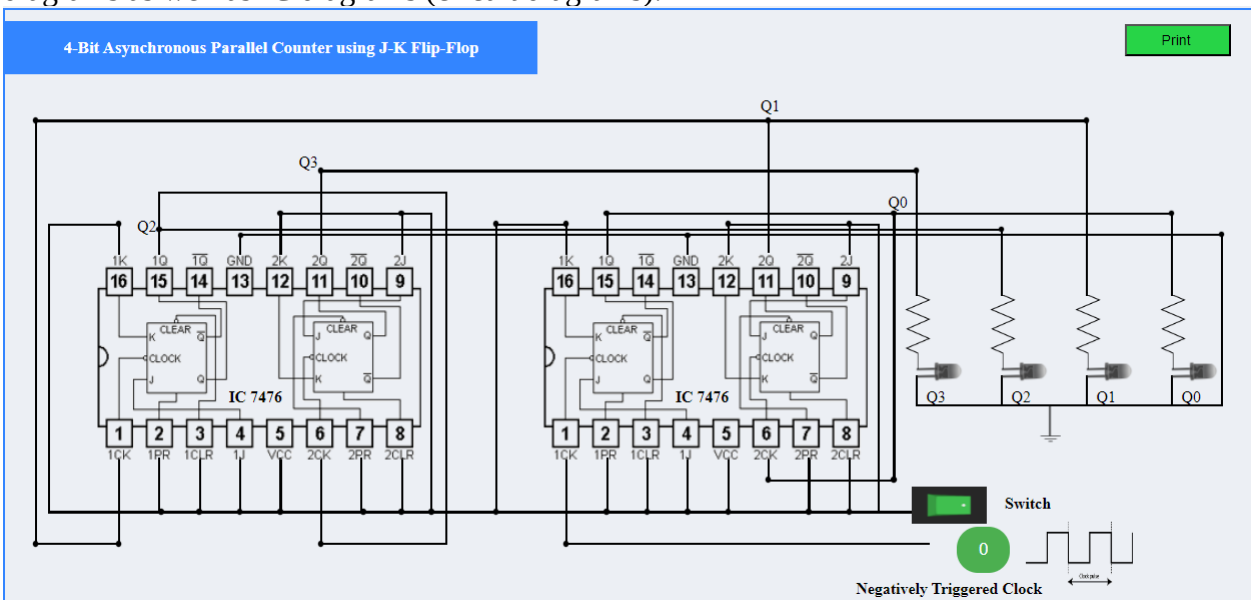
Sr. No.	Clock	Q3	Q2	Q1	Q0
1.	0	X	X	X	X
2.	1	0	0	0	0

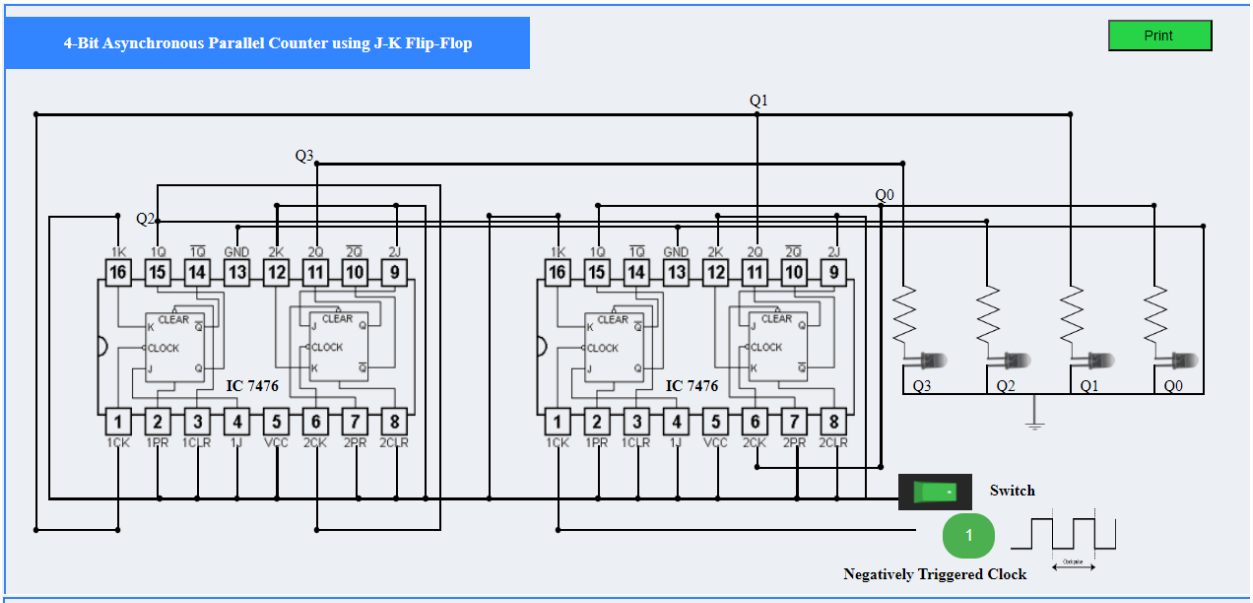
3.	2	0	0	0	1
4.	3	0	0	1	0

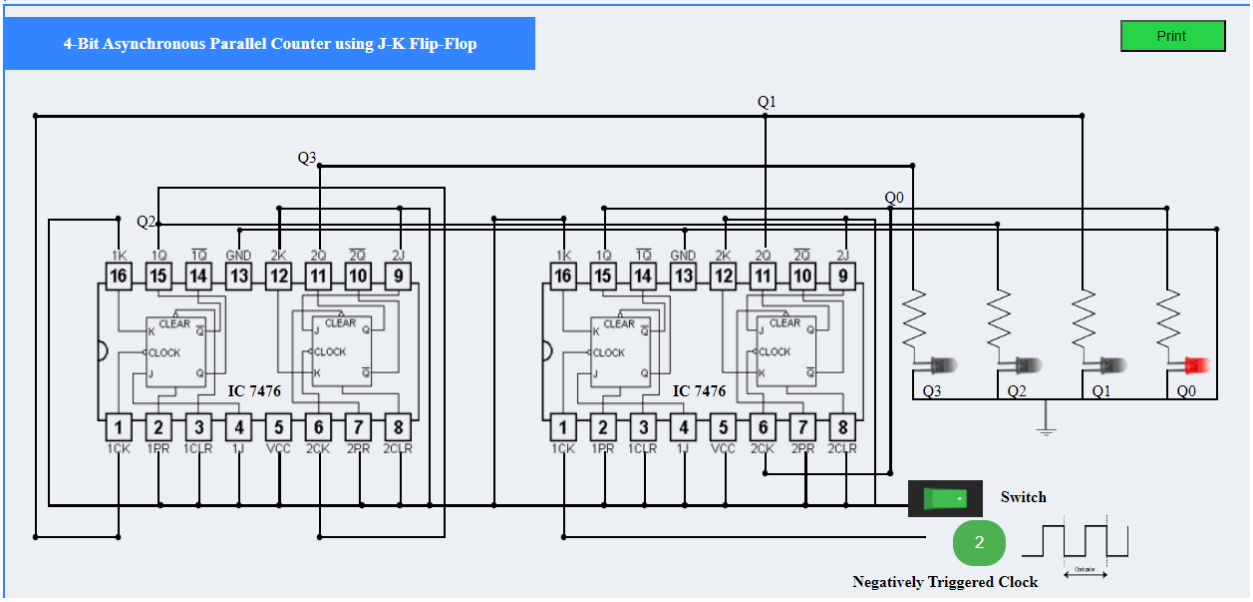
II. Synchronous Counter

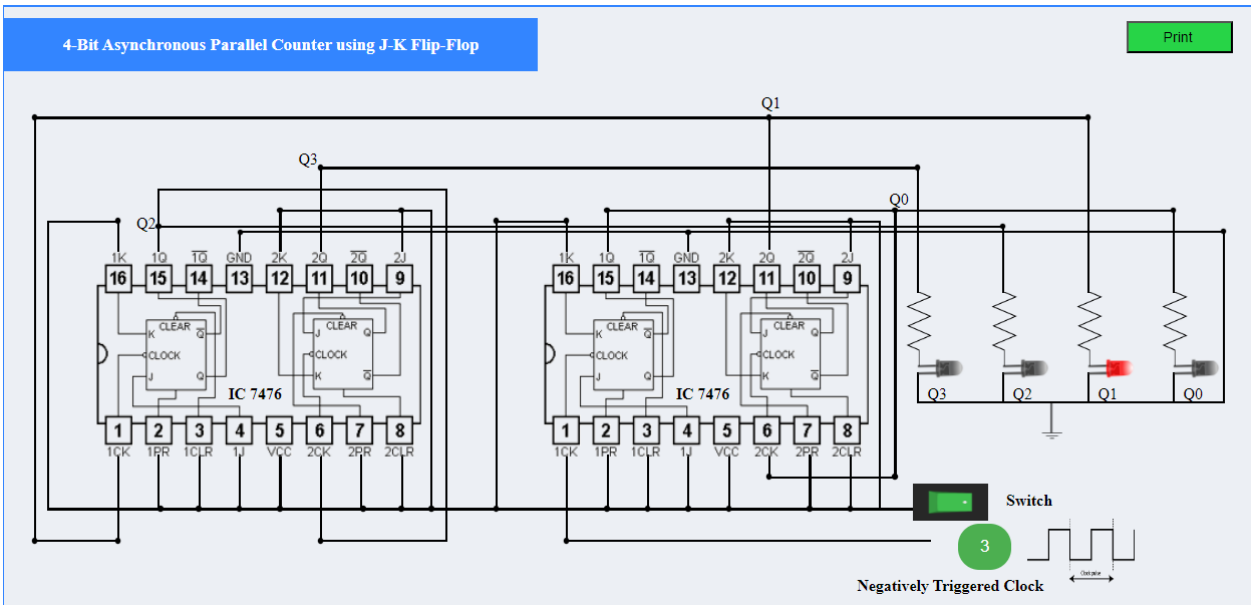
Sr. No.	Clock	Q3	Q2	Q1	Q0
1.	1	0	0	0	0
2.	2	0	0	0	1
3.	3	0	0	1	0
4.	4	0	0	1	1

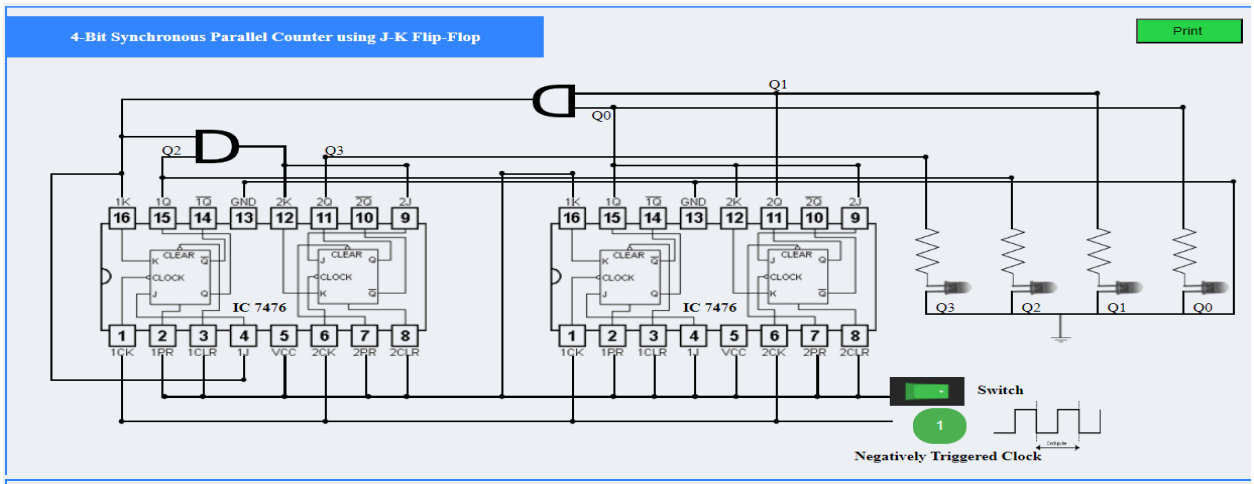
Output: Attach the screenshots of the simulation of both the counters with their respective timing diagrams as well as IC diagrams (circuit diagrams).

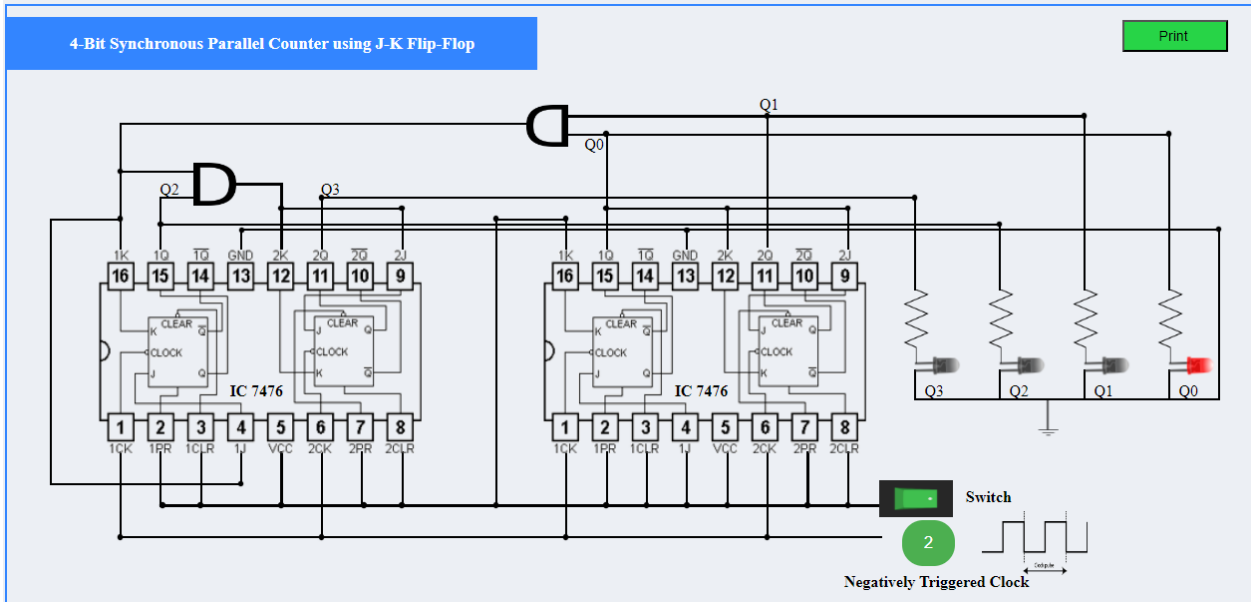


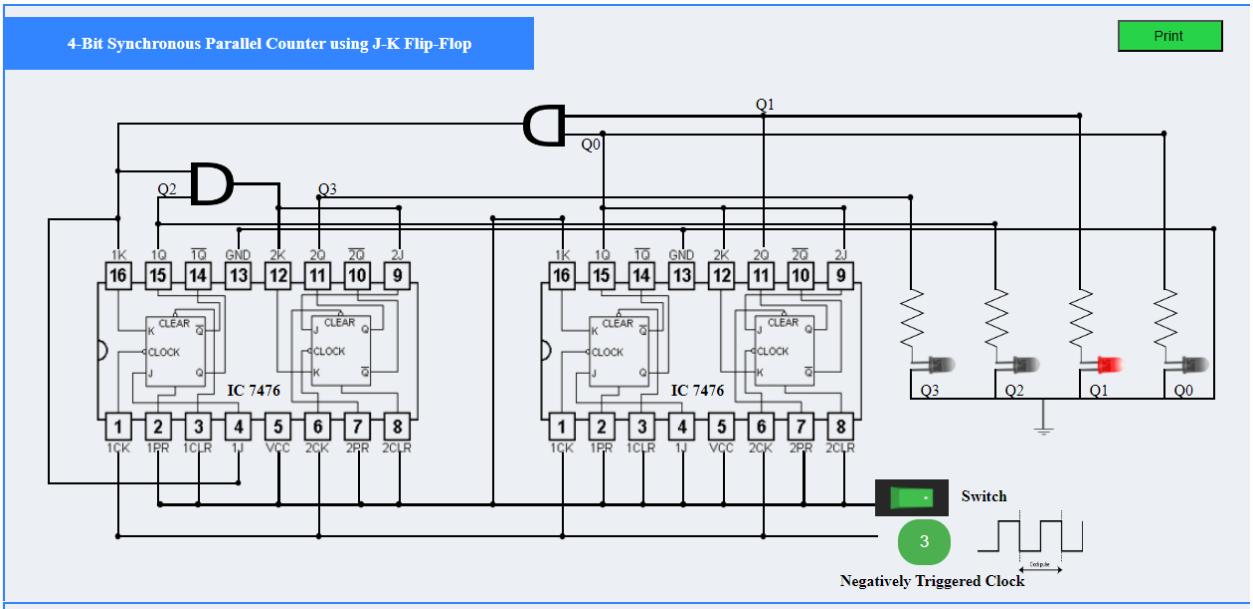

4-Bit Asynchronous Parallel Counter using J-K Flip-Flop
Print
Q1
Q3
Q0
Q2
IC 7476
IC 7476
Q3
Q2
Q1
Q0
Switch
1
Negatively Triggered Clock

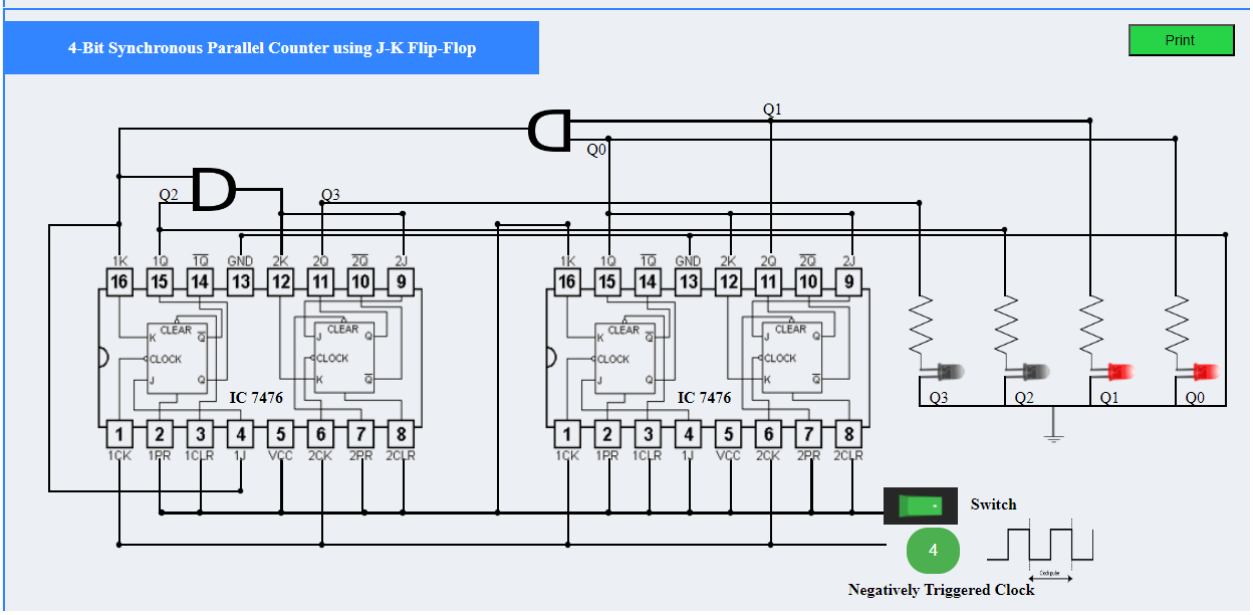

4-Bit Asynchronous Parallel Counter using J-K Flip-Flop
Print
Q1
Q3
Q0
Q2
IC 7476
IC 7476
Q3
Q2
Q1
Q0
Switch
2
Negatively Triggered Clock


4-Bit Asynchronous Parallel Counter using J-K Flip-Flop
Print
Q1
Q3
Q0
Q2
IC 7476
IC 7476
Q3
Q2
Q1
Q0
Switch
3
Negatively Triggered Clock


4-Bit Synchronous Parallel Counter using J-K Flip-Flop
Print
Q1
Q0
Q2
Q3
IC 7476
IC 7476
Q3
Q2
Q1
Q0
Switch
1
Negatively Triggered Clock


4-Bit Synchronous Parallel Counter using J-K Flip-Flop
Print
Q1
Q0
Q2
Q3
IC 7476
IC 7476
Q3
Q2
Q1
Q0
Switch
2
Negatively Triggered Clock





Result:

The 4- Bit Synchronous and Asynchronous Counters using JK Flip Flop are designed and verified.