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EXPERIMENT-2 (A)

Aim:

To design and implement Half & Full adders using logic gates for performing binary addition.

Requirements:

1) Virtual Lab (Website)

2) MyDaq, Breadboard, Logic Gates or ICs and Wires (Hardware)

3) NI-ELVIS Mx (Software)

Theory:

Half Adder: -

A half adder is a digital circuit that takes in two binary inputs, usually denoted as A and B, and produces two outputs: the sum (S) and the carry (C). The sum is the binary addition of A and B, while the carry is the bit that needs to be added to the next digit position. The truth table for a half adder is as follows:

The equations for the sum and carry outputs in a half adder are:

$S = A \oplus B$

$C = A\ B$

Full Adder: -

A full adder, on the other hand, takes in three binary inputs: A, B, and the carry-in (Ci), and produces two outputs: the sum (S) and the carry-out (Co). The sum output is the binary addition of A, B, and Ci, while the carry-out is the bit that needs to be added to the next digit position. The truth table for a full adder is as follows:

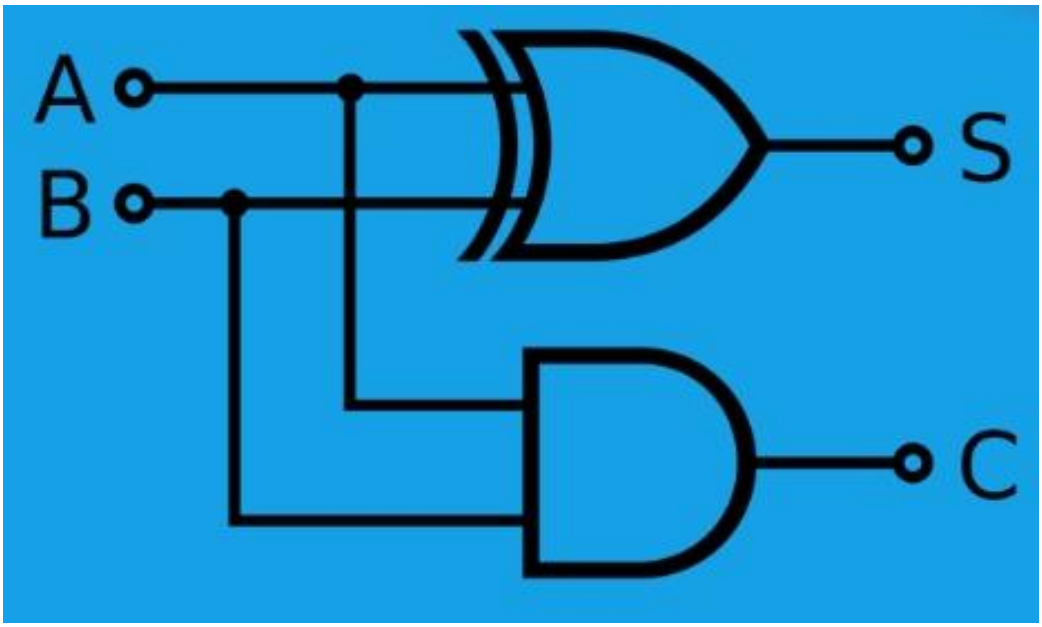
The equations for the sum and carry outputs in a full adder are:

$S = A \oplus B \oplus Ci$

$Co = (A\ B) + (A\ C) + (B\ C)$

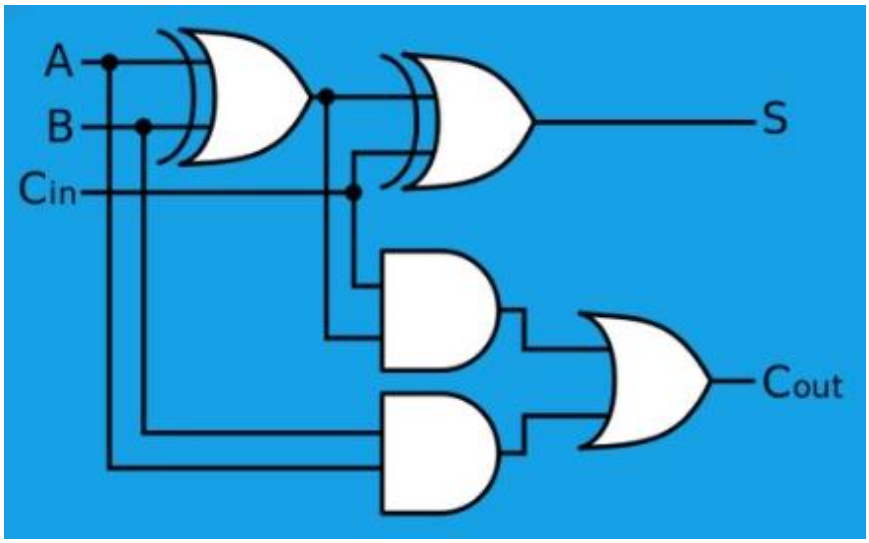
Circuit Diagram:

Half Adder Circuit Diagram:



In the above circuit diagram, the two input variables are A and B, and the two output variables are S (sum) and C (carry).

Full Adder Circuit Diagram:



In the above circuit diagram, the three input variables are A, B, and Ci (carry-in), and the two output variables are S (sum) and Co(carry-out).

Observation Table:

I. **Half Adder**

Input Variables- A, B
Output Variables- S, C
Where S represents Sum,
C represents Carry.

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Output: Attach the screenshots of the simulation of half adder done on MyDAQ.

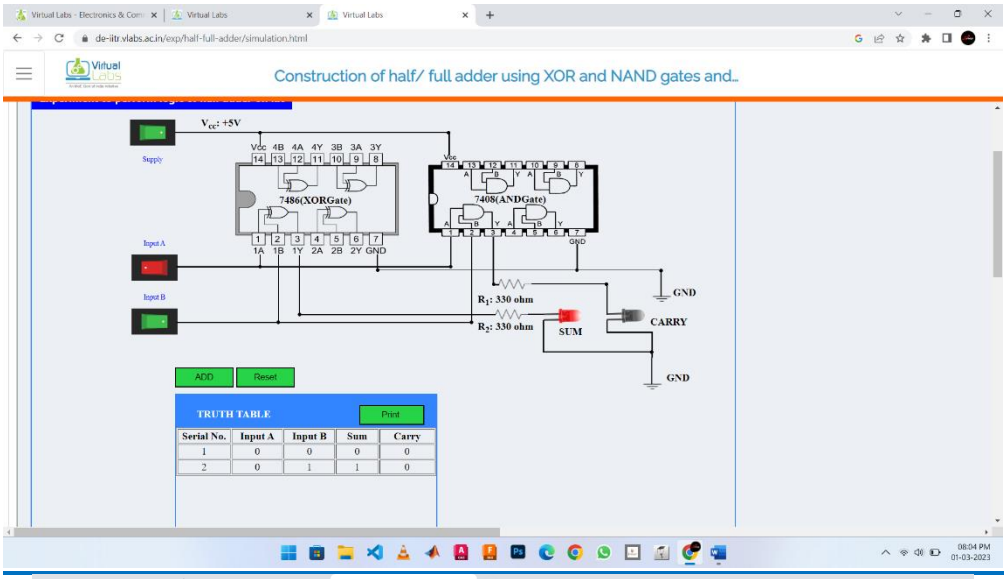
II. Full Adder

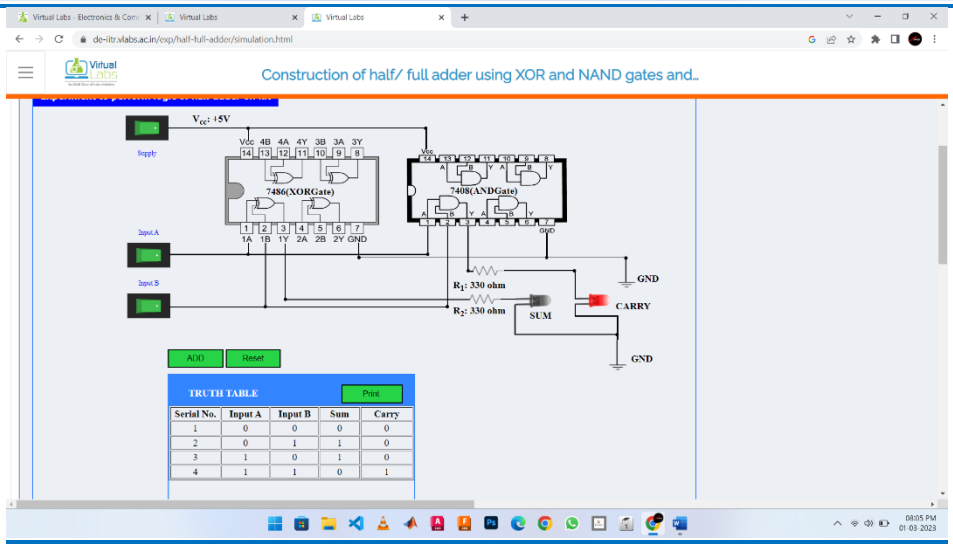
Input Variables- A, B, Ci
Output Variables- S, Co
where S represents Sum and Co represents Carry out

A	B	Ci	S	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Output:

Half Adder: -


de-iitr.vlabs.ac.in/exp/half-full-adder/simulation.html
Construction of half/ full adder using XOR and NAND gates and..
Vcc: +5V
Supply
7486(XORGate)
7408(ANDGate)
Input A
Input B
R1: 330 ohm
R2: 330 ohm
SUM
CARRY
GND
ADD
Reset
TRUTH TABLE
Print
Serial No. | Input A | Input B | Sum | Carry
1 | 0 | 0 | 0 | 0
2 | 0 | 1 | 1 | 0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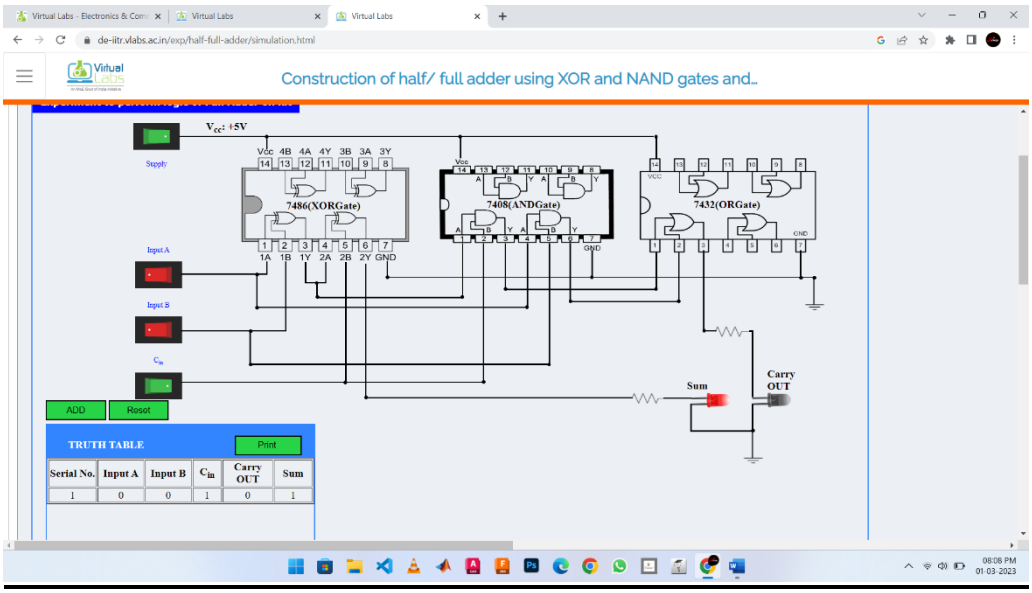
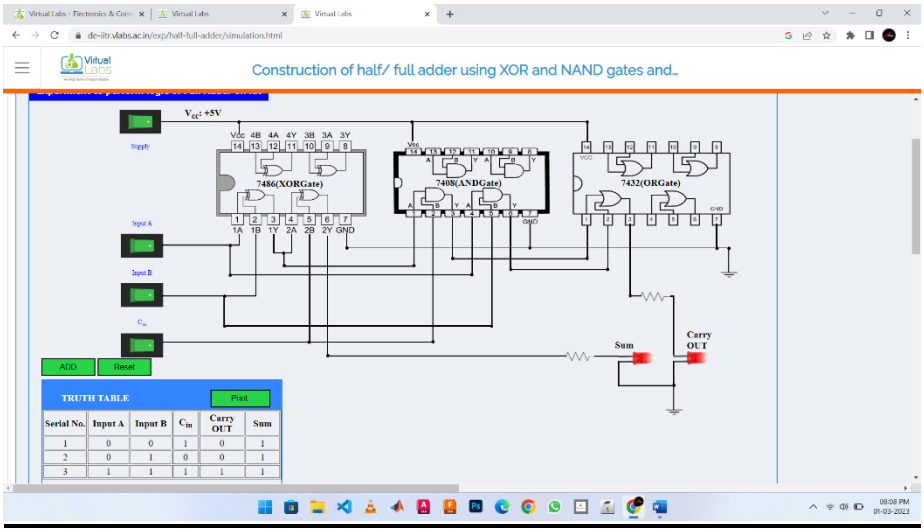
SUM
CARRY
GND
ADD
Reset
TRUTH TABLE
Print
Serial No. | Input A | Input B | Sum | Carry
1 | 0 | 0 | 0 | 0
2 | 0 | 1 | 1 | 0
3 | 1 | 0 | 1 | 0
4 | 1 | 1 | 0 | 1

Full Adder: -





Result:

Designing and implementation of Half & Full adders using logic gates for performing binary addition is done.

XPERIMENT-2 (B)

Aim:

To design and implement Half & Full subtractor using logic gates to perform binary subtraction.

Requirements:

1) Virtual Lab (Website)

2) MyDaq, Breadboard, Logic Gates or ICs and Wires (Hardware)

3) NI-ELVISmx (Software)

Theory:

Half Subtractor: -

A half subtractor is a combinational circuit that subtracts two bits and produces the difference and borrow as outputs. The circuit takes two inputs A and B, and produces two outputs, the difference D and borrow-out (Bo).

The equations for difference (D) and borrow (Bo) are:

$D = A \oplus B$

$Bo = A'B$

Full Subtractor: -

A full subtractor is a combinational circuit that subtracts three binary bits, the minuend, subtrahend, and borrow-in, and produces the difference and borrow-out as outputs. The circuit takes three inputs A, B, and (Bi) and produces two outputs, the difference D and borrow-out (Bo).

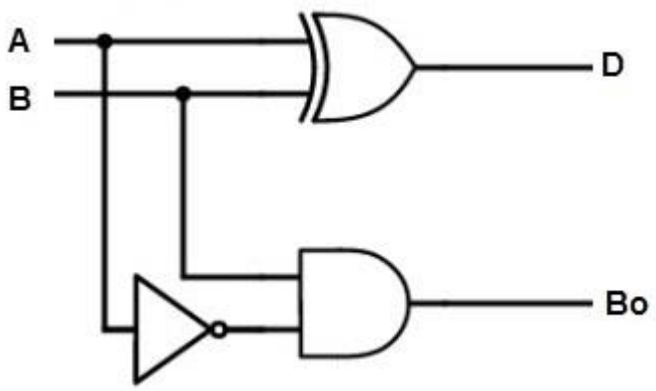
The equations for difference (D) and borrow (Bo) are:

$D = A \oplus B \oplus Bi$

$Bo = (A'B + Bi' A)$

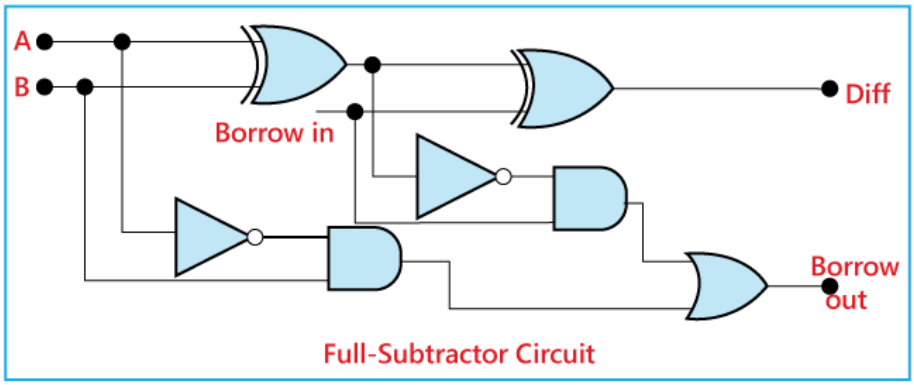
Circuit Diagram:

Half Subtractor Circuit Diagram:



In the above circuit diagram, the two input variables are A and B, and the two output variables are D (difference) and Co (carry).

Full Subtractor Circuit Diagram:



In the above circuit diagram, the three input variables are A, B, and Bi (borrow-in), and the two output variables are D (difference) and Bo(borrow-out).

Observation Table:

I. Half Subtractor

Input Variables- A, B
Output Variables- D, B_{out}
Where D represents Difference,
B_{out} represents Borrow.

A	B	S	C
0	0	0	0
0	1	1	1

1	0	1	0
1	1	0	0

Output: Attach the screenshots of the simulation of half subtractor done on MyDAQ.

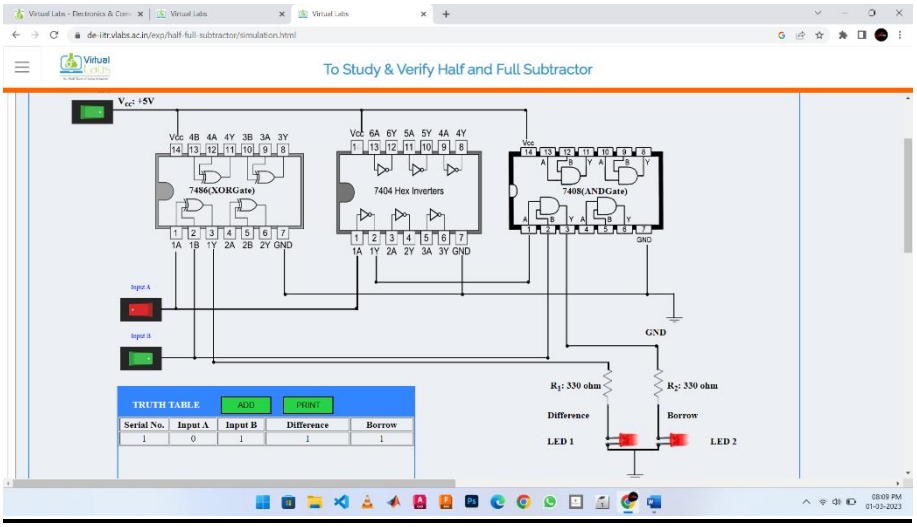
II. Full Subtractor

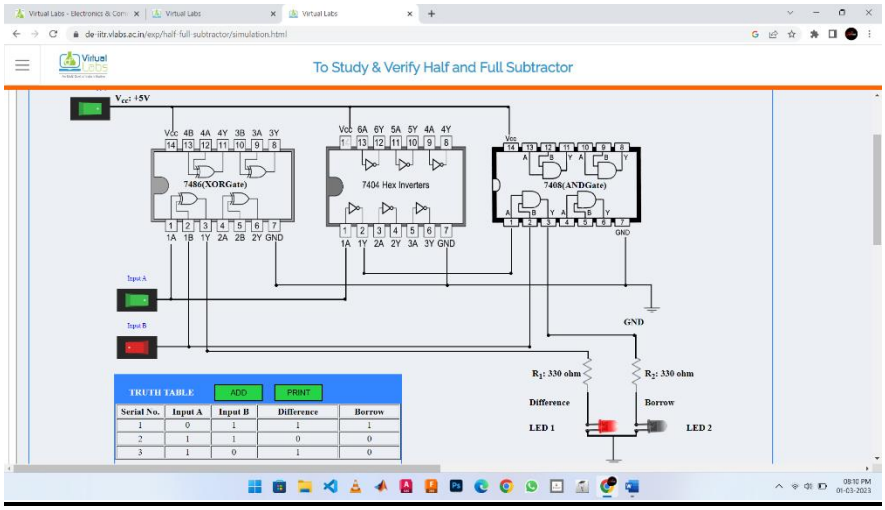
Input Variables- A, B, B_{in}
Output Variables- D, B_{out}
Where, D represents Difference,
B_{out} represents Borrow

A	B	Ci	S	Co
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

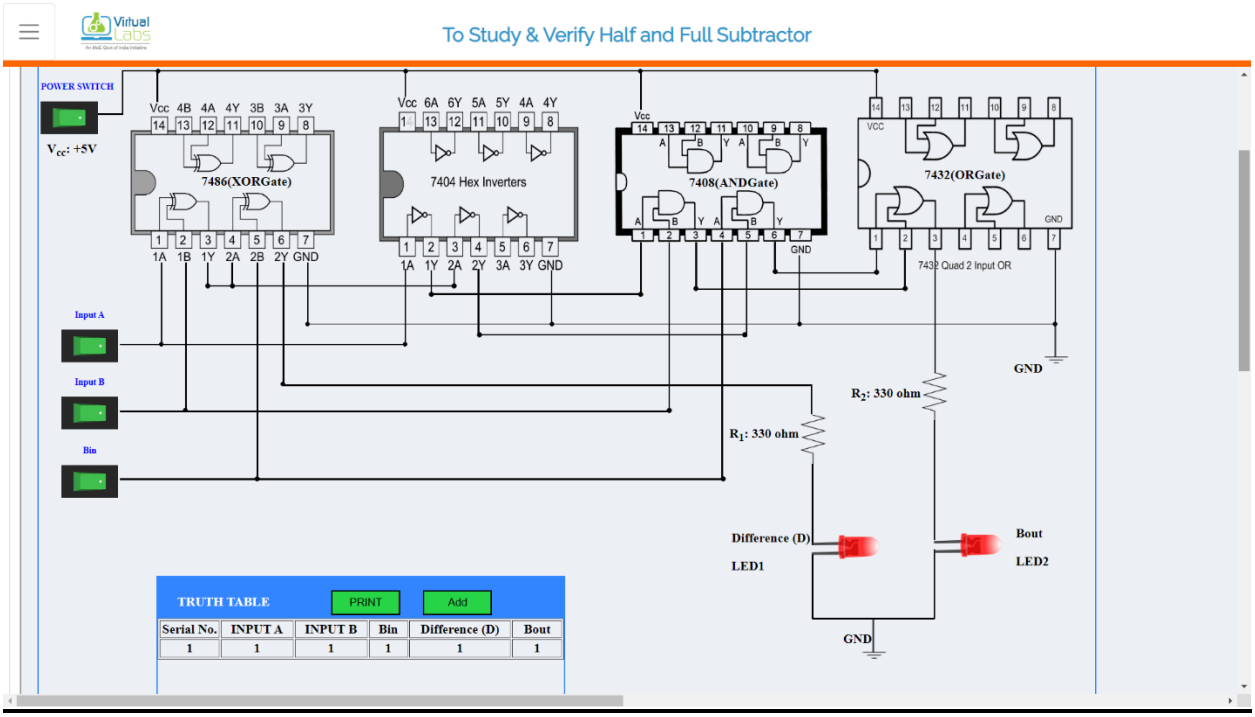
Output: -

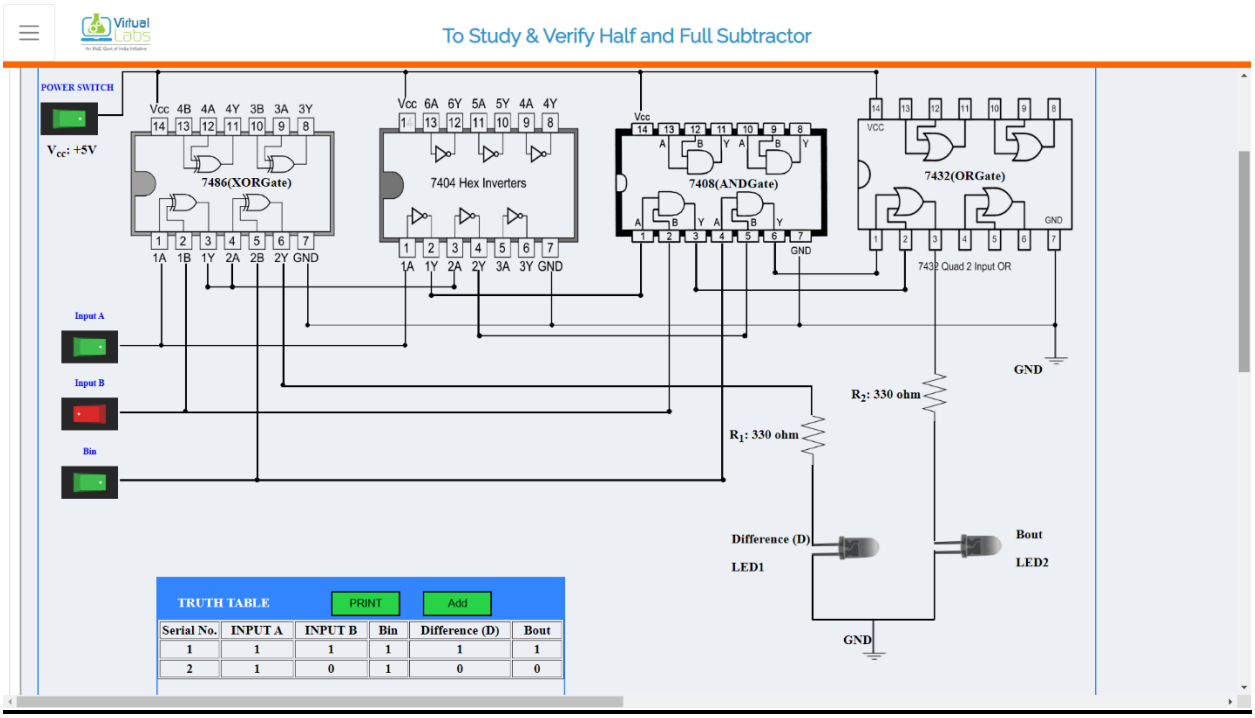
Half Subtractor: -





Full Subtractor: -





Result:

Designing and implementation of Half & Full subtractor using logic gates for performing binary subtraction is done.