

# Computer Architecture Assignment - 3

## Project Description:

Design a direct-mapped cache of variables cache and block sizes.

## Report:

I have tried my best to implement the cache. It seems everything is correct in my code but it is not. I am getting a hit ratio of 1. I tried debugging the code but I couldn't find out where I am going wrong.

```
PROBLEMS  OUTPUT  TERMINAL  DEBUG CONSOLE
harsha@harsha:~/Desktop/Cache$ python3 IMT2020085_cache.py
Enter the size of the cache in kilo bytes : 64
Enter the size of block in bytes : 4
miss ratio : 0.0
hit ratio : 1.0
harsha@harsha:~/Desktop/Cache$
```