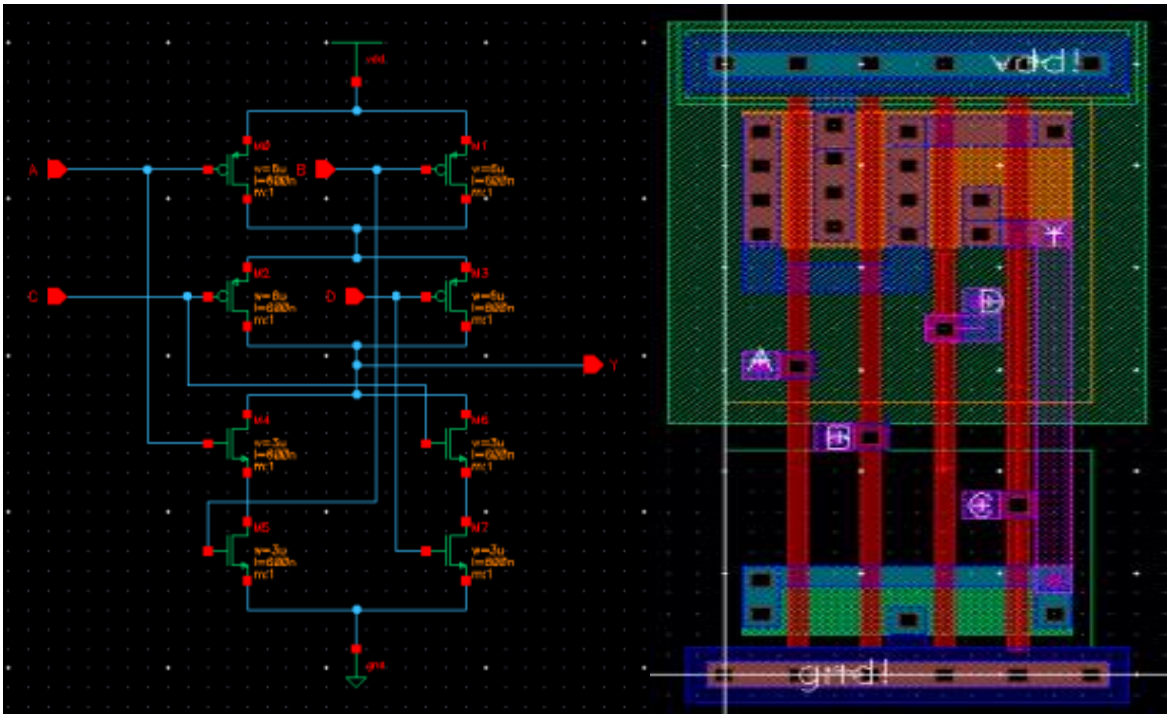
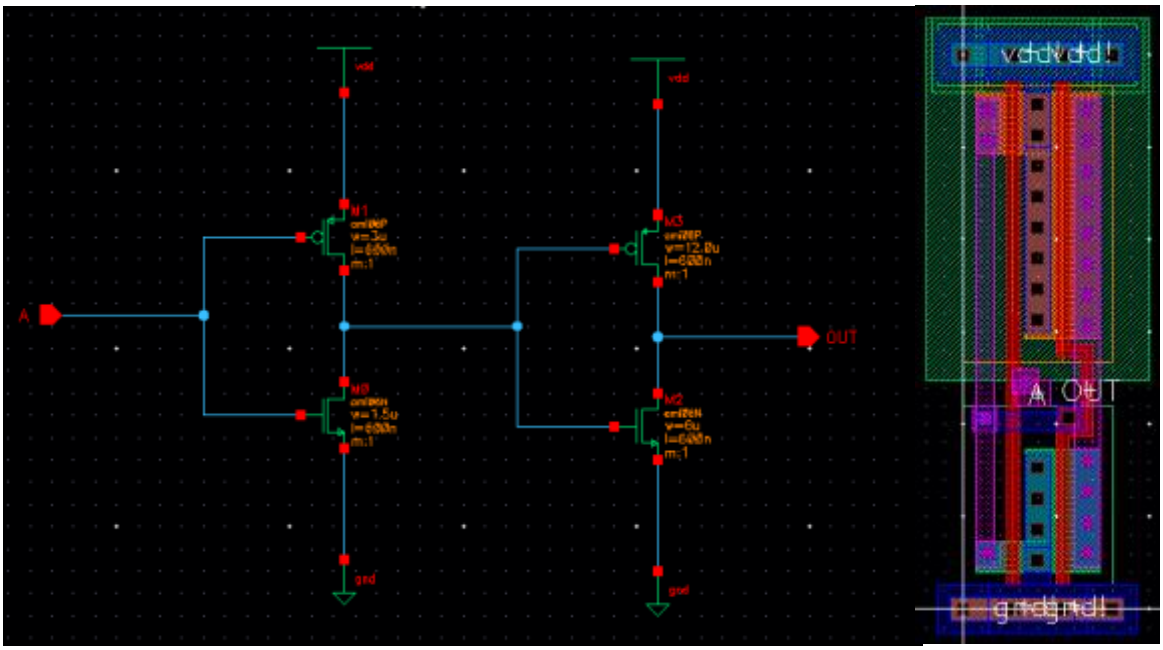
STANDARD CELL LIBRARY DESCRIPTION

- AOI4X1



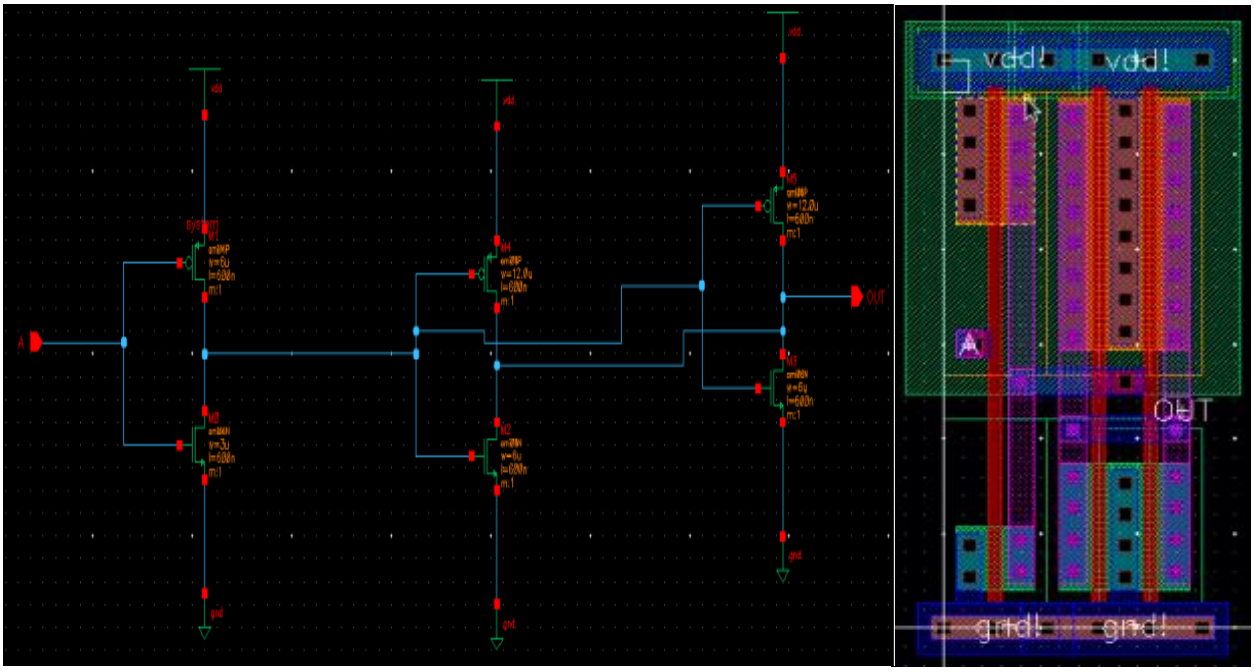
AOI4X1 refers to AND OR INVERT gate with four inputs A,B,C,D and an output Y(4X1).It implements the logical function Y=~((A&B)|(C&D)).The gate dimensions are 27x12 and an area of 324 sq.micron.

- BUFX4



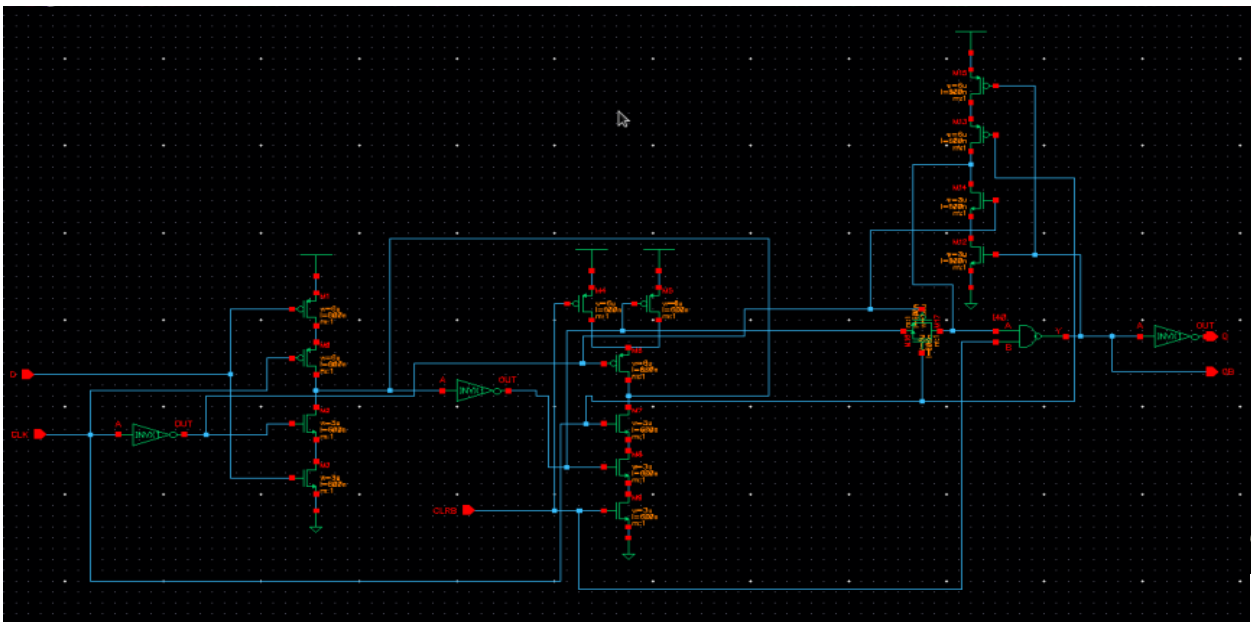
BUFX4 refers to a BUFFER with a drive strength of 4 with an input A and an output OUT. It implements the logical function OUT=~ (~A).The gate dimensions are 27x7.2 and an area of 194.4 sq.micron.

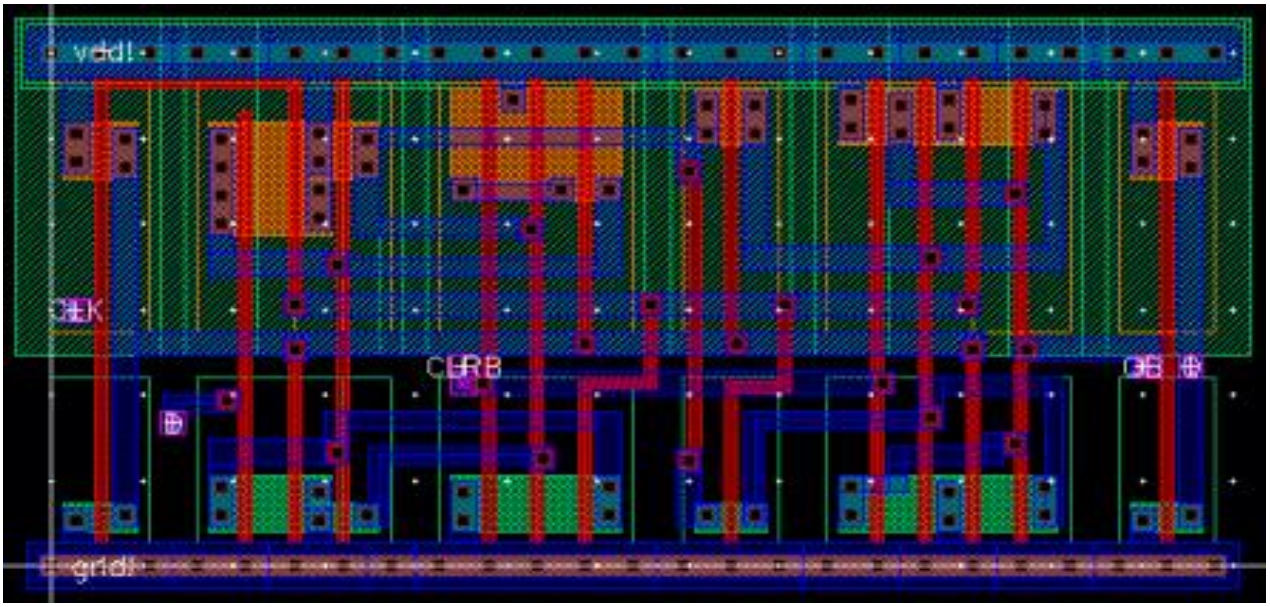
- BUFX8



BUFX8 refers to a BUFFER with a drive strength of 8 and it has a single input A and one output OUT. It implements the logical function OUT=~ (~A).The buffer dimensions are 27x12 and an area of 324 sq.micron.

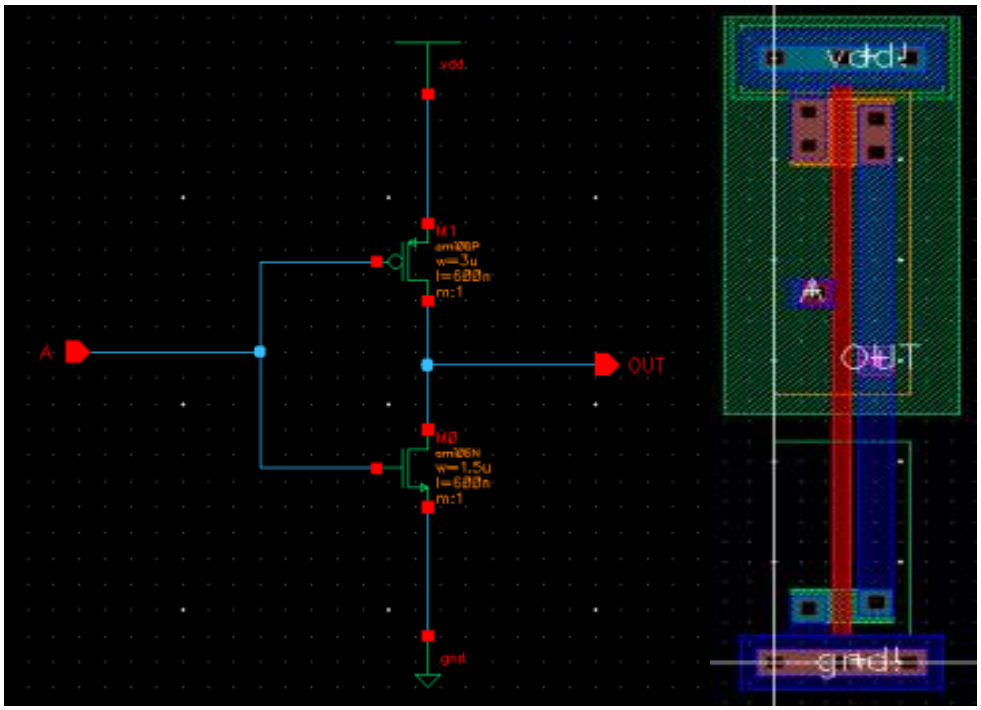
- DFF





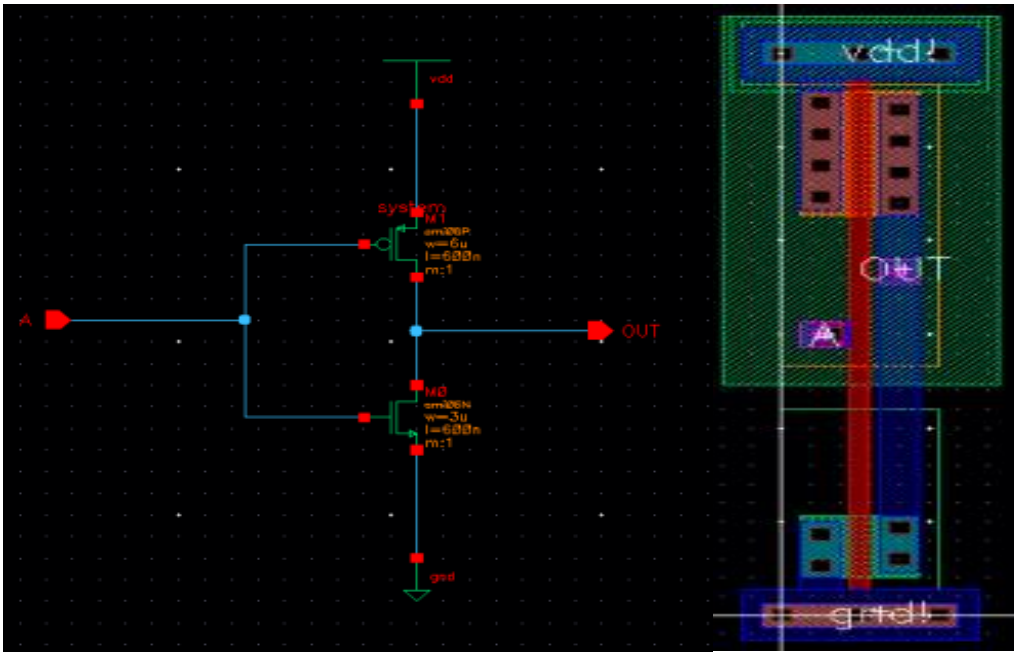
DFF refers to D-FLIPFLOP with Master Slave Configuration. It has an asynchronous clear. The gate dimensions are 27x57.6 and an area of 1555.2 sq.micron.

- INVX1



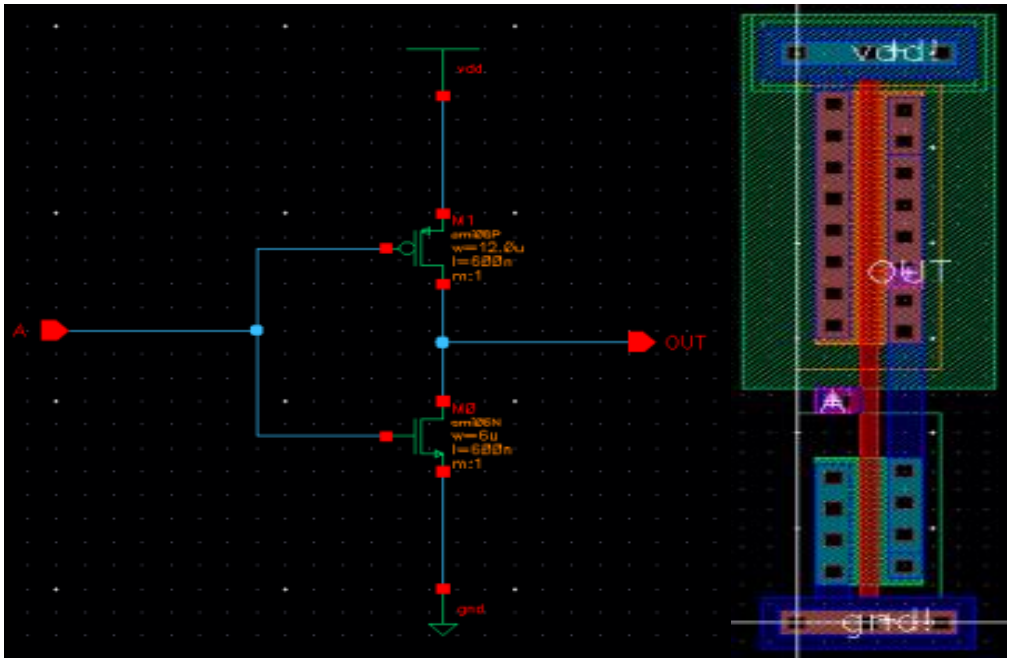
INVX1 refers to INVERTOR gate with a single inputs A and a single output OUT. It implements the logical function OUT=~ (A).The gate dimensions are 27x4.8 and an area of 129.6 sq.micron.

- INVX2



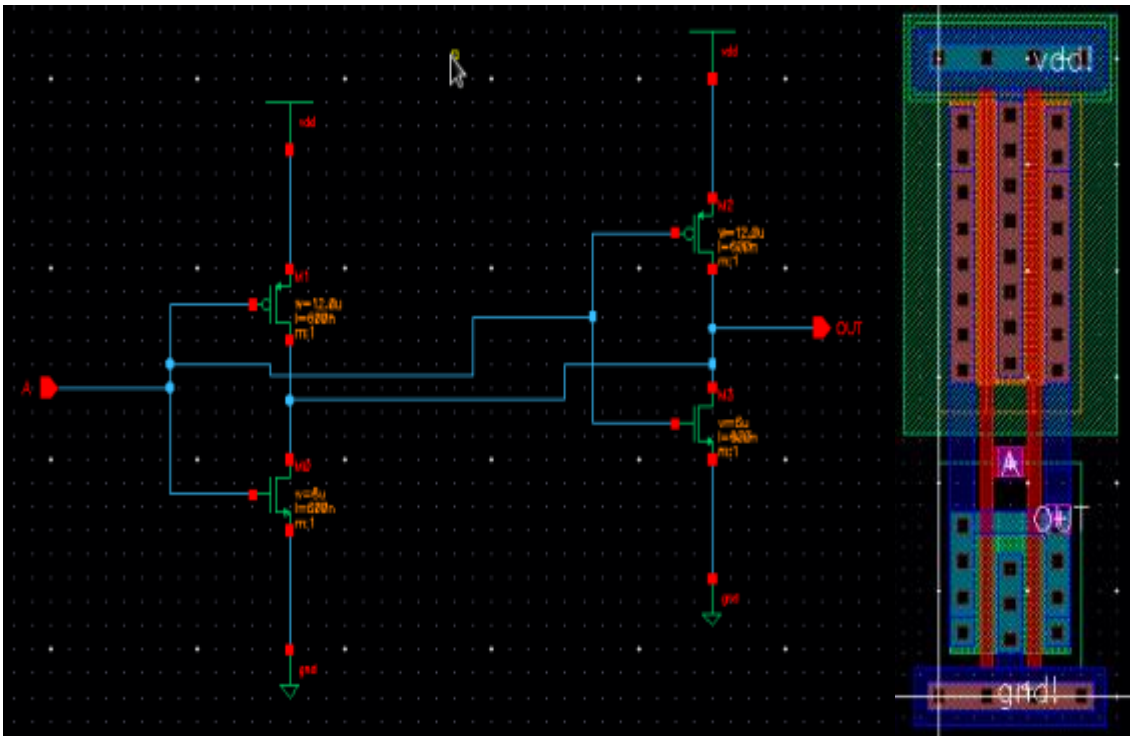
INVX2 refers to INVERTOR gate with a single inputs A and a single output OUT and a drive strength of 2. It implements the logical function OUT=~(A).The gate dimensions are 27x4.8 and an area of 129.6 sq.micron.

- INVX4



INVX4 refers to INVERTOR gate with a single inputs A and a single output OUT and a drive strength of 4. It implements the logical function OUT=~(A).The gate dimensions are 27x4.8 and an area of 129.6 sq.micron.

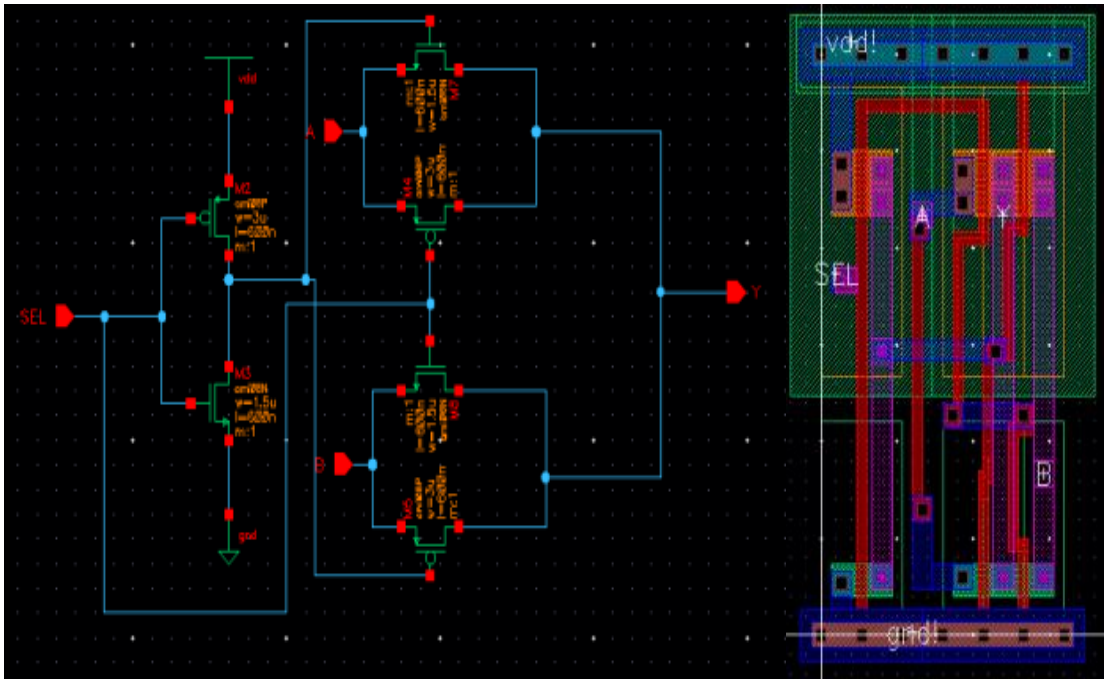
- INVX8



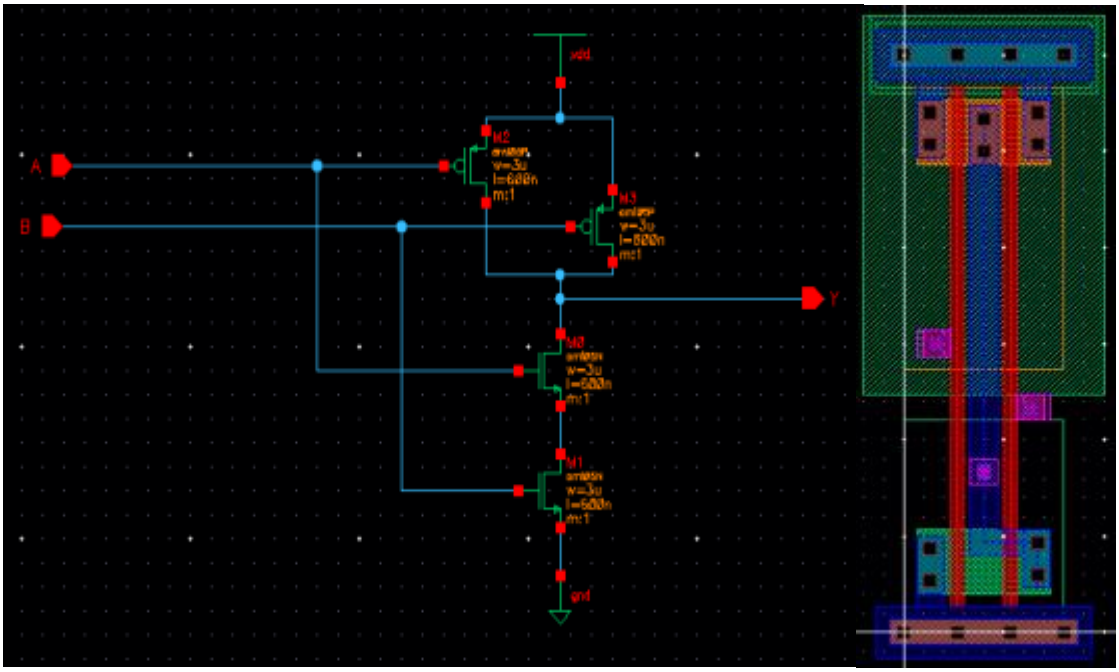
INVX8 refers to INVERTOR gate with a single inputs A and a single output OUT and a drive strength of 8. It implements the logical function OUT= ~ (A).The gate dimensions are 27x7.2 and an area of 194.4 sq.micron.

- MUX2X1

MUX2X1 refers to 2:1 MULTIPLEXOR gate with an input A and select input SEL and an output Y.It implements the logical function Y=(~SEL&A|SEL&A).The gate dimensions are 27x14.4 and an area of 388.8 sq.microns.

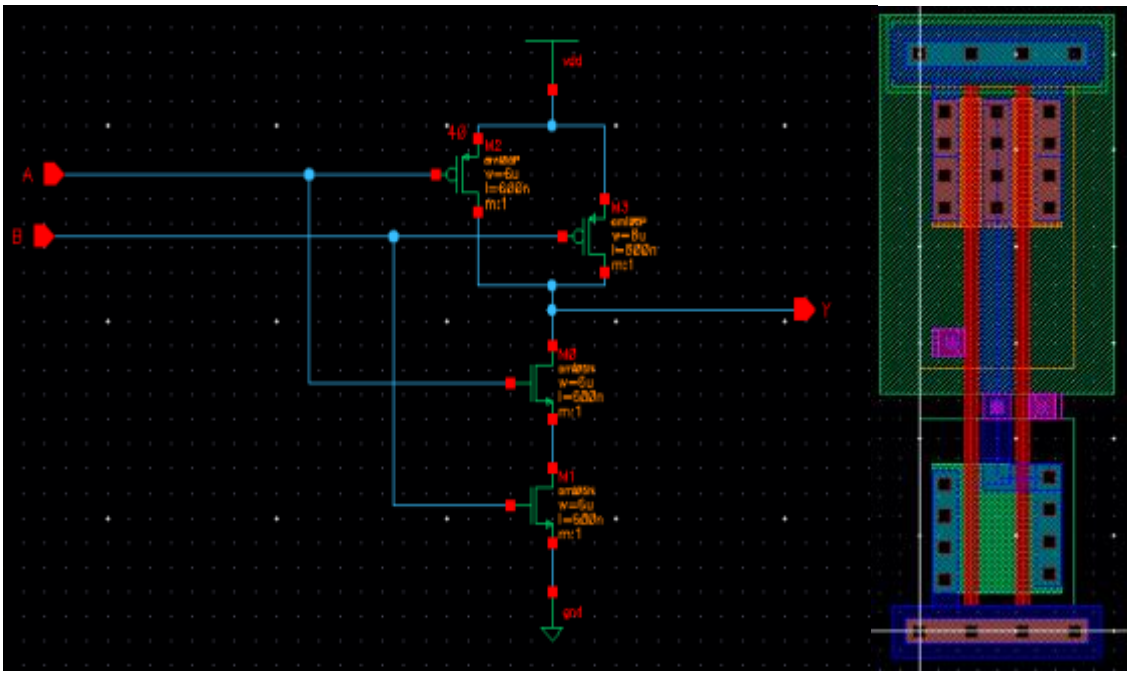


- NAND2X1



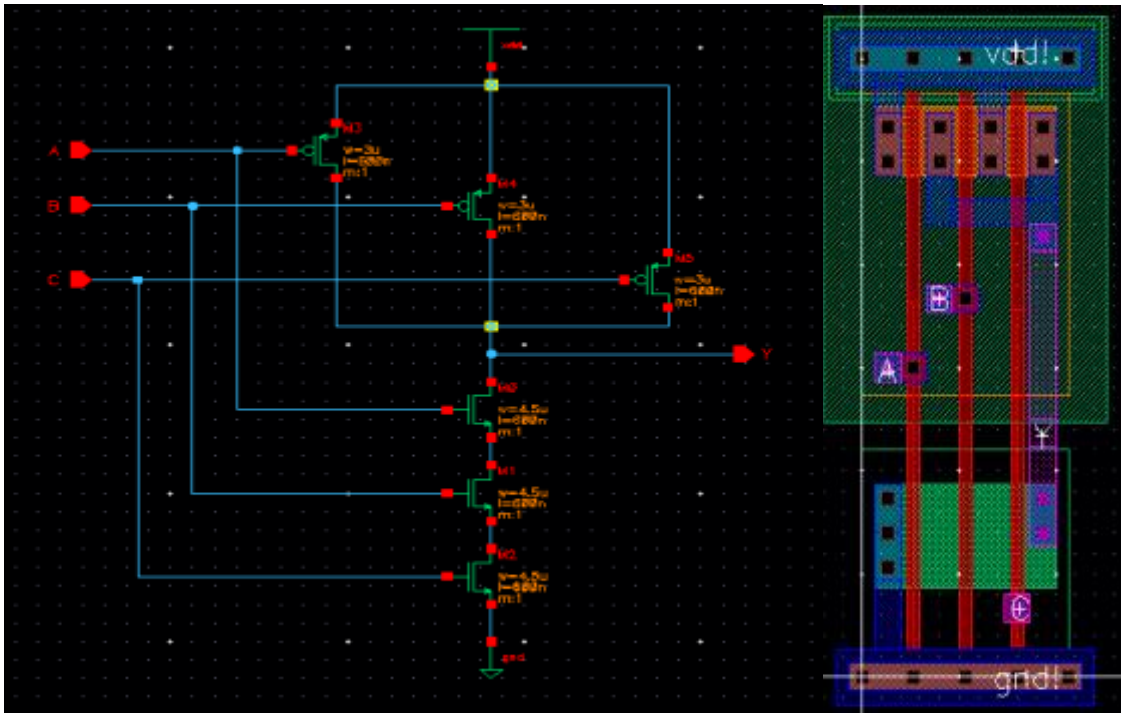
NAND2X1 refers to 2 input NAND gate with inputs A,B and an output Y.It implements the logical function Y=~(A&B).The gate dimensions are 27x7.2 and an area of 194.4 sq.micron.

- NAND2X2



NAND2X2 refers to 2 input NAND gate with inputs A,B and an output Y and a drive strength of 2.It implements the logical function Y=~(A&B).The gate dimensions are 27x7.2 and an area of 194.4 sq.micron.

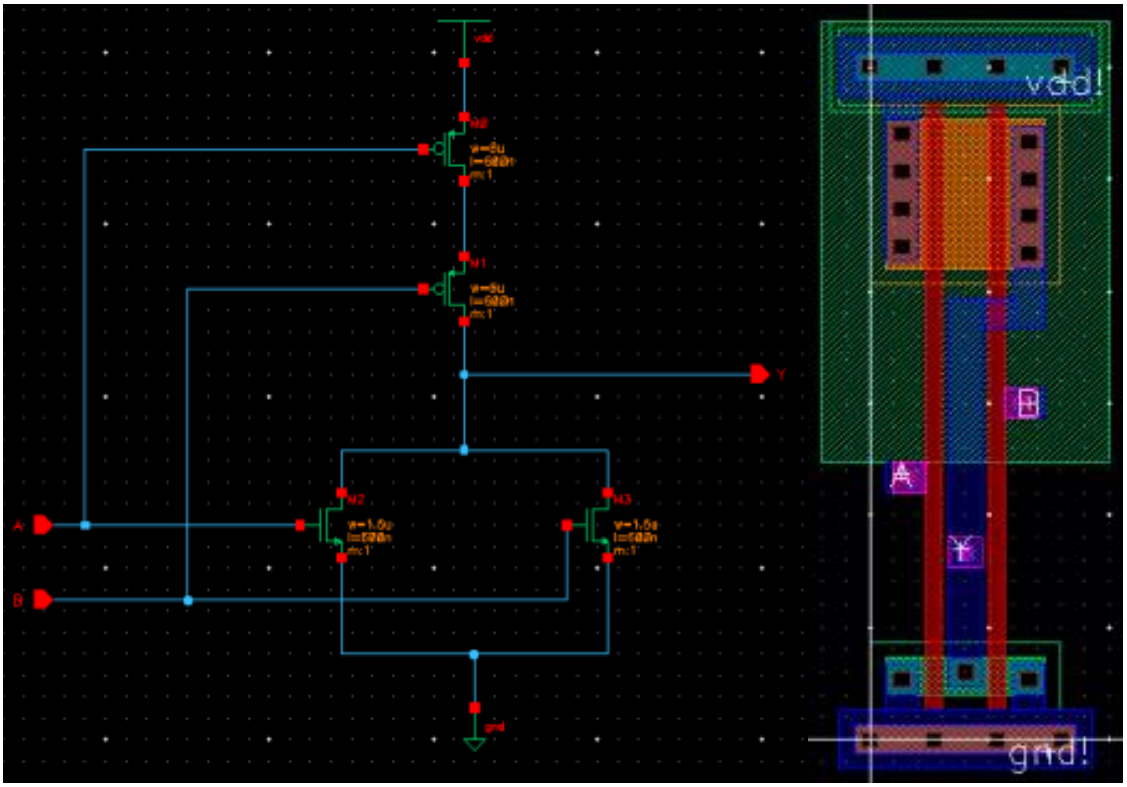
- NAND3X1



NAND3X1 refers to 3 input NAND gate with inputs A,B,C and an output Y.It implements the logical function Y=~(A&B&C).The gate dimensions are 27x9.6 and an area of 259.2 sq.micron.

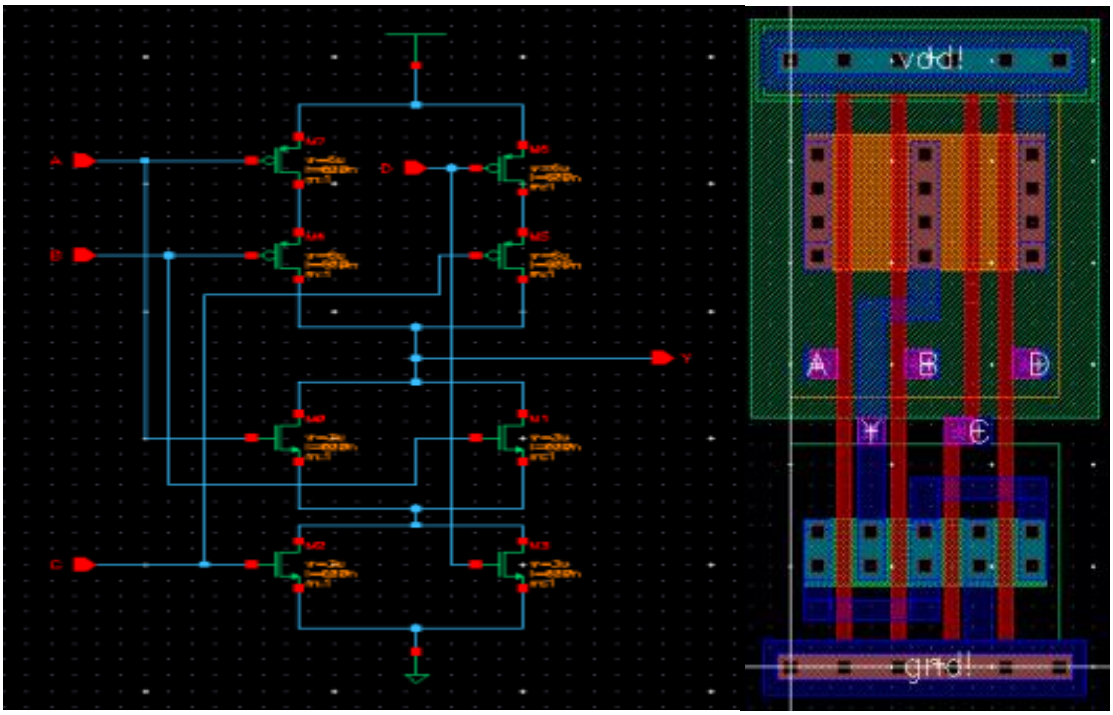
- NOR2X1

NOR2X1 refers to 2 input NOR gate with inputs A, B and an output Y. It implements the logical function Y=~ (A|B).The gate dimensions are 27x7.2 and an area of 194.4 sq.micron.

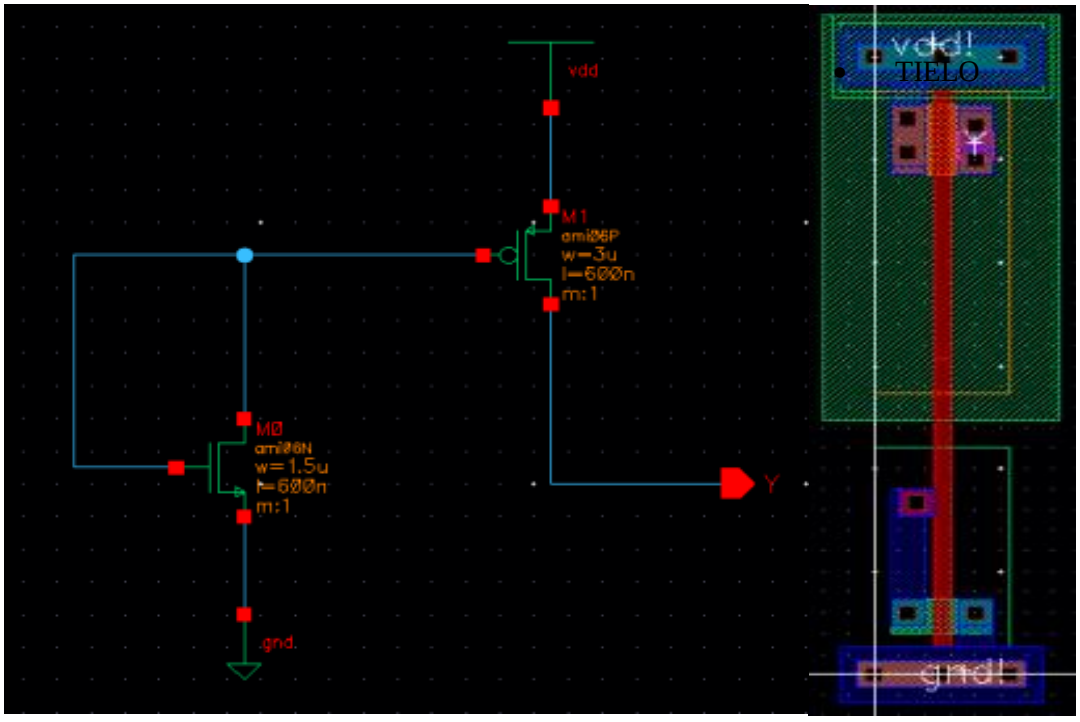


- OAI4X1

OAI4X1 refers to OR AND INVERT gate with four inputs A,B,C,D and one output Y(4X1).It implements the logical function Y=~((A|B)&(C|D)).The gate dimensions are 27x12 and an area of 324 sq.micron.


vdd!
A
B
D
C
Y
gnd!

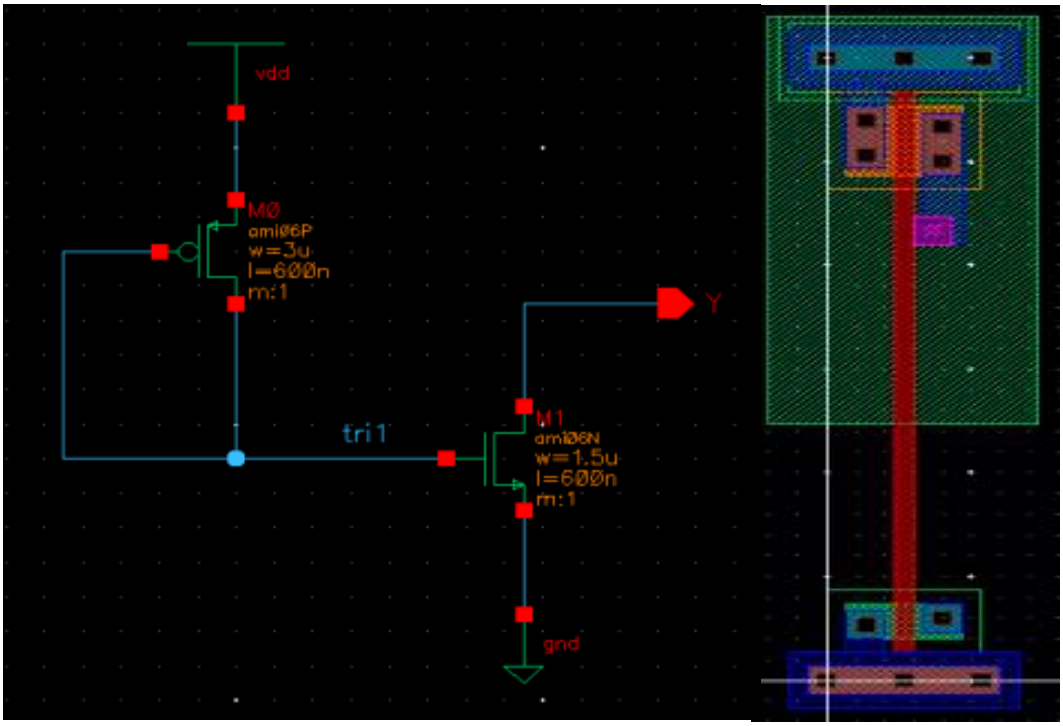
- TIEHI


vdd
M1
ami06P
w=3u
l=600n
m:1
M0
ami06N
w=1.5u
l=600n
m:1
Y
gnd.
vdd!
gnd!

- TIELO

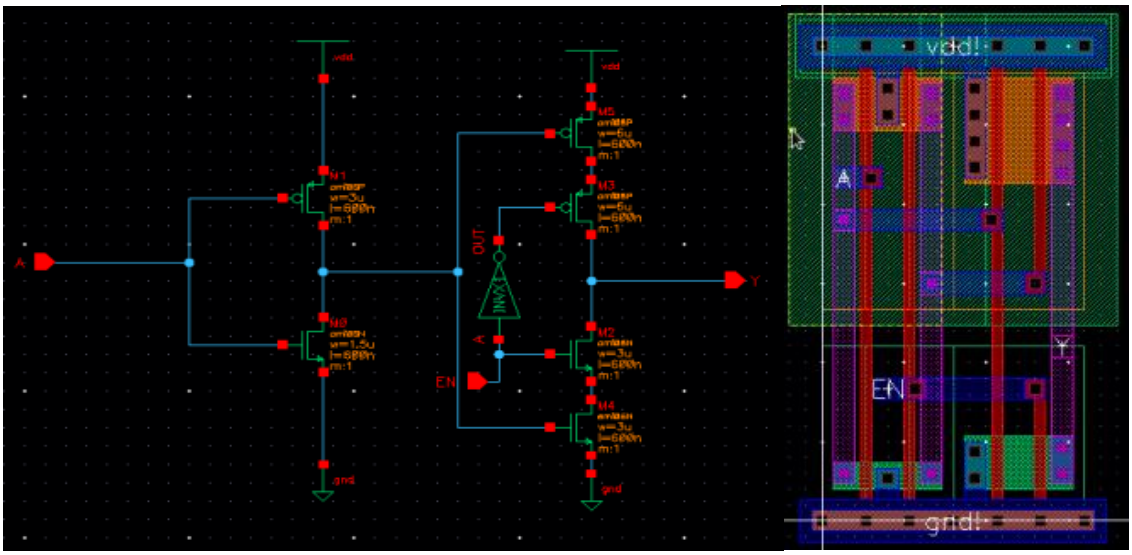
TIEHI refers to TIE HIGH gate with an output Y.It The TIEHI cell uses a diode-connected nmos device that provides a low voltage to the gate of the pmos transistor.function.The gate dimensions are 27x4.8 and an area of 129.6 sq.micron.

- TIELO



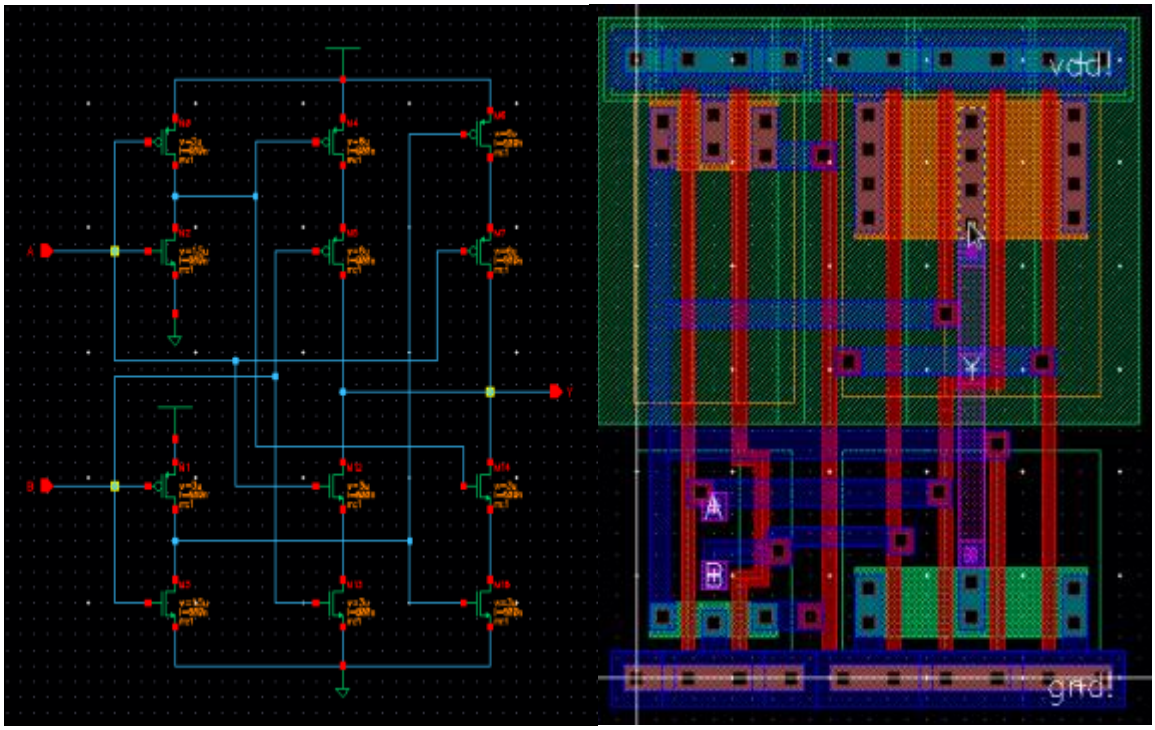
TIELO refers to TIE LOW gate with an output Y.It The The TIELO is similar, using a diode-connected pmos and regular nmos to provide a low voltage at the nmos drain .The gate dimensions are 27x4.8 and an area of 129.6 sq.micron.

- TRI



TRI refers to A TRISTATE INVERTOR gate with an input A and an enable signal EN and one output Y(4X1). The gate dimensions are 27x14.4 and an area of 388.8 sq.micron.

- XOR2X1



XOR refers to an EXCLUSIVE OR gate with two inputs A,B and one output Y. It implements a logical function of A^B.The gate dimensions are 27x21 and an area of 587.25 sq.micron.