DISSERTATION

DATA TRANSFER USING LIGHT-FIDELITY TECHNOLOGY

Submitted in partial fulfilment of the requirements of

M.Tech. Software Engineering Degree Program

By

Harshali Chopade
ID No. 2015CY93014

Under the supervision of

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Dissertation work carried out at

Cybage Software Pvt.Ltd. Pune

BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE
PILANI (RAJASTHAN)

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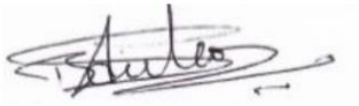
CERTIFICATE

This is to certify that the Dissertation entitled **Data Transfer using LI-FI Technology** and submitted by **Harshali Chopade**, ID **No. 2015CY93014** in partial fulfillment of the requirements of **SEAY ZG629T Dissertation**, embodies the bonafide work done by him under my supervision.



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DATA TRANSFER USING LIGHT-FIDELITY TECHNOLOGY

Abstract

Li-Fi stands for Light-Fidelity. Li-Fi technology, proposed by the German physicist — Harald Haas, provides transmission of data through illumination by sending data through an LED light bulb that varies in intensity faster than the human eye can follow. The new Li-Fi technology can be well managed very easily and it is pretty simple. At one corner you will be having a led which will be working as a light source and on the other corner a Light Sensor or a photo detector. Light Sensor detect light as soon as the LED light starts glowing and will give an output of either binary 1 or binary 0.

Similar prototype has been created using hardware microcontroller, UART, LED source, Photo Diode and Software Matlab and NI Multi Sim. In this Prototype, we have transmitter application in which MATLAB selects the image and sends it to COM PORT using UART, microcontroller which receives this information from COM PORT and transmits light using binary 0s and 1s and receiver in which light emitted is detected by Photo diode which is integrated with microcontroller and send it to COM PORT, here MATLAB receiver application receives data from COM PORT. This binary data is then reverse engineered to restore selected image.

Key words: LED (Light Emitting Diode) , UART – Universal asynchronous receiver/transmitter

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Chapter 1

Introduction

Light Fidelity (Li-Fi) [1] refers to a bidirectional, high-speed and fully networked wireless communication technology similar to Wi-Fi. The term was coined by Harald Haas and is a form of visible light communication and a subset of optical wireless communications (OWC) and could be a complement to RF communication (Wi-Fi or cellular networks), or even a replacement in contexts of data broadcasting. It is wire and UV visible-light communication or infrared and near-ultraviolet instead of radio-frequency spectrum, part of optical wireless communications technology, which carries much more information and has been proposed as a solution to the RF-bandwidth limitations.

1.1 Background

Harald Haas, coined the term "Li-Fi" at his TED Global Talk where he introduced the idea of "Wireless data from every light". He is Chairman of Mobile Communications at the University of Edinburgh and co-founder of pureLiFi. The general term visible light communication (VLC), whose history dates back to the 1880s, includes any use of the visible light portion of the electromagnetic spectrum to transmit information. The D-Light project at Edinburgh's Institute for Digital Communications was funded from January 2010 to January 2012. Haas promoted this technology in his 2011 TED Global talk and helped start a company to market it. PureLiFi, formerly pureVLC, is an original equipment manufacturer (OEM) firm set up to commercialize Li-Fi products for integration with existing LED-lighting systems.

In October 2011, companies and industry groups formed the Li-Fi Consortium, to promote high-speed optical wireless systems and to overcome the limited amount of radio-based wireless spectrum available by exploiting a completely different part of the electromagnetic spectrum. A number of companies offer uni-directional VLC products, which is not the same as Li-Fi - a term defined by the IEEE 802.15.7r1 standardization committee.

VLC technology was exhibited in 2012 using Li-Fi. By August 2013, data rates of over 1.6 Gbit/s were demonstrated over a single color LED. In September 2013, a press release said that Li-Fi, or VLC systems in general, do not require line-of-sight conditions. In October 2013, it was reported Chinese manufacturers were working on Li-Fi development kits.

In April 2014, the Russian company Stins Coman announced the development of a Li-Fi

wireless local network called BeamCaster. Their current module transfers data at 1.25 gigabytes per second but they foresee boosting speeds up to 5 GB/second in the near future. In 2014 a new record was established by Sisoft (a Mexican company) that was able to transfer data at speeds of up to 10 Gbit/s across a light spectrum emitted by LED lamps.
Recent integrated CMOS optical receivers for Li-Fi systems are implemented with avalanche photo diodes (APDs) which has a low sensitivity. In July 2015, IEEE has operated the APD in Geiger-mode as a single photon avalanche diode (SPAD) to increase the efficiency of energy-usage and makes the receiver more sensitive. Also this operation could be performed as quantum-limited sensitivity that makes receivers detect weak signals from far distance.

1.2 Motivation

Li-Fi, which uses visible light to transmit signals wirelessly, is an emerging technology poised to compete with Wi-Fi. One main advantage of Li-Fi is security. Since light cannot pass through opaque structures, Li-Fi Internet is available only to the users within a room and cannot be breached by users in other rooms or buildings.

1.3 Problem Statement

Design and build a device which can transfer data using Li-Fi technology.

1.4 Objectives

The objectives are as follows:

- Demonstrate that light can be used to transfer data using Li-fi technology.
- Create a prototype that transfers data using Li-fi technology.
- Create end to end application for data transmission and reception.

Chapter 2

System Architecture

System architecture consists details of hardware controllers, sensors and software to transmit and receive data.

2.1 Working Principle

The block diagram of Li-Fi is working on simple working principle. [2] On this system, light emitter on one end, for example, an LED, and a photo detector on the other. The photo detector registers a binary one when the LED is on; and a binary zero if the LED is off. To build up a message, flash the LED numerous times or use an array of LEDs of perhaps a few different colors, to obtain data rates in the range of hundreds of megabits per second. Light-emitting diodes can be switched on and off faster than the human eye can detect, causing the light source to appear to be on continuously, even though it is in fact 'flickering'. The on-off activity of the

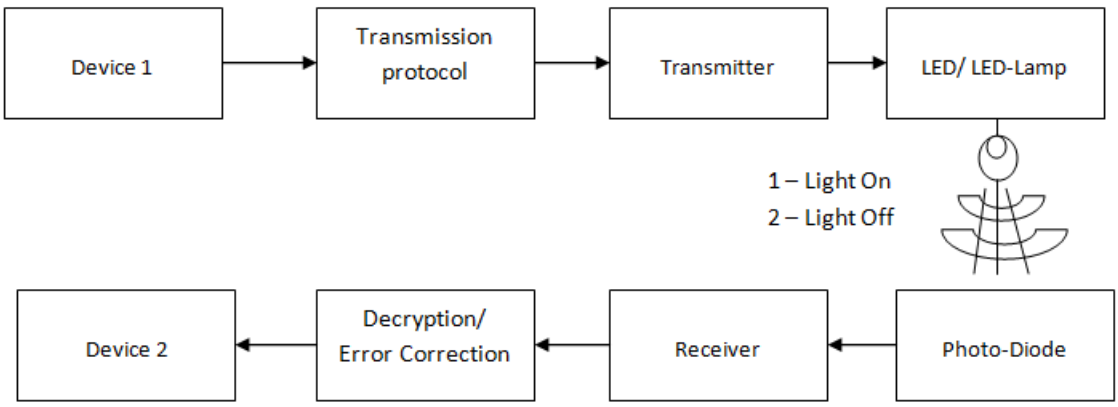

Figure A.1: Block diagram of Li-Fi communication

bulb which seems to be invisible enables data transmission using binary codes: switching on an LED is a logical '1', switching it off is a logical '0'. By varying the rate at which the LEDs flicker on and off, information can be encoded in the light to different combinations of 1s and 0s . The data can be encoded in the light by varying the flickering rate at which the LEDs flicker on and off to generate different strings of 1s and 0s. The LED intensity is modulated so rapidly

that human eye cannot notice, so the light of the LED appears constant to humans . Block Diagram of Li-Fi System The method of using transmit information wirelessly is technically referred to as Visible Light Communication (VLC), though it is popular called as Li-Fi because it can compete with its radio based rival Wi-Fi connection devices within room. Many other sophisticated techniques can be used to dramatically increase VLC data rate. The LED data rate is directly transmits a different data streams.

2.2 Circuit Diagram

The transmitter and receiver circuit diagram simulation is done by using Multisim. The results suggests that when data stream bit is '1' the voltage at receiver end is 5V which can be used by micro controller. When the data stream bit is '0', the receiving voltage will be 0V.

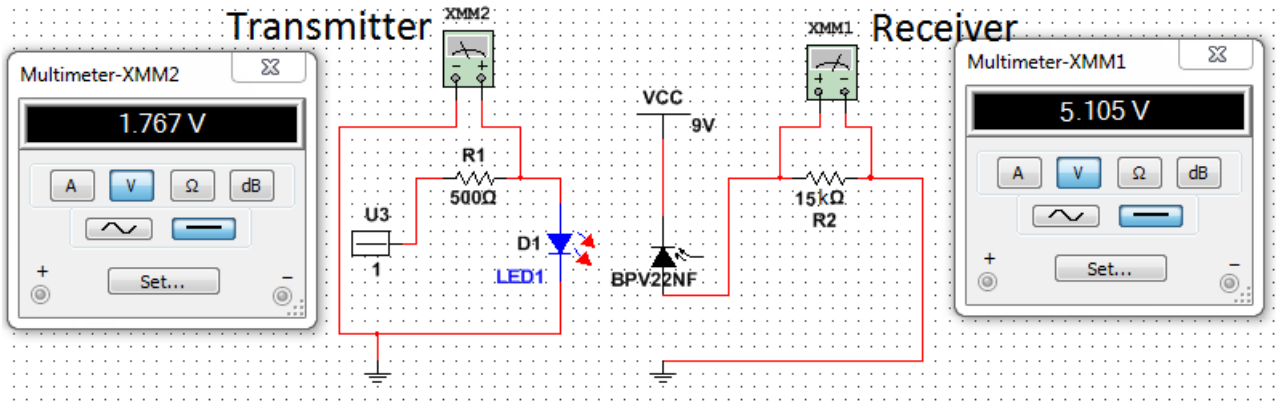

Figure A.2: Circuit Diagram (LED ON)

2.3 Construction of Li-Fi system

Li-Fi is a fast and cheap optical version of Wi-Fi. It based on Visible Light Communication (VLC). VLC is a data communication medium, which uses visible light between 400 THz (780 nm) and 800 THz (375 nm) as optical carrier for data transmission and illumination. It uses fast pulses of light to transmit information wirelessly. The main components of Li-Fi system are as follows:

- a high brightness white LED which acts as transmission source.
- a silicon photodiode with good response to visible light as the receiving element.

LEDs can be switched on and off to generate digital strings of different combination of 1s and 0s. To generate a new data stream, data can be encoded in the light by varying the flickering rate of the LED. The LEDs can be used as a sender or source, by modulating the LED light with the data signal. The LED output appears constant to the human eye by virtue of the fast flickering rate of the LED. Communication rate greater than 100 Mbps is possible by using high speed LEDs with the help of various multiplexing techniques. VLC data rate can

be increased by parallel data transmission using an array of LEDs where each LED transmits a different data stream. The Li-Fi emitter system consists of 4 primary sub assemblies:

- Bulb
- RF power amplifier circuit (PA) (Internal in MSP430)
- Printed circuit board (PCB)
- Enclosure

The PCB controls the electrical inputs and outputs of the lamp and houses the microcontroller used to manage different lamp functions. A RF (radio-frequency) signal is generated by the solid-state PA and is guided into an electric field about the bulb. The high concentration of energy in the electric field vaporizes the contents of the bulb to a plasma state at the bulbs center; this controlled plasma generates an intense source of light.

The bulb sub-assembly is the heart of the Li-Fi emitter. It consists of a sealed bulb which is embedded in a dielectric material. This design is more reliable than conventional light sources that insert degradable electrodes into the bulb. The dielectric material serves two purposes. It acts as a waveguide for the RF energy transmitted by the PA. It also acts as an electric field concentrator that focuses energy in the bulb. The energy from the electric field rapidly heats the material in the bulb to a plasma state that emits light of high intensity and full spectrum.

There are various inherent advantages of this approach which includes high brightness, excellent color quality and high luminous efficacy of the emitter in the range of 150 lumens per watt or greater. The structure is mechanically robust without typical degradation and failure mechanisms associated with tungsten electrodes and glass to metal seals, resulting in useful lamp life of 30,000+ hours. In addition, the unique combination of high temperature plasma and digitally controlled solid state electronics results in an economically produced family of lamps scalable in packages from 3,000 to over 100,000 lumens.

Chapter 3

Resources

Following are the resources that will be used in Lifi-system:

- Hardware
  - MSP430g2553 micro controller launchpad
  - LED
  - Photo-Diode
  - Device
  - Batteries
  - Resistors
  - Devices
    - Computer
    - Mobile
- Software
  - NI MultiSim 14.0V
  - IAR Embedded Workbench
  - MatLab 2017a application

3.1 Transmitter

Light source can theoretically be used as transmitting device for VLC. However, some are better suited than others. For instance, incandescent lights quickly break down when switched on and off frequently. These are thus not recommended as VLC transmitters. More promising alternatives are fluorescents lights and LEDs. VLC transmitters are usually also used for providing illumination of the rooms in which they are used. This makes fluorescent lights a particularly popular choice, because they can flicker quickly enough to transmit a meaningful amount of data and are already widely used for illumination purposes. VLC will probably not be used for massive data transmission. High data rates as the ones referred to above, were reached under meticulous setups which cannot be expected to be reproduced in real-life scenarios. One can expect to see data rates of about 5 kbit/s in average applications, such as location estimation.

3.2 MSP430g2553 launchpad

The Texas Instruments MSP430 [3] family of ultra-low-power micro controllers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator(DCO) allows wake-up from low-power modes to active mode in less than 1 s. The key feature of MSP430 are Basic Clock Module Configurations like Internal Frequencies up to 16 MHz With Four Calibrated Frequency, Internal Very-Low-Power Low-Frequency Oscillator, 32-kHz Crystal Programmable Code Protection by Security, External Digital Clock Source.

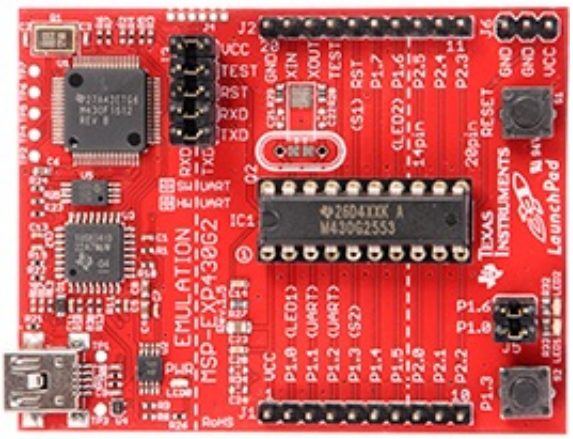

Figure A.1: MSP430 micro controller

3.3 Sensors

3.3.1 Light Emitting Diode

A light-emitting diode (LED) is a two-lead semiconductor light source. It is a pn junction diode, which emits light when activated. When a suitable voltage is applied to the leads, electrons are able to recombine with electron holes within the device, releasing energy in the form of photons.

3.3.2 Photo Diode

A photo diode is a semiconductor device that converts light into current. The current is generated when photons are absorbed in the photo diode. A small amount of current is also produced when no light is present. Photo diodes may contain optical filters, built-in lenses, and may have large or small surface areas. Photo diodes usually have a slower response time as their surface area increases.

3.4 The UART: What it is & How it works

The Universal Asynchronous Receiver/Transmitter (UART) controller is the key component of the serial communications subsystem of a computer. The UART takes bytes of data and transmits the individual bits in a sequential fashion. At the destination, a second UART re-assembles the bits into complete bytes.

Serial transmission is commonly used with modems and for non-networked communication between computers, terminals and other devices. There are two primary forms of serial transmission: Synchronous and Asynchronous. Depending on the modes that are supported by the hardware, the name of the communication sub-system will usually include if it supports Asynchronous communications and if it supports Synchronous communications. Some common acronyms are: UART Universal Asynchronous Receiver/Transmitter and USART Universal Synchronous-Asynchronous Receiver/Transmitter.

UART will be used to get data through MSP430 to computer/laptop and vice-versa.

3.5 Inverting Amplifier

The inverting amplifier using an op-amp is one of the most widely used operational amplifier circuits especially as it can be used as a summing amplifier or virtual earth mixer. As the open loop DC gain of an Operational Amplifiers is extremely high we can therefore afford to lose some of this high gain by connecting a suitable resistor across the amplifier from the output terminal back to the inverting input terminal to both reduce and control the overall gain of the amplifier. This then produces and effect known commonly as Negative Feedback, and thus produces a very stable Operational Amplifier based system.

Negative Feedback is the process of feeding back a fraction of the output signal back to the input, but to make the feedback negative, we must feed it back to the negative or inverting

input terminal of the op-amp using an external Feedback Resistor called R. This feedback connection between the output and the inverting input terminal forces the differential input voltage towards zero. This effect produces a closed loop circuit to the amplifier resulting in the gain of the amplifier now being called its Closed-loop Gain. Then a closed-loop inverting amplifier uses negative feedback to accurately control the overall gain of the amplifier, but at a cost in the reduction of the amplifiers gain. This negative feedback results in the inverting input terminal having a different signal on it than the actual input voltage as it will be the sum of the input voltage plus the negative feedback voltage giving it the label or term of a Summing Point. We must therefore separate the real input signal from the inverting input by using an Input Resistor, Rin.

As we are not using the positive non-inverting input this is connected to a common ground or zero voltage terminal as shown below, but the effect of this closed loop feedback circuit results in the voltage potential at the inverting input being equal to that at the non-inverting input producing a Virtual Earth summing point because it will be at the same potential as the grounded reference input. In other words, the op-amp becomes a differential amplifier.

Chapter 4

Modulation techniques for Li-Fi

Modulation techniques [4] developed for intensity modulation and direct detection (IM/DD) optical wireless communication (OWC) systems are suitable for LiFi communications systems. However, these modulation techniques may not be suitable for all lightning regimes. LiFi transceivers are illumination devices enabled for data communications. Therefore adapting IM/DD modulation technique should first satisfy certain illumination requirements before being Li Fi enabled. For example, modulation techniques should support dimmable illumination so that communication would be still available when the illumination is not required.

LiFi uses offtheshelf light emitting diodes (LEDs) and photodiodes (PDs) as channel frontend devices. This restricts signals propagating throughout the channel to strictly positive signals. Single carrier modulation (SCM) techniques are straight forward to implement in Li Fi. Modulation techniques, such as onoff keying (OOK), pulseposition modulation (PPM), and M ary pulse amplitude modulation (M PAM), can be easily implemented. However, due to the dispersive nature of optical wireless channels, such schemes require complex equalizers at the receiver. Therefore, the performance of these schemes degrades as their spectral efficiency (SE) increases.

On the other hand, multiple carrier modulation (MCM) techniques, such as the orthogonal frequency division multiplexing (OFDM), have been shown to be potential candidates for optical wireless channels since they only require single tap equalizer at the receiver. Adaptive bit and power loading can maximize the achievable data rates of OFDMbased LiFi systems by adapting the system loading to the channel frequency response. Moreover, the DC wander and low frequency interference can be easily avoided in OFDM by optimizing the adaptive bit/power loading to avoid the low frequency subcarriers. Colour modulation techniques are unique to LiFi communication systems as the information is modulated on the instantaneous colour changes.

4.1 Optical Wireless Modulation Techniques

4.1.1 Single Carrier Modulation Techniques

Single carrier modulation techniques [5] were first proposed for IM/DD optical wireless communications based on infrared communications. Modulation techniques, such as pulse amplitude

modulation (PAM), pulse width modulation (PWM), and PPM, are straightforward to implement for Li Fi systems. In general, single carrier modulation techniques are suitable candidates for LiFi when lowtomoderate data rates applications are required. By switching the LED between on and off states, the incoming bits can be modulated into the light intensity. Illumination control can be supported by adjusting the light intensities of the on and off states, without affecting the system performance. Compensation symbols are proposed in the visible light communications standard, IEEE 802.15.7, to facilitate the illumination control at the expense of reducing the SE. If the link budget offers high signal to noise ratios (SNR), MPAM can be used to modulate the incoming bits on the amplitude of the optical pulse.

The position of the optical pulse is modulated into shorter duration chips in PPM with a position index that varies depending on the incoming bits. The PPM is more power efficient than OOK, however, it requires more bandwidth than OOK to support equivalent data rates. Differential PPM (DPPM) was proposed to achieve power and/or SE gains [10], however the effect of unequal bit duration for the different incoming symbols could affect the illumination performance. A solution was proposed in to ensure that the duty cycle is similar among the different symbols to prevent any possible flickering. Variable PPM (VPPM) was proposed in the VLC standard IEEE 802.15.7 to support dimming for the PPM technique and prevent any possible flickering. The pulse dimming in VPPM is controlled by the width of the pulse rather than the pulse amplitude. Therefore, VPPM can be considered as a combination of PPM and PWM techniques. Multiple PPM (MPPM) was proposed as a solution to the dimming capability of PPM, where it was reported that it achieves higher spectral efficiencies than VPPM with less optical power dissipation

4.1.2 Optical OFDM

Single carrier modulation techniques require a complex equalization process when employed at high data rates. In addition, effects such as DC wandering and flickering interference of florescent lights may influence the system performance at the lower frequency regions of the used bandwidth. On the other hand, multicarrier modulation techniques such as OFDM can convert the frequency selective fading of the communication channel into a flat fading by employing the computationally efficient single tap equalizer.

In addition, OFDM [5] supports adaptive power and bit loading which can adapt the channel utilization to the frequency response of the channel. This can maximize the system performance. Supporting multiuser communication systems is an inherent advantage of OFDM, where each user could be allocated certain subcarriers. At the OFDM transmitter, the incoming bits are modulated into specific modulation formats such as M QAM. The M QAM symbols are loaded afterwards into orthogonal subcarriers with subcarrier spacing equal to multiple of the symbol duration. The parallel symbols can then be multiplexed into a serial time domain output, generally using inverse fast Fourier transformation (IFFT). The physical link of LiFi is achieved using offtheshelf optoelectronic devices such as LED and photodetectors (PD). Due to the fact that these light sources produce an incoherent light, the OFDM timedomain waveforms are used in LiFi to modulate the intensity of the LED source. Therefore, these waveforms are

required to be both unipolar and real valued.

4.1.3 LiFi Unique Modulation Technique

The modulation frequency in Li Fi systems does not correspond to the carrier frequency of the LED. All the aforementioned modulation techniques are baseband modulation techniques. It is practically difficult to modulate the carrier frequency of the LEDs, however, it is practically straightforward to change its colour. This feature adds a new degree of freedom to Li Fi systems. Colour tunable LEDs such as the red green blue LED (RGB LED) can illuminate with different colours based on the intensity applied on each LED element. The IEEE 802.15.7 standard proposes colour shift keying (CSK) [5] as a modulation technique for VLC. The incoming bits are mapped into a constellation of colours from the chromatic CIE 1931 colour space. The CIE 1931 is the widely used illumination model for human eye colour perception. Any colour in the model can be represented by the chromaticity dimension [x, y].

In CSK, the overall intensity of the output colour is constant, however, the relative intensities between the multiple used colours are changed. Therefore the instantaneous colour of the multicolour LED is modulated. Seven wavelengths are defined in IEEE 802.15.7 specify the vertices of a triangle where the constellation point lies in. The intensity of each RGB LED element is changed to match the constellation point while maintaining a constant optical power and a constant illumination colour. This is desirable in Li Fi systems, since the constant illumination colour naturally mitigates any flickering. An amplitude dimming is used for brightness control in CSK while the center colour of the colour constellation constant is kept.

However, colour shift is possible due to the presence of any improper driving current used for dimming control. Constellation sizes up to 16CSK were proposed in the IEEE 802.15.7 standard based on tri colour LEDs. Constellation points design based on CIE 1931 was also investigated by Drost and Sadler using billiard algorithms, by Monterio and Hranilovic using interior point method, by Singh et al. using quad LED (QLED), and by Jiang et al. using extrinsic transfer (EXIT) charts for an iterative CSK transceiver design

4.2 LiFi Modulation Techniques Challenges

LiFi is an emerging high speed, low cost solution to the scarcity of the radio frequency (RF) spectrum, therefore it is expected to be realized using the widely deployed off-the-shelf opto-electronic LEDs.[5] Due to the mass production of these inexpensive devices, they lack accurate characterizations. In LiFi, light is modulated on the subtle changes of the light intensity, therefore, the communication link would be affected by the non-linearity of the voltageluminance characteristic.

As a solution, predistortion techniques were proposed to mitigate nonlinear distortion . However, as the LED temperature increases the voltageluminance (VL) characteristic experiences memoryeffects. Therefore, the LED non linearity mitigation is still an open research problem. The limited bandwidth of LiFi communication channel leads to inter symbol interference (ISI) at high data rates. The LED frequency response is modeled as a lowpass filter,

and it is the major contributor to the frequency selectivity of Li Fi channels.

The modulation bandwidth over which the frequency response of most commercially available LEDs can be considered flat is around 2-20 MHz. However, the usable bandwidth in LiFi could be extended beyond the 3 dB cutoff frequency. Therefore, modulation techniques with higher spectral efficiencies are key elements in a LiFi system design. Satisfying the illumination requirements is a key element in Li Fi. Most of the research on modulation techniques has been on the communication system performance of Li-Fi system. Factors such as dimming, illumination level control and flickering have been analyzed as secondary parameters of a LiFi system. The Li-Fi systems should be also considered as an illumination system with communications capability, not the reverse.

Chapter 5

IEEE Standards

Like Wi-Fi, Li-Fi is wireless and uses similar 802.11 protocols; but it uses visible light communication (instead of radio frequency waves), which has much bigger bandwidth.

One part of VLC is modeled after communication protocols established by the IEEE 802 workgroup. However, the IEEE 802.15.7 standard is out-of-date, it fails to consider the latest technological developments in the field of optical wireless communications, specifically with the introduction of optical orthogonal frequency-division multiplexing (O-OFDM) modulation methods which have been optimized for data rates, multiple-access and energy efficiency.[35] The introduction of O-OFDM means that a new drive for standardization of optical wireless communications is required.

Nonetheless, the IEEE 802.15.7 standard defines the physical layer (PHY) and media access control (MAC) layer. The standard is able to deliver enough data rates to transmit audio, video and multimedia services. It takes into account optical transmission mobility, its compatibility with artificial lighting present in infrastructures, and the interference which may be generated by ambient lighting. The MAC layer permits using the link with the other layers as with the TCP/IP protocol.

The standard defines three PHY layers with different rates:

- The PHY 1 was established for outdoor application and works from 11.67 kbit/s to 267.6 kbit/s.
- The PHY 2 layer permits reaching data rates from 1.25 Mbit/s to 96 Mbit/s.
- The PHY 3 is used for many emissions sources with a particular modulation method called color shift keying (CSK). PHY III can deliver rates from 12 Mbit/s to 96 Mbit/s.

The modulation formats recognized for PHY I and PHY II are on-off keying (OOK) and variable pulse position modulation (VPPM). The Manchester coding used for the PHY I and PHY II layers includes the clock inside the transmitted data by representing a logic 0 with an OOK symbol "01" and a logic 1 with an OOK symbol "10", all with a DC component. The DC component avoids light extinction in case of an extended run of logic 0's.[citation needed]

The first VLC smartphone prototype was presented at the Consumer Electronics Show in Las Vegas from January 710 in 2014. The phone uses SunPartner's Wysips CONNECT, a

technique that converts light waves into usable energy, making the phone capable of receiving and decoding signals without drawing on its battery.[37][38] A clear thin layer of crystal glass can be added to small screens like watches and smartphones that make them solar powered. Smartphones could gain 15

Philips lighting company has developed a VLC system for shoppers at stores. They have to download an app on their smartphone and then their smartphone works with the LEDs in the store. The LEDs can pinpoint where they are located in the store and give them corresponding coupons and information based on which aisle they are on and what they are looking at.

Chapter 6

Comparison between Wi-fi and Li-fi

Li-Fi is the name given to describe visible light communication technology applied to obtain high speed wireless communication. It derived this name by virtue of the similarity to Wi-Fi. Wi-Fi works well for general wireless coverage within buildings, and Li-Fi is ideal for high density wireless data coverage inside a confined area or room and for relieving radio interference issues.

The table 6.1 shows a comparison [6] of transfer speed of various wireless technologies. Table II shows a comparison of various technologies that are used for connecting to the end user. WiFi currently offers high data rates. The IEEE 802.11.n in most implementations provides up to 150Mbit/s although practically, very less speed is received.

Sr. No	Li-Fi	Wi-Fi
1	Data transmission takes place using bits	Data transmission takes place using radio waves
2	Fast speed internet (1- 3.5Gbp0073)	Comparatively slow speed (54-250 Mbps)
3	Range is limited (10 Meters)	Extended range (20-100 meters)
4	The Spectrum range is 10000 times than Wi-Fi	It has radio spectrum range.
5	It uses Point-To-Point network topology.	It uses Point-To-Multi network topology
6	It uses light as its data transfer medium	It uses radio spectrum as data transfer medium
7	The frequency band is 100 times of Tera HZ	The frequency band is 2.4GHz
8	It is cheaper because free band doesnt need license and it uses light	Expensive because it uses radio spectrum
9	Data density is high	Data Density is comparatively low
10	Lifi is more secured	Comparatively less secured
11	Market Maturity is low	Market Maturity is high

Table 6.1: Comparison between Li-Fi and Wi-Fi

Chapter 7

Applications and Disadvantages

Li-Fi, which uses visible light to transmit signals wirelessly, is an emerging technology poised to compete with Wi-Fi.[7]

7.1 Advantages of Li-Fi technology

- Efficiency: Li-Fi works on visible light technology. Since homes and offices already have LED bulbs for lighting purposes, the same source of light can be used to transmit data. Hence, it is very efficient in terms of costs as well as energy. Light must be on to transmit data, so when there is no need for light, it can be reduced to a point where it appears off to human eye, but is actually still on and working.
- Availability: Wherever there is a light source, there can be Internet. Light bulbs are present everywhere in homes, offices, shops, malls and even planes, meaning that high-speed data transmission could be available everywhere
- Security: One main advantage of Li-Fi is security. Since light cannot pass through opaque structures, Li-Fi Internet is available only to the users within a room and cannot be breached by users in other rooms or buildings.

7.2 Disadvantages of Li-Fi technology

- Internet cannot be used without a light source. This could limit the locations and situations in which Li-Fi could be used.
- Because it uses visible light, and light cannot penetrate walls, the signal's range is limited by physical barriers.
- Other sources of light may interfere with the signal. One of the biggest potential drawbacks is the interception of signals outdoors. Sunlight will interfere the signals, resulting in interrupted Internet.
- A whole new infrastructure for Li-Fi would need to be constructed.

Chapter 8

Applications of Li-Fi

Li-Fi applications are varied as a result of its key features, such as directional lighting, energy efficiency, intrinsic security, high data rate capability, signal blocking by walls and integrated networking capability. Each light fixture in the application environment becomes a separate data channel. These channels can supply different data into each separate pool of light, delivered at the full rated download speed for that channel.

8.1 Cellular communication

In external urban environments, the use of Li-Fi enabled street lamps would provide a network of internet access points. In cellular communication, the distance between radio base stations has come down to about 200-500 metres. So, instead of deploying new radio base stations in our cities, street lamps could provide both, illumination during night, and high speed data communication 24/7. Surprisingly, even when the lights are off as perceived by the eye, full data communication rates are still possible. There is also an additional cost benefit as installing new radio base stations usually comes with large cost for installation and site lease.

8.2 Underwater communication

Radio waves are quickly absorbed in water, preventing underwater radio communications, but light can penetrate for large distances. Therefore, Li-Fi can enable communication from diver to diver, diver to mini-sub, diver to drilling rig, etc.

8.3 Safety environments

In explosion hazard environments, the use of electrical equipment, including mobile phones, is generally greatly restricted. The use of Li-Fi to pass data will simplify the configuration of data networks in such environments, and can enable new systems to enhance security in these environments.

8.4 Intelligent transportation systems

Car headlights and tail lights are steadily being replaced with LED versions. This offers the prospect of car-to-car communication over Li-Fi, allowing development of anti-collision systems and exchange of information on driving conditions between vehicles. Traffic lights already use LED lighting, so that there is also the prospect offered of city wide traffic management systems. This would enable car systems to download information from the network and have real time information on optimal routes to take, and update the network regarding conditions recently experienced by individual vehicles.

8.5 Connectivity

Our homes already have lighting widely installed. The use of Li-Fi enabled lighting will transform the applications that can be envisaged, not only the interconnection of devices, such as televisions, computers and Hi-Fi, but also connecting ordinary domestic appliances, such as fridges, washing machines, microwaves and vacuums. The internet of everything.

8.6 Sensitive data and Security

Hospitals are a specific case of an environment where both EMI sensitivity and security of data are issues. Li-Fi can enable the better deployment of secure networked medical instruments, patient records, etc.
In a meeting room environment, the access area of each channel is the width of the light pool, and can be accessed by multiple users. Each user can receive higher data rates than would be the case for an equivalent Wi-Fi channel. In the Wi-Fi case, each user or group of users directly competes for access to bandwidth. The net result is that the more connections there are, the slower the download speeds are for all. By contrast, in the case of Li-Fi, with its greater number of available access points, each pool of light provides full channel data rates with fewer simultaneous users. The overall net benefit to each user is up to 1000 times greater speeds. In addition, and in contrast to radio waves, the light does not pass through the walls. Therefore, with minimal precautions to avoid leakage from windows, etc., security is fundamentally enhanced as compared with Wi-Fi.

8.7 Indoor navigation

By identifying each light (for example, through the use of the widely used MAC codes used by data routers and computers) it is possible to provide a smart means of navigating through urban environments. The identification of each code would be linked to a specific location.

Chapter 9

Results

Photo Diode and LED have been interfaced with MS430 and results were analyzed. The main focus of mid-sem was on designing and simulation of circuits for transmitting and receiving data (stream of '1' and '0'). NI Multisim was used for simulation of circuit designed for receiving data.

9.1 Transmission code of MatLab

This code contains selecting image from folder structure of computer and converting it into binary array. This array is sent to COM PORT as mentioned in code.

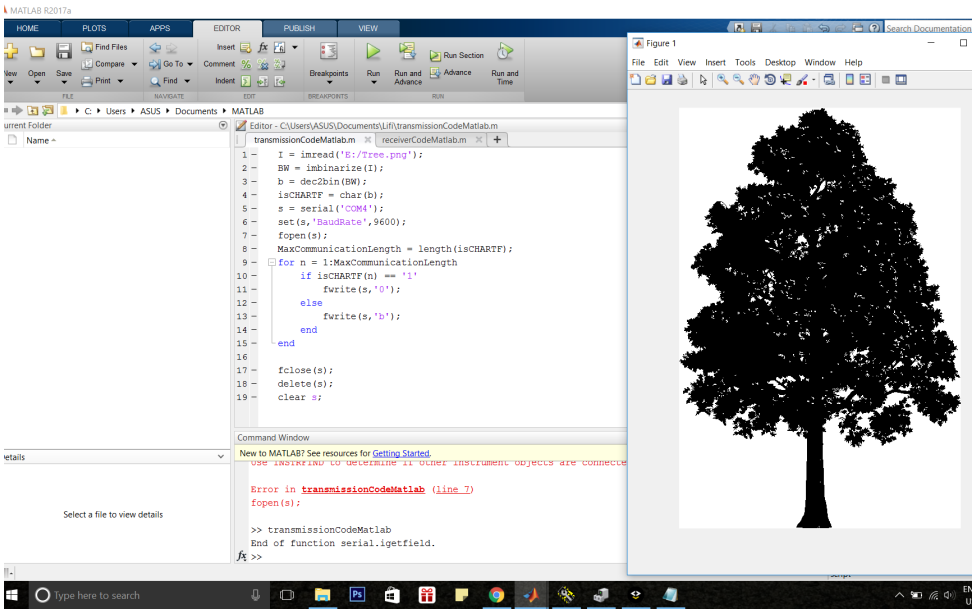

Figure A.1: Code snippet for transmitter for Matlab

9.2 Transmission code of MSP430

This code is burned/dumped in micro controller. Whenever data is available at the COM port, the data is read and send to LED through P1 out pin to blink it.

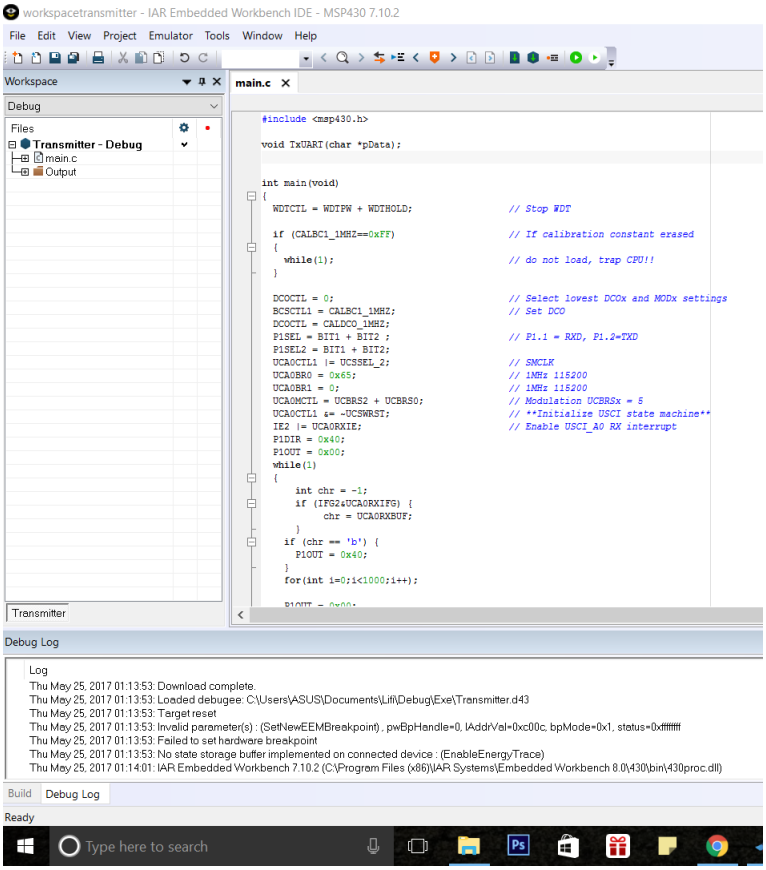

Figure A.2: Code snippet for transmitter for MSP430

9.3 Transmitter Debugging using Hercules

Hercules utility tool is used to debug the data on COM PORT. For transmission, 'b' for blink, character is sent to COM PORT and MSP blinks the LED according to input to P1 out pin.

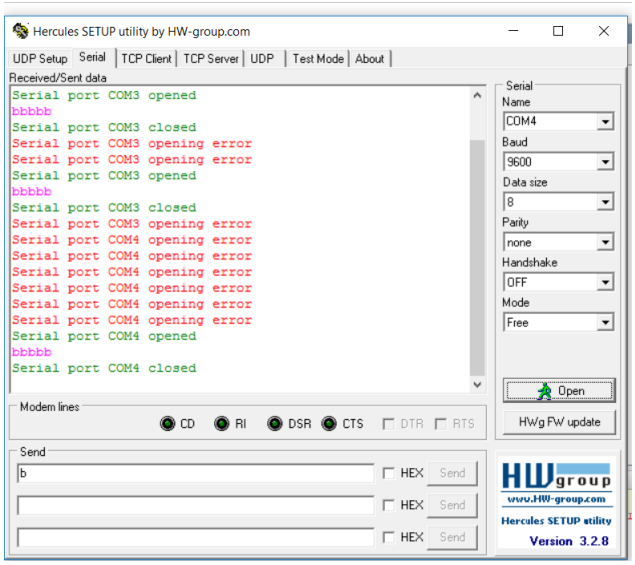

Figure A.3: Transmitter Debugging using Hercules

9.4 Receiver code of MSP430

This code is burned/dumped in micro controller. Whenever data is available at the photo diode, the data is read and send to COM PORT.

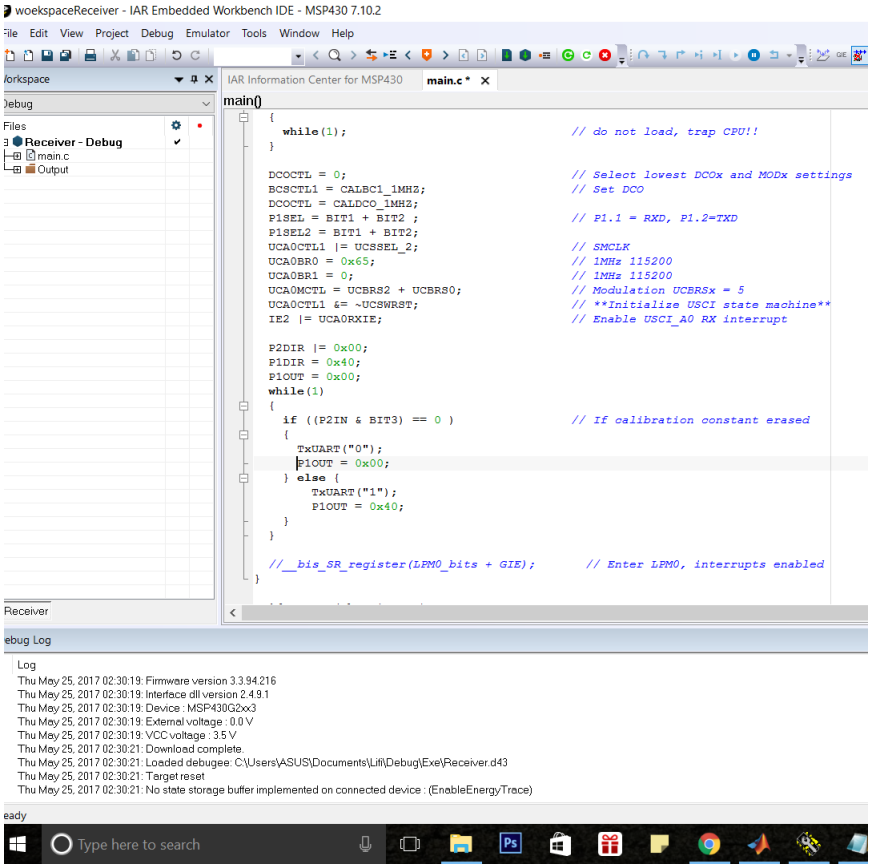

Figure A.4: Code snippet for receiver for MSP430

9.5 Receiver Debugging using Hercules

Hercules utility tool is used to debug the data from COM PORT. The port is being read and data is shown in below figure.

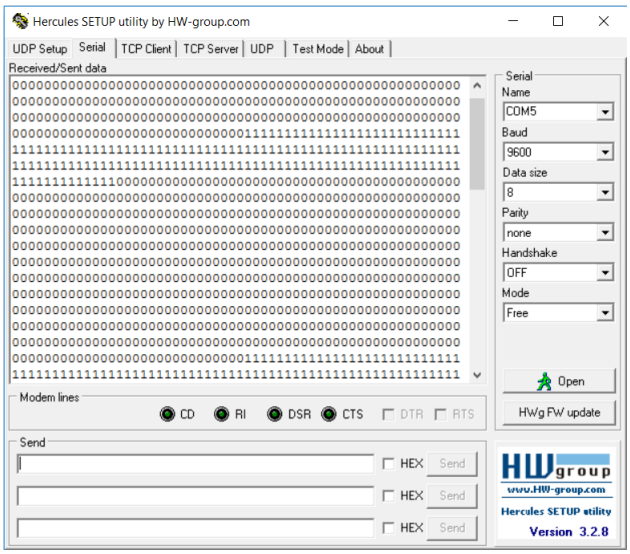

Figure A.5: Receiver Debugging using Hercules

9.6 Receiver code of MatLab

This section will be covered in future scope. In current process, the data is read from COM port but it is giving timeout error. In independent code of MATLAB, the image is being recovered from array that is used in transmission.

9.7 Problem faced

During receiving data, the reception data stream does not match with stream that was transmitted. The sensitivity of receiver should be increased and this can be done using feedback op-amp at receiver.

Chapter 10

Future Scope and Conclusion

LI-FI is an emerging technology and hence it has vast potential. A lot of research can be conducted in this field. Already, a lot of scientists are involved in extensive research in this field. This technology, pioneered by Harald Haas, can become one of the major technologies in the near future. If this technology can be used efficiently, we might soon have something of the kind of WI-FI hotspots wherever a light bulb is available. It will be cleaner and greener and the future of mankind will be safe. As the amount of available bandwidth is limited, the airwaves are becoming increasingly clogged, making it more and more difficult to get a reliable, high-speed signal. The LI-FI technology can solve this crisis. Moreover, it will allow inter access in places such as operation theaters and aircrafts where internet access is usually not allowed. The future of LI-FI is GI-FI. GI-FI or gigabit wireless refers to wireless communication at a data rate of more than one billion bits (gigabit) per second.

In 2008 researchers at the University of Melbourne demonstrated a transceiver integrated on a single integrated circuit (chip) that operated at 60 GHz on the CMOS process. It will allow wireless transfer of audio and video data at up to 5 gigabits per second, ten times the current maximum wireless transfer rate, at one-tenth the cost. Researchers chose the 5764 GHz unlicensed frequency band since the millimeter-wave range of the spectrum allowed high component on-chip integration as well as the integration of very small high gain arrays. The available 7 GHz of spectrum results in very high data rates, up to 5 gigabits per second to users within an indoor environment, usually within a range of 10 meters. Some press reports called this "Gi-Fi". It was developed by Melbourne University-based laboratories of NICTA (National ICT Australia Limited), Australias Information and Communications Technology Research Centre of Excellence.

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[1] Harald Haas, Liang Yin, Yunlu Wang, and Cheng Chen. What is lifi? *Journal of Lightwave Technology*, 34(10):1533 – 1544, 2015.

[2] S. Hossain, S. Islam, and Z. Abadin. Methodology to Achieve Enhanced Data Transmission Rate using LiFi in VLC Technology. *International Journal of Engineering Research*, 2014.

[3] Chris Nagy. *Embedded Systems Design Using the TI MSP430 Series*. Em- bedded Technolgy Series, Newnes, USA, 2003.

[4] Prateek Gawande, Aditya Sharma, and Prashant Kushwaha. Various Modulation Techniques for LiFi. *International Journal of Advanced Research in Computer and Communication Engineering*, 2016.

[5] Mohamed Sufyan Islim and Harald Haas. Modulation Techniques for LiFi. *ZTE Communications*, 2016.

[6] Wafa S. M. Elbasher, Amin B. A. Mustafa, and Ashraf A. Osman. A Comparison between Li-Fi, Wi-Fi, and Ethernet Standards. *International Journal of Science and Research*, 2016.

[7] S Chatterjee, S. Agarwal, and A. Nath. Scope and Challenges in Light Fidelity(LiFi) Technology in Wireless Data Communication. *International Journal of Innovative Research in Advanced Engineering*, 2015.

Appendix

MIXED SIGNAL MICROCONTROLLER

FEATURES

- Low Supply-Voltage Range: 1.8 V to 3.6 V
- Ultra-Low Power Consumption
  - Active Mode: 230 µA at 1 MHz, 2.2 V
  - Standby Mode: 0.5 µA
  - Off Mode (RAM Retention): 0.1 µA
- Five Power-Saving Modes
- Ultra-Fast Wake-Up From Standby Mode in Less Than 1 µs
- 16-Bit RISC Architecture, 62.5-ns Instruction Cycle Time
- Basic Clock Module Configurations
  - Internal Frequencies up to 16 MHz With Four Calibrated Frequency
  - Internal Very-Low-Power Low-Frequency (LF) Oscillator
  - 32-kHz Crystal
  - External Digital Clock Source
- Two 16-Bit Timer_A With Three Capture/Compare Registers
- Up to 24 Capacitive-Touch Enabled I/O Pins
- Universal Serial Communication Interface (USCI)
  - Enhanced UART Supporting Auto Baudrate Detection (LIN)
  - IrDA Encoder and Decoder
  - Synchronous SPI
  - I^2C™
- On-Chip Comparator for Analog Signal Compare Function or Slope Analog-to-Digital (A/D) Conversion
- 10-Bit 200-ksps Analog-to-Digital (A/D) Converter With Internal Reference, Sample-and-Hold, and Autoscan (See Table 1)
- Brownout Detector
- Serial Onboard Programming, No External Programming Voltage Needed, Programmable Code Protection by Security Fuse
- On-Chip Emulation Logic With Spy-Bi-Wire Interface
- Family Members are Summarized in Table 1
- Package Options
  - TSSOP: 20 Pin, 28 Pin
  - PDIP: 20 Pin
  - QFN: 32 Pin
- For Complete Module Descriptions, See the *MSP430x2xx Family User's Guide* (SLAU144)

DESCRIPTION

The Texas Instruments MSP430 family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 µs.

The MSP430G2x13 and MSP430G2x53 series are ultra-low-power mixed signal microcontrollers with built-in 16-bit timers, up to 24 I/O capacitive-touch enabled pins, a versatile analog comparator, and built-in communication capability using the universal serial communication interface. In addition the MSP430G2x53 family members have a 10-bit analog-to-digital (A/D) converter. For configuration details see Table 1.

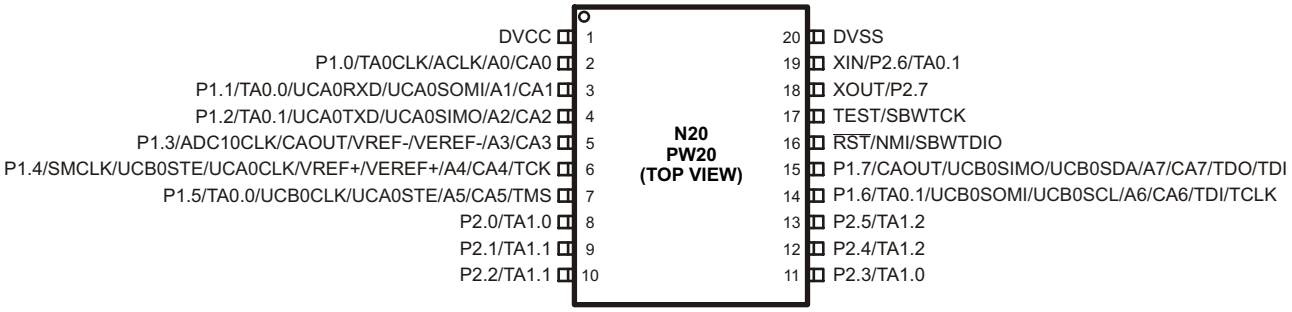
Typical applications include low-cost sensor systems that capture analog signals, convert them to digital values, and then process the data for display or for transmission to a host system.

Table 1. Available Options[1][2]

Device	BSL	EEM	Flash (KB)	RAM (B)	Timer_A	COMP_A+ Channel	ADC10 Channel	USCI_A0, USCI_B0	Clock	I/O	Package Type
MSP430G2553IRHB32	1	1	16	512	2x TA3	8	8	1	LF, DCO, VLO	24	32-QFN
MSP430G2553IPW28										24	28-TSSOP
MSP430G2553IPW20										16	20-TSSOP
MSP430G2553IN20										16	20-PDIP
MSP430G2453IRHB32	1	1	8	512	2x TA3	8	8	1	LF, DCO, VLO	24	32-QFN
MSP430G2453IPW28										24	28-TSSOP
MSP430G2453IPW20										16	20-TSSOP
MSP430G2453IN20										16	20-PDIP
MSP430G2353IRHB32	1	1	4	256	2x TA3	8	8	1	LF, DCO, VLO	24	32-QFN
MSP430G2353IPW28										24	28-TSSOP
MSP430G2353IPW20										16	20-TSSOP
MSP430G2353IN20										16	20-PDIP
MSP430G2253IRHB32	1	1	2	256	2x TA3	8	8	1	LF, DCO, VLO	24	32-QFN
MSP430G2253IPW28										24	28-TSSOP
MSP430G2253IPW20										16	20-TSSOP
MSP430G2253IN20										16	20-PDIP
MSP430G2153IRHB32	1	1	1	256	2x TA3	8	8	1	LF, DCO, VLO	24	32-QFN
MSP430G2153IPW28										24	28-TSSOP
MSP430G2153IPW20										16	20-TSSOP
MSP430G2153IN20										16	20-PDIP
MSP430G2513IRHB32	1	1	16	512	2x TA3	8	-	1	LF, DCO, VLO	24	32-QFN
MSP430G2513IPW28										24	28-TSSOP
MSP430G2513IPW20										16	20-TSSOP
MSP430G2513IN20										16	20-PDIP
MSP430G2413IRHB32	1	1	8	512	2x TA3	8	-	1	LF, DCO, VLO	24	32-QFN
MSP430G2413IPW28										24	28-TSSOP
MSP430G2413IPW20										16	20-TSSOP
MSP430G2413IN20										16	20-PDIP
MSP430G2313IRHB32	1	1	4	256	2x TA3	8	-	1	LF, DCO, VLO	24	32-QFN
MSP430G2313IPW28										24	28-TSSOP
MSP430G2313IPW20										16	20-TSSOP
MSP430G2313IN20										16	20-PDIP
MSP430G2213IRHB32	1	1	2	256	2x TA3	8	-	1	LF, DCO, VLO	24	32-QFN
MSP430G2213IPW28										24	28-TSSOP
MSP430G2213IPW20										16	20-TSSOP
MSP430G2213IN20										16	20-PDIP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

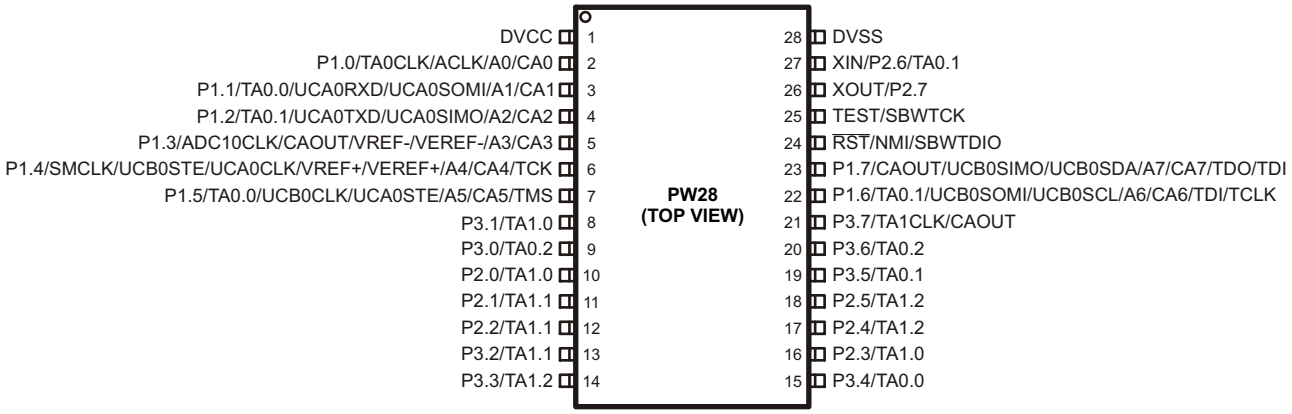
Device Pinout, MSP430G2x13 and MSP430G2x53, 20-Pin Devices, TSSOP and PDIP



NOTE: ADC10 is available on MSP430G2x53 devices only.

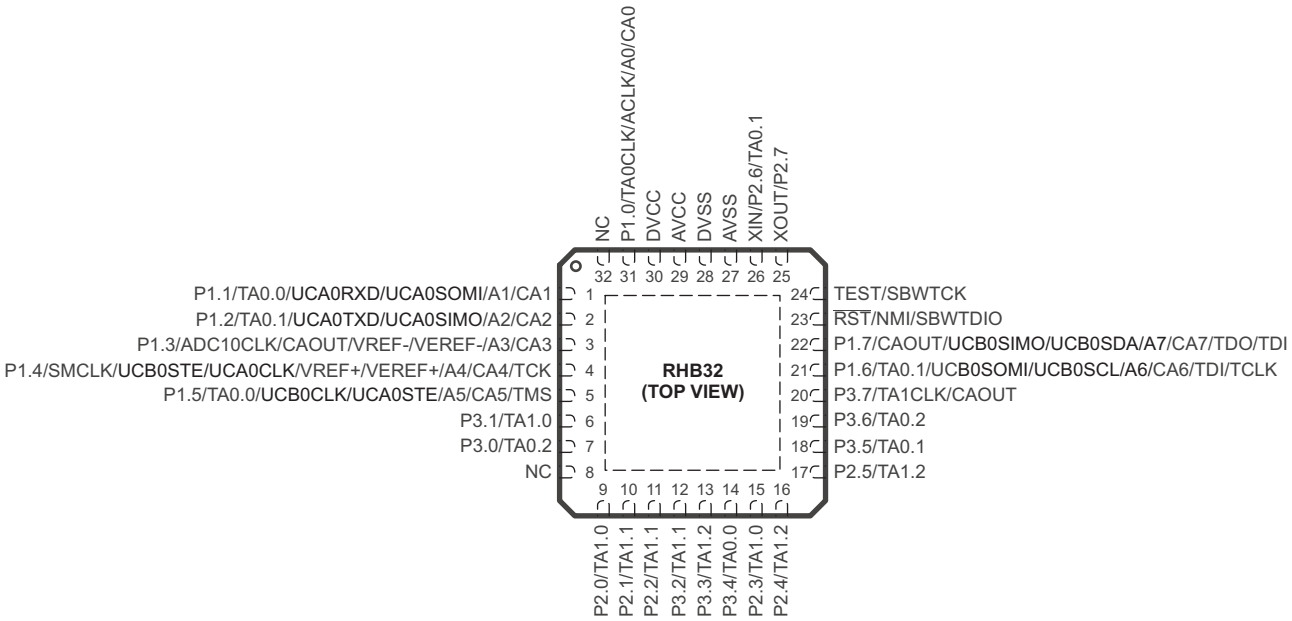
NOTE: The pulldown resistors of port P3 should be enabled by setting P3REN.x = 1.

Device Pinout, MSP430G2x13 and MSP430G2x53, 28-Pin Devices, TSSOP



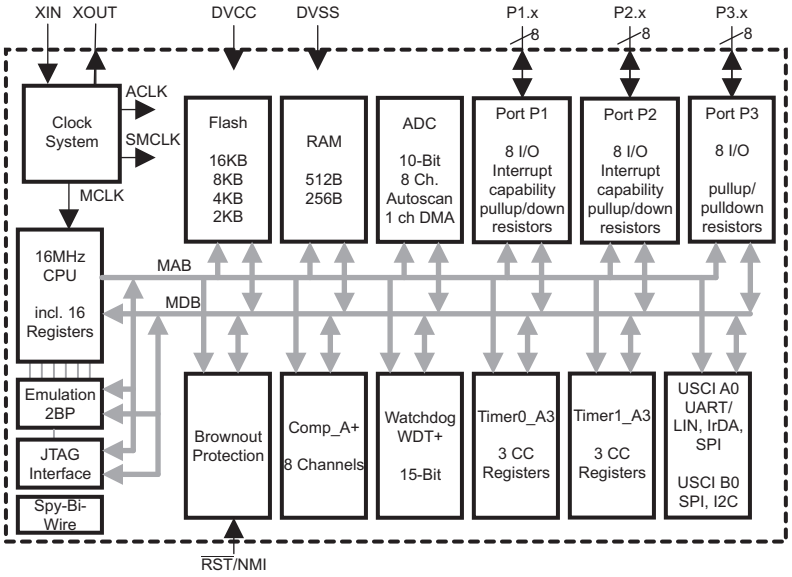
NOTE: ADC10 is available on MSP430G2x53 devices only.

Device Pinout, MSP430G2x13 and MSP430G2x53, 32-Pin Devices, QFN



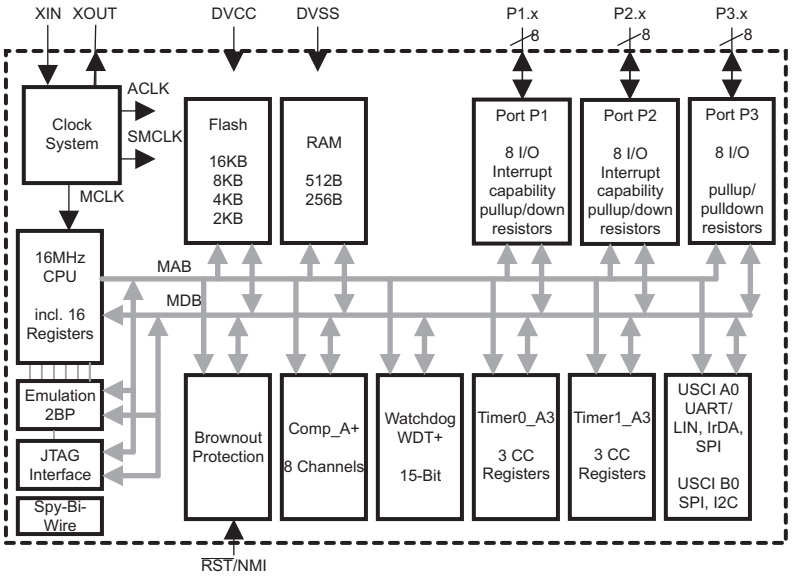
NOTE: ADC10 is available on MSP430G2x53 devices only.

Functional Block Diagram, MSP430G2x53



NOTE: Port P3 is available on 28-pin and 32-pin devices only.

Functional Block Diagram, MSP430G2x13



NOTE: Port P3 is available on 28-pin and 32-pin devices only.

Table 2. Terminal Functions

TERMINAL				I/O	DESCRIPTION
NAME	NO.				
	PW20, N20	PW28	RHB32		
P1.0/ TA0CLK/ ACLK/ A0 CA0	2	2	31	I/O	General-purpose digital I/O pin Timer0_A, clock signal TACLK input ACLK signal output ADC10 analog input A0 (1) Comparator_A+, CA0 input
P1.1/ TA0.0/ UCA0RXD/ UCA0SOMI/ A1/ CA1	3	3	1	I/O	General-purpose digital I/O pin Timer0_A, capture: CCI0A input, compare: Out0 output / BSL transmit USCI_A0 UART mode: receive data input USCI_A0 SPI mode: slave data out/master in ADC10 analog input A1 (1) Comparator_A+, CA1 input
P1.2/ TA0.1/ UCA0TXD/ UCA0SIMO/ A2/ CA2	4	4	2	I/O	General-purpose digital I/O pin Timer0_A, capture: CCI1A input, compare: Out1 output USCI_A0 UART mode: transmit data output USCI_A0 SPI mode: slave data in/master out ADC10 analog input A2 (1) Comparator_A+, CA2 input
P1.3/ ADC10CLK/ A3/ VREF-/VEREF-/ CA3/ CAOUT	5	5	3	I/O	General-purpose digital I/O pin ADC10, conversion clock output (1) ADC10 analog input A3 (1) ADC10 negative reference voltage (1) Comparator_A+, CA3 input Comparator_A+, output
P1.4/ SMCLK/ UCB0STE/ UCA0CLK/ A4/ VREF+/VEREF+/ CA4/ TCK	6	6	4	I/O	General-purpose digital I/O pin SMCLK signal output USCI_B0 slave transmit enable USCI_A0 clock input/output ADC10 analog input A4 (1) ADC10 positive reference voltage (1) Comparator_A+, CA4 input JTAG test clock, input terminal for device programming and test
P1.5/ TA0.0/ UCB0CLK/ UCA0STE/ A5/ CA5/ TMS	7	7	5	I/O	General-purpose digital I/O pin Timer0_A, compare: Out0 output / BSL receive USCI_B0 clock input/output USCI_A0 slave transmit enable ADC10 analog input A5 (1) Comparator_A+, CA5 input JTAG test mode select, input terminal for device programming and test

(1) MSP430G2x53 devices only

Table 2. Terminal Functions (continued)

TERMINAL				I/O	DESCRIPTION
NAME	NO.				
	PW20, N20	PW28	RHB32		
P1.6/ TA0.1/ A6/ CA6/ UCB0SOMI/ UCB0SCL/ TDI/TCLK	14	22	21	I/O	General-purpose digital I/O pin Timer0_A, compare: Out1 output ADC10 analog input A6 (1) Comparator_A+, CA6 input USCI_B0 SPI mode: slave out master in USCI_B0 I2C mode: SCL I2C clock JTAG test data input or test clock input during programming and test
P1.7/ A7/ CA7/ CAOUT/ UCB0SIMO/ UCB0SDA/ TDO/TDI	15	23	22	I/O	General-purpose digital I/O pin ADC10 analog input A7 (1) Comparator_A+, CA7 input Comparator_A+, output USCI_B0 SPI mode: slave in master out USCI_B0 I2C mode: SDA I2C data JTAG test data output terminal or test data input during programming and test (2)
P2.0/ TA1.0	8	10	9	I/O	General-purpose digital I/O pin Timer1_A, capture: CCI0A input, compare: Out0 output
P2.1/ TA1.1	9	11	10	I/O	General-purpose digital I/O pin Timer1_A, capture: CCI1A input, compare: Out1 output
P2.2/ TA1.1	10	12	11	I/O	General-purpose digital I/O pin Timer1_A, capture: CCI1B input, compare: Out1 output
P2.3/ TA1.0	11	16	15	I/O	General-purpose digital I/O pin Timer1_A, capture: CCI0B input, compare: Out0 output
P2.4/ TA1.2	12	17	16	I/O	General-purpose digital I/O pin Timer1_A, capture: CCI2A input, compare: Out2 output
P2.5/ TA1.2	13	18	17	I/O	General-purpose digital I/O pin Timer1_A, capture: CCI2B input, compare: Out2 output
XIN/ P2.6/ TA0.1	19	27	26	I/O	Input terminal of crystal oscillator General-purpose digital I/O pin Timer0_A, compare: Out1 output
XOUT/ P2.7	18	26	25	I/O	Output terminal of crystal oscillator (3) General-purpose digital I/O pin
P3.0/ TA0.2	-	9	7	I/O	General-purpose digital I/O pin Timer0_A, capture: CCI2A input, compare: Out2 output
P3.1/ TA1.0	-	8	6	I/O	General-purpose digital I/O pin Timer1_A, compare: Out0 output
P3.2/ TA1.1	-	13	12	I/O	General-purpose digital I/O pin Timer1_A, compare: Out1 output
P3.3/ TA1.2	-	14	13	I/O	General-purpose digital I/O Timer1_A, compare: Out2 output
P3.4/ TA0.0	-	15	14	I/O	General-purpose digital I/O Timer0_A, compare: Out0 output

(2) TDO or TDI is selected via JTAG instruction.
(3) If XOUT/P2.7 is used as an input, excess current flows until P2SEL.7 is cleared. This is due to the oscillator output driver connection to this pad after reset.

Table 2. Terminal Functions (continued)

TERMINAL				I/O	DESCRIPTION
NAME	NO.				
	PW20, N20	PW28	RHB32		
P3.5/ TA0.1	-	19	18	I/O	General-purpose digital I/O Timer0_A, compare: Out1 output
P3.6/ TA0.2	-	20	19	I/O	General-purpose digital I/O Timer0_A, compare: Out2 output
P3.7/ TA1CLK/ CAOUT	-	21	20	I/O	General-purpose digital I/O Timer1_A, clock signal TACLK input Comparator_A+, output
$\overline{\text{RST}}$/ NMI/ SBWTDIO	16	24	23	I	Reset Nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test
TEST/ SBWTCK	17	25	24	I	Selects test mode for JTAG pins on Port 1. The device protection fuse is connected to TEST. Spy-Bi-Wire test clock input during programming and test
AVCC	NA	NA	29	NA	Analog supply voltage
DVCC	1	1	30	NA	Digital supply voltage
DVSS	20	28	27, 28	NA	Ground reference
NC	NA	NA	8, 32	NA	Not connected
QFN Pad	NA	NA	Pad	NA	QFN package pad. Connection to VSS is recommended.

SHORT-FORM DESCRIPTION

CPU

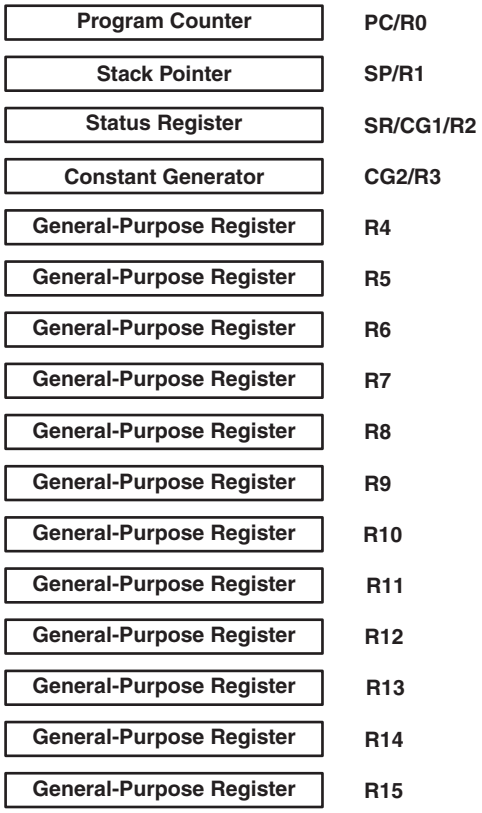
The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.



Instruction Set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 3 shows examples of the three types of instruction formats; Table 4 shows the address modes.

Table 3. Instruction Word Formats

INSTRUCTION FORMAT	EXAMPLE	OPERATION
Dual operands, source-destination	ADD R4,R5	R4 + R5 ---> R5
Single operands, destination only	CALL R8	PC -->(TOS), R8--> PC
Relative jump, un/conditional	JNE	Jump-on-equal bit = 0

Table 4. Address Mode Descriptions(1)

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	✓	✓	MOV Rs,Rd	MOV R10,R11	R10 -- --> R11
Indexed	✓	✓	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5) -- --> M(6+R6)
Symbolic (PC relative)	✓	✓	MOV EDE,TONI		M(EDE) -- --> M(TONI)
Absolute	✓	✓	MOV &MEM,&TCDAT		M(MEM) -- --> M(TCDAT)
Indirect	✓		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) -- --> M(Tab+R6)
Indirect autoincrement	✓		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) -- --> R11 R10 + 2-- --> R10
Immediate	✓		MOV #X,TONI	MOV #45,TONI	#45 -- --> M(TONI)

(1) S = source, D = destination

Operating Modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
  - DCO's dc generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc generator is disabled
  - Crystal oscillator is stopped

Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are located in the address range 0FFFFh to 0FFC0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0FFFEh) contains 0FFFFh (for example, flash is not programmed), the CPU goes into LPM4 immediately after power-up.

Table 5. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-Up External Reset Watchdog Timer+ Flash key violation PC out-of-range(1)	PORIFG RSTIFG WDTIFG KEYV(2)	Reset	0FFFEh	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG(2)(3)	(non)-maskable (non)-maskable (non)-maskable	0FFFCh	30
Timer1_A3	TA1CCR0 CCIFG(4)	maskable	0FFFAh	29
Timer1_A3	TA1CCR2 TA1CCR1 CCIFG, TAIFG(2)(4)	maskable	0FFF8h	28
Comparator_A+	CAIFG(4)	maskable	0FFF6h	27
Watchdog Timer+	WDTIFG	maskable	0FFF4h	26
Timer0_A3	TA0CCR0 CCIFG(4)	maskable	0FFF2h	25
Timer0_A3	TA0CCR2 TA0CCR1 CCIFG, TAIFG (5)(4)	maskable	0FFF0h	24
USCI_A0/USCI_B0 receive USCI_B0 I2C status	UCA0RXIFG, UCB0RXIFG(2)(5)	maskable	0FFEEh	23
USCI_A0/USCI_B0 transmit USCI_B0 I2C receive/transmit	UCA0TXIFG, UCB0TXIFG(2)(6)	maskable	0FFECh	22
ADC10 (MSP430G2x53 only)	ADC10IFG(4)	maskable	0FFEAh	21
			0FFE8h	20
I/O Port P2 (up to eight flags)	P2IFG.0 to P2IFG.7(2)(4)	maskable	0FFE6h	19
I/O Port P1 (up to eight flags)	P1IFG.0 to P1IFG.7(2)(4)	maskable	0FFE4h	18
			0FFE2h	17
			0FFE0h	16
See (7)			0FFDEh	15
See (8)			0FFDEh to 0FFC0h	14 to 0, lowest

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address ranges.
(2) Multiple source flags
(3) (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.
(4) Interrupt flags are located in the module.
(5) In SPI mode: UCB0RXIFG. In I2C mode: UCALIFG, UCNACKIFG, ICSTTIFG, UCSTPIFG.
(6) In UART or SPI mode: UCB0TXIFG. In I2C mode: UCB0RXIFG, UCB0TXIFG.
(7) This location is used as bootstrap loader security key (BSLSKEY). A 0xAA55 at this location disables the BSL completely. A zero (0h) disables the erasure of the flash if an invalid password is supplied.
(8) The interrupt vectors at addresses 0FFDEh to 0FFC0h are not used in this device and can be used for regular program code if necessary.

Special Function Registers (SFRs)

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

Legend		
	rw:	Bit can be read and written.
	rw-0,1:	Bit can be read and written. It is reset or set by PUC.
	rw-(0,1):	Bit can be read and written. It is reset or set by POR.
		SFR bit is not present in device.

Table 6. Interrupt Enable Register 1 and 2

Address	7	6	5	4	3	2	1	0
00h			**ACCVIE**	**NMIIE**			**OFIE**	**WDTIE**
			rw-0	rw-0			rw-0	rw-0

WDTIE	Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode.
OFIE	Oscillator fault interrupt enable
NMIIE	(Non)maskable interrupt enable
ACCVIE	Flash access violation interrupt enable

Address	7	6	5	4	3	2	1	0
01h					**UCB0TXIE**	**UCB0RXIE**	**UCA0TXIE**	**UCA0RXIE**
					rw-0	rw-0	rw-0	rw-0

UCA0RXIE	USCI_A0 receive interrupt enable
UCA0TXIE	USCI_A0 transmit interrupt enable
UCB0RXIE	USCI_B0 receive interrupt enable
UCB0TXIE	USCI_B0 transmit interrupt enable

Table 7. Interrupt Flag Register 1 and 2

Address	7	6	5	4	3	2	1	0
02h				**NMIIFG**	**RSTIFG**	**PORIFG**	**OFIFG**	**WDTIFG**
				rw-0	rw-(0)	rw-(1)	rw-1	rw-(0)

WDTIFG	Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on V_{CC} power-on or a reset condition at the $\overline{RST}$/NMI pin in reset mode.
OFIFG	Flag set on oscillator fault.
PORIFG	Power-On Reset interrupt flag. Set on V_{CC} power-up.
RSTIFG	External reset interrupt flag. Set on a reset condition at $\overline{RST}$/NMI pin in reset mode. Reset on V_{CC} power-up.
NMIIFG	Set via $\overline{RST}$/NMI pin

Address	7	6	5	4	3	2	1	0
03h					**UCB0TXIFG**	**UCB0RXIFG**	**UCA0TXIFG**	**UCA0RXIFG**
					rw-1	rw-0	rw-1	rw-0

UCA0RXIFG	USCI_A0 receive interrupt flag
UCA0TXIFG	USCI_A0 transmit interrupt flag
UCB0RXIFG	USCI_B0 receive interrupt flag
UCB0TXIFG	USCI_B0 transmit interrupt flag

Memory Organization

Table 8. Memory Organization

		MSP430G2153	MSP430G2253 MSP430G2213	MSP430G2353 MSP430G2313	MSP430G2453 MSP430G2413	MSP430G2553 MSP430G2513
Memory	Size	1kB	2kB	4kB	8kB	16kB
Main: interrupt vector	Flash	0xFFFF to 0xFFC0	0xFFFF to 0xFFC0	0xFFFF to 0xFFC0	0xFFFF to 0xFFC0	0xFFFF to 0xFFC0
Main: code memory	Flash	0xFFFF to 0xFC00	0xFFFF to 0xF800	0xFFFF to 0xF000	0xFFFF to 0xE000	0xFFFF to 0xC000
Information memory	Size	256 Byte	256 Byte	256 Byte	256 Byte	256 Byte
	Flash	010FFh to 01000h	010FFh to 01000h	010FFh to 01000h	010FFh to 01000h	010FFh to 01000h
RAM	Size	256 Byte	256 Byte	256 Byte	512 Byte	512 Byte
		0x02FF to 0x0200	0x02FF to 0x0200	0x02FF to 0x0200	0x03FF to 0x0200	0x03FF to 0x0200
Peripherals	16-bit	01FFh to 0100h	01FFh to 0100h	01FFh to 0100h	01FFh to 0100h	01FFh to 0100h
	8-bit	0FFh to 010h	0FFh to 010h	0FFh to 010h	0FFh to 010h	0FFh to 010h
	8-bit SFR	0Fh to 00h	0Fh to 00h	0Fh to 00h	0Fh to 00h	0Fh to 00h

Bootstrap Loader (BSL)

The MSP430 BSL enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the *MSP430 Programming Via the Bootstrap Loader User's Guide* (SLAU319).

Table 9. BSL Function Pins

BSL FUNCTION	20-PIN PW PACKAGE 20-PIN N PACKAGE	28-PIN PACKAGE PW	32-PIN PACKAGE RHB
Data transmit	3 - P1.1	3 - P1.1	1 - P1.1
Data receive	7 - P1.5	7 - P1.5	5 - P1.5

Flash Memory

The flash memory can be programmed via the Spy-Bi-Wire/JTAG port or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually or as a group with segments 0 to n. Segments A to D are also called *information memory*.
- Segment A contains calibration data. After reset segment A is protected against programming and erasing. It can be unlocked but care should be taken not to erase this segment if the device-specific calibration data is required.

Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x2xx Family User's Guide* (SLAU144).

Oscillator and System Clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power low-frequency oscillator and an internal digitally controlled oscillator (DCO). The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 µs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced either from a 32768-Hz watch crystal or the internal LF oscillator.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

The DCO settings to calibrate the DCO output frequency are stored in the information memory segment A.

Main DCO Characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter S_{DCO}.
- Modulation control bits MODx select how often $f_{DCO(RSEL,DCO+1)}$ is used within the period of 32 DCOCLK cycles. The frequency $f_{DCO(RSEL,DCO)}$ is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{DCO(RSEL,DCO)} \times f_{DCO(RSEL,DCO+1)}}{MOD \times f_{DCO(RSEL,DCO)} + (32 - MOD) \times f_{DCO(RSEL,DCO+1)}}$$

Calibration Data Stored in Information Memory Segment A

Calibration data is stored for both the DCO and for ADC10 organized in a tag-length-value structure.

Table 10. Tags Used by the ADC Calibration Tags

NAME	ADDRESS	VALUE	DESCRIPTION
TAG_DCO_30	0x10F6	0x01	DCO frequency calibration at V_{CC} = 3 V and T_A = 30°C at calibration
TAG_ADC10_1	0x10DA	0x10	ADC10_1 calibration tag
TAG_EMPTY	-	0xFE	Identifier for empty memory areas

Table 11. Labels Used by the ADC Calibration Tags

LABEL	ADDRESS OFFSET	SIZE	CONDITION AT CALIBRATION AND DESCRIPTION
CAL_ADC_25T85	0x0010	word	INCHx = 0x1010, REF2_5 = 1, T_A = 85°C
CAL_ADC_25T30	0x000E	word	INCHx = 0x1010, REF2_5 = 1, T_A = 30°C
CAL_ADC_25VREF_FACTOR	0x000C	word	REF2_5 = 1, T_A = 30°C, I_{VREF+} = 1 mA
CAL_ADC_15T85	0x000A	word	INCHx = 0x1010, REF2_5 = 0, T_A = 85°C
CAL_ADC_15T30	0x0008	word	INCHx = 0x1010, REF2_5 = 0, T_A = 30°C
CAL_ADC_15VREF_FACTOR	0x0006	word	REF2_5 = 0, T_A = 30°C, I_{VREF+} = 0.5 mA
CAL_ADC_OFFSET	0x0004	word	External VREF = 1.5 V, $f_{ADC10CLK}$ = 5 MHz
CAL_ADC_GAIN_FACTOR	0x0002	word	External VREF = 1.5 V, $f_{ADC10CLK}$ = 5 MHz
CAL_BC1_1MHZ	0x0009	byte	-
CAL_DCO_1MHZ	0x0008	byte	-
CAL_BC1_8MHZ	0x0007	byte	-
CAL_DCO_8MHZ	0x0006	byte	-
CAL_BC1_12MHZ	0x0005	byte	-
CAL_DCO_12MHZ	0x0004	byte	-
CAL_BC1_16MHZ	0x0003	byte	-
CAL_DCO_16MHZ	0x0002	byte	-

Brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

Digital I/O

Up to three 8-bit I/O ports are implemented:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition (port P1 and port P2 only) is possible.
- Edge-selectable interrupt input capability for all bits of port P1 and port P2 (if available).
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup or pulldown resistor.
- Each I/O has an individually programmable pin oscillator enable bit to enable low-cost capacitive touch detection.

Watchdog Timer (WDT+)

The primary function of the watchdog timer (WDT+) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

Timer_A3 (TA0, TA1)

Timer0/1_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 12. Timer0_A3 Signal Connections

INPUT PIN NUMBER			DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER		
PW20, N20	PW28	RHB32					PW20, N20	PW28	RHB32
P1.0-2	P1.0-2	P1.0-31	TACLK	TACLK	Timer	NA			
			ACLK	ACLK					
			SMCLK	SMCLK					
PinOsc	PinOsc	PinOsc	TACLK	INCLK					
P1.1-3	P1.1-3	P1.1-1	TA0.0	CCI0A	CCR0	TA0	P1.1-3	P1.1-3	P1.1-1
			ACLK	CCI0B			P1.5-7	P1.5-7	P1.5-5
			V_{SS}	GND				P3.4-15	P3.4-14
			V_{CC}	V_{CC}					
P1.2-4	P1.2-4	P1.2-2	TA0.1	CCI1A	CCR1	TA1	P1.2-4	P1.2-4	P1.2-2
			CAOUT	CCI1B			P1.6-14	P1.6-22	P1.6-21
			V_{SS}	GND			P2.6-19	P2.6-27	P2.6-26
			V_{CC}	V_{CC}				P3.5-19	P3.5-18
	P3.0-9	P3.0-7	TA0.2	CCI2A	CCR2	TA2		P3.0-9	P3.0-7
PinOsc	PinOsc	PinOsc	TA0.2	CCI2B				P3.6-20	P3.6-19
			V_{SS}	GND					
			V_{CC}	V_{CC}					

Table 13. Timer1_A3 Signal Connections

INPUT PIN NUMBER			DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER		
PW20, N20	PW28	RHB32					PW20, N20	PW28	RHB32
-	P3.7-21	P3.7-20	TACLK	TACLK	Timer	NA			
			ACLK	ACLK					
			SMCLK	SMCLK					
-	P3.7-21	P3.7-20	TACLK	INCLK					
P2.0-8	P2.0-10	P2.0-9	TA1.0	CCI0A	CCR0	TA0	P2.0-8	P2.0-10	P2.0-9
P2.3-11	P2.3-16	P2.3-12	TA1.0	CCI0B			P2.3-11	P2.3-16	P2.3-15
			V_{SS}	GND				P3.1-8	P3.1-6
			V_{CC}	V_{CC}					
P2.1-9	P2.1-11	P2.1-10	TA1.1	CCI1A	CCR1	TA1	P2.1-9	P2.1-11	P2.1-10
P2.2-10	P2.2-12	P2.2-11	TA1.1	CCI1B			P2.2-10	P2.2-12	P2.2-11
			V_{SS}	GND				P3.2-13	P3.2-12
			V_{CC}	V_{CC}					
P2.4-12	P2.4-17	P2.4-16	TA1.2	CCI2A	CCR2	TA2	P2.4-12	P2.4-17	P2.4-16
P2.5-13	P2.5-18	P2.5-17	TA1.2	CCI2B			P2.5-13	P2.5-18	P2.5-17
			V_{SS}	GND				P3.3-14	P3.3-13
			V_{CC}	V_{CC}					

Universal Serial Communications Interface (USCI)

The USCI module is used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3 or 4 pin) and I2C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection (LIN), and IrDA. Not all packages support the USCI functionality.

USCI_A0 provides support for SPI (3 or 4 pin), UART, enhanced UART, and IrDA.

USCI_B0 provides support for SPI (3 or 4 pin) and I2C.

Comparator_A+

The primary function of the comparator_A+ module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

ADC10 (MSP430G2x53 Only)

The ADC10 module supports fast 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator, and data transfer controller (DTC) for automatic conversion result handling, allowing ADC samples to be converted and stored without any CPU intervention.

Peripheral File Map

Table 14. Peripherals With Word Access

MODULE	REGISTER DESCRIPTION	REGISTER NAME	OFFSET
ADC10 (MSP430G2x53 devices only)	ADC data transfer start address	ADC10SA	1BCh
	ADC memory	ADC10MEM	1B4h
	ADC control register 1	ADC10CTL1	1B2h
	ADC control register 0	ADC10CTL0	1B0h
Timer1_A3	Capture/compare register	TA1CCR2	0196h
	Capture/compare register	TA1CCR1	0194h
	Capture/compare register	TA1CCR0	0192h
	Timer_A register	TA1R	0190h
	Capture/compare control	TA1CCTL2	0186h
	Capture/compare control	TA1CCTL1	0184h
	Capture/compare control	TA1CCTL0	0182h
	Timer_A control	TA1CTL	0180h
	Timer_A interrupt vector	TA1IV	011Eh
Timer0_A3	Capture/compare register	TA0CCR2	0176h
	Capture/compare register	TA0CCR1	0174h
	Capture/compare register	TA0CCR0	0172h
	Timer_A register	TA0R	0170h
	Capture/compare control	TA0CCTL2	0166h
	Capture/compare control	TA0CCTL1	0164h
	Capture/compare control	TA0CCTL0	0162h
	Timer_A control	TA0CTL	0160h
	Timer_A interrupt vector	TA0IV	012Eh
Flash Memory	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
Watchdog Timer+	Watchdog/timer control	WDTCTL	0120h

Table 15. Peripherals With Byte Access

MODULE	REGISTER DESCRIPTION	REGISTER NAME	OFFSET
USCI_B0	USCI_B0 transmit buffer	UCB0TXBUF	06Fh
	USCI_B0 receive buffer	UCB0RXBUF	06Eh
	USCI_B0 status	UCB0STAT	06Dh
	USCI B0 I2C Interrupt enable	UCB0CIE	06Ch
	USCI_B0 bit rate control 1	UCB0BR1	06Bh
	USCI_B0 bit rate control 0	UCB0BR0	06Ah
	USCI_B0 control 1	UCB0CTL1	069h
	USCI_B0 control 0	UCB0CTL0	068h
	USCI_B0 I2C slave address	UCB0SA	011Ah
	USCI_B0 I2C own address	UCB0OA	0118h
USCI_A0	USCI_A0 transmit buffer	UCA0TXBUF	067h
	USCI_A0 receive buffer	UCA0RXBUF	066h
	USCI_A0 status	UCA0STAT	065h
	USCI_A0 modulation control	UCA0MCTL	064h
	USCI_A0 baud rate control 1	UCA0BR1	063h
	USCI_A0 baud rate control 0	UCA0BR0	062h
	USCI_A0 control 1	UCA0CTL1	061h
	USCI_A0 control 0	UCA0CTL0	060h
	USCI_A0 IrDA receive control	UCA0IRRCTL	05Fh
	USCI_A0 IrDA transmit control	UCA0IRTCTL	05Eh
	USCI_A0 auto baud rate control	UCA0ABCTL	05Dh
ADC10 (MSP430G2x53 devices only)	ADC analog enable 0	ADC10AE0	04Ah
	ADC analog enable 1	ADC10AE1	04Bh
	ADC data transfer control register 1	ADC10DTC1	049h
	ADC data transfer control register 0	ADC10DTC0	048h
Comparator_A+	Comparator_A+ port disable	CAPD	05Bh
	Comparator_A+ control 2	CACTL2	05Ah
	Comparator_A+ control 1	CACTL1	059h
Basic Clock System+	Basic clock system control 3	BCSCTL3	053h
	Basic clock system control 2	BCSCTL2	058h
	Basic clock system control 1	BCSCTL1	057h
	DCO clock frequency control	DCOCTL	056h
Port P3 (28-pin PW and 32-pin RHB only)	Port P3 selection 2. pin	P3SEL2	043h
	Port P3 resistor enable	P3REN	010h
	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h
Port P2	Port P2 selection 2	P2SEL2	042h
	Port P2 resistor enable	P2REN	02Fh
	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h

Table 15. Peripherals With Byte Access (continued)

MODULE	REGISTER DESCRIPTION	REGISTER NAME	OFFSET
Port P1	Port P1 selection 2	P1SEL2	041h
	Port P1 resistor enable	P1REN	027h
	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special Function	SFR interrupt flag 2	IFG2	003h
	SFR interrupt flag 1	IFG1	002h
	SFR interrupt enable 2	IE2	001h
	SFR interrupt enable 1	IE1	000h

Absolute Maximum Ratings(1)

Voltage applied at V_{CC} to V_{SS}		–0.3 V to 4.1 V
Voltage applied to any pin(2)		–0.3 V to V_{CC} + 0.3 V
Diode current at any device pin		±2 mA
Storage temperature range, T_{stg} (3)	Unprogrammed device	–55°C to 150°C
	Programmed device	–55°C to 150°C

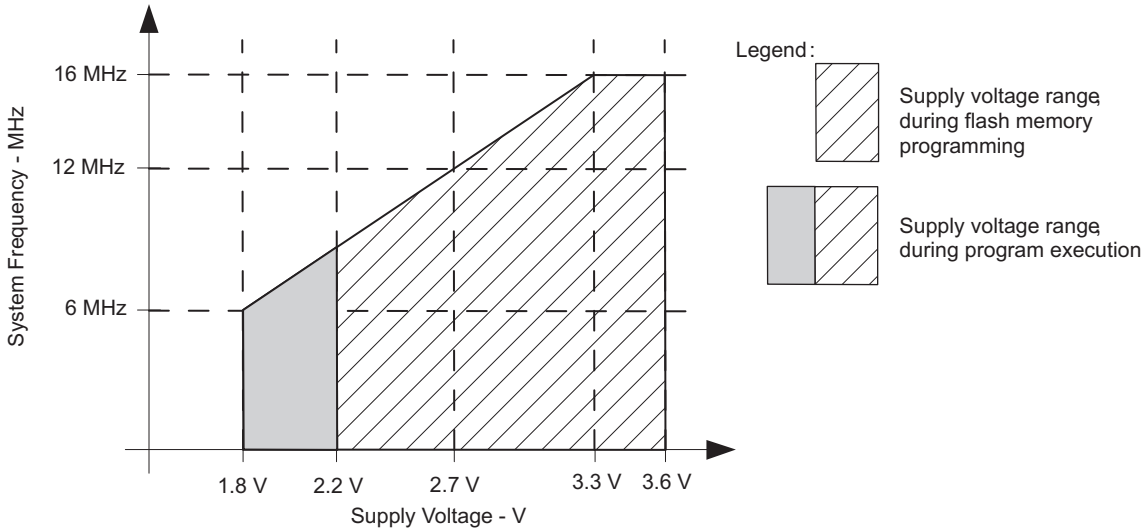
(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.
(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

Recommended Operating Conditions

Typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	During program execution	1.8		3.6	V
		During flash programming or erase	2.2		3.6	
V_{SS}	Supply voltage			0		V
T_A	Operating free-air temperature	I version	–40		85	°C
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)(1)(2)	V_{CC} = 1.8 V, Duty cycle = 50% ± 10%	dc		6	MHz
		V_{CC} = 2.7 V, Duty cycle = 50% ± 10%	dc		12	
		V_{CC} = 3.3 V, Duty cycle = 50% ± 10%	dc		16	

(1) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse duration of the specified maximum frequency.
(2) Modules might have a different maximum input clock specification. See the specification of the respective module in this data sheet.



Note: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

Figure 1. Safe Operating Area

Electrical Characteristics

Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{AM,1MHz}$	Active mode (AM) current at 1 MHz	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1 MHz, f_{ACLK} = 0 Hz, Program executes in flash, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		230		µA
				3 V		330	420	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.

Typical Characteristics, Active Mode Supply Current (Into V_{CC})

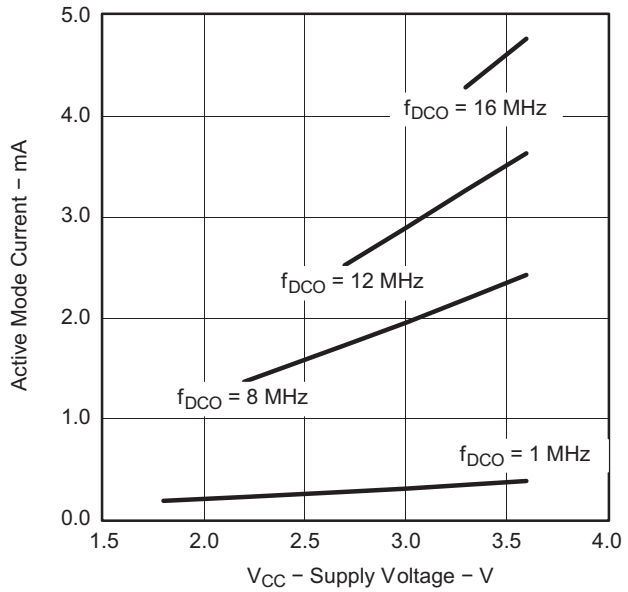


Figure 2. Active Mode Current vs V_{CC}, T_A = 25°C

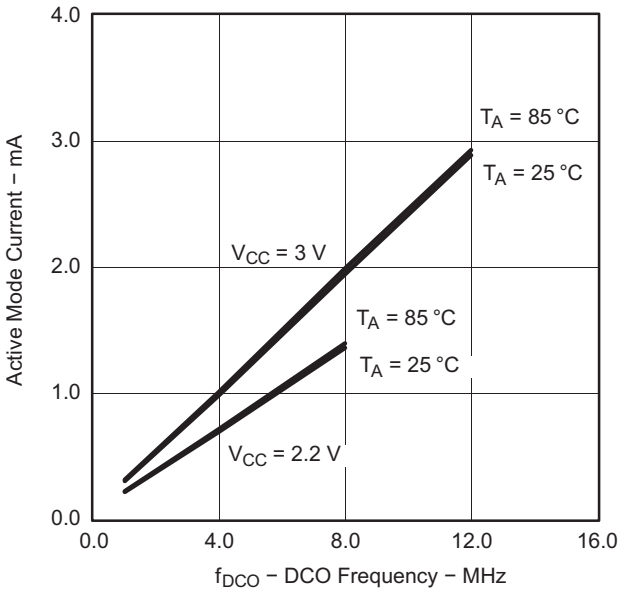


Figure 3. Active Mode Current vs DCO Frequency

Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{LPM0,1MHz}$	Low-power mode 0 (LPM0) current(3)	f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz, f_{ACLK} = 32768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0	25°C	2.2 V		56		µA
I_{LPM2}	Low-power mode 2 (LPM2) current(4)	f_{MCLK} = f_{SMCLK} = 0 MHz, f_{DCO} = 1 MHz, f_{ACLK} = 32768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	25°C	2.2 V		22		µA
$I_{LPM3,LFXT1}$	Low-power mode 3 (LPM3) current(4)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 32768 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	25°C	2.2 V		0.7	1.5	µA
$I_{LPM3,VLO}$	Low-power mode 3 current, (LPM3)(4)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	25°C	2.2 V		0.5	0.7	µA
I_{LPM4}	Low-power mode 4 (LPM4) current(5)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 0 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	25°C	2.2 V		0.1	0.5	µA
			85°C			0.8	1.7	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.
(3) Current for brownout and WDT clocked by SMCLK included.
(4) Current for brownout and WDT clocked by ACLK included.
(5) Current for brownout included.

Typical Characteristics, Low-Power Mode Supply Currents

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

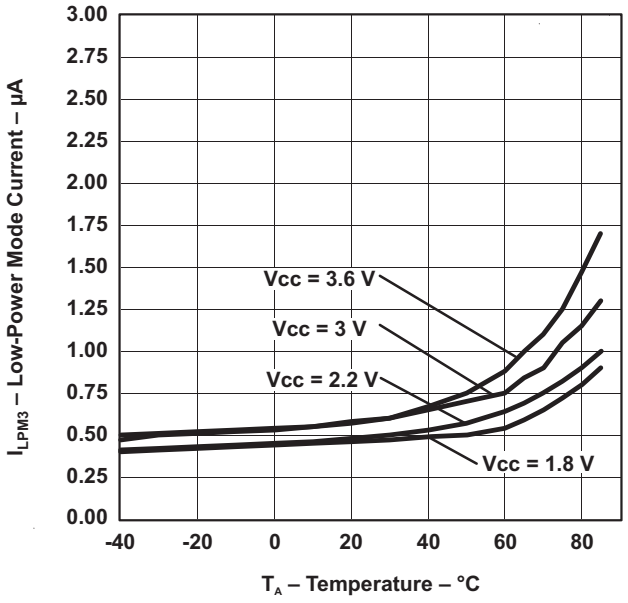


Figure 4. LPM3 Current vs Temperature

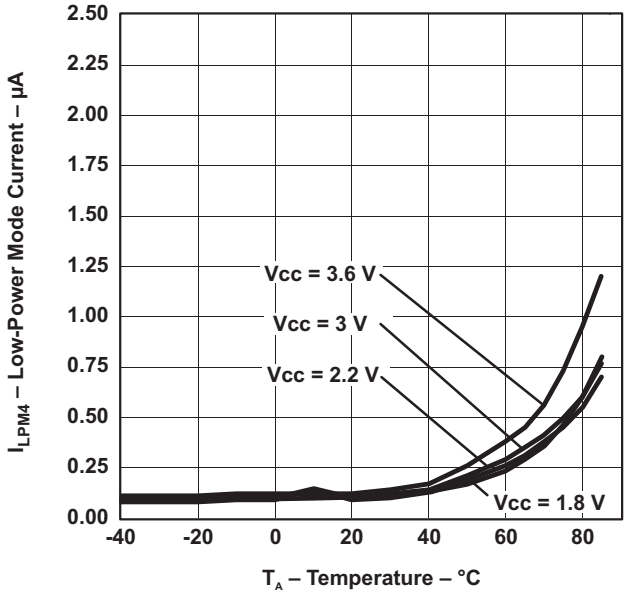


Figure 5. LPM4 Current vs Temperature

Schmitt-Trigger Inputs, Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage			0.45 V_{CC}		0.75 V_{CC}	V
			3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage			0.25 V_{CC}		0.55 V_{CC}	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)		3 V	0.3		1	V
R_{Pull}	Pullup/pulldown resistor	For pullup: $V_{IN} = V_{SS}$ For pulldown: $V_{IN} = V_{CC}$	3 V	20	35	50	kΩ
C_I	Input capacitance	$V_{IN} = V_{SS}$ or V_{CC}			5		pF

Leakage Current, Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$I_{lkg(Px.y)}$	High-impedance leakage current	(1) (2)	3 V		±50	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

Outputs, Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –6 mA(1)	3 V		V_{CC} – 0.3		V
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 6 mA(1)	3 V		V_{SS} + 0.3		V

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.

Output Frequency, Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	Px.y, C_L = 20 pF, R_L = 1 kΩ(1) (2)	3 V		12		MHz
f_{Port_CLK}	Clock output frequency	Px.y, C_L = 20 pF(2)	3 V		16		MHz

(1) A resistive divider with two 0.5-kΩ resistors between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

Typical Characteristics, Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

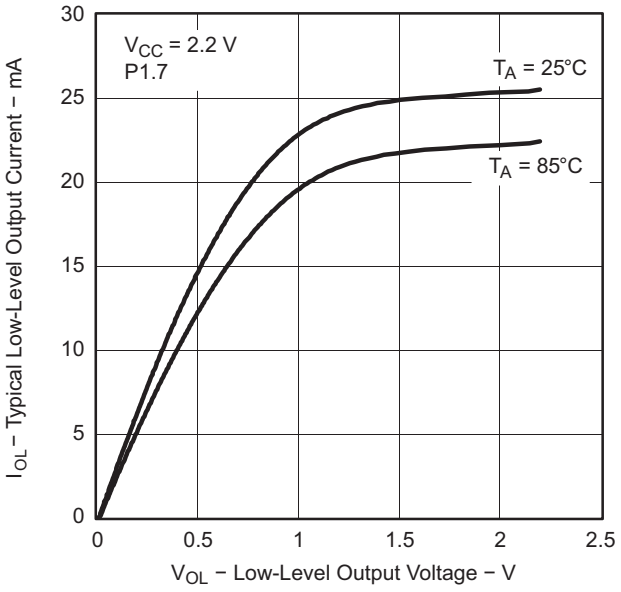


Figure 6.

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

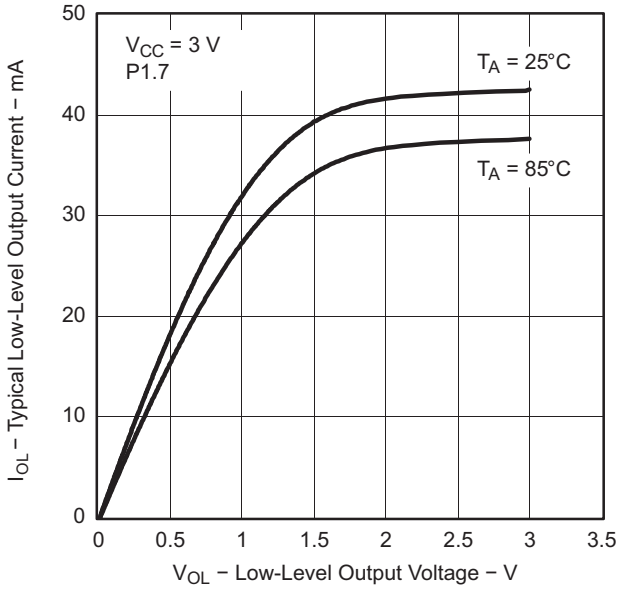


Figure 7.

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

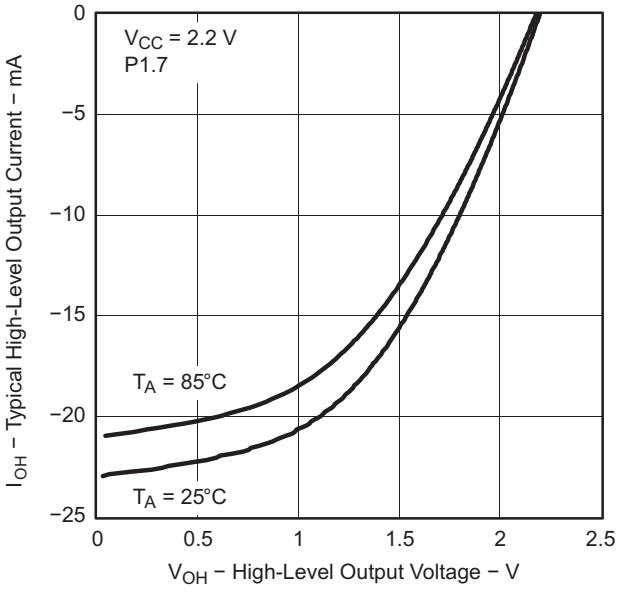


Figure 8.

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

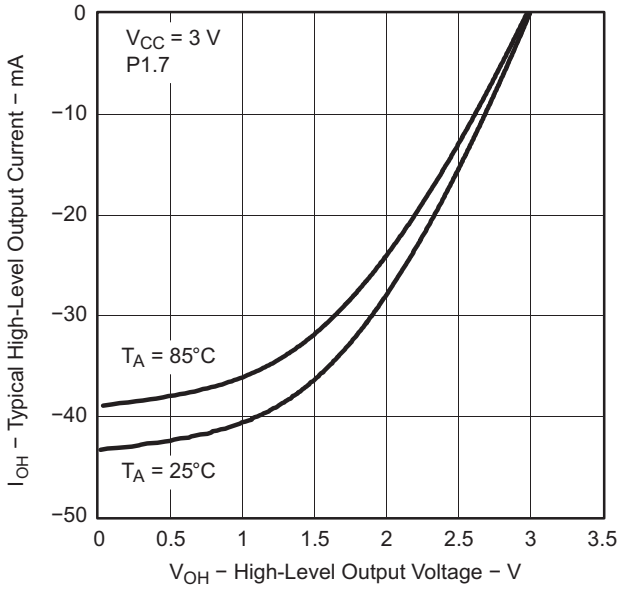


Figure 9.

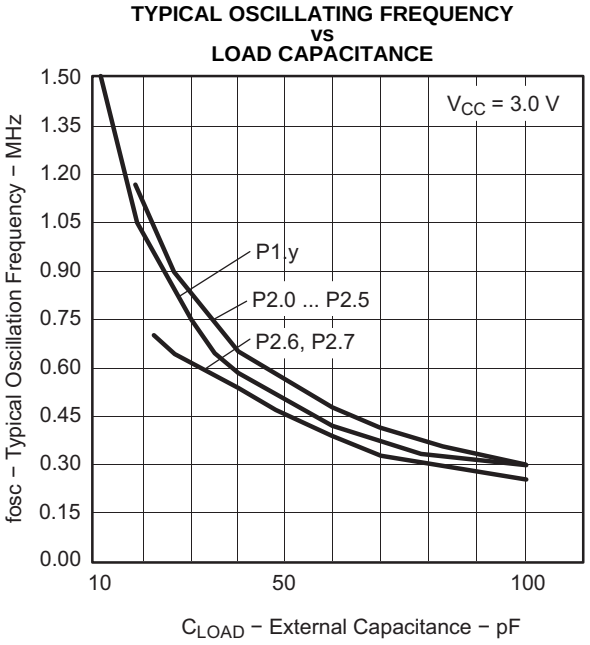
Pin-Oscillator Frequency – Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$fo_{P1.x}$	Port output oscillation frequency	P1.y, C_L = 10 pF, R_L = 100 kΩ(1)(2)	3 V		1400		kHz
		P1.y, C_L = 20 pF, R_L = 100 kΩ(1)(2)			900		
$fo_{P2.x}$	Port output oscillation frequency	P2.0 to P2.5, C_L = 10 pF, R_L = 100 kΩ(1)(2)			1800		kHz
		P2.0 to P2.5, C_L = 20 pF, R_L = 100 kΩ(1)(2)	3 V		1000		
$fo_{P2.6/7}$	Port output oscillation frequency	P2.6 and P2.7, C_L = 20 pF, R_L = 100 kΩ(1)(2)	3 V		700		kHz
$fo_{P3.x}$	Port output oscillation frequency	P3.y, C_L = 10 pF, R_L = 100 kΩ(1)(2)			1800		kHz
		P3.y, C_L = 20 pF, R_L = 100 kΩ(1)(2)			1000		

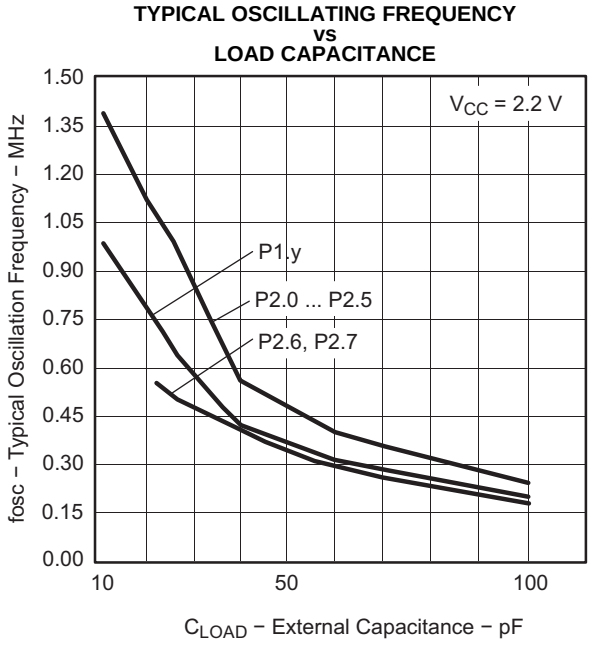
(1) A resistive divider with two 50-kΩ resistors between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

Typical Characteristics, Pin-Oscillator Frequency



A. One output active at a time.

Figure 10.



A. One output active at a time.

Figure 11.

POR, BOR(1)(2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(start)}$	See Figure 12	$dV_{CC}/dt \le 3$ V/s			0.7 × $V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$	See Figure 12 through Figure 14	$dV_{CC}/dt \le 3$ V/s			1.35		V
$V_{hys(B\_IT-)}$	See Figure 12	$dV_{CC}/dt \le 3$ V/s			140		mV
$t_{d(BOR)}$	See Figure 12				2000		µs
$t_{(reset)}$	Pulse duration needed at $\overline{RST}$/NMI pin to accepted reset internally		2.2 V	2			µs

(1) The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)}$ + $V_{hys(B_IT-)}$is ≤ 1.8 V.

(2) During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$. The default DCO settings must not be changed until $V_{CC} \ge V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency.

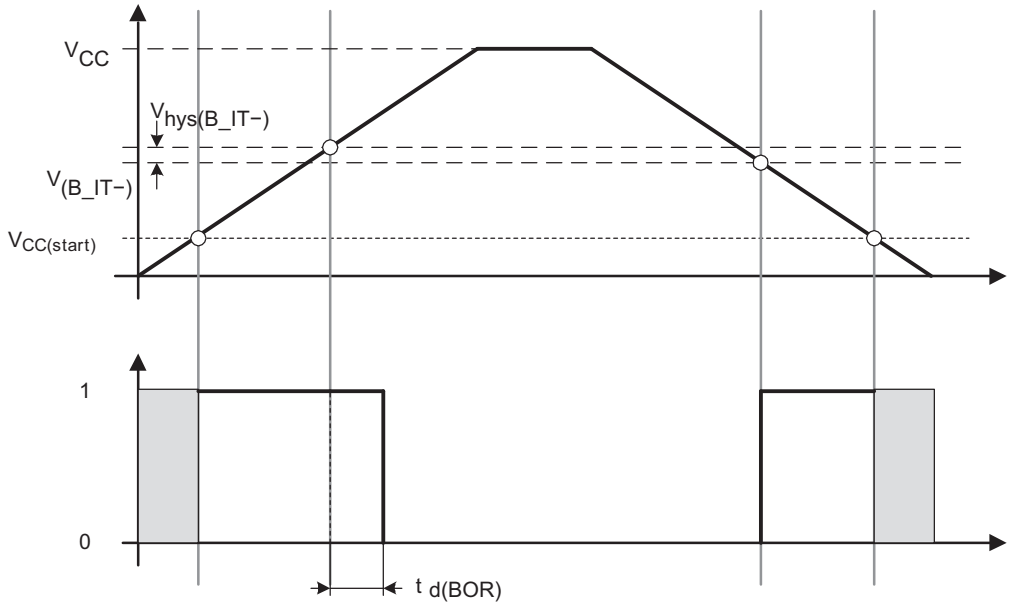


Figure 12. POR and BOR vs Supply Voltage

Typical Characteristics, POR and BOR

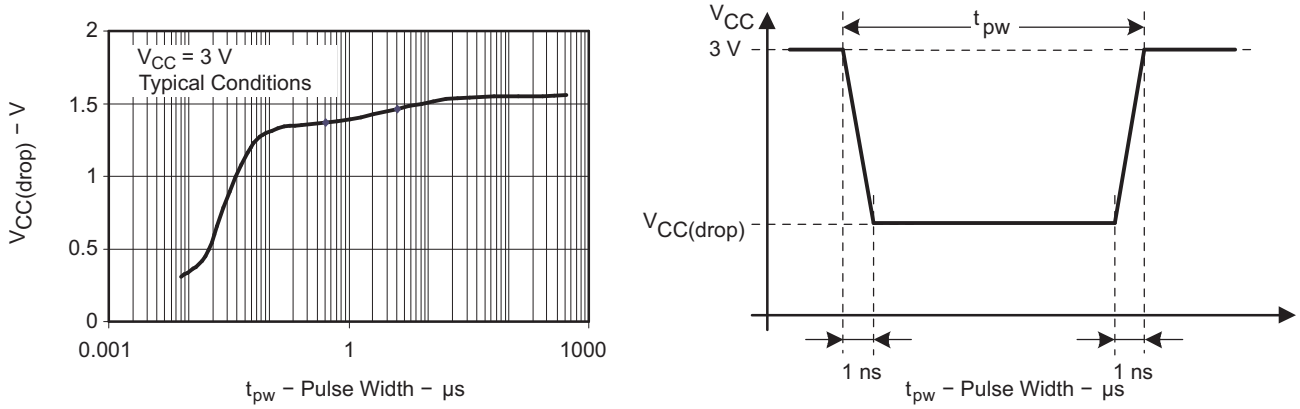


Figure 13. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR or BOR Signal

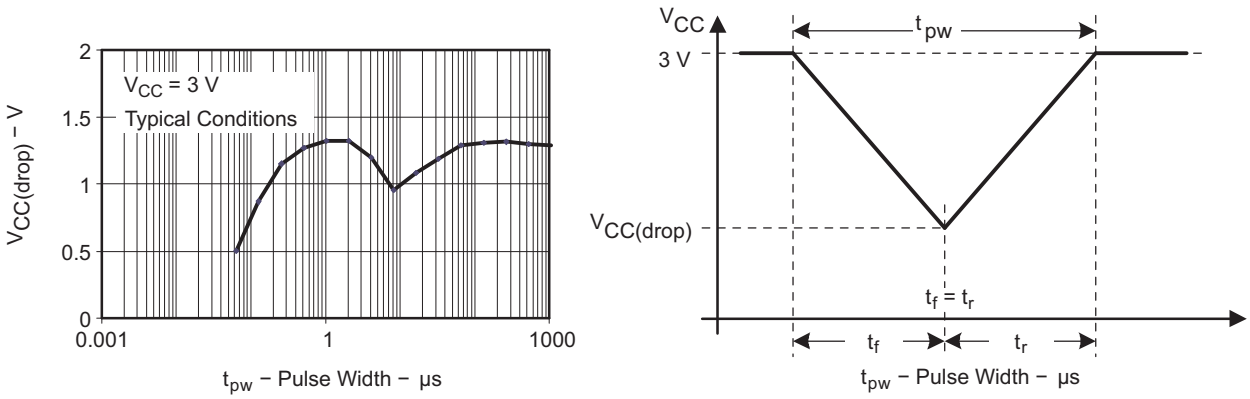


Figure 14. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR or BOR Signal

DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	RSELx < 14		1.8		3.6	V
		RSELx = 14		2.2		3.6	
		RSELx = 15		3		3.6	
$f_{DCO(0,0)}$	DCO frequency (0, 0)	RSELx = 0, DCOx = 0, MODx = 0	3 V	0.06		0.14	MHz
$f_{DCO(0,3)}$	DCO frequency (0, 3)	RSELx = 0, DCOx = 3, MODx = 0	3 V	0.07		0.17	MHz
$f_{DCO(1,3)}$	DCO frequency (1, 3)	RSELx = 1, DCOx = 3, MODx = 0	3 V		0.15		MHz
$f_{DCO(2,3)}$	DCO frequency (2, 3)	RSELx = 2, DCOx = 3, MODx = 0	3 V		0.21		MHz
$f_{DCO(3,3)}$	DCO frequency (3, 3)	RSELx = 3, DCOx = 3, MODx = 0	3 V		0.30		MHz
$f_{DCO(4,3)}$	DCO frequency (4, 3)	RSELx = 4, DCOx = 3, MODx = 0	3 V		0.41		MHz
$f_{DCO(5,3)}$	DCO frequency (5, 3)	RSELx = 5, DCOx = 3, MODx = 0	3 V		0.58		MHz
$f_{DCO(6,3)}$	DCO frequency (6, 3)	RSELx = 6, DCOx = 3, MODx = 0	3 V	0.54		1.06	MHz
$f_{DCO(7,3)}$	DCO frequency (7, 3)	RSELx = 7, DCOx = 3, MODx = 0	3 V	0.80		1.50	MHz
$f_{DCO(8,3)}$	DCO frequency (8, 3)	RSELx = 8, DCOx = 3, MODx = 0	3 V		1.6		MHz
$f_{DCO(9,3)}$	DCO frequency (9, 3)	RSELx = 9, DCOx = 3, MODx = 0	3 V		2.3		MHz
$f_{DCO(10,3)}$	DCO frequency (10, 3)	RSELx = 10, DCOx = 3, MODx = 0	3 V		3.4		MHz
$f_{DCO(11,3)}$	DCO frequency (11, 3)	RSELx = 11, DCOx = 3, MODx = 0	3 V		4.25		MHz
$f_{DCO(12,3)}$	DCO frequency (12, 3)	RSELx = 12, DCOx = 3, MODx = 0	3 V	4.30		7.30	MHz
$f_{DCO(13,3)}$	DCO frequency (13, 3)	RSELx = 13, DCOx = 3, MODx = 0	3 V	6.00	7.8	9.60	MHz
$f_{DCO(14,3)}$	DCO frequency (14, 3)	RSELx = 14, DCOx = 3, MODx = 0	3 V	8.60		13.9	MHz
$f_{DCO(15,3)}$	DCO frequency (15, 3)	RSELx = 15, DCOx = 3, MODx = 0	3 V	12.0		18.5	MHz
$f_{DCO(15,7)}$	DCO frequency (15, 7)	RSELx = 15, DCOx = 7, MODx = 0	3 V	16.0		26.0	MHz
S_{RSEL}	Frequency step between range RSEL and RSEL+1	$S_{RSEL} = f_{DCO(RSEL+1,DCO)}/f_{DCO(RSEL,DCO)}$	3 V		1.35		ratio
S_{DCO}	Frequency step between tap DCO and DCO+1	$S_{DCO} = f_{DCO(RSEL,DCO+1)}/f_{DCO(RSEL,DCO)}$	3 V		1.08		ratio
	Duty cycle	Measured at SMCLK output	3 V		50		%

Calibrated DCO Frequencies, Tolerance

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
1-MHz tolerance over temperature(1)	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, calibrated at 30°C and 3 V	0°C to 85°C	3 V	-3	±0.5	+3	%
1-MHz tolerance over V_{CC}	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, calibrated at 30°C and 3 V	30°C	1.8 V to 3.6 V	-3	±2	+3	%
1-MHz tolerance overall	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, calibrated at 30°C and 3 V	-40°C to 85°C	1.8 V to 3.6 V	-6	±3	+6	%
8-MHz tolerance over temperature(1)	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3 V	0°C to 85°C	3 V	-3	±0.5	+3	%
8-MHz tolerance over V_{CC}	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3 V	30°C	2.2 V to 3.6 V	-3	±2	+3	%
8-MHz tolerance overall	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3 V	-40°C to 85°C	2.2 V to 3.6 V	-6	±3	+6	%
12-MHz tolerance over temperature(1)	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3 V	0°C to 85°C	3 V	-3	±0.5	+3	%
12-MHz tolerance over V_{CC}	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3 V	30°C	2.7 V to 3.6 V	-3	±2	+3	%
12-MHz tolerance overall	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3 V	-40°C to 85°C	2.7 V to 3.6 V	-6	±3	+6	%
16-MHz tolerance over temperature(1)	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, calibrated at 30°C and 3 V	0°C to 85°C	3 V	-3	±0.5	+3	%
16-MHz tolerance over V_{CC}	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, calibrated at 30°C and 3 V	30°C	3.3 V to 3.6 V	-3	±2	+3	%
16-MHz tolerance overall	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, calibrated at 30°C and 3 V	-40°C to 85°C	3.3 V to 3.6 V	-6	±3	+6	%

(1) This is the frequency change from the measured frequency at 30°C over temperature.

Wake-Up From Lower-Power Modes (LPM3/4)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{DCO,LPM3/4}$	DCO clock wake-up time from LPM3/4 (1)	BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz	3 V		1.5		µs
$t_{CPU,LPM3/4}$	CPU wake-up time from LPM3/4 (2)				$1/f_{MCLK}$ + $t_{Clock,LPM3/4}$		

(1) The DCO clock wake-up time is measured from the edge of an external wake-up signal (e.g., port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
(2) Parameter applicable only if DCOCLK is used for MCLK.

Typical Characteristics, DCO Clock Wake-Up Time From LPM3/4

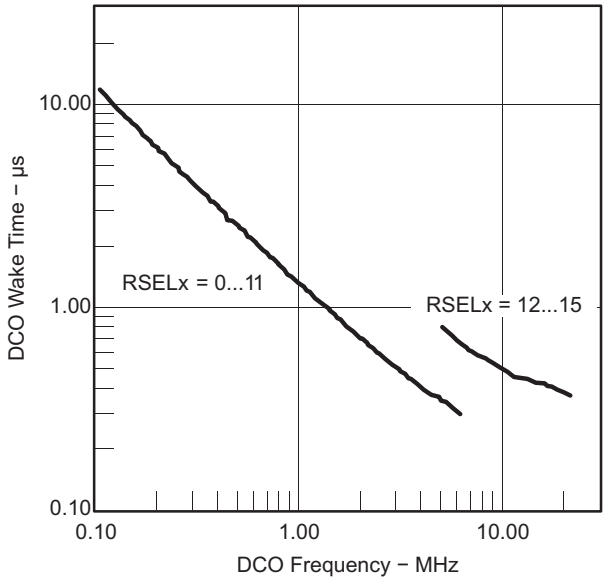


Figure 15. DCO Wake-Up Time From LPM3 vs DCO Frequency

Crystal Oscillator, XT1, Low-Frequency Mode(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{LFXT1,LF}$	LFXT1 oscillator crystal frequency, LF mode 0, 1	XTS = 0, LFXT1Sx = 0 or 1	1.8 V to 3.6 V		32768		Hz
$f_{LFXT1,LF,logic}$	LFXT1 oscillator logic level square wave input frequency, LF mode	XTS = 0, XCAPx = 0, LFXT1Sx = 3	1.8 V to 3.6 V	10000	32768	50000	Hz
OA_{LF}	Oscillation allowance for LF crystals	XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF			500		kΩ
		XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF			200		
$C_{L,eff}$	Integrated effective load capacitance, LF mode(2)	XTS = 0, XCAPx = 0			1		pF
		XTS = 0, XCAPx = 1			5.5		
		XTS = 0, XCAPx = 2			8.5		
		XTS = 0, XCAPx = 3			11		
	Duty cycle, LF mode	XTS = 0, Measured at P2.0/ACLK, $f_{LFXT1,LF}$ = 32768 Hz	2.2 V	30	50	70	%
$f_{Fault,LF}$	Oscillator fault frequency, LF mode(3)	XTS = 0, XCAPx = 0, LFXT1Sx = 3(4)	2.2 V	10		10000	Hz

(1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
(a) Keep the trace between the device and the crystal as short as possible.
(b) Design a good ground plane around the oscillator pins.
(c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
(d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
(e) Use assembly materials and process that avoid any parasitic load on the oscillator XIN and XOUT pins.
(f) If a conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.
(g) Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

(2) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

(3) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.

(4) Measured with logic-level input frequency but also applies to operation with crystals.

Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		T_A	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency	-40°C to 85°C	3 V	4	12	20	kHz
df_{VLO}/d_T	VLO frequency temperature drift	-40°C to 85°C	3 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	25°C	1.8 V to 3.6 V		4		%/V

Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TA}	Timer_A input clock frequency	SMCLK, duty cycle = 50% ± 10%			f_{SYSTEM}		MHz
$t_{TA,cap}$	Timer_A capture timing	TA0, TA1	3 V	20			ns

USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK, duty cycle = 50% ± 10%			f_{SYSTEM}		MHz
$f_{max,BITCLK}$	Maximum BITCLK clock frequency (equals baudrate in MBaud)(1)		3 V	2			MHz
t_τ	UART receive deglitch time(2)		3 V	50	100	600	ns

(1) The DCO wake-up time must be considered in LPM3 and LPM4 for baud rates above 1 MHz.
(2) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

USCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 16 and Figure 17)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK, duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
$t_{SU,MI}$	SOMI input data setup time		3 V	75			ns
$t_{HD,MI}$	SOMI input data hold time		3 V	0			ns
$t_{VALID,MO}$	SIMO output data valid time	UCLK edge to SIMO valid, C_L = 20 pF	3 V			20	ns

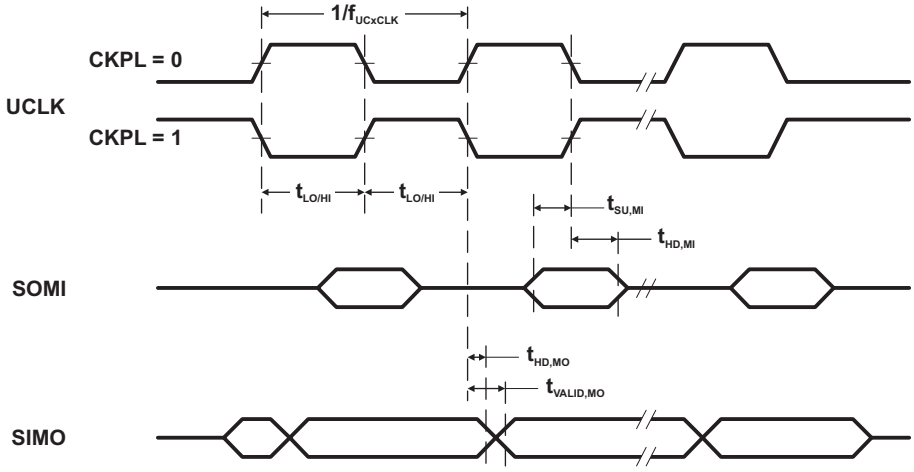


Figure 16. SPI Master Mode, CKPH = 0

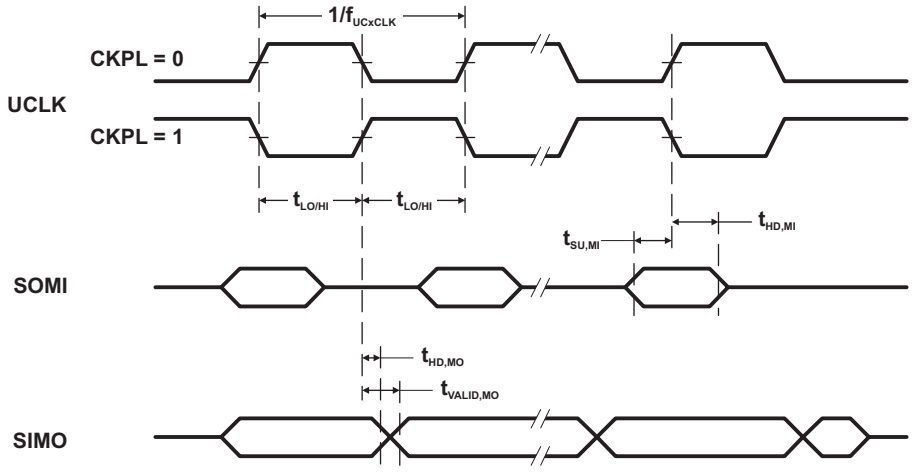


Figure 17. SPI Master Mode, CKPH = 1

USCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 18 and Figure 19)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE low to clock		3 V		50		ns
$t_{STE,LAG}$	STE lag time, Last clock to STE high		3 V	10			ns
$t_{STE,ACC}$	STE access time, STE low to SOMI data out		3 V		50		ns
$t_{STE,DIS}$	STE disable time, STE high to SOMI high impedance		3 V		50		ns
$t_{SU,SI}$	SIMO input data setup time		3 V	15			ns
$t_{HD,SI}$	SIMO input data hold time		3 V	10			ns
$t_{VALID,SO}$	SOMI output data valid time	UCLK edge to SOMI valid, C_L = 20 pF	3 V		50	75	ns

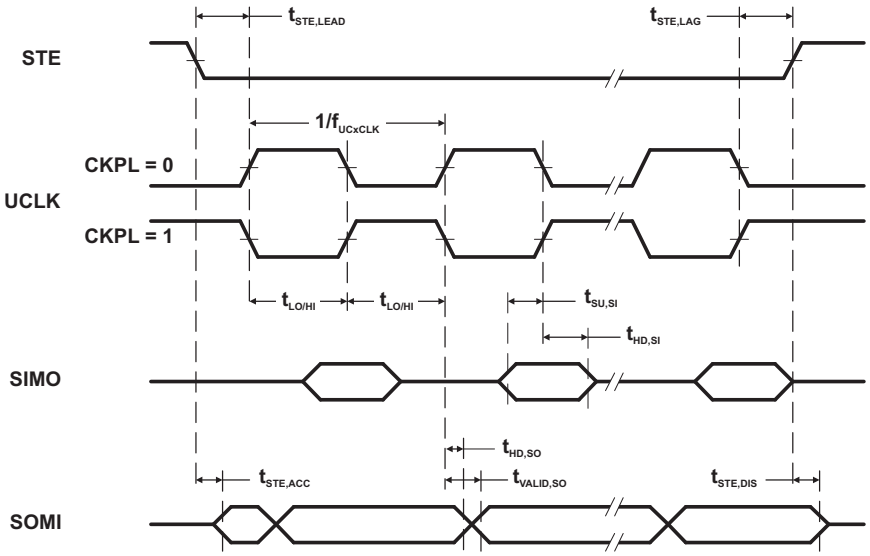


Figure 18. SPI Slave Mode, CKPH = 0

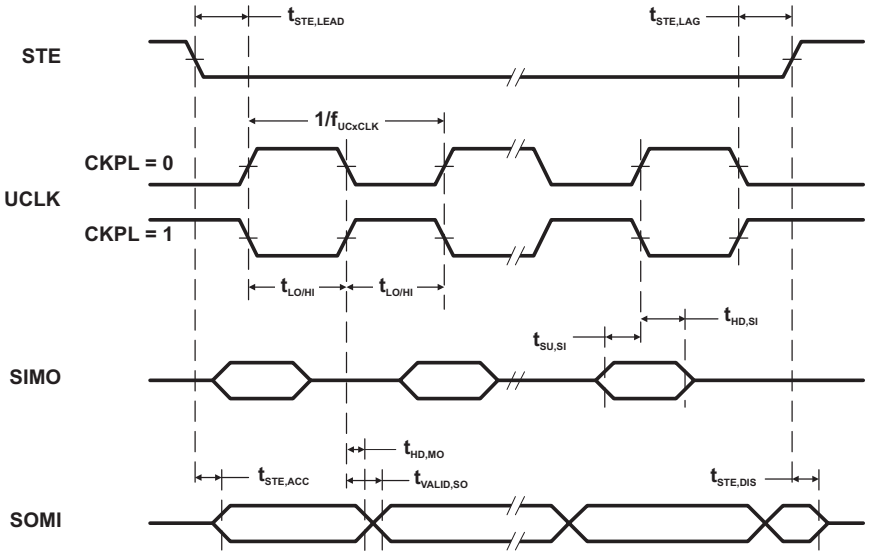


Figure 19. SPI Slave Mode, CKPH = 1

USCI (I2C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 20)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK, duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{SCL}	SCL clock frequency		3 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	$f_{SCL} \le 100$ kHz	3 V	4.0			µs
		$f_{SCL} > 100$ kHz		0.6			
$t_{SU,STA}$	Setup time for a repeated START	$f_{SCL} \le 100$ kHz	3 V	4.7			µs
		$f_{SCL} > 100$ kHz		0.6			
$t_{HD,DAT}$	Data hold time		3 V	0			ns
$t_{SU,DAT}$	Data setup time		3 V	250			ns
$t_{SU,STO}$	Setup time for STOP		3 V	4.0			µs
t_{SP}	Pulse width of spikes suppressed by input filter		3 V	50	100	600	ns

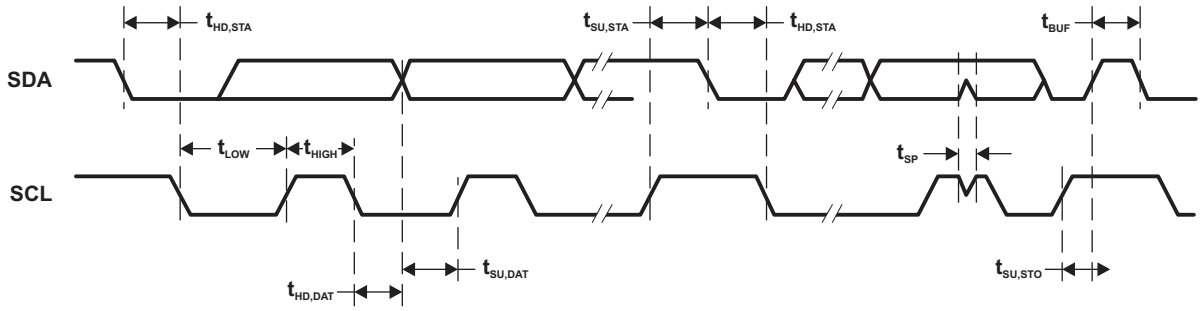


Figure 20. I2C Mode Timing

Comparator_A+

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{(DD)}$ (1)		CAON = 1, CARSEL = 0, CAREF = 0	3 V		45		µA
$I_{(Refladder/RefDiode)}$		CAON = 1, CARSEL = 0, CAREF = 1, 2, or 3, No load at CA0 and CA1	3 V		45		µA
$V_{(IC)}$	Common–mode input voltage	CAON = 1	3 V	0		V_{CC}-1	V
$V_{(Ref025)}$	(Voltage at 0.25 V_{CC} node) / V_{CC}	PCA0 = 1, CARSEL = 1, CAREF = 1, No load at CA0 and CA1	3 V		0.24		
$V_{(Ref050)}$	(Voltage at 0.5 V_{CC} node) / V_{CC}	PCA0 = 1, CARSEL = 1, CAREF = 2, No load at CA0 and CA1	3 V		0.48		
$V_{(RefVT)}$	See Figure 21 and Figure 22	PCA0 = 1, CARSEL = 1, CAREF = 3, No load at CA0 and CA1, TA = 85°C	3 V		490		mV
$V_{(offset)}$	Offset voltage (2)		3 V		±10		mV
V_{hys}	Input hysteresis	CAON = 1	3 V		0.7		mV
$t_{(response)}$	Response time (low-high and high-low)	T_A = 25°C, Overdrive 10 mV, Without filter: CAF = 0	3 V		120		ns
		T_A = 25°C, Overdrive 10 mV, With filter: CAF = 1			1.5		µs

(1) The leakage current for the Comparator_A+ terminals is identical to $I_{lkg(Px.y)}$ specification.
(2) The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A+ inputs on successive measurements. The two successive measurements are then summed together.

Typical Characteristics – Comparator_A+

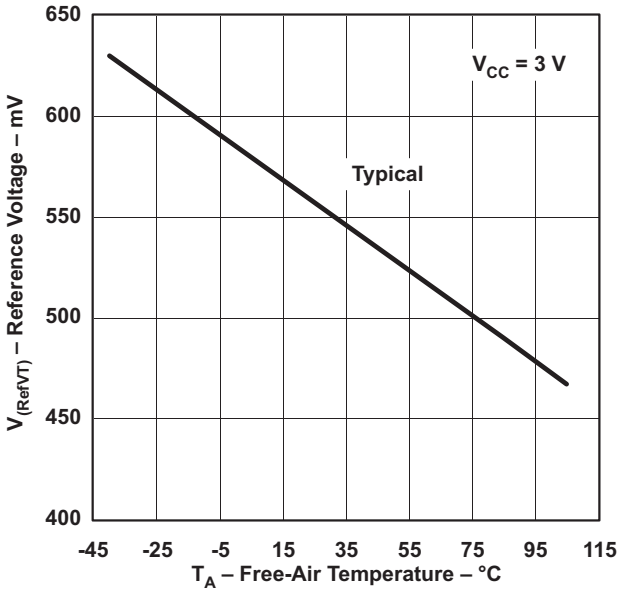


Figure 21. $V_{(RefVT)}$ vs Temperature, V_{CC} = 3 V

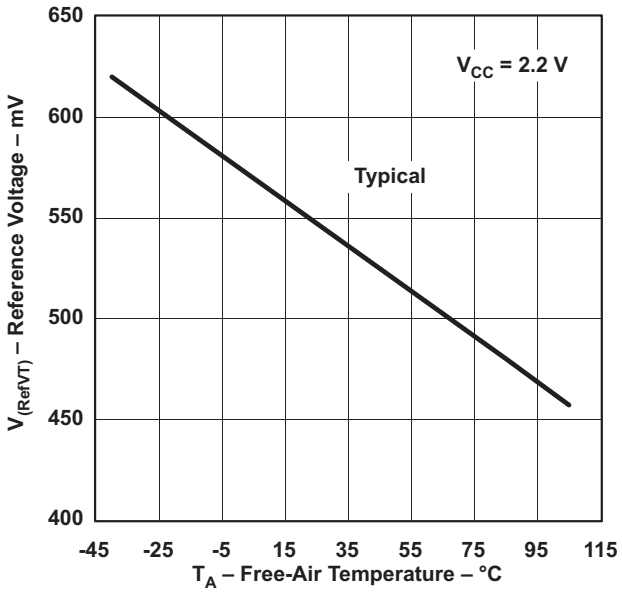


Figure 22. $V_{(RefVT)}$ vs Temperature, V_{CC} = 2.2 V

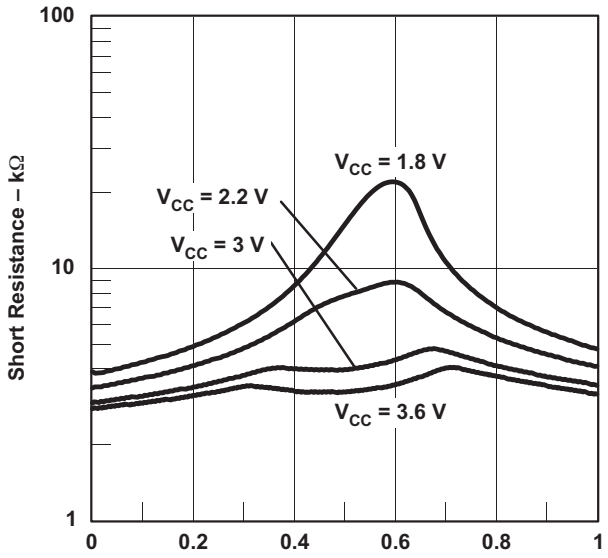


Figure 23. Short Resistance vs V_{IN}/V_{CC}

10-Bit ADC, Power Supply and Input Range Conditions (MSP430G2x53 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Analog supply voltage	V_{SS} = 0 V			2.2		3.6	V
V_{Ax}	Analog input voltage(2)	All Ax terminals, Analog inputs selected in ADC10AE register		3 V	0		V_{CC}	V
I_{ADC10}	ADC10 supply current(3)	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 1, REFON = 0, ADC10SHT0 = 1, ADC10SHT1 = 0, ADC10DIV = 0	25°C	3 V		0.6		mA
I_{REF+}	Reference supply current, reference buffer disabled(4)	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REF2_5V = 0, REFON = 1, REFOUT = 0	25°C	3 V		0.25		mA
		$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REF2_5V = 1, REFON = 1, REFOUT = 0				0.25		
$I_{REFB,0}$	Reference buffer supply current with ADC10SR = 0(4)	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR = 0	25°C	3 V		1.1		mA
$I_{REFB,1}$	Reference buffer supply current with ADC10SR = 1(4)	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR = 1	25°C	3 V		0.5		mA
C_I	Input capacitance	Only one terminal Ax can be selected at one time	25°C	3 V			27	pF
R_I	Input MUX ON resistance	0 V ≤ V_{Ax} ≤ V_{CC}	25°C	3 V		1000		Ω

(1) The leakage current is defined in the leakage current table with Px.y/Ax parameter.
(2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
(3) The internal reference supply current is not included in current consumption parameter I_{ADC10}.
(4) The internal reference current is supplied via terminal V_{CC}. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables the built-in reference to settle before starting an A/D conversion.

10-Bit ADC, Built-In Voltage Reference (MSP430G2x53 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC,REF+}$	Positive built-in reference analog supply voltage range	$I_{VREF+} \le 1$ mA, REF2_5V = 0		2.2			V
		$I_{VREF+} \le 1$ mA, REF2_5V = 1		2.9			
V_{REF+}	Positive built-in reference voltage	$I_{VREF+} \le I_{VREF+}$max, REF2_5V = 0	3 V	1.41	1.5	1.59	V
		$I_{VREF+} \le I_{VREF+}$max, REF2_5V = 1		2.35	2.5	2.65	
$I_{LD,VREF+}$	Maximum VREF+ load current		3 V			±1	mA
	VREF+ load regulation	I_{VREF+} = 500 µA ± 100 µA, Analog input voltage $V_{Ax} \approx 0.75$ V, REF2_5V = 0	3 V			±2	LSB
		I_{VREF+} = 500 µA ± 100 µA, Analog input voltage $V_{Ax} \approx 1.25$ V, REF2_5V = 1				±2	
	V_{REF+} load regulation response time	I_{VREF+} = 100 µA→900 µA, $V_{Ax} \approx 0.5 \times$ VREF+, Error of conversion result ≤ 1 LSB, ADC10SR = 0	3 V			400	ns
C_{VREF+}	Maximum capacitance at pin VREF+	$I_{VREF+} \le \pm 1$ mA, REFON = 1, REFOUT = 1	3 V			100	pF
TC_{REF+}	Temperature coefficient (1)	I_{VREF+} = const with 0 mA ≤ I_{VREF+} ≤ 1 mA	3 V			±100	ppm/°C
t_{REFON}	Settling time of internal reference voltage to 99.9% VREF	I_{VREF+} = 0.5 mA, REF2_5V = 0, REFON = 0 → 1	3.6 V			30	µs
$t_{REFBURST}$	Settling time of reference buffer to 99.9% VREF	I_{VREF+} = 0.5 mA, REF2_5V = 1, REFON = 1, REFBURST = 1, ADC10SR = 0	3 V			2	µs

(1) Calculated using the box method: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C – (–40°C))

10-Bit ADC, External Reference(1) (MSP430G2x53 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
VEREF+	Positive external reference input voltage range (2)	VEREF+ > VEREF–, SREF1 = 1, SREF0 = 0		1.4		V_{CC}	V
		VEREF– ≤ VEREF+ ≤ V_{CC} – 0.15 V, SREF1 = 1, SREF0 = 1 (3)		1.4		3	
VEREF–	Negative external reference input voltage range (4)	VEREF+ > VEREF–		0		1.2	V
ΔVEREF	Differential external reference input voltage range, ΔVEREF = VEREF+ – VEREF–	VEREF+ > VEREF– (5)		1.4		V_{CC}	V
I_{VEREF+}	Static input current into VEREF+	0 V ≤ VEREF+ ≤ V_{CC}, SREF1 = 1, SREF0 = 0	3 V		±1		μA
		0 V ≤ VEREF+ ≤ V_{CC} – 0.15 V ≤ 3 V, SREF1 = 1, SREF0 = 1 (3)	3 V		0		
$I_{VEREF–}$	Static input current into VEREF–	0 V ≤ VEREF– ≤ V_{CC}	3 V		±1		μA

(1) The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
(3) Under this condition the external reference is internally buffered. The reference buffer is active and requires the reference buffer supply current I_{REFB}. The current consumption can be limited to the sample and conversion period with REBURST = 1.
(4) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
(5) The accuracy limits the minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

10-Bit ADC, Timing Parameters (MSP430G2x53 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC10CLK}$	ADC10 input clock frequency	For specified performance of ADC10 linearity parameters	ADC10SR = 0	3 V	0.45		6.3	MHz
			ADC10SR = 1		0.45		1.5	
$f_{ADC10OSC}$	ADC10 built-in oscillator frequency	ADC10DIVx = 0, ADC10SSELx = 0, $f_{ADC10CLK} = f_{ADC10OSC}$		3 V	3.7		6.3	MHz
$t_{CONVERT}$	Conversion time	ADC10 built-in oscillator, ADC10SSELx = 0, $f_{ADC10CLK} = f_{ADC10OSC}$		3 V	2.06		3.51	μs
		$f_{ADC10CLK}$ from ACLK, MCLK, or SMCLK: ADC10SSELx ≠ 0			13 × ADC10DIV × $1/f_{ADC10CLK}$			
$t_{ADC10ON}$	Turn-on settling time of the ADC	(1)					100	ns

(1) The condition is that the error in a conversion started after $t_{ADC10ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.

10-Bit ADC, Linearity Parameters (MSP430G2x53 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error		3 V			±1	LSB
E_D	Differential linearity error		3 V			±1	LSB
E_O	Offset error	Source impedance R_S < 100 Ω	3 V			±1	LSB
E_G	Gain error		3 V		±1.1	±2	LSB
E_T	Total unadjusted error		3 V		±2	±5	LSB

10-Bit ADC, Temperature Sensor and Built-In V_{MID} (MSP430G2x53 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{SENSOR}	Temperature sensor supply current(1)	REFON = 0, INCHx = 0Ah, T_A = 25°C	3 V		60		µA
TC_{SENSOR}		ADC10ON = 1, INCHx = 0Ah (2)	3 V		3.55		mV/°C
$t_{Sensor(sample)}$	Sample time required if channel 10 is selected (3)	ADC10ON = 1, INCHx = 0Ah, Error of conversion result ≤ 1 LSB	3 V	30			µs
I_{VMID}	Current into divider at channel 11	ADC10ON = 1, INCHx = 0Bh	3 V			(4)	µA
V_{MID}	V_{CC} divider at channel 11	ADC10ON = 1, INCHx = 0Bh, $V_{MID} \neq 0.5 \times V_{CC}$	3 V		1.5		V
$t_{VMID(sample)}$	Sample time required if channel 11 is selected (5)	ADC10ON = 1, INCHx = 0Bh, Error of conversion result ≤ 1 LSB	3 V	1220			ns

(1) The sensor current I_{SENSOR} is consumed if (ADC10ON = 1 and REFON = 1) or (ADC10ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is included in I_{REF+}. When REFON = 0, I_{SENSOR} applies during conversion of the temperature sensor input (INCH = 0Ah).
(2) The following formula can be used to calculate the temperature sensor output voltage:
$V_{Sensor,typ} = TC_{Sensor}$ (273 + T [°C]) + $V_{Offset,sensor}$ [mV] or
$V_{Sensor,typ} = TC_{Sensor}$ T [°C] + $V_{Sensor}(T_A$ = 0°C) [mV]
(3) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
(4) No additional current is needed. The V_{MID} is used during sampling.
(5) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and erase supply voltage			2.2		3.6	V
f_{FTG}	Flash timing generator frequency			257		476	kHz
I_{PGM}	Supply current from V_{CC} during program		2.2 V, 3.6 V		1	5	mA
I_{ERASE}	Supply current from V_{CC} during erase		2.2 V, 3.6 V		1	7	mA
t_{CPT}	Cumulative program time(1)		2.2 V, 3.6 V			10	ms
$t_{CMErase}$	Cumulative mass erase time		2.2 V, 3.6 V	20			ms
	Program/erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	(2)			30		t_{FTG}
$t_{Block, 0}$	Block program time for first byte or word	(2)			25		t_{FTG}
$t_{Block, 1-63}$	Block program time for each additional byte or word	(2)			18		t_{FTG}
$t_{Block, End}$	Block program end-sequence wait time	(2)			6		t_{FTG}
$t_{Mass\ Erase}$	Mass erase time	(2)			10593		t_{FTG}
$t_{Seg\ Erase}$	Segment erase time	(2)			4819		t_{FTG}

(1) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
(2) These values are hardwired into the Flash Controller's state machine ($t_{FTG} = 1/f_{FTG}$).

RAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{(RAMh)}$	RAM retention supply voltage (1)	CPU halted	1.6		V

(1) This parameter defines the minimum supply voltage V_{CC} when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency		2.2 V	0		20	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse duration		2.2 V	0.025		15	µs
$t_{SBW,En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge(1))		2.2 V			1	µs
$t_{SBW,Ret}$	Spy-Bi-Wire return to normal operation time		2.2 V	15		100	µs
f_{TCK}	TCK input frequency(2)		2.2 V	0		5	MHz
$R_{Internal}$	Internal pulldown resistance on TEST		2.2 V	25	60	90	kΩ

(1) Tools accessing the Spy-Bi-Wire interface need to wait for the maximum $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

JTAG Fuse(1)

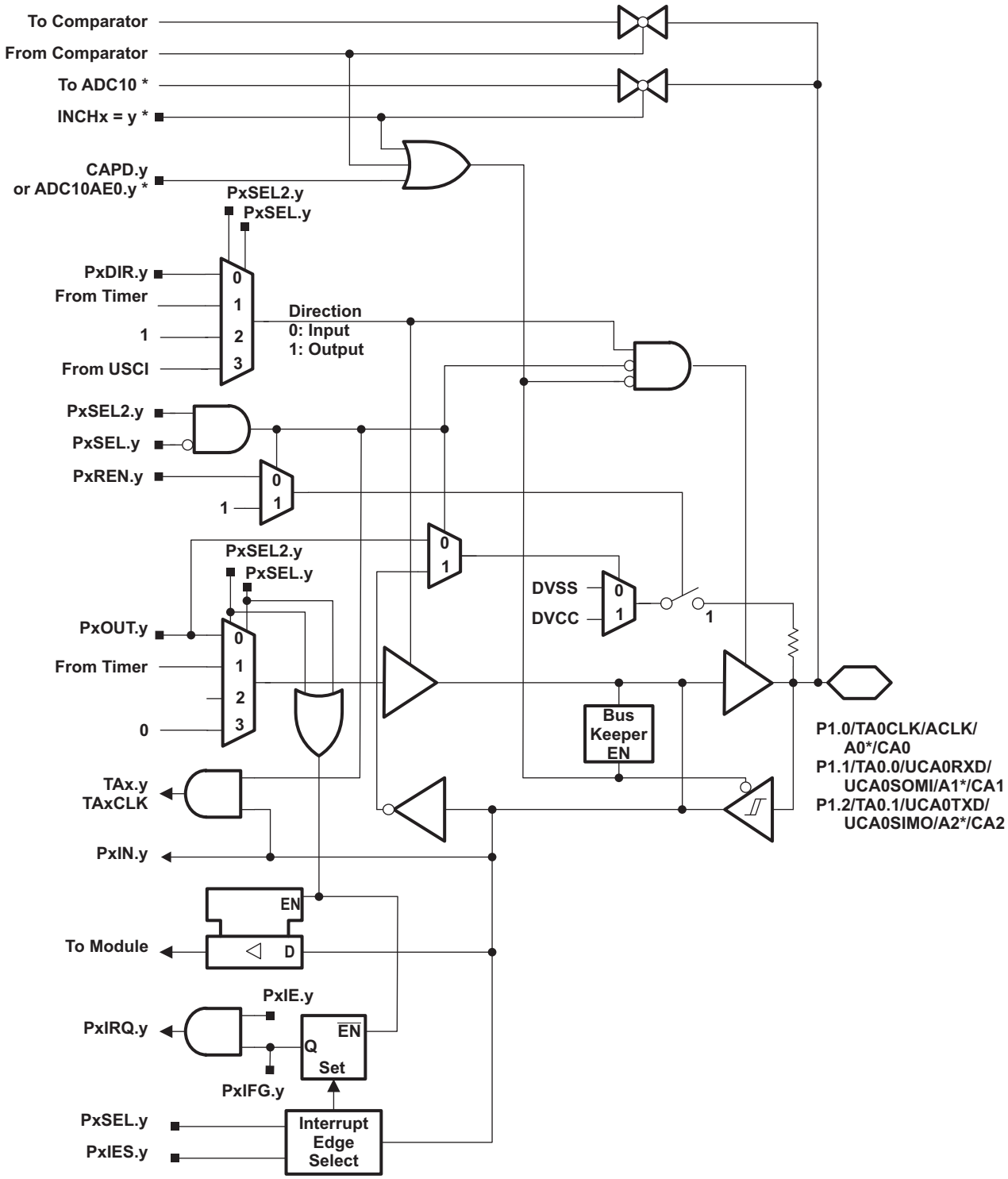
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C	2.5		V
V_{FB}	Voltage level on TEST for fuse blow		6	7	V
I_{FB}	Supply current into TEST during fuse blow			100	mA
t_{FB}	Time to blow fuse			1	ms

(1) Once the fuse is blown, no further access to the JTAG/Test, Spy-Bi-Wire, and emulation feature is possible, and JTAG is switched to bypass mode.

PORT SCHEMATICS

Port P1 Pin Schematic: P1.0 to P1.2, Input/Output With Schmitt Trigger



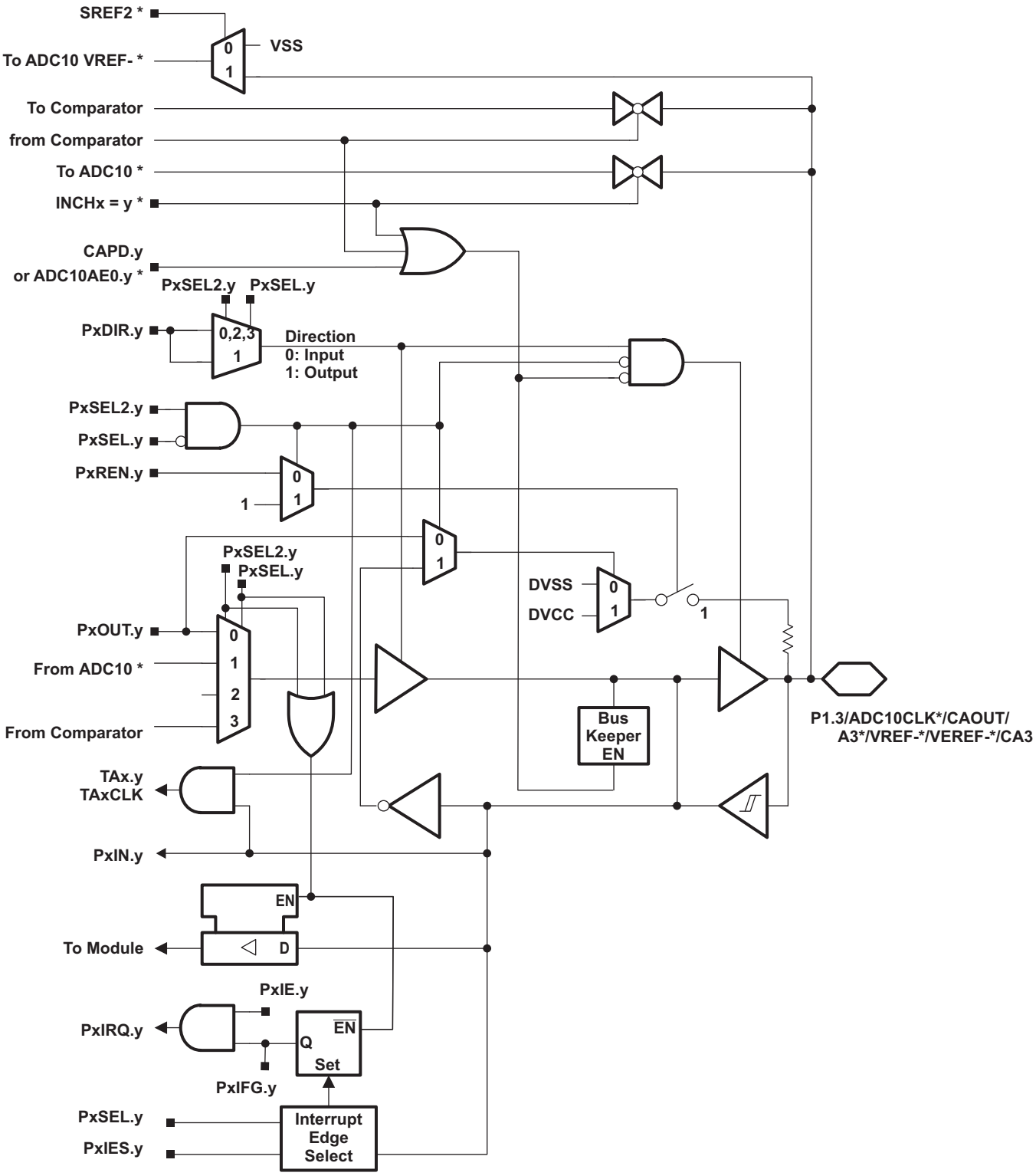
*** Note: MSP430G2x53 devices only. MSP430G2x13 devices have no ADC10.**

Table 16. Port P1 (P1.0 to P1.2) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]				
			P1DIR.x	P1SEL.x	P1SEL2.x	ADC10AE.x INCH.x=1[2]	CAPD.y
P1.0/	0	P1.x (I/O)	I: 0; O: 1	0	0	0	0
TA0CLK/		TA0.TACLK	0	1	0	0	0
ACLK/		ACLK	1	1	0	0	0
A0[2]/		A0	X	X	X	1 (y = 0)	0
CA0/		CA0	X	X	X	0	1 (y = 0)
Pin Osc		Capacitive sensing	X	0	1	0	0
P1.1/	1	P1.x (I/O)	I: 0; O: 1	0	0	0	0
TA0.0/		TA0.0	1	1	0	0	0
		TA0.CCI0A	0	1	0	0	0
UCA0RXD/		UCA0RXD	from USCI	1	1	0	0
UCA0SOMI/		UCA0SOMI	from USCI	1	1	0	0
A1[2]/		A1	X	X	X	1 (y = 1)	0
CA1/		CA1	X	X	X	0	1 (y = 1)
Pin Osc		Capacitive sensing	X	0	1	0	0
P1.2/	2	P1.x (I/O)	I: 0; O: 1	0	0	0	0
TA0.1/		TA0.1	1	1	0	0	0
		TA0.CCI1A	0	1	0	0	0
UCA0TXD/		UCA0TXD	from USCI	1	1	0	0
UCA0SIMO/		UCA0SIMO	from USCI	1	1	0	0
A2[2]/		A2	X	X	X	1 (y = 2)	0
CA2/		CA2	X	X	X	0	1 (y = 2)
Pin Osc		Capacitive sensing	X	0	1	0	0

(1) X = don't care
(2) MSP430G2x53 devices only

Port P1 Pin Schematic: P1.3, Input/Output With Schmitt Trigger



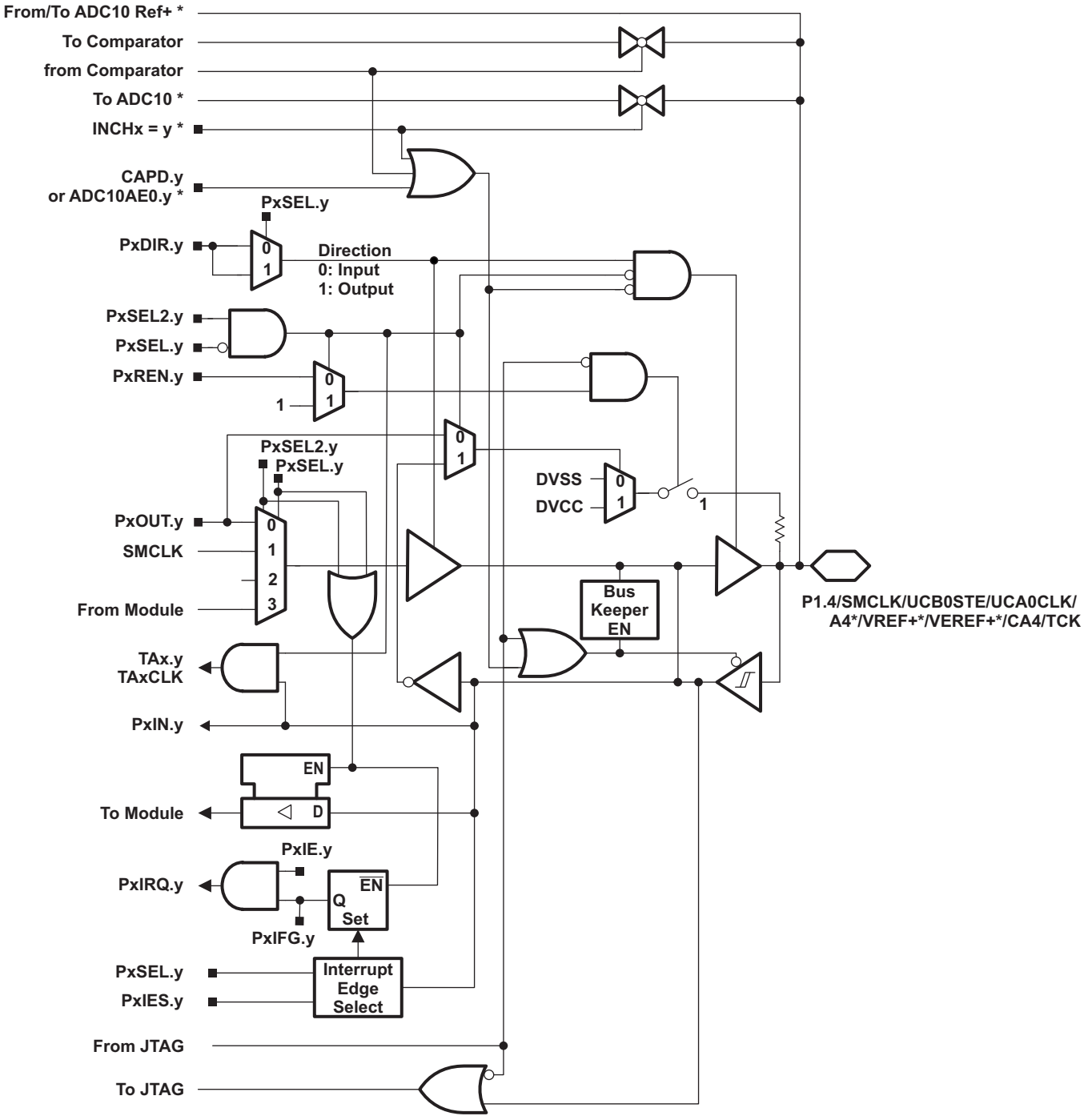
*** Note: MSP430G2x53 devices only. MSP430G2x13 devices have no ADC10.**

Table 17. Port P1 (P1.3) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]				
			P1DIR.x	P1SEL.x	P1SEL2.x	ADC10AE.x INCH.x=1[2]	CAPD.y
P1.3/	3	P1.x (I/O)	I: 0; O: 1	0	0	0	0
ADC10CLK[2]/		ADC10CLK	1	1	0	0	0
CAOUT/		CAOUT	1	1	1	0	0
A3[2]/		A3	X	X	X	1 (y = 3)	0
VREF-[2]/		VREF-	X	X	X	1	0
VEREF-[2]/		VEREF-	X	X	X	1	0
CA3/		CA3	X	X	X	0	1 (y = 3)
Pin Osc		Capacitive sensing	X	0	1	0	0

(1) X = don't care
(2) MSP430G2x53 devices only

Port P1 Pin Schematic: P1.4, Input/Output With Schmitt Trigger



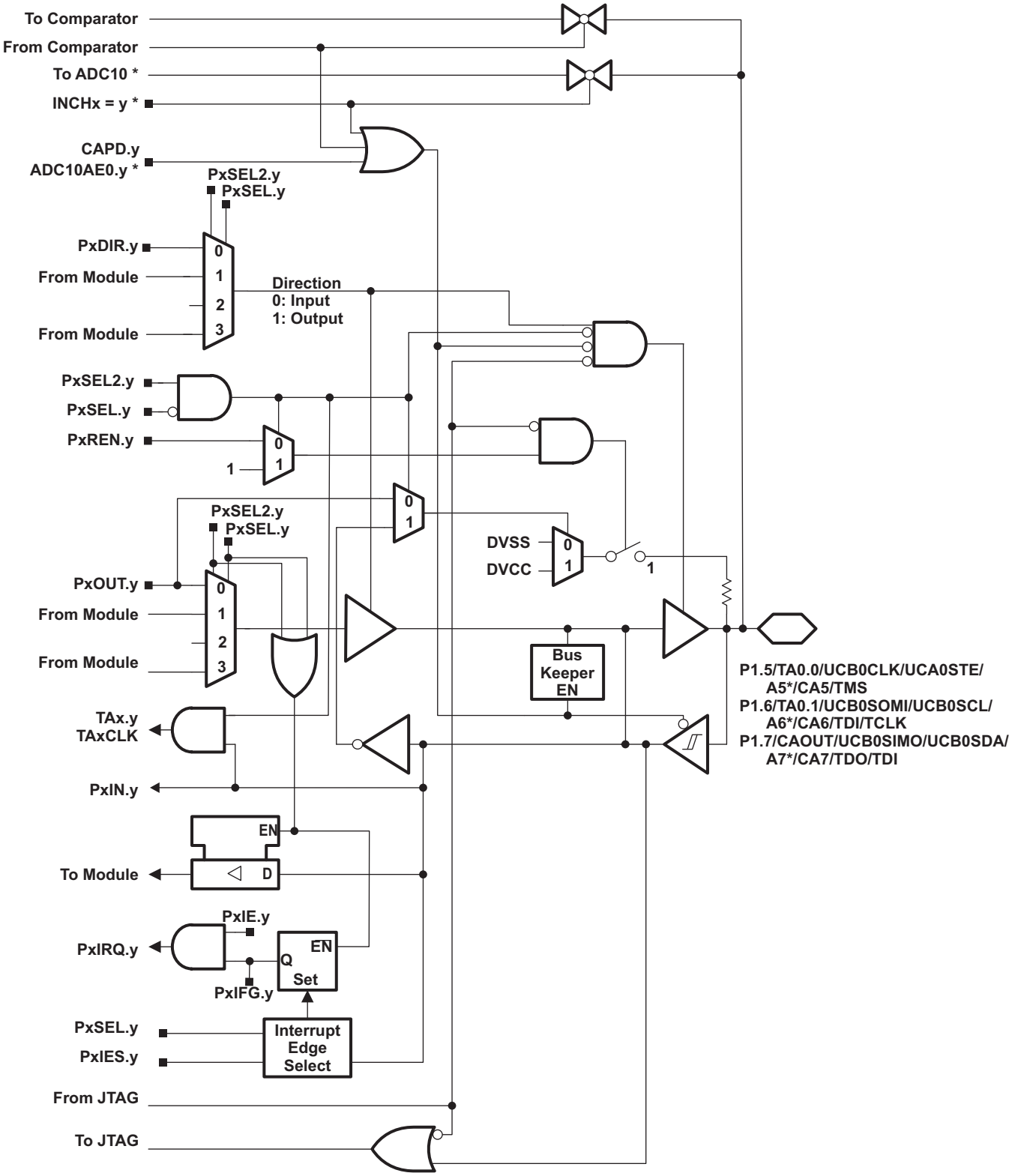
*** Note: MSP430G2x52 devices only. MSP430G2x12 devices have no ADC10.**

Table 18. Port P1 (P1.4) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]					
			P1DIR.x	P1SEL.x	P1SEL2.x	ADC10AE.x INCH.x=1[2]	JTAG Mode	CAPD.y
P1.4/	4	P1.x (I/O)	I: 0; O: 1	0	0	0	0	0
SMCLK/		SMCLK	1	1	0	0	0	0
UCB0STE/		UCB0STE	from USCI	1	1	0	0	0
UCA0CLK/		UCA0CLK	from USCI	1	1	0	0	0
VREF+[2]/		VREF+	X	X	X	1	0	0
VEREF+[2]/		VEREF+	X	X	X	1	0	0
A4[2]/		A4	X	X	X	1 (y = 4)	0	0
CA4		CA4	X	X	X	0	0	1 (y = 4)
TCK/		TCK	X	X	X	0	1	0
Pin Osc		Capacitive sensing	X	0	1	0	0	0

(1) X = don't care
(2) MSP430G2x53 devices only

Port P1 Pin Schematic: P1.5 to P1.7, Input/Output With Schmitt Trigger



* Note: MSP430G2x53 devices only. MSP430G2x13 devices have no ADC10.

Table 19. Port P1 (P1.5 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]					
			P1DIR.x	P1SEL.x	P1SEL2.x	ADC10AE.x INCH.x=1[2]	JTAG Mode	CAPD.y
P1.5/	5	P1.x (I/O)	I: 0; O: 1	0	0	0	0	0
TA0.0/		TA0.0	1	1	0	0	0	0
UCB0CLK/		UCB0CLK	from USCI	1	1	0	0	0
UCA0STE/		UCA0STE	from USCI	1	1	0	0	0
A5[2]/		A5	X	X	X	1 (y = 5)	0	0
CA5		CA5	X	X	X	0	0	1 (y = 5)
TMS		TMS	X	X	X	0	1	0
Pin Osc		Capacitive sensing	X	0	1	0	0	0
P1.6/	6	P1.x (I/O)	I: 0; O: 1	0	0	0	0	0
TA0.1/		TA0.1	1	1	0	0	0	0
UCB0SOMI/		UCB0SOMI	from USCI	1	1	0	0	0
UCB0SCL/		UCB0SCL	from USCI	1	1	0	0	0
A6[2]/		A6	X	X	X	1 (y = 6)	0	0
CA6		CA6	X	X	X	0	0	1 (y = 6)
TDI/TCLK/		TDI/TCLK	X	X	X	0	1	0
Pin Osc		Capacitive sensing	X	0	1	0	0	0
P1.7/	7	P1.x (I/O)	I: 0; O: 1	0	0	0	0	0
UCB0SIMO/		UCB0SIMO	from USCI	1	1	0	0	0
UCB0SDA/		UCB0SDA	from USCI	1	1	0	0	0
A7[2]/		A7	X	X	X	1 (y = 7)	0	0
CA7		CA7	X	X	X	0	0	1 (y = 7)
CAOUT		CAOUT	1	1	0	0	0	0
TDO/TDI/		TDO/TDI	X	X	X	0	1	0
Pin Osc		Capacitive sensing	X	0	1	0	0	0

(1) X = don't care
(2) MSP430G2x53 devices only

Port P2 Pin Schematic: P2.0 to P2.5, Input/Output With Schmitt Trigger

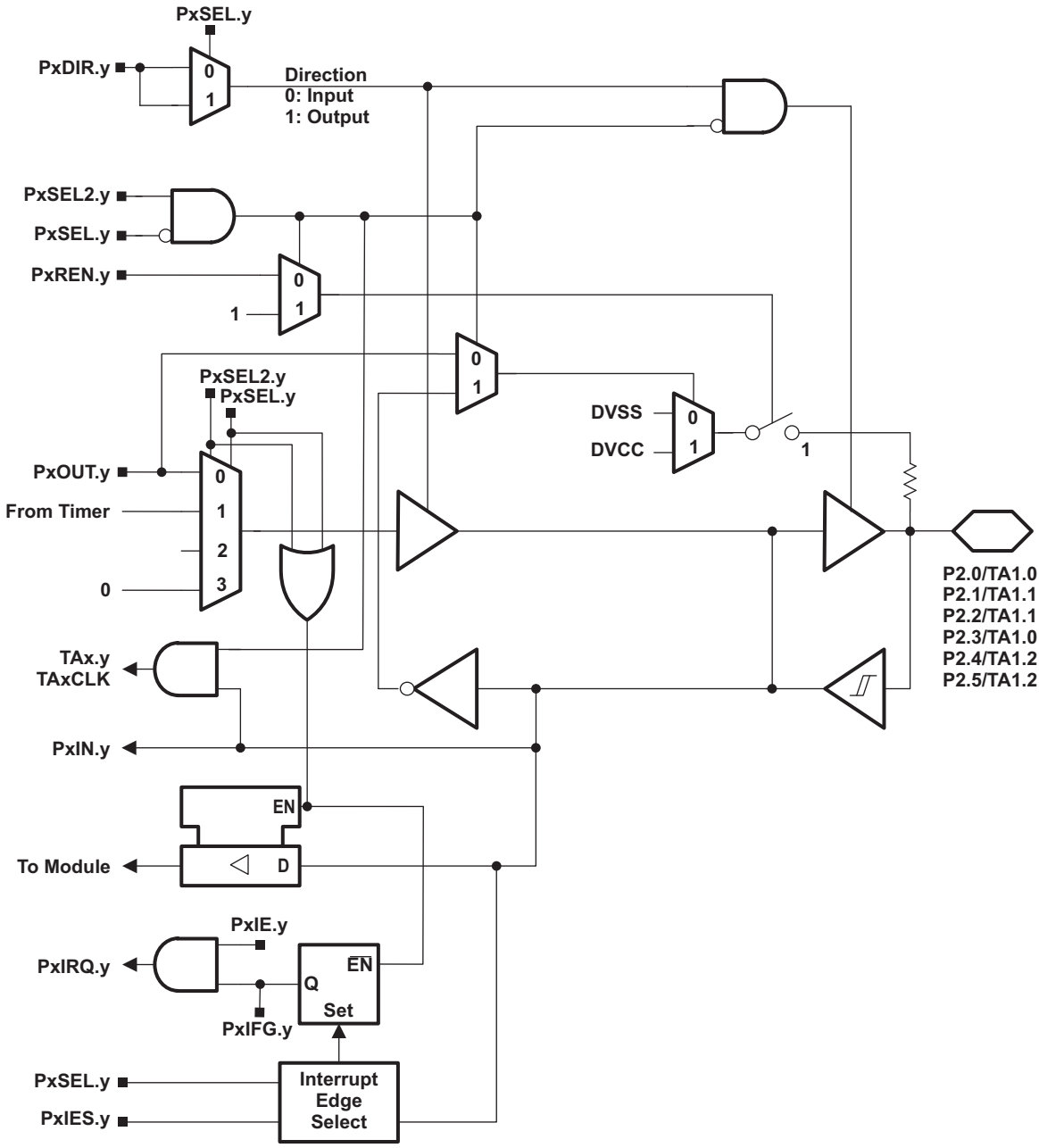


Table 20. Port P2 (P2.0 to P2.5) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)		
			P2DIR.x	P2SEL.x	P2SEL2.x
P2.0/	0	P2.x (I/O)	I: 0; O: 1	0	0
TA1.0/		Timer1_A3.CCI0A	0	1	0
		Timer1_A3.TA0	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P2.1/	1	P2.x (I/O)	I: 0; O: 1	0	0
TA1.1/		Timer1_A3.CCI1A	0	1	0
		Timer1_A3.TA1	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P2.2/	2	P2.x (I/O)	I: 0; O: 1	0	0
TA1.1/		Timer1_A3.CCI1B	0	1	0
		Timer1_A3.TA1	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P2.3/	3	P2.x (I/O)	I: 0; O: 1	0	0
TA1.0/		Timer1_A3.CCI0B	0	1	0
		Timer1_A3.TA0	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P2.4/	4	P2.x (I/O)	I: 0; O: 1	0	0
TA1.2/		Timer1_A3.CCI2A	0	1	0
		Timer1_A3.TA2	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P2.5/	5	P2.x (I/O)	I: 0; O: 1	0	0
TA1.2/		Timer1_A3.CCI2B	0	1	0
		Timer1_A3.TA2	1	1	0
Pin Osc		Capacitive sensing	X	0	1

(1) X = don't care

Port P2 Pin Schematic: P2.6, Input/Output With Schmitt Trigger

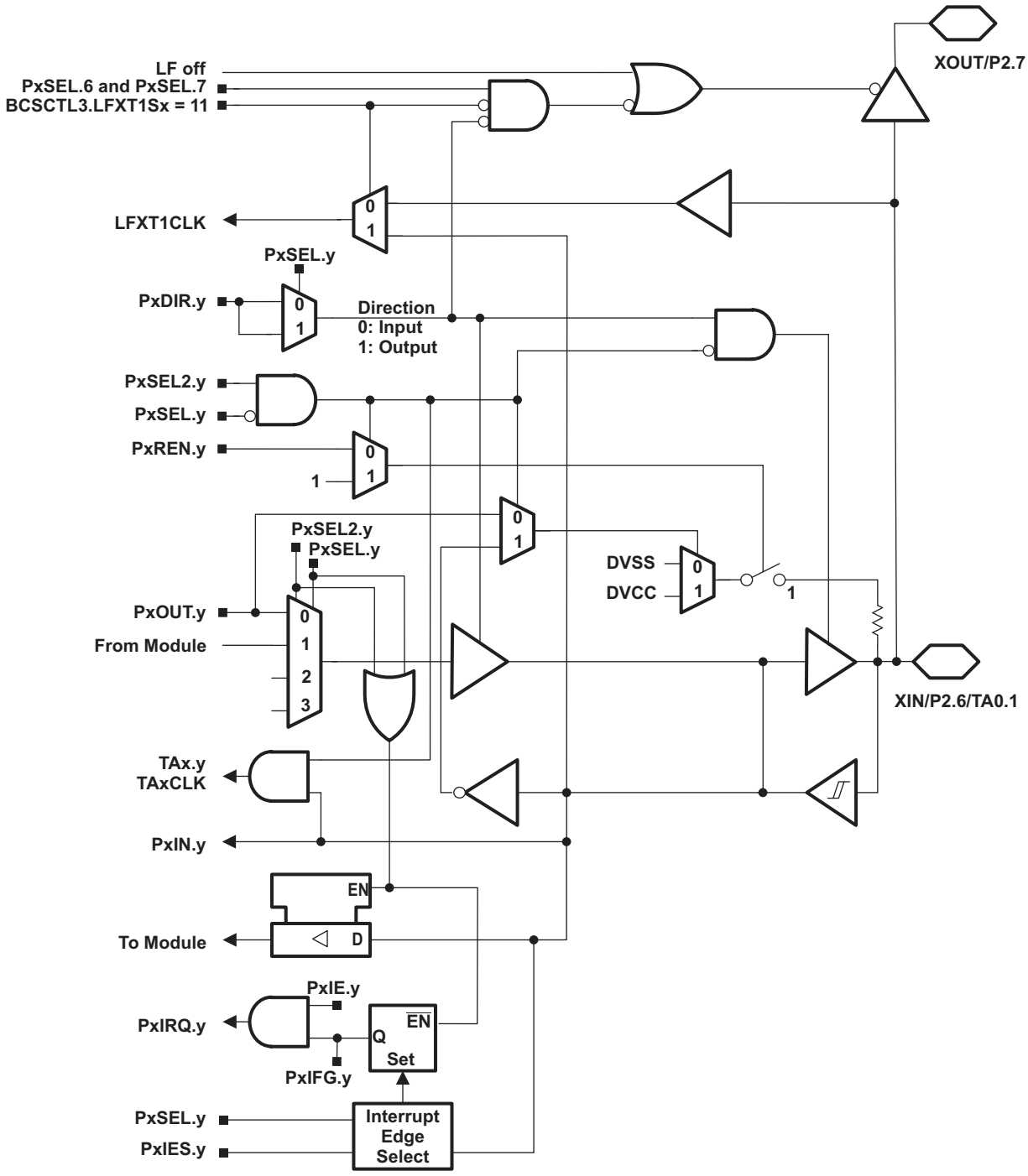


Table 21. Port P2 (P2.6) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]		
			P2DIR.x	P2SEL.6 P2SEL.7	P2SEL2.6 P2SEL2.7
XIN	6	XIN	0	1 1	0 0
P2.6		P2.x (I/O)	I: 0; O: 1	0 X	0 0
TA0.1		Timer0_A3.TA1	1	1 0	0 0
Pin Osc		Capacitive sensing	X	0 X	1 X

(1) X = don't care

Port P2 Pin Schematic: P2.7, Input/Output With Schmitt Trigger

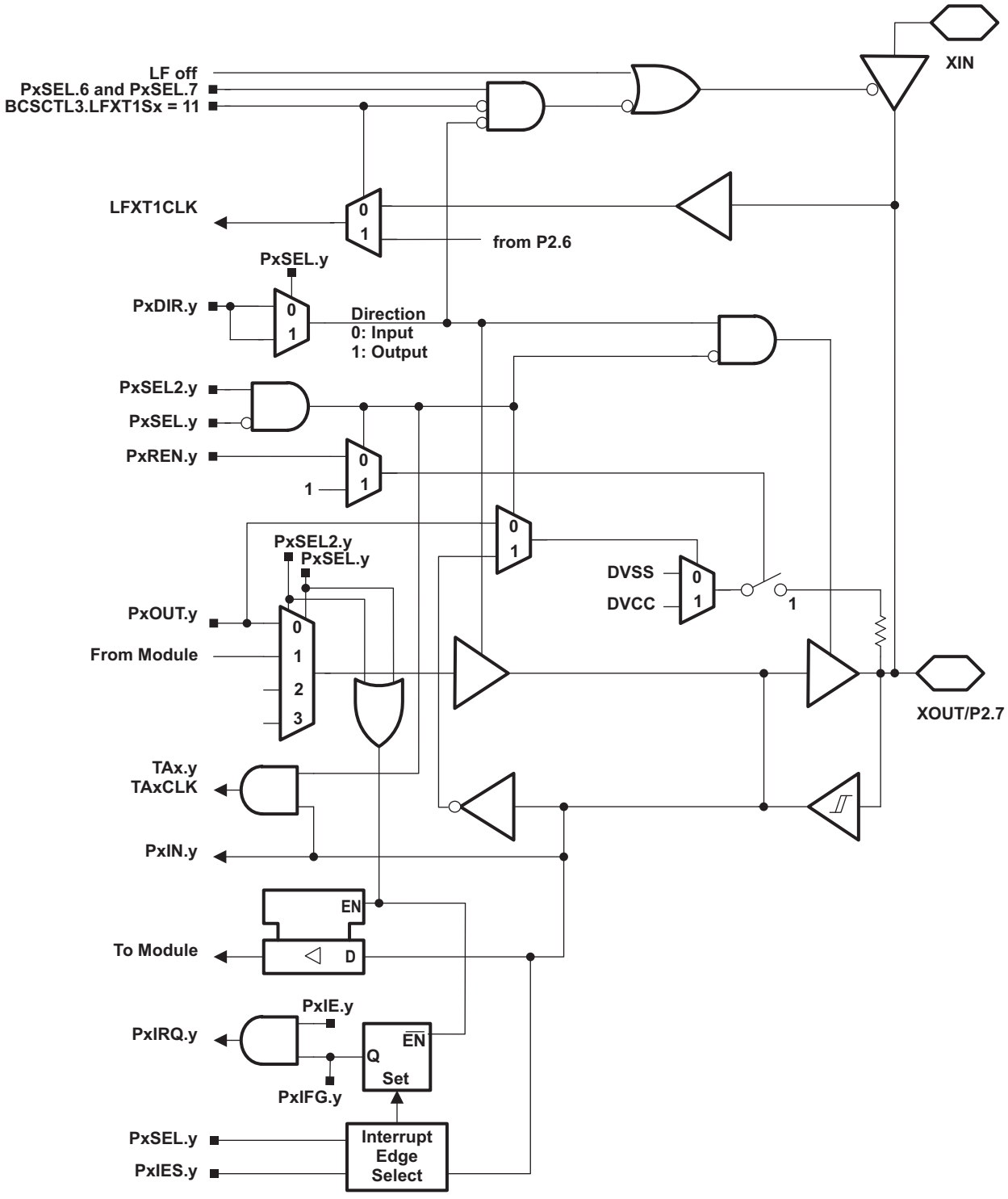


Table 22. Port P2 (P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]		
			P2DIR.x	P2SEL.6 P2SEL.7	P2SEL2.6 P2SEL2.7
XOUT/	7	XOUT	1	1 1	0 0
P2.7/		P2.x (I/O)	I: 0; O: 1	0 X	0 0
Pin Osc		Capacitive sensing	X	0 X	1 X

(1) X = don't care

Port P3 Pin Schematic: P3.0 to P3.7, Input/Output With Schmitt Trigger (28-Pin PW and 32-Pin RHB Packages Only)

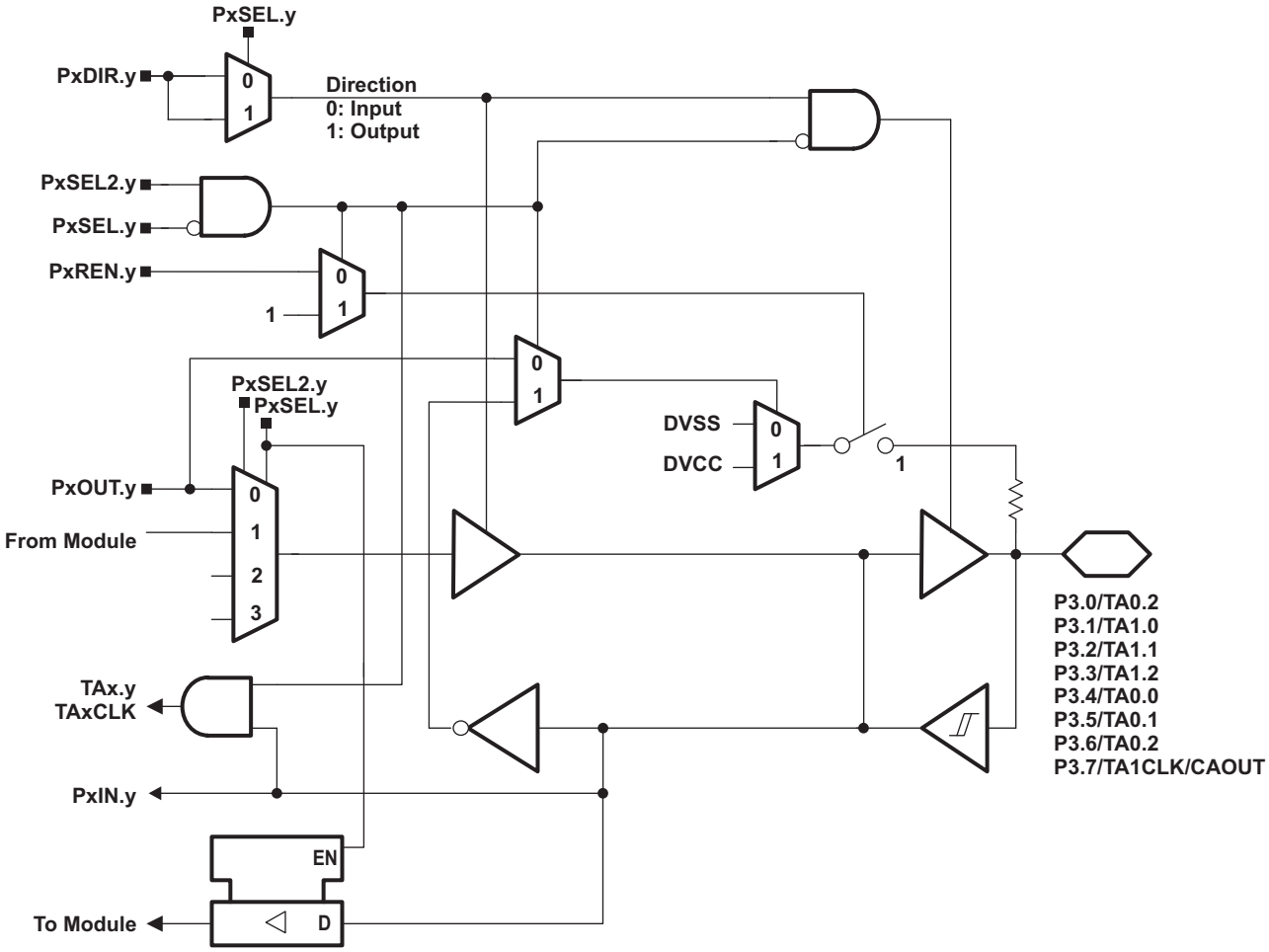


Table 23. Port P3 (P3.0 to P3.7) Pin Functions (28-Pin PW and 32-Pin RHB Packages Only)

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)		
			P3DIR.x	P3SEL.x	P3SEL2.x
P3.0/	0	P3.x (I/O)	I: 0; O: 1	0	0
TA0.2/		Timer0_A3.CCI2A	0	1	0
		Timer0_A3.TA2	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P3.1/	1	P3.x (I/O)	I: 0; O: 1	0	0
TA1.0/		Timer1_A3.TA0	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P3.2/	2	P3.x (I/O)	I: 0; O: 1	0	0
TA1.1/		Timer1_A3.TA1	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P3.3/	3	P3.x (I/O)	I: 0; O: 1	0	0
TA1.2/		Timer1_A3.TA2	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P3.4/	4	P3.x (I/O)	I: 0; O: 1	0	0
TA0.0/		Timer0_A3.TA0	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P3.5/	5	P3.x (I/O)	I: 0; O: 1	0	0
TA0.1/		Timer0_A3.TA1	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P3.6/	6	P3.x (I/O)	I: 0; O: 1	0	0
TA0.2/		Timer0_A3.TA2	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P3.7/	7	P3.x (I/O)	I: 0; O: 1	0	0
TA1CLK/		Timer1_A3.TACLK	0	1	0
CAOUT/		Comparator output	1	1	0
Pin Osc		Capacitive sensing	X	0	1

(1) X = don't care

REVISION HISTORY

REVISION	DESCRIPTION
SLAS735	Initial release
SLAS735A	Changed Control Bits / Signals column in Table 18 Changed Pin Name and Function columns in Table 23
SLAS735B	Changed Storage temperature range limit in Absolute Maximum Ratings Added BSL functions to P1.1 and P1.5 in Table 2. Added CAOUT information to Table 17.
SLAS735C	Changed T_{stg}, Programmed device, to -55°C to 150°C in Absolute Maximum Ratings. Changed TAG_ADC10_1 value to 0x10 in Table 10.
SLAS735D	Added AVCC (RHB package only, pin 29) to Table 2 Terminal Functions. Corrected typo in P3.7/TA1CLK/CAOUT description in Table 2. Corrected PW28 terminal assignment in Input and Output Pin Number columns in Table 13. Changed all port schematics (added buffer after PxOUT.y mux) in Port Schematics.
SLAS735E	Table 5 and Table 14, Corrected Timer_A register names.
SLAS735F	Added note on TC_{REF+} in 10-Bit ADC, Built-In Voltage Reference (MSP430G2x53 Only). Corrected signal names on Port P1 Pin Schematic: P1.4, Input/Output With Schmitt Trigger.
SLAS735G	Recommended Operating Conditions, Removed mention of USART module from f_{SYSTEM} description. Port P3 Pin Schematic: P3.0 to P3.7, Input/Output With Schmitt Trigger (28-Pin PW and 32-Pin RHB Packages Only), Added PW28 to available packages.
SLAS735H	Recommended Operating Conditions, Added test conditions for typical values. Pin-Oscillator Frequency – Ports Px, Corrected resistor value in note (1). POR, BOR, Added note (2).
SLAS735I	Throughout, Changed all variations of touch sense(1) to capacitive touch.
SLAS735J	Removed all information regarding MSP430G2113.

(1) TouchSense is a trademark of Immersion Corporation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430G2113IN20	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430G2113	Samples
MSP430G2113IRHB32R	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2113	Samples
MSP430G2153IN20	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430G2153	Samples
MSP430G2153IPW20	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2153	Samples
MSP430G2153IPW20R	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2153	Samples
MSP430G2153IPW28	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2153	Samples
MSP430G2153IPW28R	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2153	Samples
MSP430G2153IRHB32R	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2153	Samples
MSP430G2153IRHB32T	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2153	Samples
MSP430G2213IN20	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430G2213	Samples
MSP430G2213IPW20	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2213	Samples
MSP430G2213IPW20R	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2213	Samples
MSP430G2213IPW28	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2213	Samples
MSP430G2213IPW28R	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2213	Samples
MSP430G2213IRHB32R	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2213	Samples
MSP430G2213IRHB32T	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2213	Samples
MSP430G2253IN20	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430G2253	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430G2253IPW20	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2253	Samples
MSP430G2253IPW20R	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2253	Samples
MSP430G2253IPW28	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2253	Samples
MSP430G2253IPW28R	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2253	Samples
MSP430G2253IRHB32R	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2253	Samples
MSP430G2253IRHB32T	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2253	Samples
MSP430G2313IN20	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430G2313	Samples
MSP430G2313IPW20	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2313	Samples
MSP430G2313IPW20R	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2313	Samples
MSP430G2313IPW28	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2313	Samples
MSP430G2313IPW28R	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2313	Samples
MSP430G2313IRHB32R	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2313	Samples
MSP430G2313IRHB32T	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2313	Samples
MSP430G2353IN20	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430G2353	Samples
MSP430G2353IPW20	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2353	Samples
MSP430G2353IPW20R	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2353	Samples
MSP430G2353IPW28	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2353	Samples
MSP430G2353IPW28R	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2353	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430G2353IRHB32R	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2353	Samples
MSP430G2353IRHB32T	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2353	Samples
MSP430G2413IN20	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430G2413	Samples
MSP430G2413IPW20	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2413	Samples
MSP430G2413IPW20R	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2413	Samples
MSP430G2413IPW28	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2413	Samples
MSP430G2413IPW28R	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2413	Samples
MSP430G2413IRHB32R	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2413	Samples
MSP430G2413IRHB32T	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2413	Samples
MSP430G2453IN20	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430G2453	Samples
MSP430G2453IPW20	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2453	Samples
MSP430G2453IPW20R	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2453	Samples
MSP430G2453IPW28	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2453	Samples
MSP430G2453IPW28R	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2453	Samples
MSP430G2453IRHB32R	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2453	Samples
MSP430G2453IRHB32T	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2453	Samples
MSP430G2513IN20	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430G2513	Samples
MSP430G2513IPW20	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2513	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430G2513IPW20R	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2513	Samples
MSP430G2513IPW28	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2513	Samples
MSP430G2513IPW28R	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2513	Samples
MSP430G2513IRHB32R	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2513	Samples
MSP430G2513IRHB32T	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2513	Samples
MSP430G2553IN20	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430G2553	Samples
MSP430G2553IPW20	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2553	Samples
MSP430G2553IPW20R	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2553	Samples
MSP430G2553IPW28	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2553	Samples
MSP430G2553IPW28R	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2553	Samples
MSP430G2553IRHB32R	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2553	Samples
MSP430G2553IRHB32T	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2553	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF MSP430G2453, MSP430G2553 :

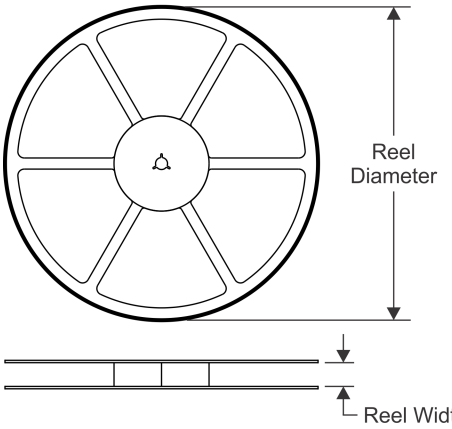
- Automotive: MSP430G2453-Q1, MSP430G2553-Q1

NOTE: Qualified Version Definitions:

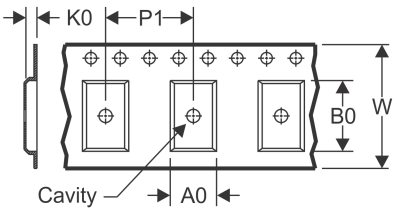
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

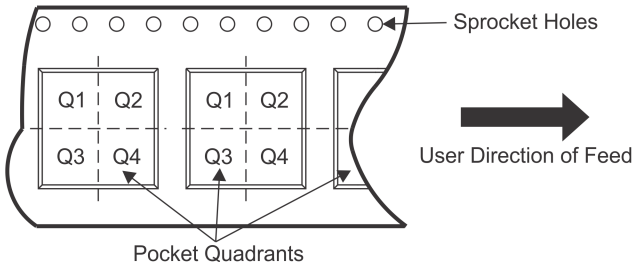


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

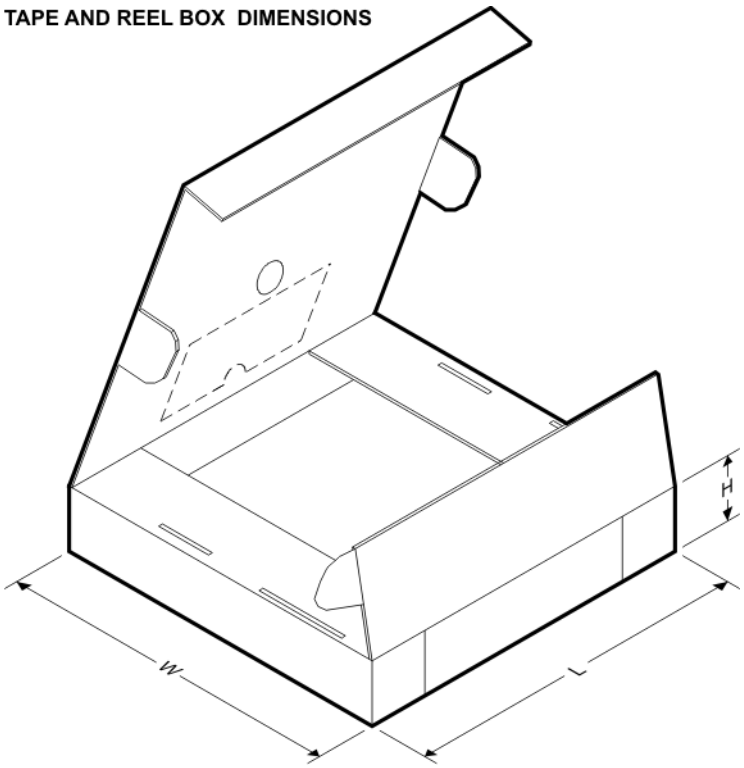


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430G2153IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2153IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2153IPW28R	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430G2153IPW28R	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430G2153IRHB32R	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2153IRHB32T	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2213IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2213IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2213IPW28R	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430G2213IPW28R	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430G2213IRHB32R	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2213IRHB32T	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2253IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2253IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2253IPW28R	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430G2253IPW28R	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430G2253IRHB32R	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2253IRHB32T	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430G2313IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2313IPW28R	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430G2313IRHB32R	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2313IRHB32T	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2353IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2353IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2353IPW28R	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430G2353IRHB32R	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2353IRHB32T	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2413IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2413IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2413IPW28R	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430G2413IPW28R	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430G2413IRHB32R	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2413IRHB32T	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2453IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2453IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2453IPW28R	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430G2453IRHB32R	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2453IRHB32T	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2513IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2513IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2513IPW28R	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430G2513IRHB32R	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2513IRHB32T	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2553IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2553IPW28R	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430G2553IRHB32R	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2553IRHB32T	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

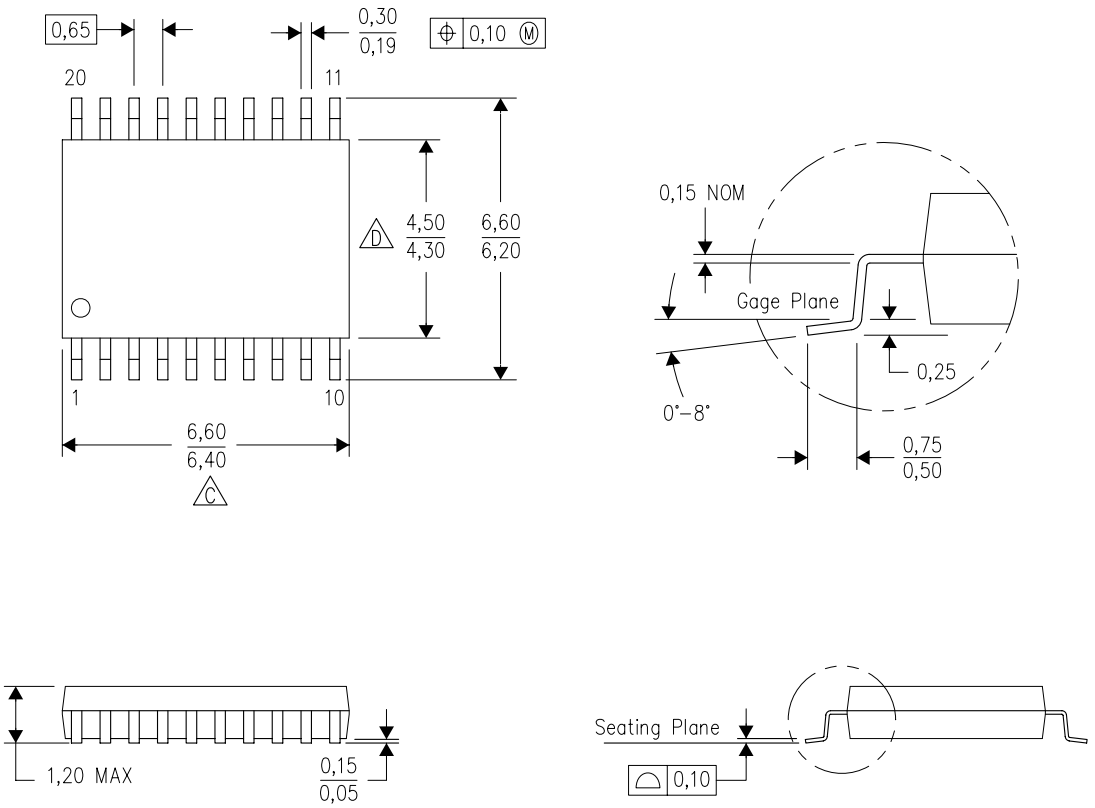


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430G2153IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2153IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2153IPW28R	TSSOP	PW	28	2000	367.0	367.0	38.0
MSP430G2153IPW28R	TSSOP	PW	28	2000	367.0	367.0	38.0
MSP430G2153IRHB32R	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430G2153IRHB32T	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430G2213IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2213IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2213IPW28R	TSSOP	PW	28	2000	367.0	367.0	38.0
MSP430G2213IPW28R	TSSOP	PW	28	2000	367.0	367.0	38.0
MSP430G2213IRHB32R	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430G2213IRHB32T	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430G2253IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2253IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2253IPW28R	TSSOP	PW	28	2000	367.0	367.0	38.0
MSP430G2253IPW28R	TSSOP	PW	28	2000	367.0	367.0	38.0
MSP430G2253IRHB32R	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430G2253IRHB32T	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430G2313IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2313IPW28R	TSSOP	PW	28	2000	367.0	367.0	38.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430G2313IRHB32R	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430G2313IRHB32T	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430G2353IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2353IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2353IPW28R	TSSOP	PW	28	2000	367.0	367.0	38.0
MSP430G2353IRHB32R	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430G2353IRHB32T	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430G2413IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2413IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2413IPW28R	TSSOP	PW	28	2000	367.0	367.0	38.0
MSP430G2413IPW28R	TSSOP	PW	28	2000	367.0	367.0	38.0
MSP430G2413IRHB32R	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430G2413IRHB32T	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430G2453IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2453IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2453IPW28R	TSSOP	PW	28	2000	367.0	367.0	38.0
MSP430G2453IRHB32R	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430G2453IRHB32T	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430G2513IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2513IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2513IPW28R	TSSOP	PW	28	2000	367.0	367.0	38.0
MSP430G2513IRHB32R	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430G2513IRHB32T	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430G2553IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2553IPW28R	TSSOP	PW	28	2000	367.0	367.0	38.0
MSP430G2553IRHB32R	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430G2553IRHB32T	VQFN	RHB	32	250	210.0	185.0	35.0

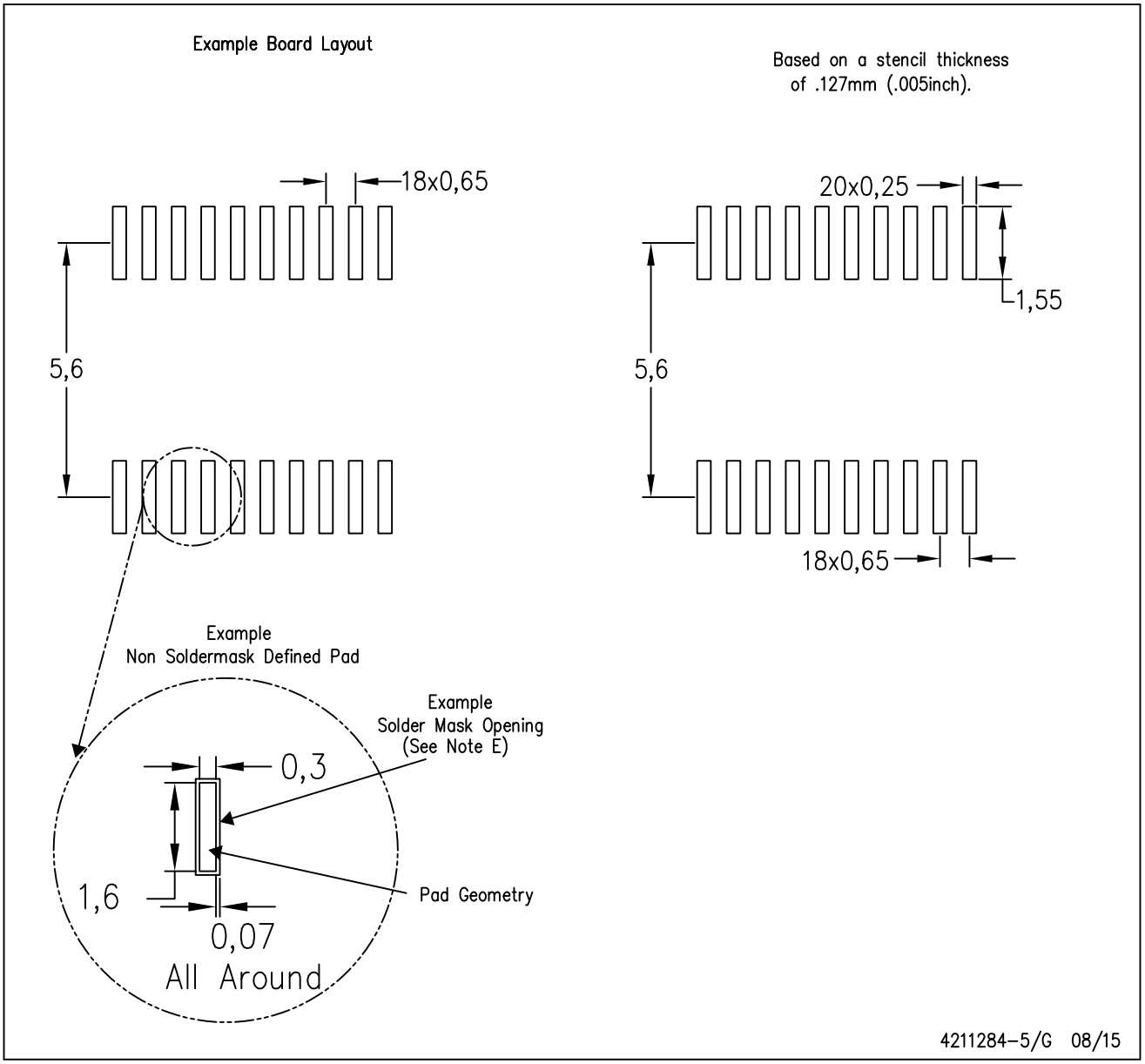
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



4040064–5/G 02/11

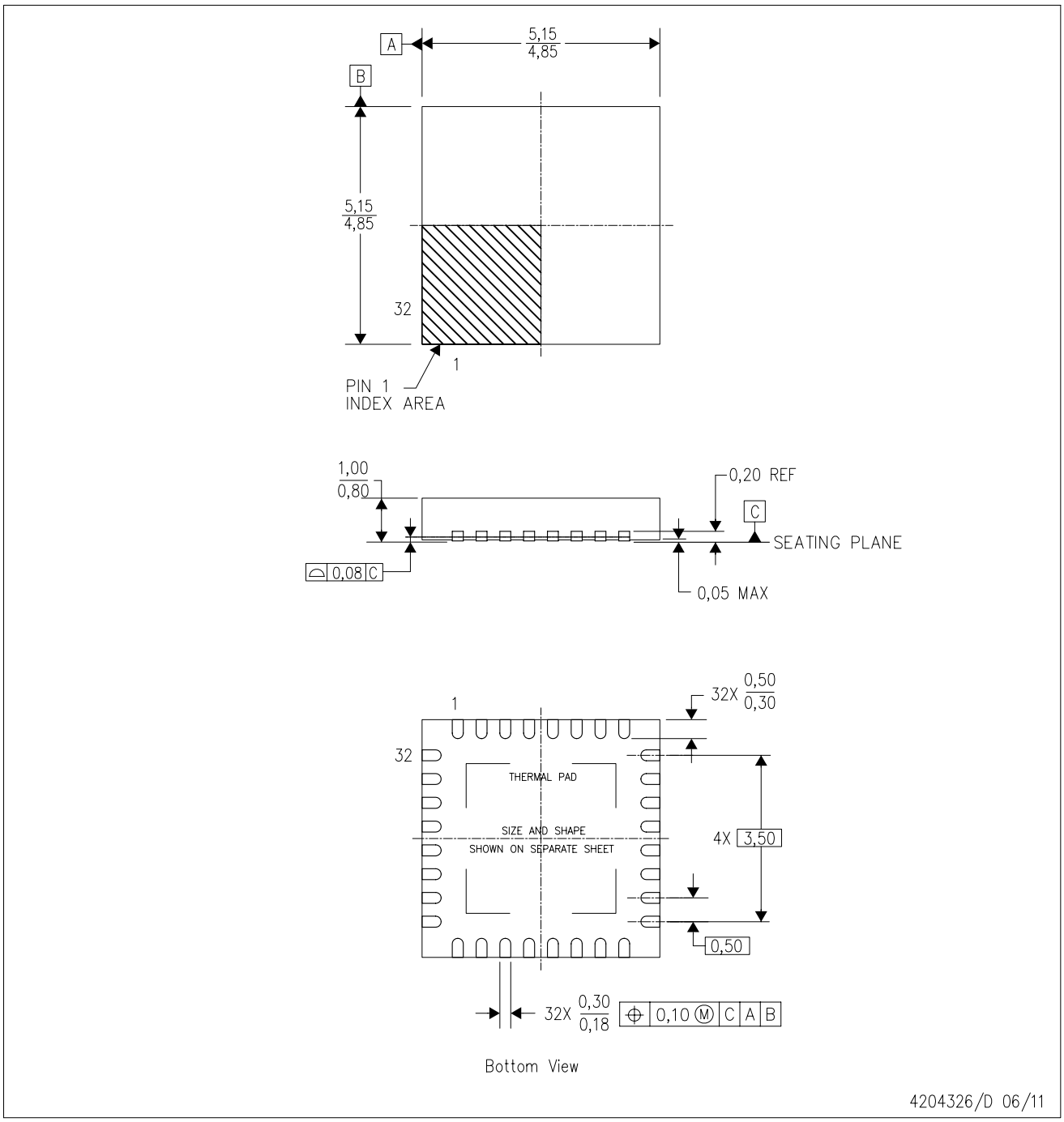
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

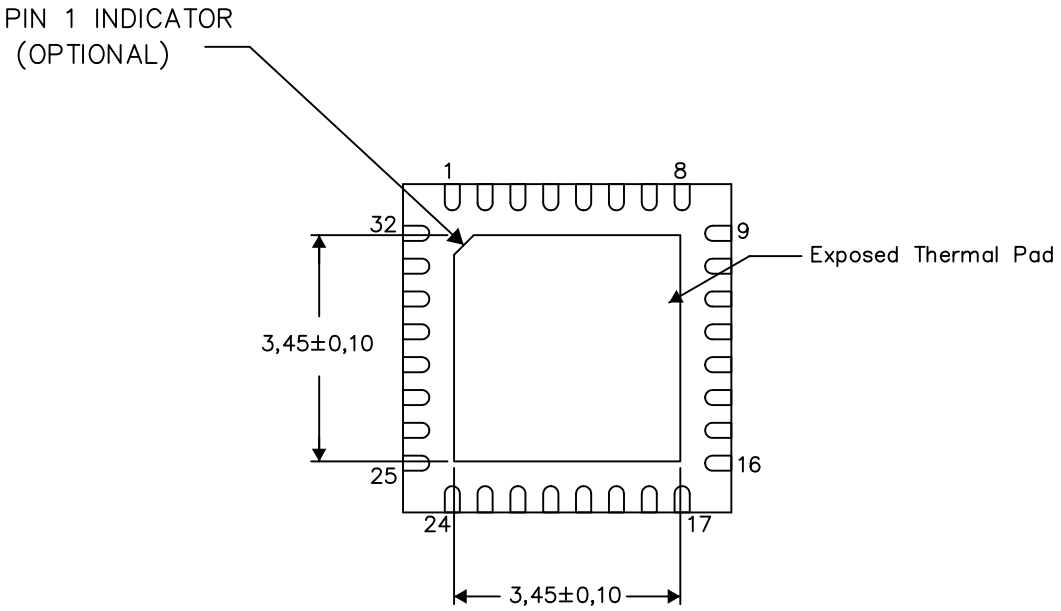
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



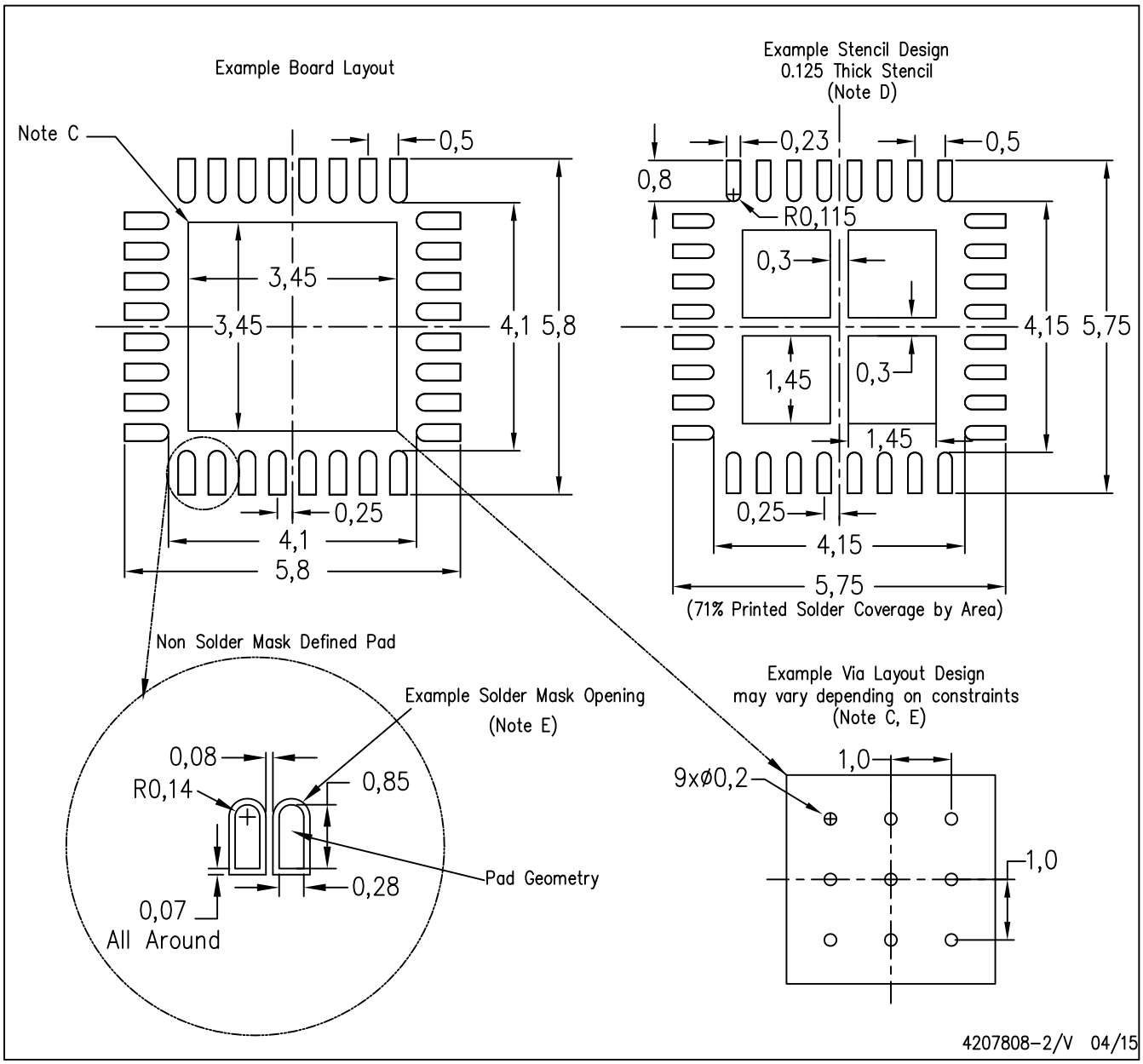
Bottom View

Exposed Thermal Pad Dimensions

4206356–2/AC 05/15

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

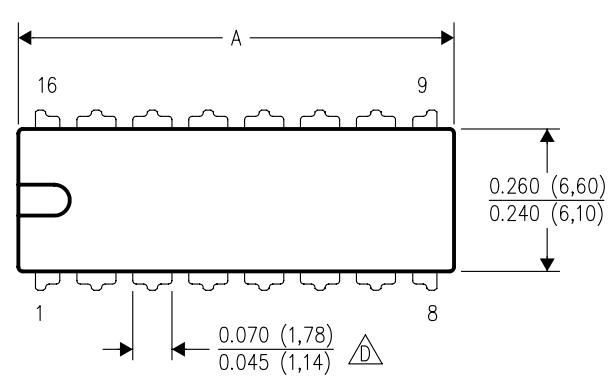


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

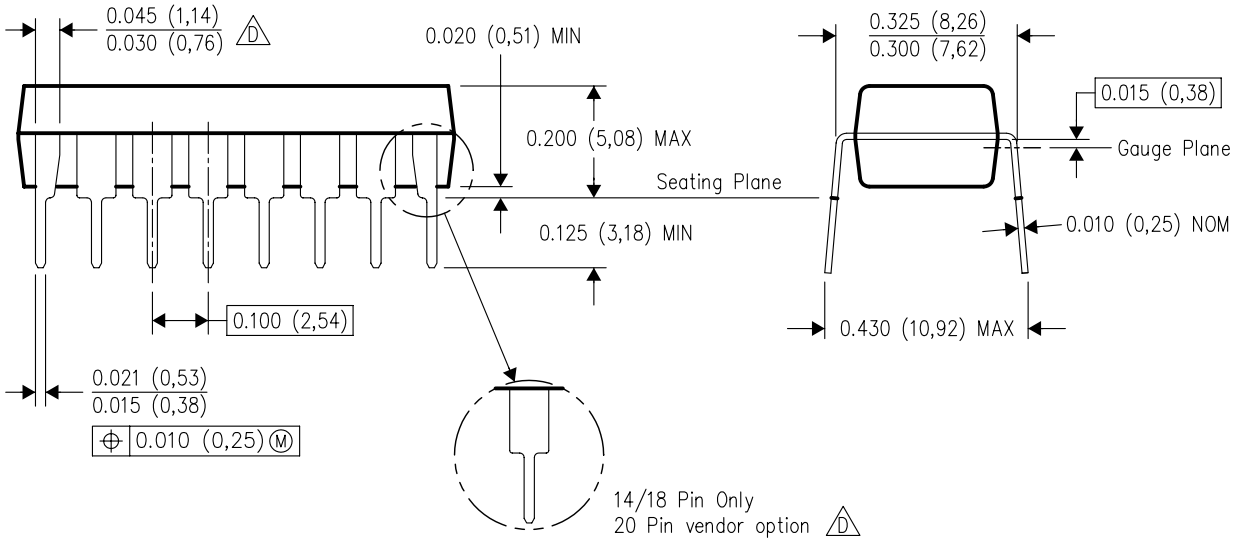
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



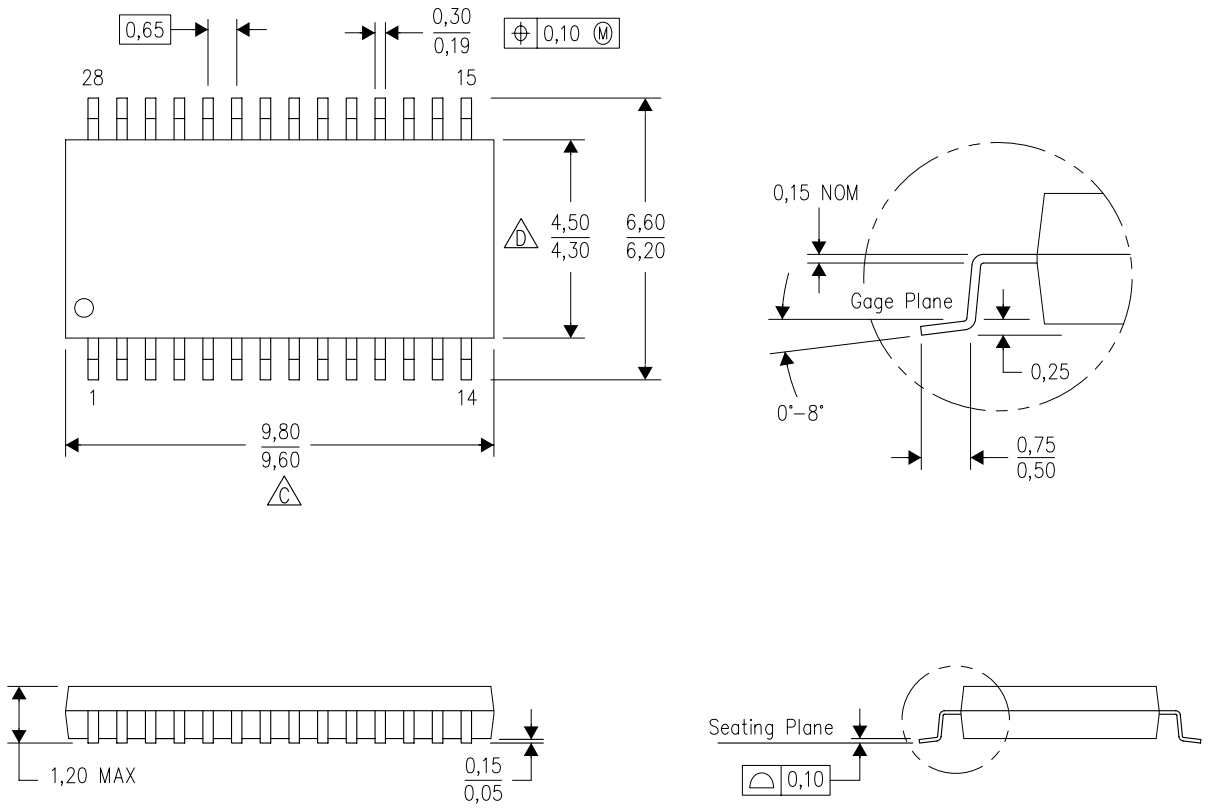
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

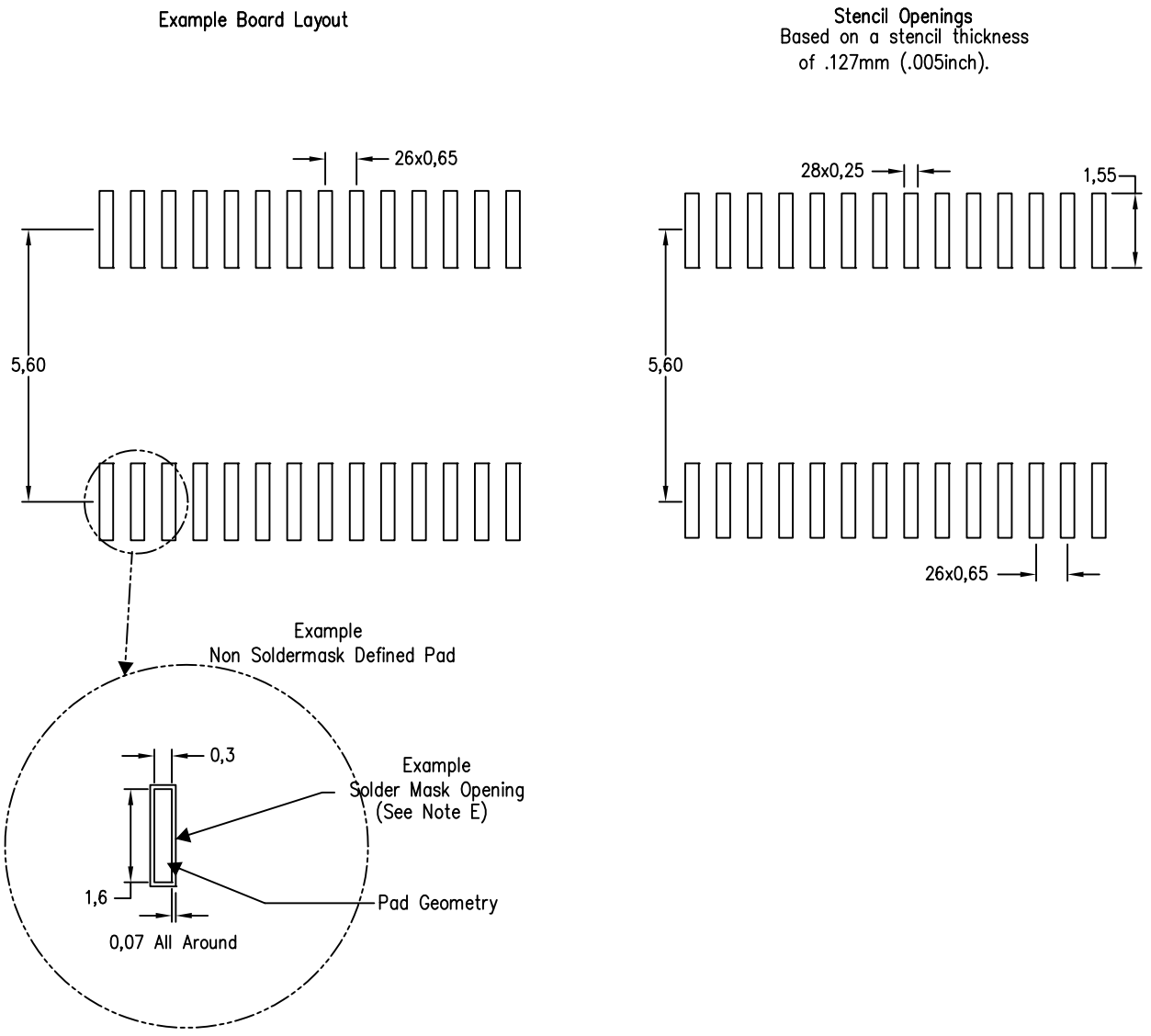
PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



4040064–7/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Technical Data Sheet
5 mm Round White LED (T-1 3/4)

Preliminary

334-15/T1C1-4WYA

Features

- Popular T-1 3/4 colorless 5mm package.
- High luminous power.
- Typical chromaticity coordinates x=0.30, y=0.29 according to CIE1931.
- Bulk, available taped on reel.
- ESD-withstand voltage: up to 4KV
- The product itself will remain within RoHS compliant version.

Descriptions

- The series is designed for application required high luminous intensity.
- The phosphor filled in the reflector converts the blue emission of InGaN chip to ideal white.

Applications

- Outdoor Displays
- Optical Indicators
- Backlighting
- Marker Lights

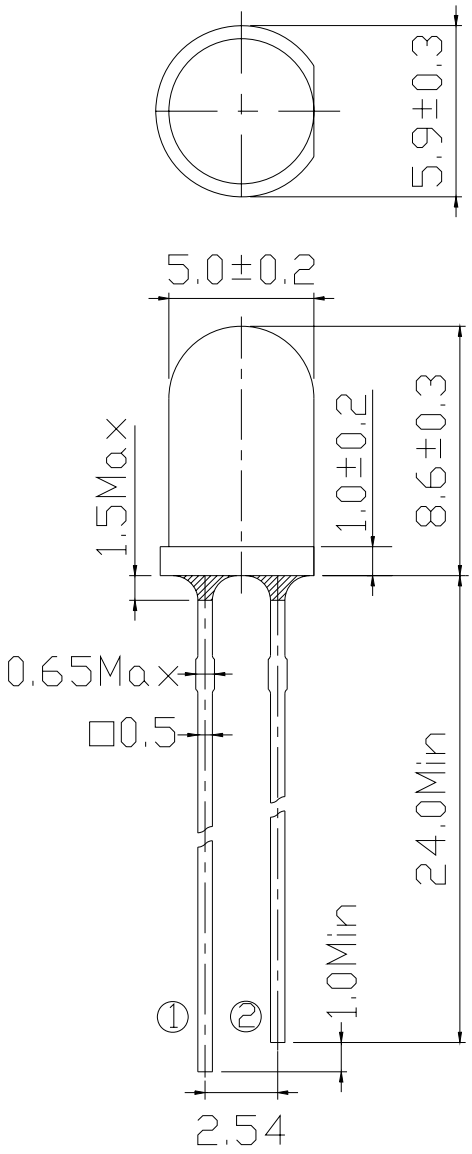
Device Selection Guide

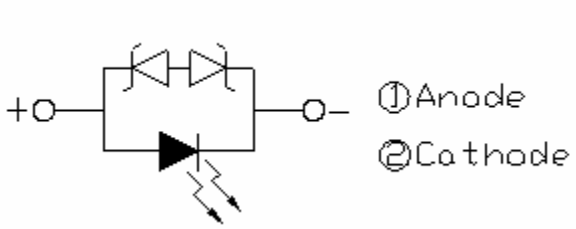
PART NO.	Chip		Lens Color
	Material	Emitted Color	
334-15/T1C1-4WYA	InGaN	White	Water Clear

Technical Data Sheet
5 mm Round White LED (T-1 3/4) Preliminary

334-15/T1C1-4WYA

Package Dimensions





Notes:

1.All dimensions are in millimeters, and tolerance is 0.25mm except being specified.

2.Lead spacing is measured where the lead emerges from the package.

3.Protruded resin under flange is 1.5mm Max. LED.

Technical Data Sheet
5 mm Round White LED (T-1 3/4) Preliminary

334-15/T1C1-4WYA

Absolute Maximum Ratings (Ta=25℃)

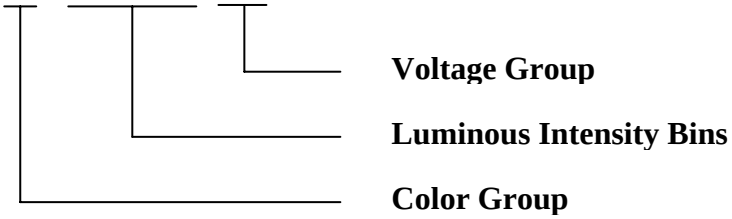
Parameter	Symbol	Rating	Unit
Continuous Forward Current	I_F	30	mA
Peak Forward Current(Duty /10 @ 1KHZ)	I_{FP}	100	mA
Reverse Voltage	V_R	5	V
Operating Temperature	T_{opr}	-40 ~ +85	℃
Storage Temperature	T_{stg}	-40 ~ +100	℃
Soldering Temperature (T=5 sec)	T_{sol}	260 ± 5	℃
Power Dissipation	P_d	100	mW
Zener Reverse Current	Iz	100	mA
Electrostatic Discharge	ESD	4K	V

Technical Data Sheet
5 mm Round White LED (T-1 3/4) Preliminary

334-15/T1C1-4WYA

Production Designation

334-15/T1C1-□ □ □ □



Electro-Optical Characteristics (Ta=25℃)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Forward Voltage	V_F	I_F=20mA	3.0	----	3.6	V
Zener Reverse Voltage	Vz	Iz=5mA	5.2	----	----	V
Reverse Current	I_R	V_R=5V	----	----	50	uA
Luminous Intensity	I_V	I_F=20mA	14250	----	28500	mcd
Viewing Angle	2θ 1/2	I_F=20mA	----	15	----	deg
Chromaticity Coordinates	x	I_F=20mA	----	0.30	----	
	y		----	0.29	----	

Luminous Intensity Combination (mcd at 20mA)

Rank	Min	Max
W	14250	18000
X	18000	22500
Y	22500	28500

*Measurement Uncertainty of Luminous Intensity: ±15%

Forward Voltage Combination (V at 20mA)

Group	A			
Rank	0	1	2	3
Min.	2.80	3.00	3.20	3.40
Max.	3.00	3.20	3.40	3.60

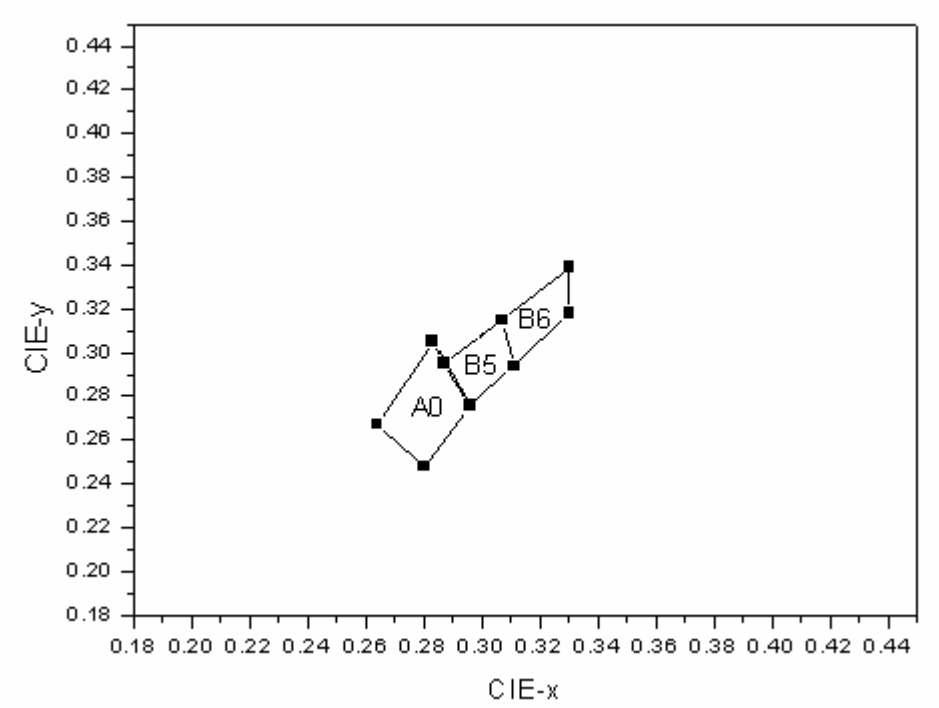
*Measurement Uncertainty of Forward Voltage：±0.1V

Color Combination (at 20mA)

Group	Bins
4	A0+B5+B6

334-15/T1C1-4WYA

CIE Chromaticity Diagram



Color Ranks (IF=20mA，Ta=25℃)

Color Ranks		CIE			
A0	X	0.264	0.283	0.296	0.28
	Y	0.267	0.305	0.267	0.248
B5	X	0.287	0.307	0.311	0.296
	Y	0.295	0.315	0.294	0.276
B6	X	0.307	0.33	0.33	0.311
	Y	0.315	0.339	0.318	0.294

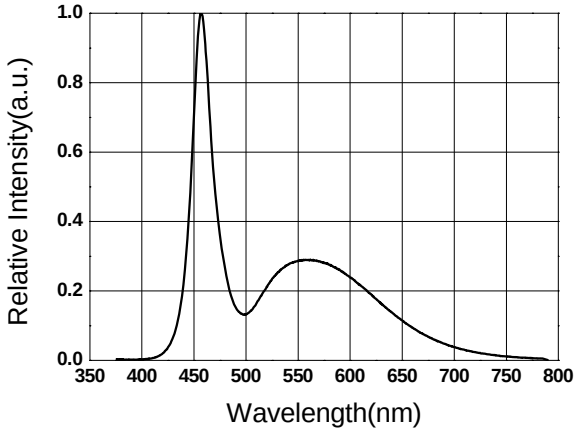
*Measurement uncertainty of the color coordinates：±0.01

Technical Data Sheet
5 mm Round White LED (T-1 3/4) Preliminary

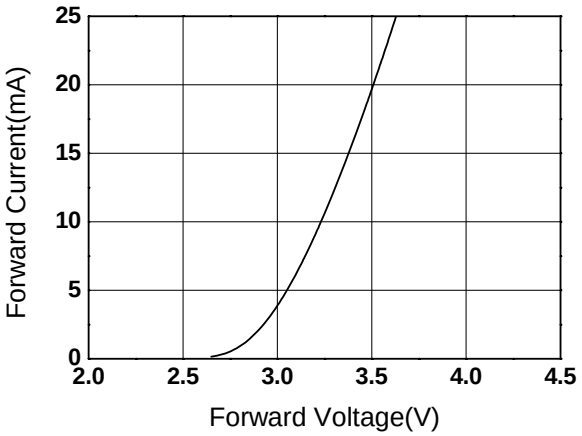
334-15/T1C1-4WYA

Typical Electro-Optical Characteristics Curves

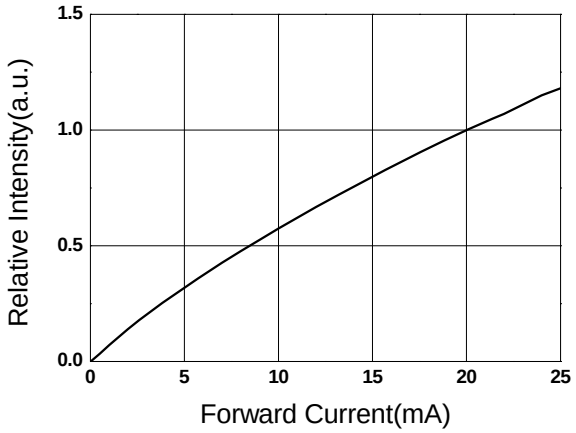
Relative Intensity vs. Wavelength



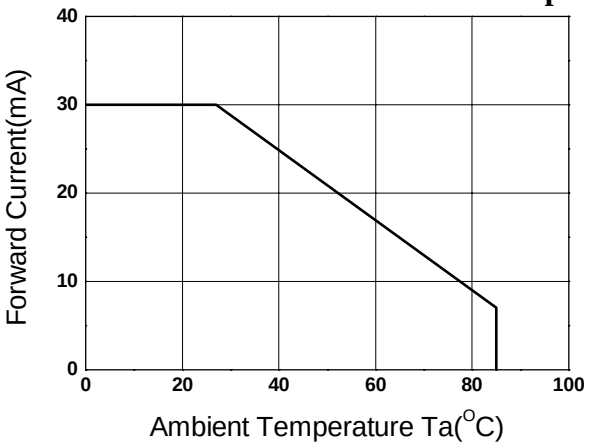
Forward Current vs. Forward Voltage



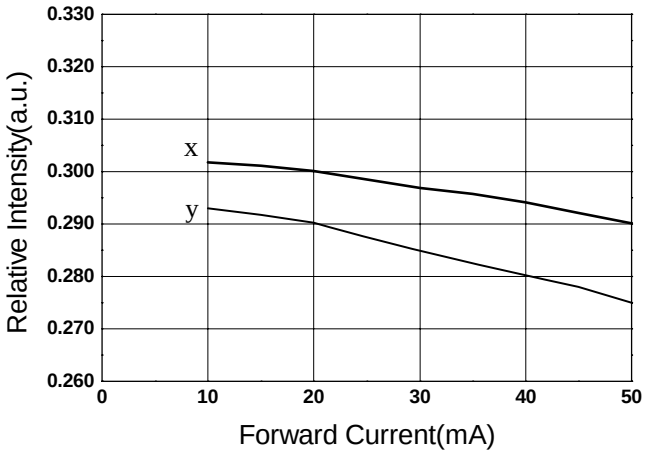
Relative Intensity vs. Forward Current



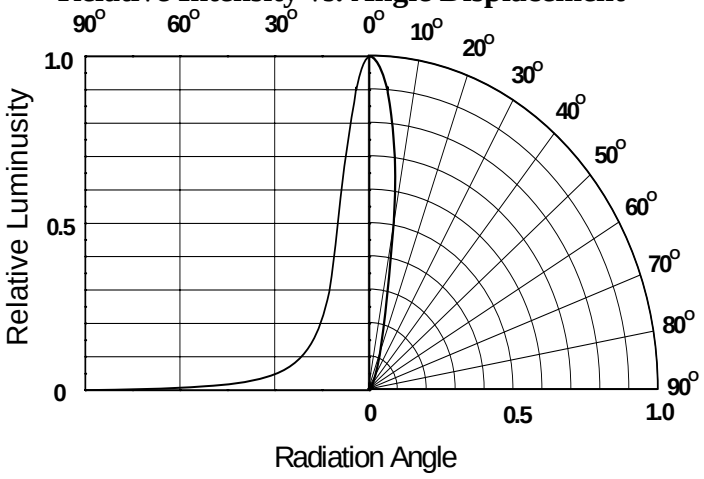
Forward Current vs. Ambient Temp.



Chromaticity Coordinate vs. Forward Current



Relative Intensity vs. Angle Displacement



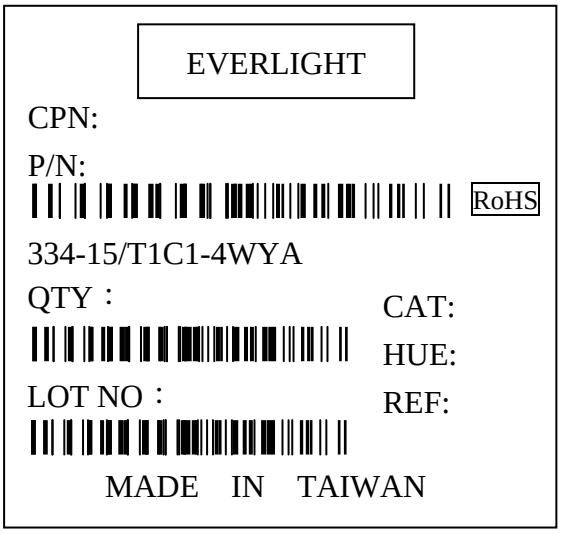
Technical Data Sheet
5 mm Round White LED (T-1 3/4) Preliminary

334-15/T1C1-4WYA

Packing Quantity Specification

1. 500PCS/1Bag，5Bags/1Box
2. 10Boxes/1Carton

Label Form Specification

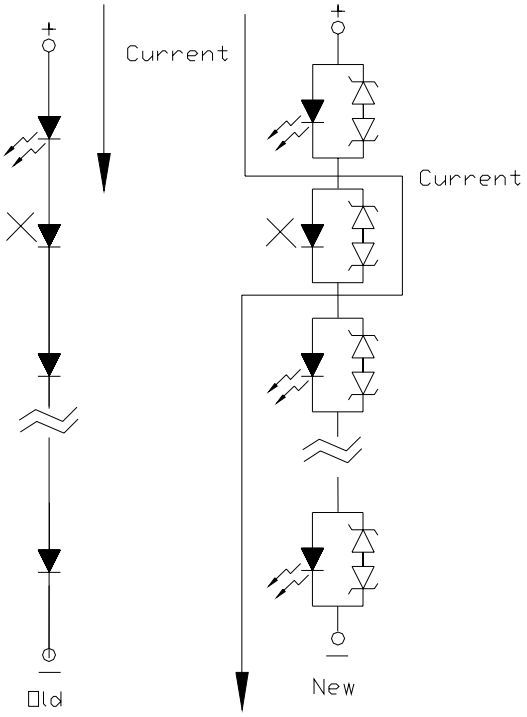


CPN: Customer's Production Number
P/N: Production Number
QTY: Packing Quantity
CAT: Ranks of Luminous Intensity and Forward Voltage
HUE: Color Rank
REF: Reference
LOT No: Lot Number
MADE IN TAIWAN: Production Place

334-15/T1C1-4WYA

Notes

1. Above specification may be changed without notice. EVERLIGHT will reserve authority on material change for above specification.
2. When using this product, please observe the absolute maximum ratings and the instructions for using outlined in these specification sheets. EVERLIGHT assumes no responsibility for any damage resulting from use of the product which does not comply with the absolute maximum ratings and the instructions included in these specification sheets.
3. These specification sheets include materials protected under copyright of EVERLIGHT corporation. Please don't reproduce or cause anyone to reproduce them without EVERLIGHT's consent.
4. Below the zener reference voltage Vz, all the current flows through LED and as the voltage rises to Vz, the zener diode "breakdown." If the voltage tries to rise above Vz current flows through the zener branch to keep the voltage at exactly Vz.
5. When the LED is connected using serial circuit, if either piece of LED is no light up but current can't flow through causing others to light down. In new design, the LED is parallel with zener diode. if either piece of LED is no light up but current can flow through causing others to light up



6. Soldering Condition

Careful attention should be paid during soldering. When soldering, leave more then 3mm from solder joint to case, and soldering beyond the base of the tie bar is recommended.

Avoiding applying any stress to the lead frame while the LEDs are at high temperature particularly when soldering.

Recommended soldering conditions:

Hand Soldering		DIP Soldering	
Temp. at tip of iron	400℃ Max. (30W Max.)	Preheat temp.	100℃ Max. (60 sec Max.)
Soldering time	3 sec Max.	Bath temp.	265 Max.
Distance	3mm Min.(From solder joint to case)	Bath time.	5 sec Max.
		Distance	3mm Min.

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Office: No 25, Lane 76, Sec 3, Chung Yang Rd, Tucheng, Taipei 236, Taiwan, R.O.C
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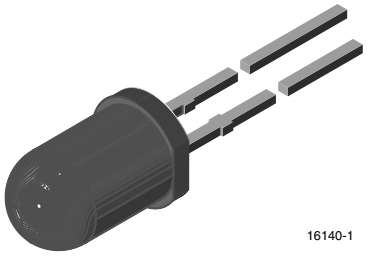
Fax: 886-2267-6244, 2267-6189, 2267-6306
http:\\www.everlight.com

Silicon PIN Photodiode



FEATURES

- Package type: leaded
- Package form: T-1¾
- Dimensions (in mm): Ø 5
- Radiant sensitive area (in mm^2): 0.78
- Leads with stand-off
- High radiant sensitivity
- Daylight blocking filter matched with 870 nm to 950 nm emitters
- High bandwidth: > 100 MHz at V_R = 12 V
- Fast response times
- Angle of half sensitivity: φ = ± 20°
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

e4

RoHS COMPLIANT

DESCRIPTION

BPV10NF is a PIN photodiode with high speed and high radiant sensitivity in black, T-1¾ plastic package with daylight blocking filter. Filter bandwidth is matched with 870 nm to 950 nm IR emitters.

APPLICATIONS

- High speed detector for infrared radiation
- Infrared remote control and free air data transmission systems, e.g. in combination with TSFFxxxx series IR emitters

PRODUCT SUMMARY			
COMPONENT	I_{ra} (µA)	φ (deg)	$\lambda_{0.5}$ (nm)
BPV10NF	60	± 20	790 to 1050

Note

- Test condition see table “Basic Characteristics”

ORDERING INFORMATION			
ORDERING CODE	PACKAGING	REMARKS	PACKAGE FORM
BPV10NF	Bulk	MOQ: 4000 pcs, 4000 pcs/bulk	T-1¾
BPV10NF-CS21	Reel	MOQ: 5000 pcs, 1000 pcs/reel	T-1¾

Note

- MOQ: minimum order quantity

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25 °C, unless otherwise specified)				
PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Reverse voltage		V_R	60	V
Power dissipation	$T_{amb} \leq 25$ °C	P_V	215	mW
Junction temperature		T_j	100	°C
Operating temperature range		T_{amb}	-40 to +100	°C
Storage temperature range		T_{stg}	-40 to +100	°C
Soldering temperature	t ≤ 5 s, 2 mm from body	T_{sd}	260	°C
Thermal resistance junction / ambient	Connected with Cu wire, 0.14 mm^2	R_{thJA}	350	K/W

BASIC CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)						
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Forward voltage	I_F = 50 mA	V_F		1.0	1.3	V
Breakdown voltage	I_R = 100 µA, E = 0	$V_{(BR)}$	60			V
Reverse dark current	V_R = 20 V, E = 0	I_{ro}		1	5	nA
Diode capacitance	V_R = 0 V, f = 1 MHz, E = 0	C_D		11		pF
Open circuit voltage	E_e = 1 mW/cm², λ = 870 nm	V_O		450		mV
Short circuit current	E_e = 1 mW/cm², λ = 870 nm	I_K		50		µA
Reverse light current	E_e = 1 mW/cm², λ = 870 nm, V_R = 5 V	I_{ra}		55		µA
	E_e = 1 mW/cm², λ = 950 nm, V_R = 5 V	I_{ra}	30	60		µA
Temperature coefficient of I_{ra}	E_e = 1 mW/cm², λ = 870 nm, V_R = 5 V	TK_{Ira}		-0.1		%/K
Absolute spectral sensitivity	V_R = 5 V, λ = 870 nm	s(λ)		0.55		A/W
Angle of half sensitivity		φ		± 20		deg
Wavelength of peak sensitivity		λ_p		940		nm
Range of spectral bandwidth		$\lambda_{0.5}$		790 to 1050		nm
Quantum efficiency	λ = 950 nm	η		70		%
Noise equivalent power	V_R = 20 V, λ = 950 nm	NEP		3×10^{-14}		W/√Hz
Detectivity	V_R = 20 V, λ = 950 nm	D*		3×10^{12}		cm√Hz/W
Rise time	V_R = 50 V, R_L = 50 Ω, λ = 820 nm	t_r		2.5		ns
Fall time	V_R = 50 V, R_L = 50 Ω, λ = 820 nm	t_f		2.5		ns

BASIC CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

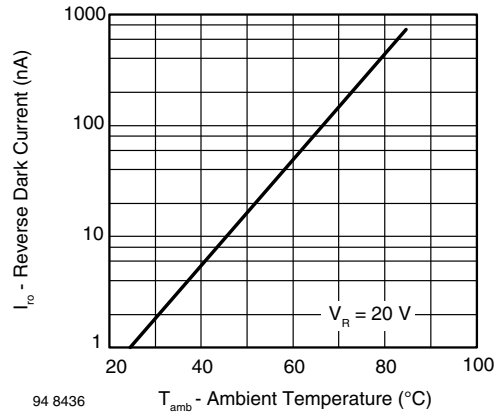


Fig. 1 - Reverse Dark Current vs. Ambient Temperature

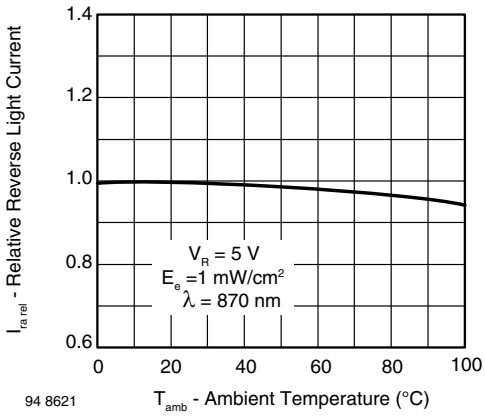


Fig. 2 - Relative Reverse Light Current vs. Ambient Temperature

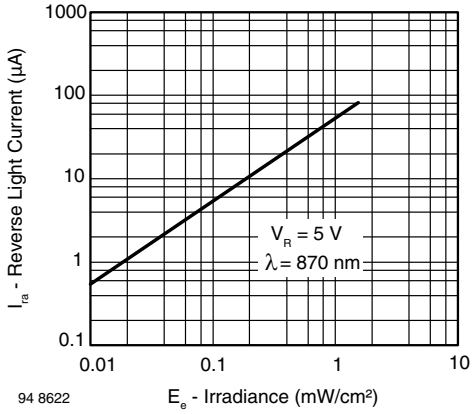


Fig. 3 - Reverse Light Current vs. Irradiance

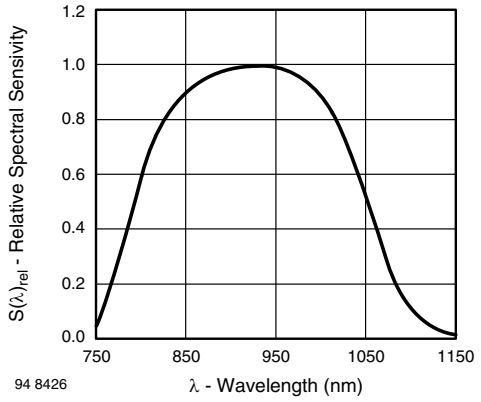


Fig. 6 - Relative Spectral Sensitivity vs. Wavelength

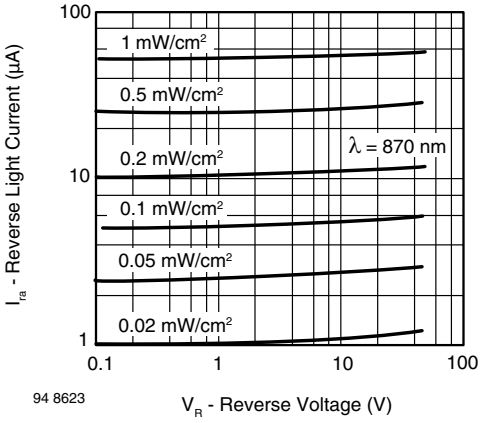


Fig. 4 - Reverse Light Current vs. Reverse Voltage

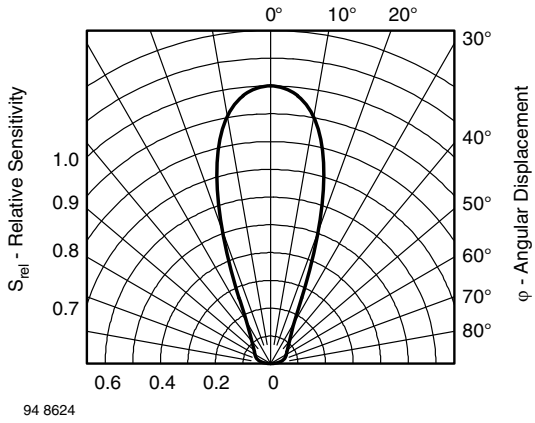


Fig. 7 - Relative Radiant Sensitivity vs. Angular Displacement

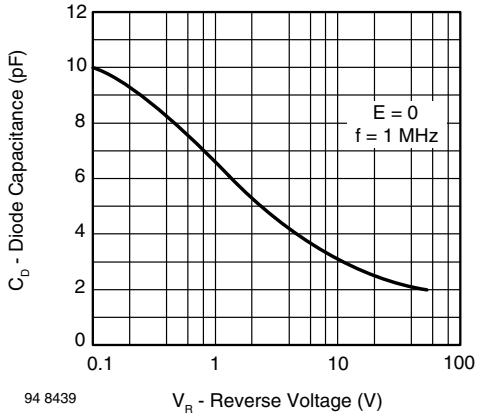
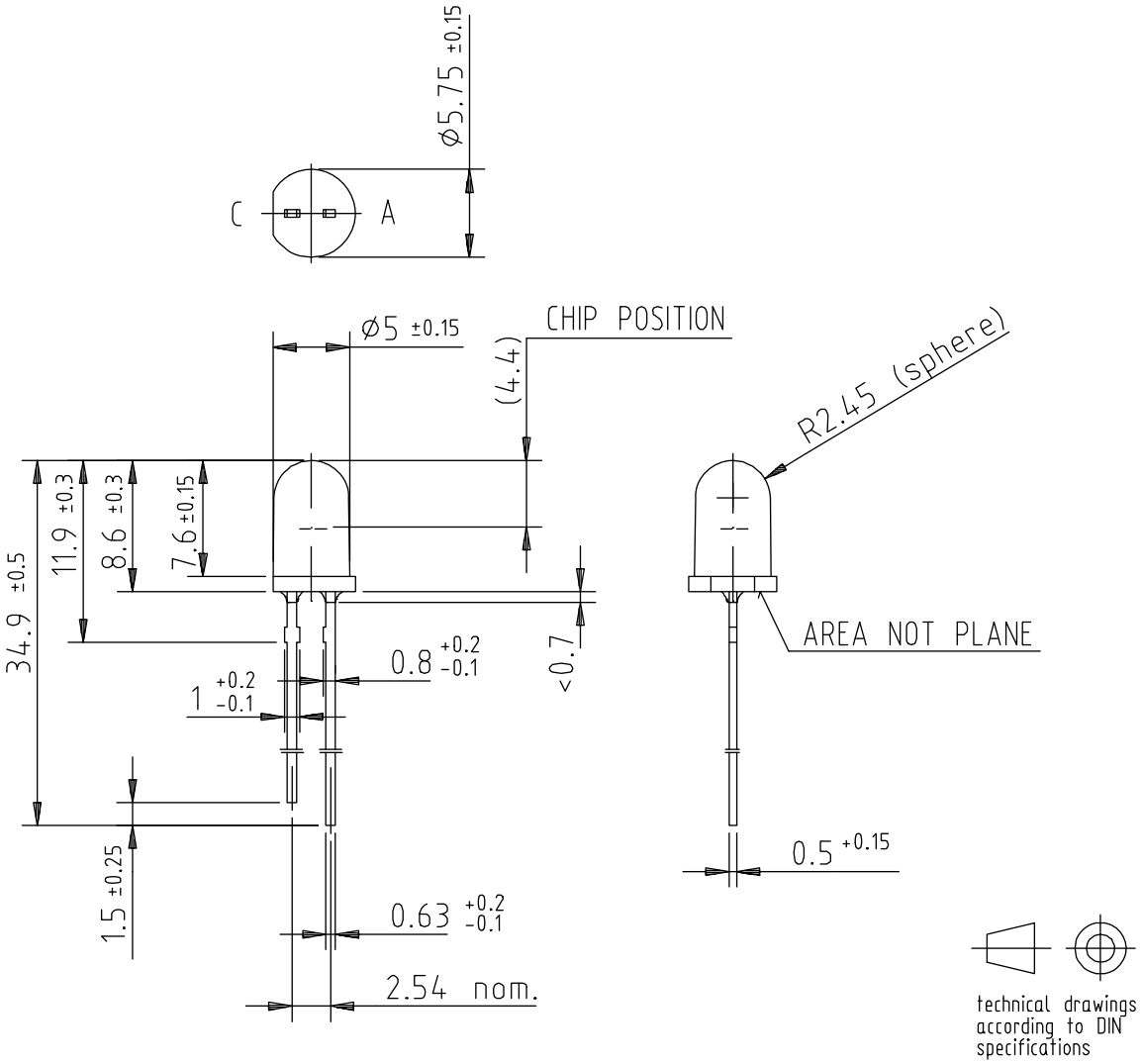


Fig. 5 - Diode Capacitance vs. Reverse Voltage

PACKAGE DIMENSIONS in millimeters



Drawing-No.: 6.544-5185.01-4

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S.N	Checklist Item	Y/N
1	Is the Cover page in proper format?	✓
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3	Is the Certificate from the Supervisor in proper format? Has it been signed?	✓
4	Is Abstract included in the Report? Is it properly written?	✓
5	Does the Table of Contents' page include chapter page numbers?	✓
6	Is Introduction included in the report? Is it properly written?	✓
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	ii. Are the Figures numbered properly?	✓
	iii. Are the Tables numbered properly?	✓
	iv. Are the Captions for the Figures and Tables proper?	✓
	v. Are the Appendices numbered?	✓
7	Does the Report have Conclusions/ Recommendations of the work?	✓
8	Are References/ Bibliography given in the Report?	✓
9	Have the References been cited in the Report?	✓
10	Is the citation of References/ Bibliography in proper format?	✓