PERFORMANCE ANALYSIS OF HIGH SPEED HYBRID CMOS FULL ADDERS CIRCUITS FOR LOW VOLTAGE VLSI DESIGN

A PROJECT REPORT

Submitted in partial fulfillment of the requirement for the award of the Degree of

BACHELOR OF TECHNOLOGY
IN
ELECTRONICS AND COMMUNICATION ENGINEERING

by

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May 2020

CERTIFICATE

This is to certify that the Project work titled "***Performance Analysis of High Speed Hybrid CMOS Full Adder Circuits for Low Voltage VLSI Design***" that is being submitted by ***V Shiva Sai (17BEC1216), M Bala Venkata Sri Harsha(17BEC1195)*** and ***C Harshavardhan Reddy (17BEC1200)*** is in partial fulfillment of the requirements for the award of **Bachelor of Technology in Electronics and Communication Engineering**, is a record of bonafide work done under my guidance. The contents of this Project work, in full or in parts, have neither been taken from any other source nor have been submitted to any other Institute or University for award of any degree or diploma and the same is certified.

Dr. Ravi Sankar A
(Guide)

The Project Report is satisfactory / unsatisfactory

Internal Examiner **External Examiner**

Approved by

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ACKNOWLEDGEMENT

The students are free to acknowledge all those he/she feels to acknowledge on the basis of the guidance and help provided during the implementation of the project.

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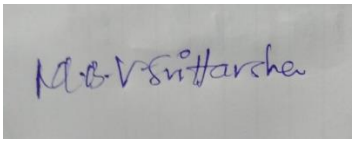

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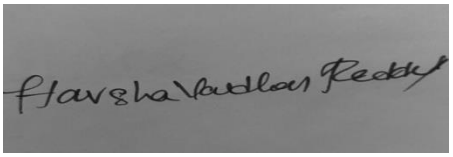

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ABSTRACT

The performance of many digital signal systems depends on the functioning of mathematical circuits to perform difficult computations such as convolution, optimization. Fast arithmetic calculation circuits include add, subtract and multiplier circuits that are widely used in mass compression systems (VLSI). With advancement in technology, several researchers have tried design adders which supply high speed, low power consumption.

In addition, Now-a-days companies push their limits on features and specializations on hand held devices, so companies tries to improve the battery life by reducing the power consumption in devices, and designers are forced to go all-out for a smaller area of silicon, the size and weight of wires. Some of them use one complete adder style while others use multiple styles in their operation.

Power or Energy is an important factor, which is why designers do their best to save while building a circuitry. Power mainly depends on switching performance, node capacitance (composed of gates, distribution, and wire strength). At the circuit level, decreasing the VDD voltage and decreasing the Vth accordingly can lessen power consumption.

There are many methodologies which are available to implement low power designs. At present we mainly focus on full adders because in any device it consists of ALU which is responsible for complex addition, subtraction and in a single chip consists of billions of transistors which has its own responsibility so a single ALU part consuming huge amount of power is not appreciable. But, low power improves latency of the circuit and undermines the stability of circuits proposed in a particular conceptual style. The main important difficulty is to lowering the supply voltage is a large number of transistor counts and the problem of Vth loss. By selecting the right amount (W / L) we can reduce the power distribution without reducing the transmission power.

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CHAPTER 1

INTRODUCTION

The performance of many digital signal systems depends on the functioning of mathematical circuits to perform difficult computations such as convolution, optimization. Fast arithmetic calculation circuits include add, subtract and multiplier circuits that are widely used in mass compression systems (VLSI). In addition, Now-a-days companies push their limits on features and specializations on hand held devices, so companies tries to improve the battery life by reducing the power consumption in devices, and designers are forced to go all-out for a smaller area of silicon, the size and weight of wires. Some of them use one complete adder style while others use multiple styles in their operation.

There are many methodologies which are available to implement low power designs. At present we mainly focus on full adders because in any device it consists of ALU which is responsible for complex addition, subtraction and in a single chip consists of billions of transistors which has its own responsibility so a single ALU part consuming huge amount of power is not appreciable

1.1 Objectives:

The following are the objectives of this project:

- To design different styles of full adders.
- To decrease the transistor count for construction of full adder.
- To observe the characteristics of power, delay and PDP with respective to supply voltage.
- To simulate the designed full adders in Cadence Software using 45nm technology
- To reduce the power consumption in 1-bit full adder.

1.2 Background and Literature Survey:

A similar project was undertaken by various papers and they have implemented 1-bit full adder using different logic styles. There are different ways in order to build a full adder some of them are build by using pass transistor, transmission gates and hybrid XOR/XNOR logic styles. The main use of these styles is to reduce the transistor count which in turn helps in power reduction. From the given below literature survey we have observed that the new hybrid XOR/XNOR logic styles produces comparatively less power dissipation than other. By using this literature survey we have designed different types of full adders and observed their power , delay and PDP characteristics in according to the supply voltage.

Table 1.1 shows the articles and journals which had the information about different designs of full adders and their power, delay analysis.

Table 1.1 Literature Survey

Sl. No	Name of article	Name of journal	Information included
1.	Low Power High Speed 1-bit Full Adder Circuit design at 45nm CMOS Technology	International conference on Recent Innovations is Signal Processing and Embedded Systems (RISE - 2017) 27-29 October,2017	Power, Delay, PDP Analysis of 10T Full Adder.
2.	Low Power Full Adder using 9T Structure	Int. J. on Recent Trends in Engineering and Technology, Vol. 8, No. 2, Jan 2013	Design and Analysis of 9T Full Adder
3.	Performance Analysis of low power full adder cells using 45nm CMOS technology	International Journal of Microelectronics Engineering (IJME), Vol. 1, No.1 , 2015	10 transistor Full Adder power, delay, PDP.
4.	A Novel Ultra-Low Power and PDP 8T Full Adder Design Using Bias Voltage	2017 2nd International Conference for Convergence in Technology (I2CT)	Design and Analysis of 8 Transistor Full Adder
5.	Performance Analysis of High Speed Hybrid CMOS Full Adder Circuits for Low Voltage VLSI Design	Hindawi Publishing Corporation VLSI Design Volume 2012	Comparative analysis of 10T, 9T, 8T Full Adders
6.	Design of Low Power Full Adder Circuits Using CMOS Technique	2019 3rd International Conference on Recent Developments in Control, Automation & Power Engineering (RDCAPE)	Analysis of 6 transistor full adder.
7.	An Area Efficient Low Power TG Full Adder Design using CMOS Nano Technology	International Journal of Engineering Research & Technology (IJERT) Vol. 3 Issue 4, April – 2014	Full Adder using Transmission gate logic.
8.	Low Power-Area Pass Transistor Logic Based ALU Design Using Low Power Full Adder Design	IEEE Sponsored 9th International Conference on Intelligent Systems and Control (ISCO)20I5	Pass transistor logic.

1.3 Need for Low Power Design:

The main need for opting low power designs is to reducing the static and dynamic power dissipation in any integrated circuits. Now-a-days companies push their limits on features and specializations on hand held devices, so companies tries to improve the battery life by reducing the power consumption in devices. There are many methodologies which are available to implement low power designs. At present we mainly focus on full adders because in any device it consists of ALU which is responsible for complex addition, subtraction and in a single chip consists of billions of transistors which has its own responsibility so a single ALU part consuming huge amount of power is not appreciable, so in these cases low power designs are used to reduce the power consumption.

1.4 Organization of the Report

The remaining chapters of the project report are described as follows:

- Chapter 2 contains the methodology, and designing of Full Adder using pass-transistor (PT) logic and transmission-gate logic.
- Chapter 3 contains the design implementation of hybrid topologies such as XOR-XNOR models and verification of their truth tables.
- Chapter 4 describes about the designing of different types of Full Adders by using the hybrid XOR-XNOR models discussed in chapter 3.
- Chapter 5 compiles the simulation results obtained in 45nm technology after the project was implemented in cadence software.
- Chapter 6 concludes the report with discussions about the results obtained and their future implications.

CHAPTER 2

IMPLEMENTATION OF FULL ADDERS USING PASS-TRANSISTOR LOGIC

2.1METHODOLOGY FOR PASS TRANSISTOR:

The pass-transistor logic (PTL) illustrates various logic networks that are used in the basic design of embedded or integrated circuits. It mainly reduces the total number of transistors that are used to design different logic gates, by ignoring unnecessary transistors.

In general, transistors are moderately used as independent switches to get the necessary logic levels between nodes of circuit, rather than the switches connected directly to the supplying voltages. This reduces the count of active devices, but basically it has disadvantages like the variation of the voltage between higher and lower levels comes down at each period of time. Every transistor that is connected in series is somewhat little saturated at its output side than its input side.

By comparing, the conventional CMOS logic controls the transistors so that the output connects to the power supply, so the logic levels of voltage in a sequential concern do not drop off.

For correct working, the rules and conditions of design limit the organization of the circuits so that the sneak tracks, slow switching, and sharing of charges can be prevented. Basic simulation of the design circuits is necessary to guarantee sufficient operation.

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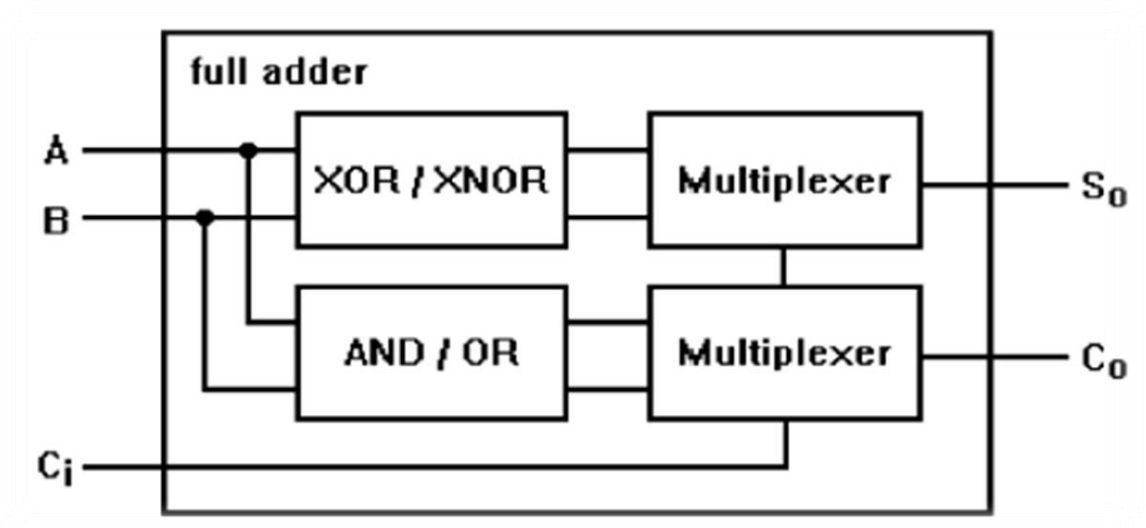


Figure2.1 Methodology for implementation of full adders using P T Logic

2.2 Design Approach

- The concept of pass-transistor logic refers to a logic network basically designed for specific benefits.
- Here, in this section, we have taken the basic gates of XOR and XNOR to help build a complete design of full adder.
- The basic method is to design circuits in cadence software using 45nm technology and then copy and view the results obtained.
- The width of the transistor is taken into account in the construction of the models and the width of the PMOS doubles the width of the NMOS in the construction.
- Finally, we should record the power values of the differential input voltage and compare them with a graphical format.

2.3 DOUBLE PASS-TRANSISTOR LOGIC (DPL):

This section describes the existing and proposed models using the P-Transistor logic.

The DPL basically removes some inverter phases that are essential in the CPL concept by including both N and P channel transistor switches in two logic modes for all functions. It has less driving power and it has very high speed due to its less power at input.

The DPL portable tree switch includes NMOS and PMOS transistors, unlike the CPL switching tree, only the NMOS transistors are used. Full swing performance is achieved by just adding the PMOS transistors same way as adding NMOS transistors. Anyway, this will lead to an increase in input power. The CPL flexible shaft contains only NMOS transistors, resulting in low input power. The full output power output of the DPL gateway is done with a alliance of the NMOS and the PMOS transistors, rather than PMOS inverters and latches that are used in concept of CPL.

SUM (S_0) = ((A (XOR) B) * C') + ((A (XNOR) B) * C)

CARRY (C_0) = ((A.B) * C') + ((A + B) * C)

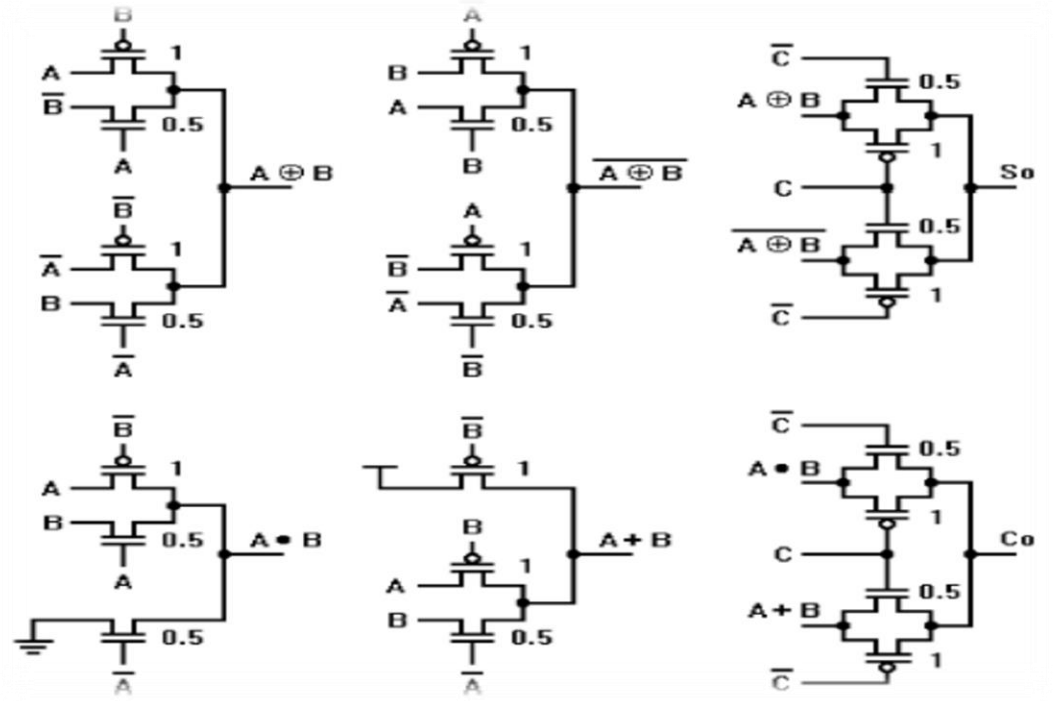


Figure2.2 Parts of Circuit Diagram for FA using DPL Logic.

2.4 SWING-RESTORED COMPLEMENTARY PT LOGIC:

SRCPL is identical to CPL as it uses the same NMOS PT logic network. There are 2 integrated kind of inverters that are exploited to get the required output signal. The main benefit of PT logic is its design

simpleness, but the con of SRCPL is same as the disadvantage of normal CMOS, i.e. the fluctuations in the supply power that happen while switching.

To keep the high speed performance and to make sure that the output has the corresponding voltage swing compared to the input, it is essential to use PMOS type latches or to use inverters at output. This basically has the trouble of something to take place in the supply power at time of the switching. The voltage levels at input are similar as those of standard CMOS input voltage levels, and this mainly has the difficulty that is the voltage swing is close to VDD of design.

SUM (S_0) = ((A (XOR) B) * C') + ((A (XNOR) B) * C)

CARRY (C_0) = ((A.B) * C') + ((A + B) * C)

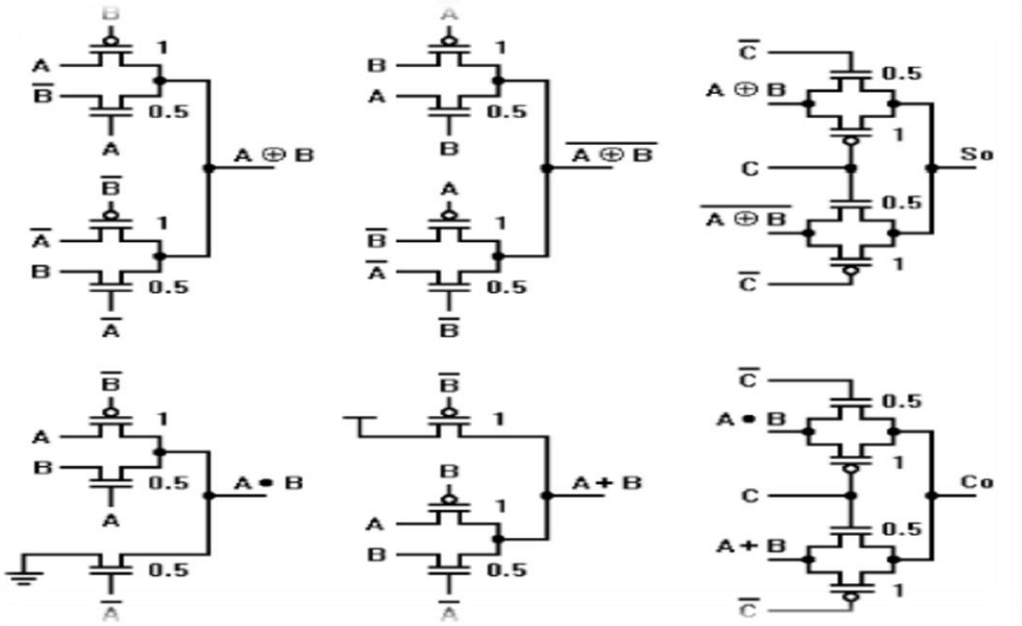


Figure2.3 Parts of Circuit Diagram for FA using SRC-PL Logic.

2.5 IMPLEMENTING FULL ADDER USING PASS-TRANSISTOR LOGIC:

2.5.1 Circuit Diagram

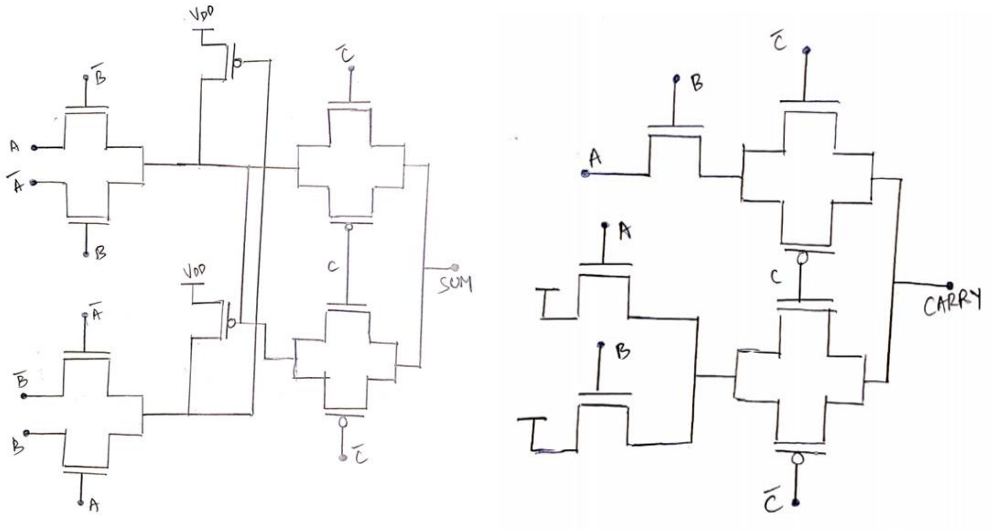


Figure2.4 Circuit Diagram of full adders using Pass Transistor Logic.

Here we can observe that the SUM is equal to the value of A (XOR) B when C is equal to zero (0), and it is equal to A (XNOR) B when C is equal to one (1).

And the 2 * 1 multiplexer is used to discover the exact value to return C input as signal of select. By following the identical operation, the required output CARRY(C) is equal to A.B when C is equal to 0, and it is equal to A + B when C is equal to 1.

Similarly, C is used to choose the appropriate measure of the necessary condition, to drive multiplexer. So, another idea for designing the FA cell is built with logic block to get A & B signals, and other block to get the (A.B) and (A+B) symbols, In the same way,2 multiplexers are completely driven by input C to produce results of SUM and CARRY, as in Figure 2.5.1.

The features and benefits of this conceptual framework are as follows.

- These symbols aren't created internally to regulate the selection of the multiplexers at output.
- The signal at input, C that shows complete power fluctuations and no additional delays. It is used to drive the multiplexers by decreasing complete distribution of delays.
- The load capacitance of input C is reduced. It is connected to other gates and no longer operates on other terminals or resource sources, as the diffusion power becomes greater in the sub micrometer technology.
- Delays in spread of Carry and Sum results can be corrected by rearranging XOR, XNOR, AND&OR gates.

2.5.2 Transistor Comparison:

	DPL	SR-CPL	Pass transistor Logic
NMOS	11	11	11
PMOS	11	9	6
Total	22	20	17

Table 2.5 Tabulation for transistor count .

2.6 TRANSMISSION GATE PSEUDO ADDER CELL:

- This fully redesigned add-on is basically the combination of the low power TG& NMOS artificial gates as shown in Fig 2.6.
- Here there is very less decrease in power in the output. It needs twice the count of transistors to design similar operation.
- The pseudo NMOS FA circuit works with a pseudonym, called a scale model. The full extension circuit basically uses 14 transistors to obtain additional negative function. The advantage of a fake NMOS adder cell is its high speed (compared to conventional full-size additives) and low transistor counts. The disadvantage of the fake cell-NMOS is the constant power consumption of the pull transistor and the decrease in voltage output, making this cell adder vulnerable to external noise.

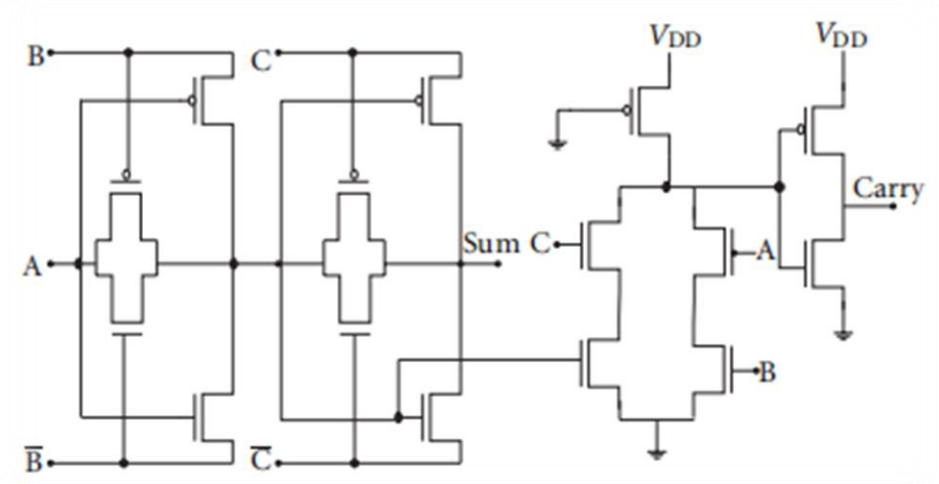


Figure 2.6: FULL ADDER USING TRANSMISSION GATE LOGIC.

2.7 SUMMARY

The principal here is to present high-performance designing and energy efficiency of the device by taking multiplexer as the basis for PT logic. The full extension construction here is available with various concepts like DPL and SRCPL. In addition, another design is enforced by using PT logic integrated along with different concept. The transistor count required to detect a integrated CMOS transducer is less than the number of transistors required to detect full-scale construction by taking CMOS transistors individually. Therefore, the necessary logic is set up inside the spread environment that works quicker than the standard configuration of the static CMOS full adder.

CHAPTER 3

DESIGN OF HYBRID XOR/XNOR TOPOLOGIES

This chapter describes the designing of hybrid XOR/XNOR models. It describes the design and implementation of 3T XOR, 3T XNOR, 2T XNOR, 2TXOR.

3.1 Design of 3T XOR Model

XOR is a digital gate which is also called exclusive OR(XOR) the functionality of this gate is that it's a inequality detector , means whenever we provide 2 inputs to this gate in the form of logic high(1) and logic low(0) it compares both and give logic high output (1) when ever both inputs are unequal or different. And it gives logic low output (0) whenever the inputs are equal or same. The given below fig 3.1 is the truth table of a basic 2 input XOR gate.

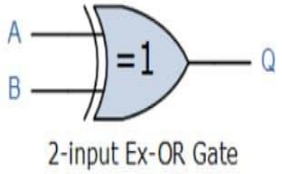
Symbol	Truth Table		
	A	B	Q
 2-input Ex-OR Gate	0	0	0
	0	1	1
	1	0	1
	1	1	0
Boolean Expression Q = A XOR B			

Figure 3.1 Truth table and symbol of XOR gate

Boolean expression for XOR is given as A XOR B = A * B' + A' * B. But if we use general CMOS method to construct XOR it requires around 14 transistors to build. So now we use PT logic to reduce the transistors count and build XOR gate using 3 transistors (3T) only.

3.1.1 3T XOR Circuit Explanation:

The circuit diagram of 3T XOR is given below fig: 3.2. We have constructed XOR gate using 2 PMOS (M2 and M3) and 1 NMOS (M1) so total 3 transistors are used in the design. Input A is given as input to transistors M1 and M2 and its given in pass transistor logic to M3. B is given as input to M3 and acts as supply voltage to M2. And M1 is only grounded. Now we will try to understand the XOR logic for the following in cases.

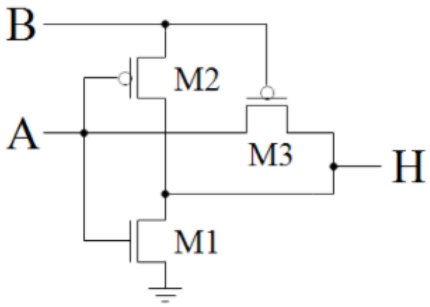


Figure 3.2 circuit diagram of 3T XOR gate

Case1: When B is logic low (0) then both M1 and M2 are short circuited due to same potential and M3 will be ON and whatever the input given at A is directly passed through M3 to output.

Therefore if B=0 then output=A.

Case2: When B is logic high (1) then M3 will be OFF, and the logic high behaves as the supply voltage to M2 and then M1, M2 both behave as a general CMOS inverter and the output will be compliment of input A.

Therefore if B=1 then output=A' (compliment of A).

3.1.2 SUMMARY:

1. If A=0, B=0 then output H=A=0
2. If A=0, B=1 then output H=A'=1
3. If A=1, B=0 then output H=A=1
4. If A=1, B=1 then output H=A'=0
5. Therefore the XOR logic gate is designed using 3T and verified.

A	B	H	OUTPUT
0	0	A=0	0
0	1	A'=1	1
1	0	A=1	1
1	1	A'=0	0

Table 3.3 3T XOR gate truth table .

3.2 Design of 3T XNOR Model

XNOR is a digital gate which is also called exclusive NOR(XOR) the functionality of this gate is that its a equality detector , means whenever we provide 2 inputs to this gate in the form of logic high(1) and logic low(0) it compares both and give logic high output (1) when ever both inputs are equal or same. And it gives logic low output (0) whenever the inputs are unequal or different. The given below fig 3.1 is the truth table of a basic 2 input XNOR gate.

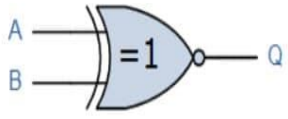
Symbol	Truth Table		
 2-input Ex-NOR Gate	A	B	Q
	0	0	1
	0	1	0
	1	0	0
	1	1	1
Boolean Expression Q = A XNOR B			

Figure 3.4 Truth table and symbol of XNOR gate

The expression for XNOR is given as A XNOR B = A' * B' + A * B. But if we use general CMOS method to construct XNOR it requires around 14 transistors to build. So now we use PT logic to reduce the transistors count and build XNOR gate using 3 transistors (3T) only.

3.2.1 3T XNOR Circuit Explanation:

The circuit diagram of 3T XNOR is given below fig: 3.5. We have constructed XNOR gate using 2 NMOS (M5 and M6) and 1 PMOS (M4) so total 3 transistors are used in the design. Input A is given as input to transistors M4 and M5 and it's given in pass transistor logic to M6. B is given as input to M6 and acts as ground to M5. And M4 is only attached to supply voltage. Now we will try to understand the XNOR logic for the following in cases.

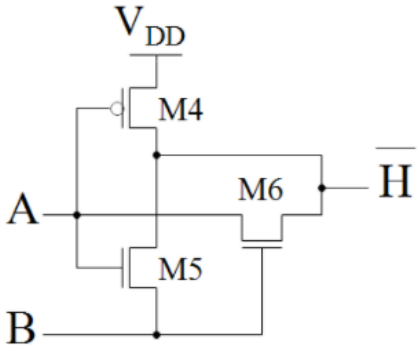


Figure 3.5 circuit diagram of 3T XNOR gate

Case1: When B is logic low (0) then both M4 and M5 will behave as CMOS inverter and M6 will be OFF and whatever the input given at A is complimented and given as output.

Therefore if B=0 then output=A' (compliment of A).

Case2: When B is logic high (1) then M6 will be ON, and the logic high behaves as the supply voltage to M5and then M4, M5 both have same potential so short circuited and the input A directly passes through M6 as output.

Therefore if B=1 then output=A.

3.2.2 SUMMARY:

1. If A=0, B=0 then output X=A'=1.
2. If A=0, B=1 then output X=A=0.
3. If A=1, B=0 then output X=A'=0.
4. If A=1, B=1 then output X=A=1.
5. Therefore the XNOR logic gate is designed using 3T and verified.

A	B	X	OUTPUT
0	0	A'=1	1
0	1	A=0	0
1	0	A'=0	0
1	1	A=1	1

Table 3.6 3T XNOR gate truth table .

3.3 Design of 2T XNOR Model:

The circuit diagram of 2T XNOR model is shown below fig 3.7. In design of the following model we require one VDD power supply and one PMOS and one NMOS. The explanation of the model is given below.

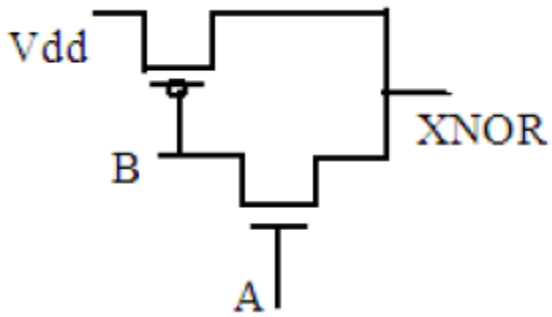


Figure 3.7 Circuit Diagram of 2T XNOR Model.

3.3.1 2T XNOR Circuit Explanation:

1. When B is logic low (0) and A is logic low (0) then PMOS will turn ON and NMOS will be in OFF state and VDD is directly passed through output indicating logic high (1).

2. When input A is logic low state (0) and input B is logic high state (1) then both PMOS and NMOS will be turned OFF and output becomes logic low state (0).

3. When input A is logic high state (1) and input B is logic low state (0) then both PMOS and NMOS will be turned ON and the value of B is passed as output indicating logic low (0).

4. When A is logic high (1) and logic high (1) then NMOS will ON and B is passed through output indicating logic high (1).

3.4 Design of 2T XOR gate Model:

The circuit diagram of 2T XOR model is shown below fig 3.8. In design of the following model we require two PMOS. The explanation of the model is given below.

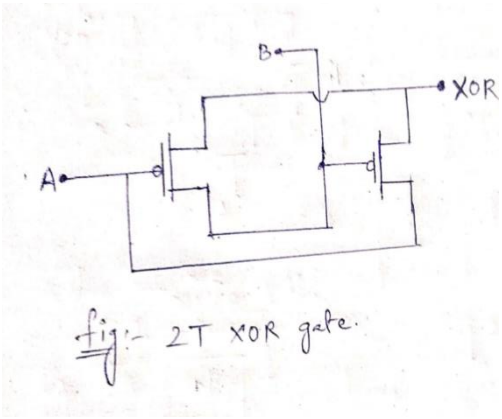


Figure 3.8 Circuit Diagram of 2T XOR Model.

3.4.1 2T XOR Circuit Explanation:

1. When B is logic low (0) and A is logic low (0) then both PMOS are ON and then the value of A and B is passed as output indicating logic low (0).
2. When input A is logic low state (0) and input B is logic high state (1) then PMOS1 will be ON and PMOS2 is OFF and the value of B is passed as output indicating logic high (1).
3. When input A is logic high state (1) and input B is logic low state (0) then PMOS1 will be OFF and PMOS2 is ON and the value of A is passed as output indicating logic high (1).
4. When A is logic high (1) and logic high (1) then both PMOS will be OFF and the output indicating logic low (1).

3.5 SUMMARY:

In this module we have learnt about design of hybrid XOR/XNOR topologies and their characteristics. We have designed the models with less no. of transistors as possible.

CHAPTER 4

IMPLEMENTATION OF FULL ADDER USING HYBRID XOR/XNOR MODELS

In this Chapter we will discuss about designing of full adders using hybrid models. We will design 10T, 9T, 8T, 6T types of full adders.

4.1 Design of 10T Full Adder:

In order to create a 10T full adder we use both 3T XOR and 3T XNOR Models and the diagram of 10Transistor full adder is given below figure 4.2 and block diagram of a full adder is shown in fig 4.1.

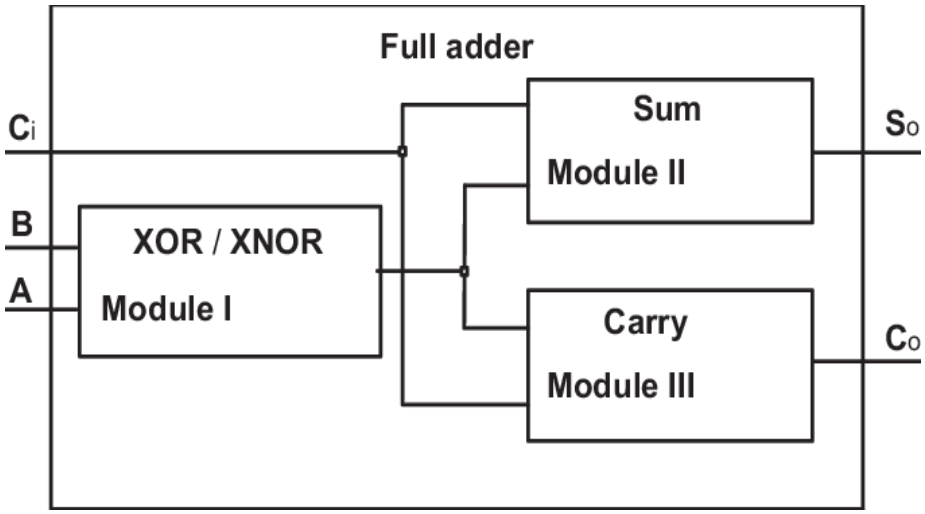


Figure 4.1 Block Diagram of full adder Circuit.

In the shown Block diagram there are three module where module 1 can be XOR/XNOR modules and module 2 is SUM and module 3 is CARRY of the circuit.

4.1.1 10T Full Adder Circuit Explanation:

As shown in fig 4.2 M1,2,3 transistors are used to build XOR gate and transistors M4,5,6, are used to build XNOR gate and M7,8 are used as multiplexer with C as the select line the output of the MUX is SUM and the inputs of the first MUX are outputs of XOR and XNOR. From here we get SUM. The second MUX is build by using M9,10 transistors and select line is output of XOR and the inputs of the MUX are A and C respectively the output we get from here the CARRY.

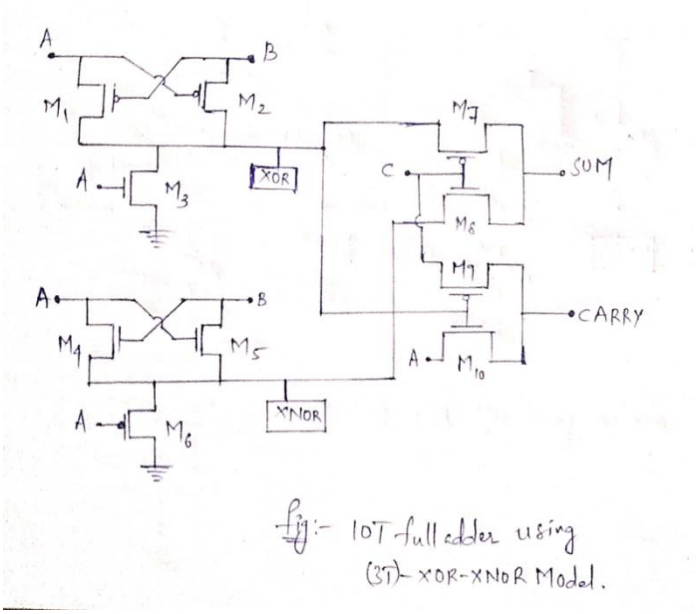


Figure 4.2 Circuit Diagram of 10T full adder.

4.1.2 Explanation of SUM Function:

In the previous Chapter 3.1, 3.2 we have learnt about 3T XOR and 3T XNOR models we will now mainly focus on MUX part for the first MUX whenever C is logic low (0) then PMOS (M7) will be ON and NMOS (M8) will be turned OFF therefore the XOR output will be the output of the SUM and if C is logic high (1) then PMOS (M7) will be OFF and NMOS (M8) will ON which will allow output of XNOR to be the output of SUM.

INPUT C	OUTPUT OF SUM
0	A XOR B
1	A XNOR B

Table 4.3 Logic for SUM Function in 10T full adder .

Now we will try to relate this logic to the actual 3 input full adder logic style.

A	B	C	OUTPUT	SUM
0	0	0	A XOR B=0	0
0	0	1	A XNOR B=1	1
0	1	0	A XOR B=1	1
0	1	1	A XNOR B=0	0
1	0	0	A XOR B=1	1
1	0	1	A XNOR B=0	0
1	1	0	A XOR B =0	0
1	1	1	A XNOR B=1	1

Table 4.4 Truth Table of SUM in 10T full adder .

As we can clearly observe the output of the SUM from the designed 10T full adder is as same as the general 3input full adder which confirms us that the designed 10T full adder SUM is correct. Now we will verify the CARRY part as well.

4.1.3 Explanation of CARRY Function:

If we observe the second MUX where XOR is the select line so whenever the output of XOR is logic low (0) then PMOS (M9) will be ON and NMOS (M10) will be turned OFF therefore the value of A will be the output of CARRY and if XOR is logic high (1) then PMOS (M9) will be OFF and NMOS (M10) will ON which will allow the value of C to be the output of CARRY.

INPUT A XOR B	OUTPUT OF CARRY
0	A
1	C

Table 4.5 Logic for CARRY in 10T full adder .

Now we will try to correlate the above logic to the actual 3 input full adder.

A	B	C	A XOR B	OUTPUT	CARRY
0	0	0	0	A=0	0
0	0	1	0	A=0	0
0	1	0	1	C=0	0
0	1	1	1	C=1	1
1	0	0	1	C=0	0
1	0	1	1	C=1	1
1	1	0	0	A=1	1
1	1	1	0	A=1	1

Table 4.6 Truth Table of CARRY in 10T full adder .

4.2 Design of 9T Full Adder:

In order to create a 9T Full Adder we follow the same set of steps as described for 10T Full Adder but to reduce the one transistor we will remove 3T XNOR model and replace it with the inverter connected at the output of the 3T XOR gate which in turn gives us the XNOR logic so by this way we have reduced 10T full adder to 9T full adder. The shown below fig 4.4 is the circuit diagram of 9Transistor full adder.

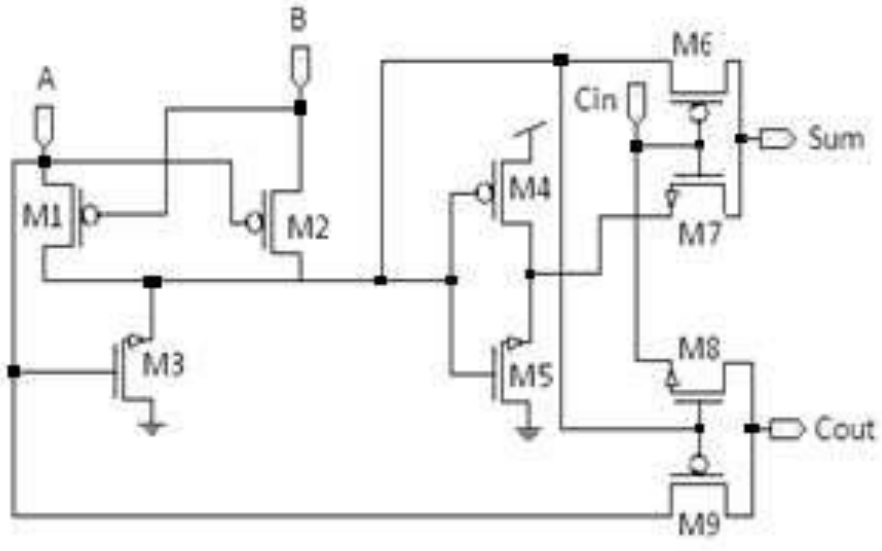


Figure 4.7 Circuit Diagram of 9T full adder.

4.3 Design of 8T Full Adder:

In this module we will try to understand the designing of 8T full adder in order to build 8T full adder we require one 3T XOR gate, 2PMOS and 3 NMOS. The design of 3T XOR model is explained in chapter 3.1. In the design shown below transistors M1, 2, 3 are used to construct 3T XOR gate and M4,5,6 are used for SUM and M7,8 are used for CARRY of the Full Adder.

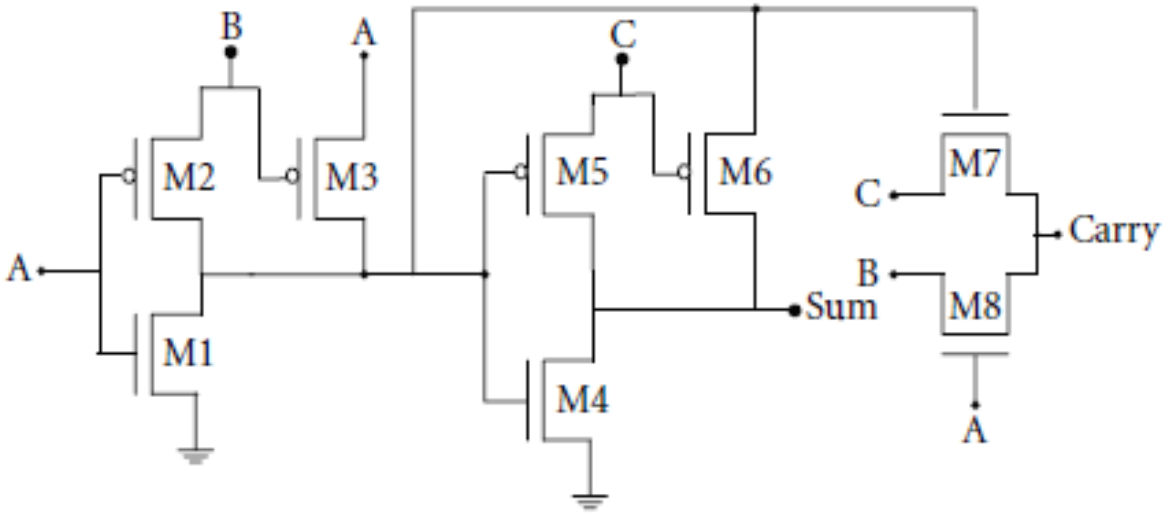


Figure 4.8 Circuit Diagram of 8T full adder.

4.3.1 Explanation of SUM Function:

If we try to focus on the SUM part of the full adder then it mainly depends on the value of C.

Case1: Whenever C is logic low (0) then transistors M4,5 are short circuited due to same potential level and transistor M6 will be turned ON and the output of 3T XOR is passed as the output of SUM.

Case2: If C is logic high (1) then transistor M6 will be OFF and then M5,M4 will now behave as a inverter and C logic high behaves as the supply voltage and the output of XOR gate is complimented and given as the output of the SUM.

INPUT C	OUTPUT SUM
0	A XOR B
1	A XNOR B

Table 4.9 Logic for SUM in 8T full adder .

Now will correlate this logic to the actual 3 input full adder and verify the SUM in full adder logic style.

INPUT A	INPUT B	INPUT C	OUTPUT	SUM
0	0	0	A XOR B=0	0
0	0	1	A XNOR B=1	1
0	1	0	A XOR B=1	1
0	1	1	A XNOR B=0	0
1	0	0	A XOR B=1	1
1	0	1	A XNOR B=0	0
1	1	0	A XOR B=0	0
1	1	1	A XNOR B=1	1

Table 4.10 Truth Table for SUM in 8T full adder .

4.3.2 Explanation of CARRY Function:

In order to generate CARRY part of the full adder in depends on both the output of XOR and A since both M7,8 are NMOS then whenever its high then only it will be ON. If A XOR B is high then M& will be ON and C is passed as the output but if A is high then M8 will be ON and B is passed as output. There are cases when both are turned OFF then output will be considered low (0).

Since it depends on both XOR and A parameters we will consider 4 different cases

INPUT A XOR B	INPUT A	OUTPUT	ACTIVITY
0	0	0	BOTH M7,8 OFF
0	1	B	M8 ON, M7 OFF
1	0	C	M7 ON, M8 OFF
1	1	B+C	BOTH M7,8 ON

Table 4.11 Logic for CARRY in 8T full adder .

A XORB	**A**	**B**	**C**	OUTPUT	CARRY
0	**0**	**0**	**0**	0	0
0	**0**	**0**	**1**	0	0
1	**0**	**1**	**0**	C	0
1	**0**	**1**	**1**	C	1
1	**1**	**0**	**0**	B+C	0
1	**1**	**0**	**1**	B+C	1
0	**1**	**1**	**0**	B	1
0	**1**	**1**	**1**	B	1

Table 4.12 Truth Table for CARRY in 8T full adder .

Therefore the characteristics of full adder using 8T full adder are verified correctly.

4.4 Design of 6T Full Adder:

In the shown below fig 4.13, is the circuit diagram of 6T Full adder. Where M1, 2 PMOS are used to construct 2T XOR model which gives output A XOR B and then M3, 4 are also behaves as XOR gate and the final output will be A XOR B XOR C which is in turn the Boolean equation of SUM . Therefore M1, 2, 3, 4 are used to design SUM and M 1, 2, 5, 6 are used in design of CARRY.

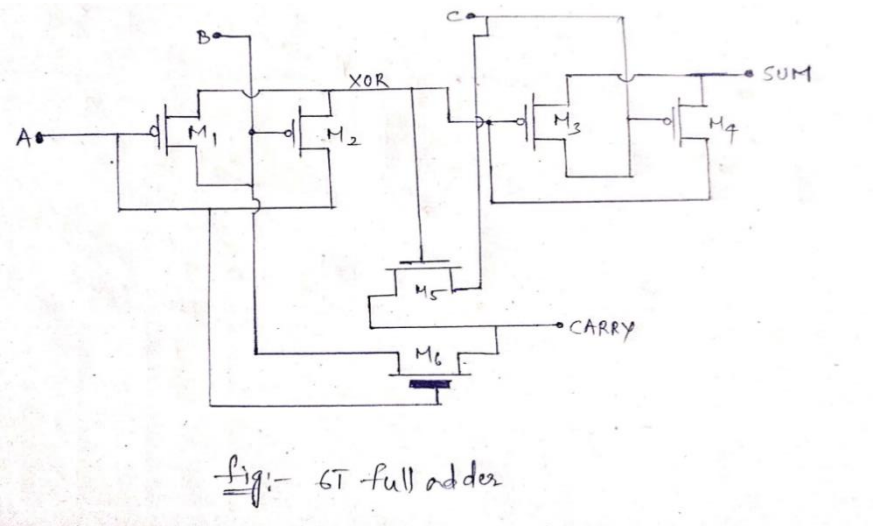


Figure 4.13 Circuit Diagram of 6T full adder.

4.5 Summary:

In this Chapter we have learnt how to construct 10T, 9T, 8T, 6T Full Adders using the hybrid XOR/XNOR topologies and verified their truth table characteristics. We have also learnt about the logic behind the Sum and Carry function in order to build the full adder.

CHAPTER 5
SIMULATION RESULTS IN 45NM TECHNOLOGY

5.1 Simulation Results for 3T XOR gate:

The following is the schematic snapshot of 3Transistor XOR gate in cadence software and the circuit is build over 45nm technology is shown in Figure 5.1. And the output graph of 3T XOR gate is shown in Figure 5.2.

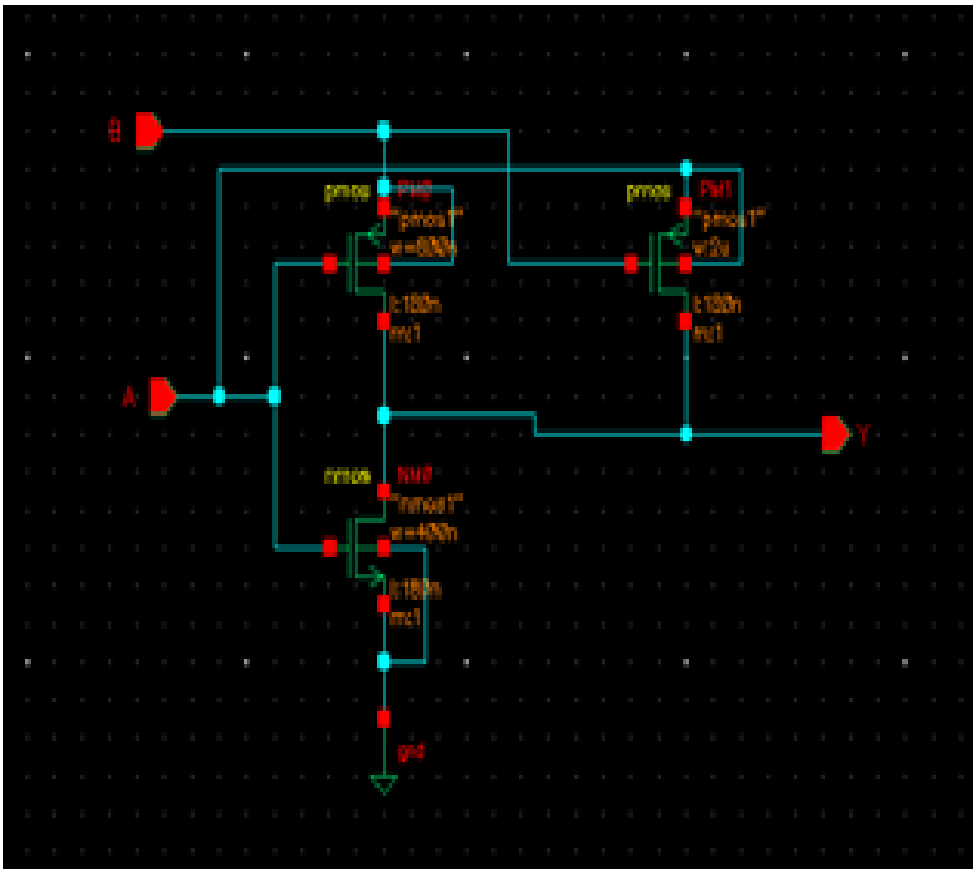


Figure 5.1 Schematic Circuit of 3Transistor XOR gate.

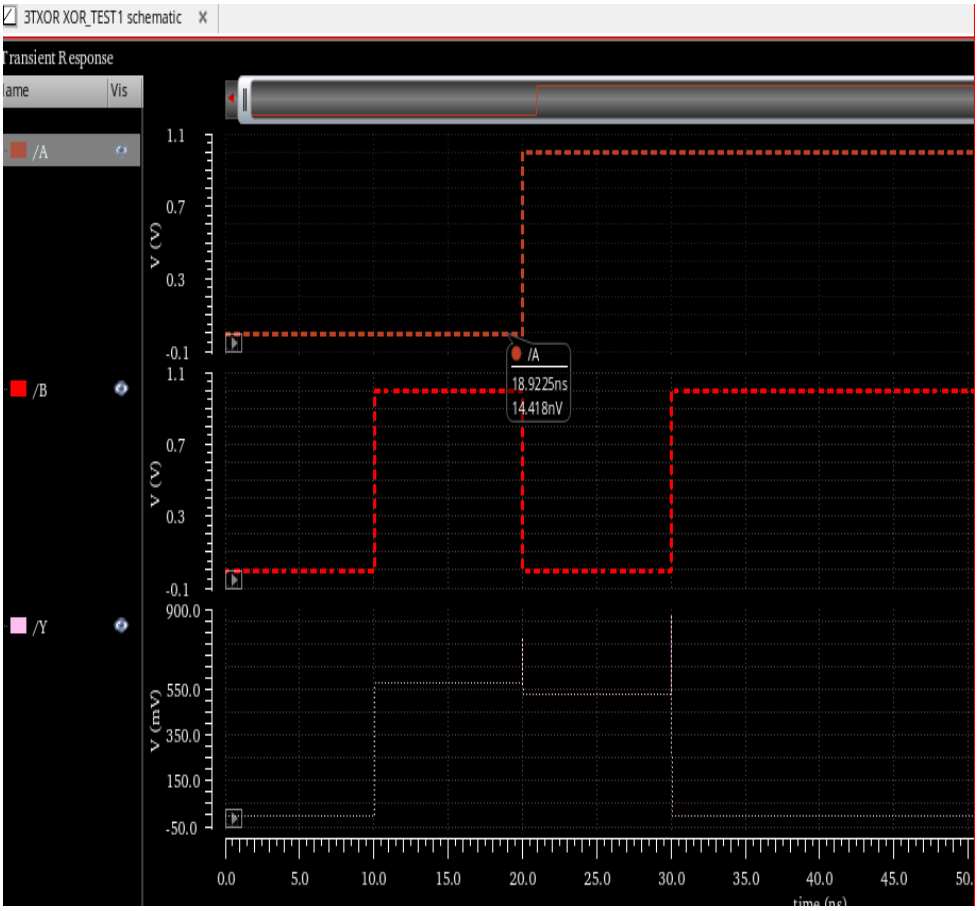


Figure 5.2 Output graph of 3T XOR gate

5.2 Simulation of 10T full adder in 45nm:

The following are the simulation of 10T Full Adder in Cadence software and the circuit is designed in 45nm technology with a cut off voltage of 0.3v and operating voltage of 0.7v and we have made a tabulation Table 5.5, of power and delay for different values if supply voltage and we noted the values and graphs 5.6, 5.7 are made.

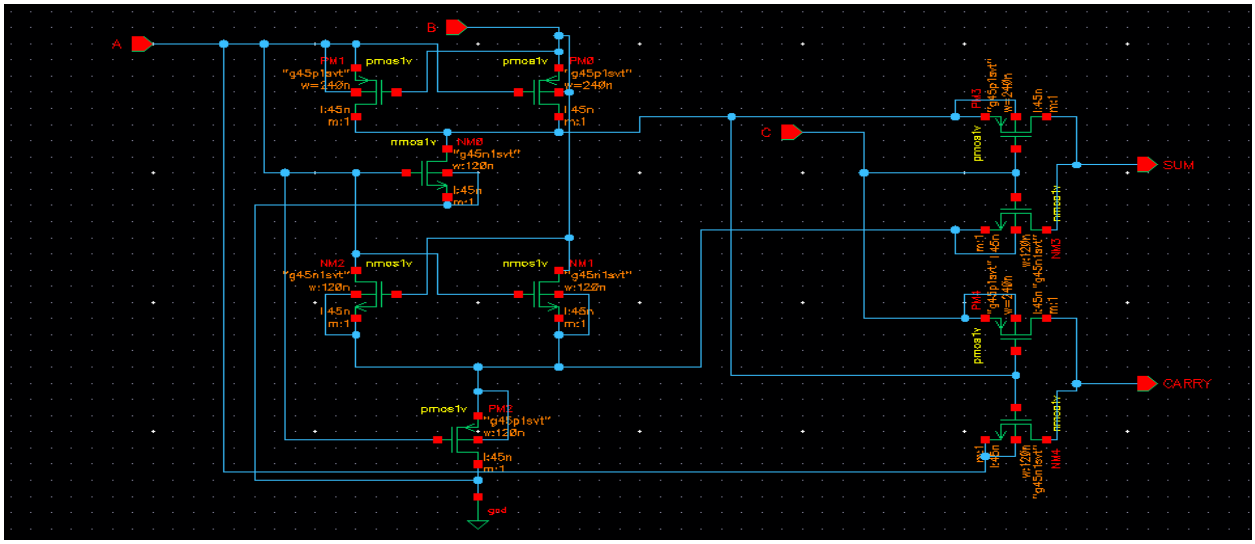


Figure 5.3 Schematic of 10T Full Adder in 45nm.

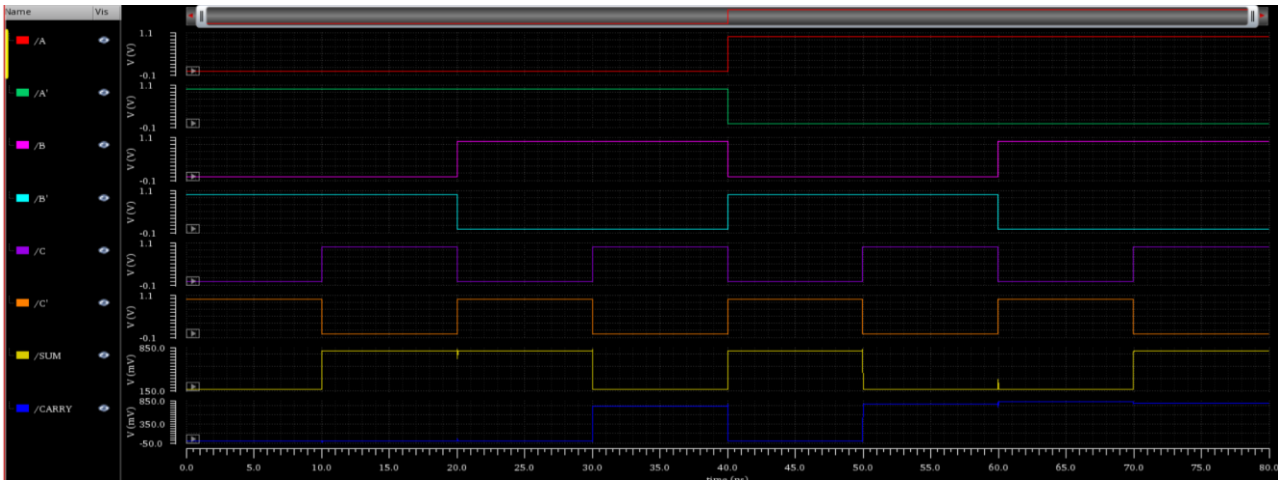
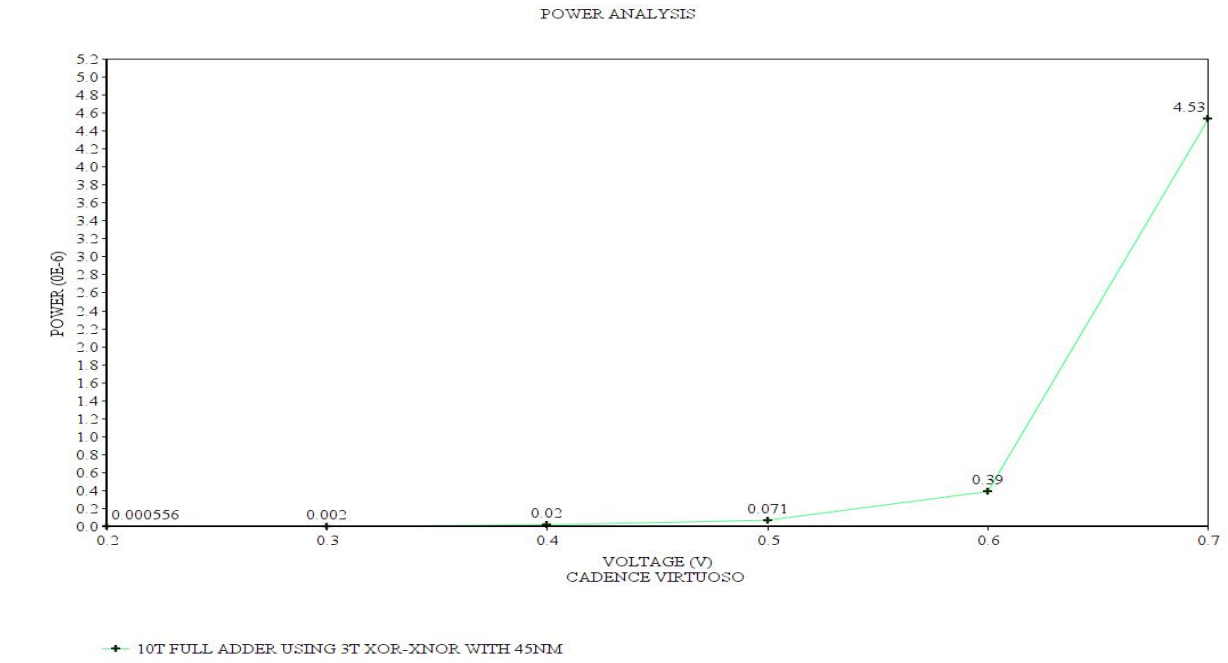


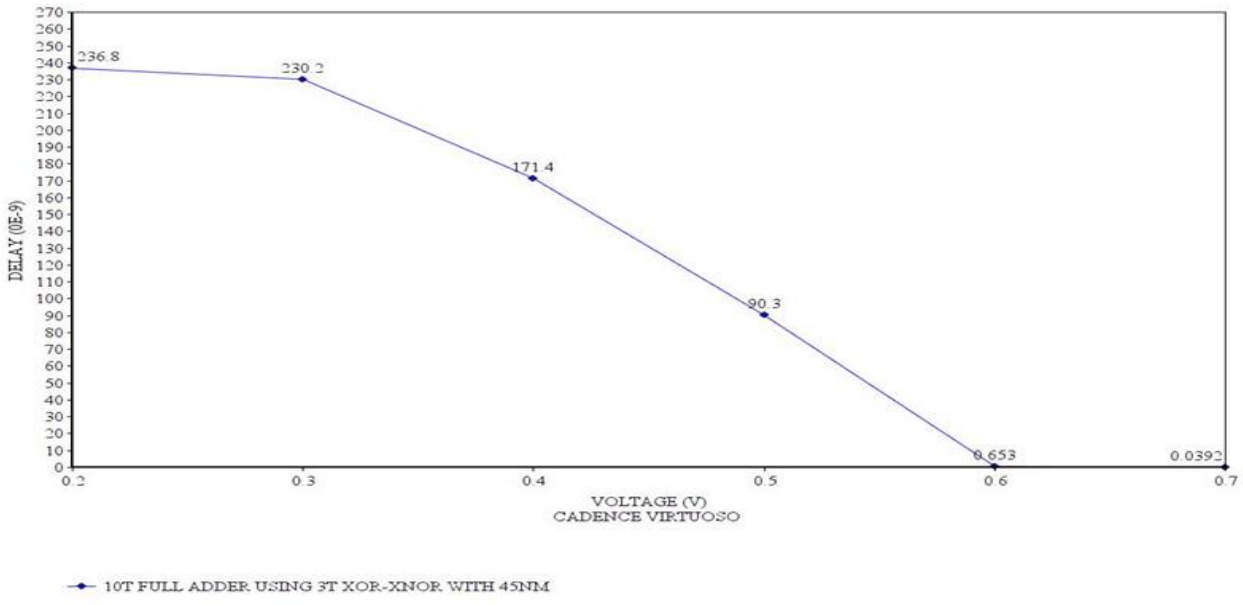
Figure 5.4 Output graph of 10T Full Adder.

VOLTAGE(V)	POWER(W)	DELAY(S)
0.2	556.8(E-12)	236.8(E-9)
0.3	2.2(E-9)	230.2(E-9)
0.4	20.5(E-9)	171.4(E-9)
0.5	71.4(E-9)	90.3(E-9)
0.6	390.3(E-9)	653.1(E-12)
0.7	4.53(E-6)	39.2(E-12)

Table 5.5 Power and Delay table for different voltages of 10T Full Adder in 45nm.



Graph 5.6 Power Analysis Graph for different voltages of 10T Full Adder in 45nm.



Graph 5.7 Delay Graph for different voltages of 10T Full Adder in 45nm.

5.3 Simulation of 9T Full Adder in 45nm:

The following are the simulation of 9T Full Adder in Cadence software and the circuit is designed in 45nm technology with a cut off voltage of 0.3v and operating voltage of 0.7v and we have made a tabulation Table 5.9, of power and delay for different values if supply voltage and we noted the values and graphs 5.10, 5.11 are made.

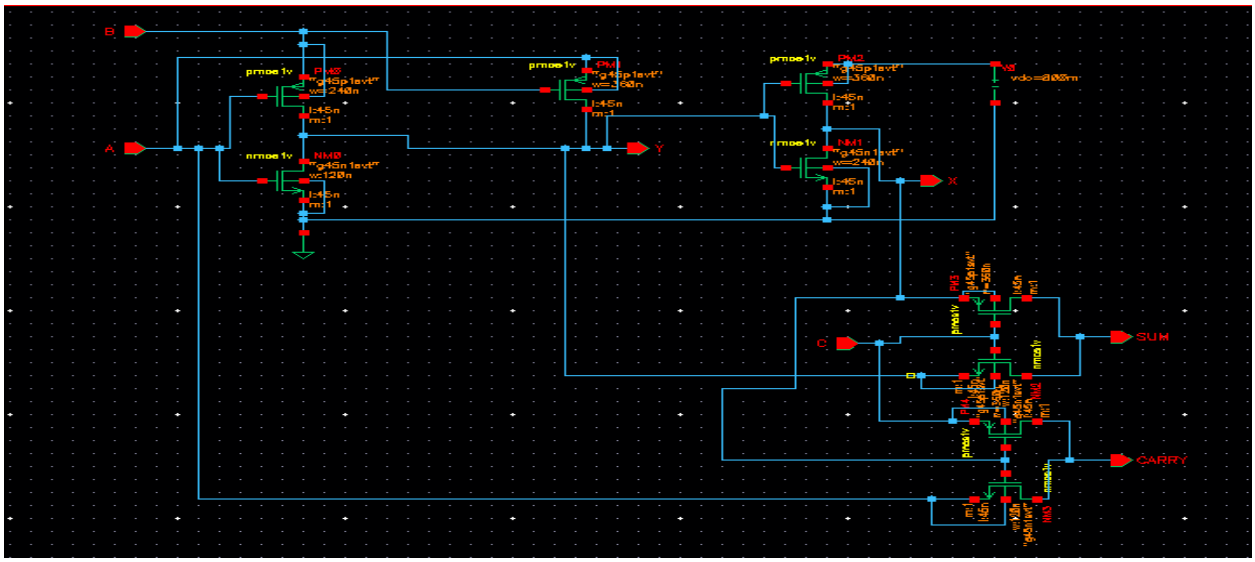
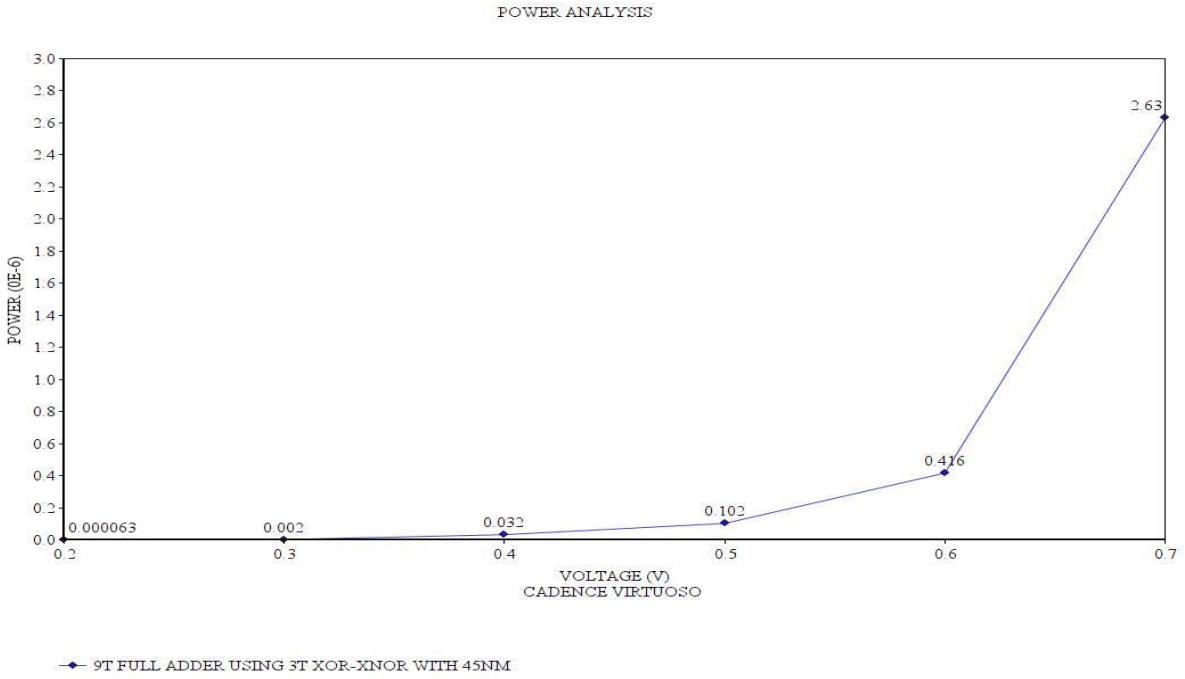


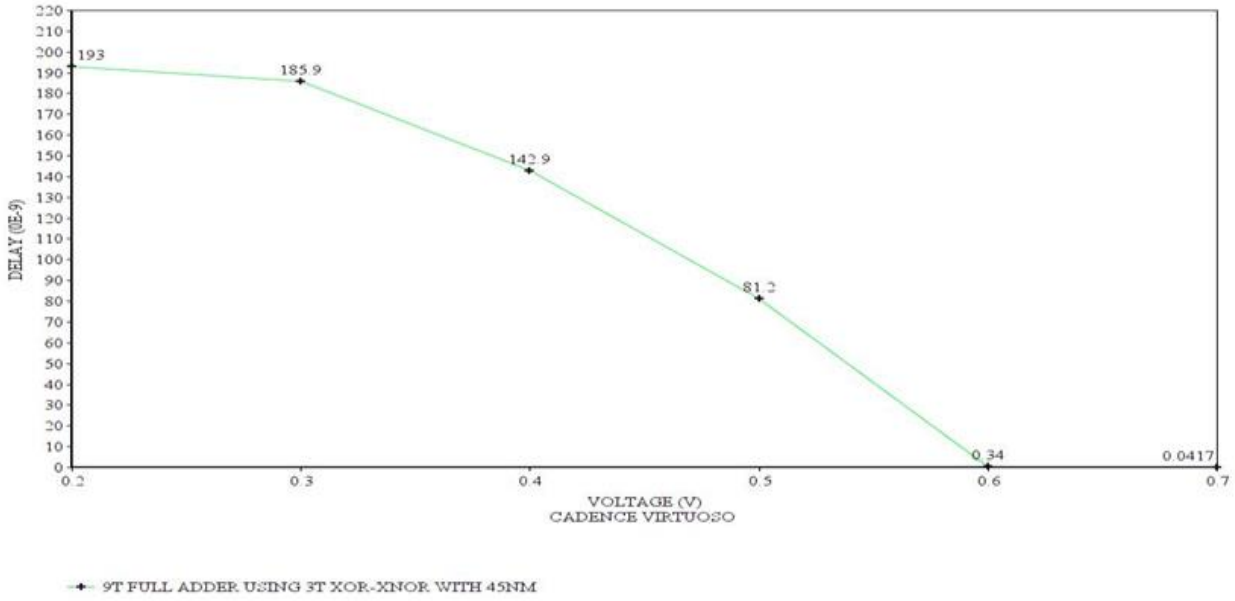
Figure 5.8 Schematic of 9T Full Adder in 45nm.

VOLTAGE(V)	POWER(W)	DELAY(S)
0.2	63(E-12)	193(E-9)
0.3	2.94(E-9)	185.9(E-9)
0.4	32.3(E-9)	142.9(E-9)
0.5	102.9(E-9)	81.2(E-9)
0.6	416.2(E-9)	340.3(E-12)
0.7	2.63(E-6)	41.7(E-12)

Table 5.9 Power and Delay table for different voltages of 9T Full Adder in 45nm.



Graph 5.10 Power Analysis Graph for different voltages of 9T Full Adder in 45nm.



Graph 5.11 Delay Graph for different voltages of 9T Full Adder in 45nm.

5.4 Simulation of 8Transistor FA in 45nm:

The following are the simulation of 8T Full Adder in Cadence software and the circuit is designed in 45nm technology with a cut off voltage of 0.3v and operating voltage of 0.7v and we have made a tabulation Table 5.13 of power and delay for different values if supply voltage and we noted the values and graphs 5.14, 5.15 are made.

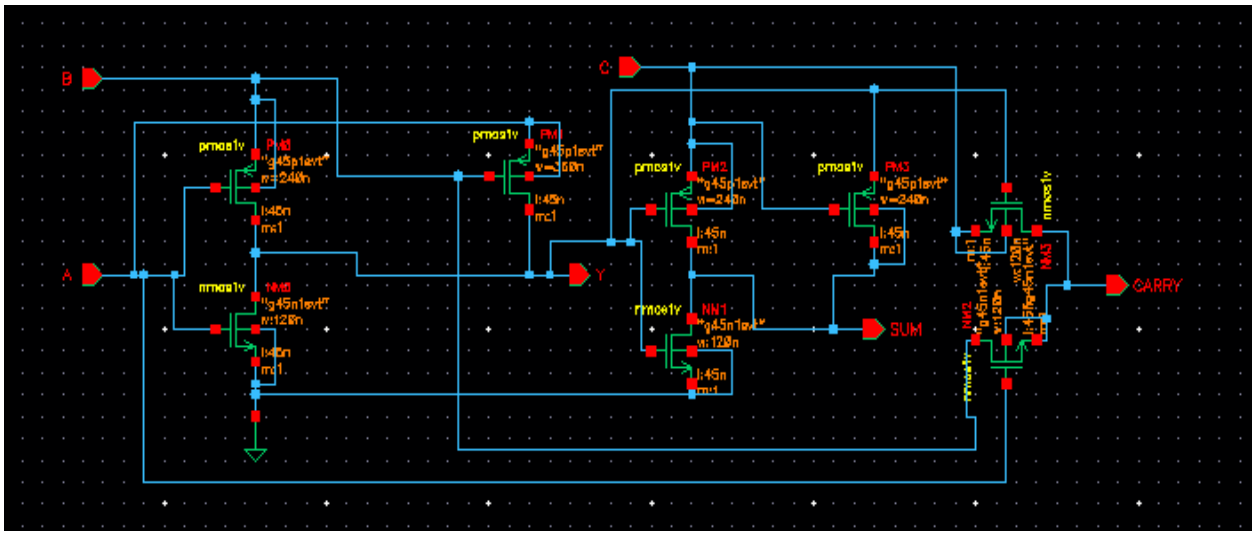
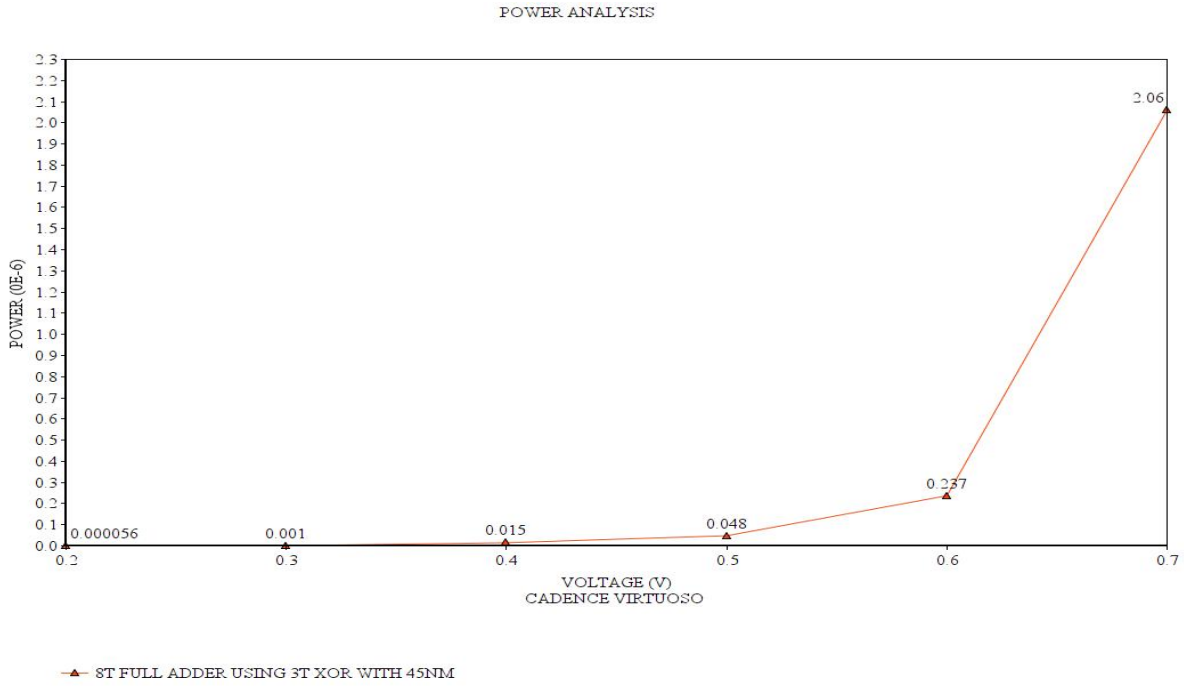


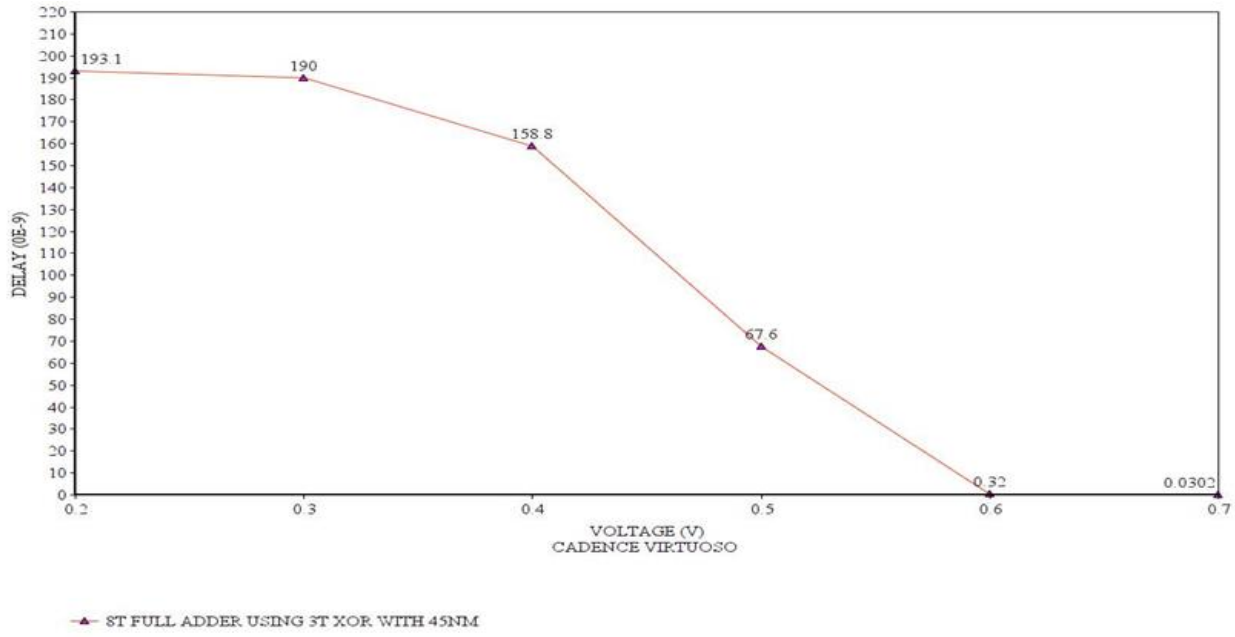
Figure 5.12 Schematic of 8T Full Adder in 45nm.

VOLTAGE(V)	POWER(W)	DELAY(S)
0.2	56.9(E-12)	193.1(E-9)
0.3	1.39(E-9)	190(E-9)
0.4	15.7(E-9)	148.8(E-9)
0.5	48.8(E-9)	67.6(E-9)
0.6	237.6(E-9)	320(E-12)
0.7	2.06(E-6)	30.2(E-12)

Table 5.13 Power and Delay table for different voltages of 8T Full Adder in 45nm.



Graph 5.14 Power Analysis Graph for different voltages of 8T Full Adder in 45nm.



Graph 5.15 Delay Graph for different voltages of 8T Full Adder in 45nm.

5.5 Simulation of 6T Full Adder in 45nm:

The following are the simulation of 6T Full Adder in Cadence software and the circuit is designed in 45nm technology with a cut off voltage of 0.3v and operating voltage of 0.7v and we have made a tabulation Table 5.17, of power and delay for different values if supply voltage and we noted the values and graphs 5.18, 5.19 are made.

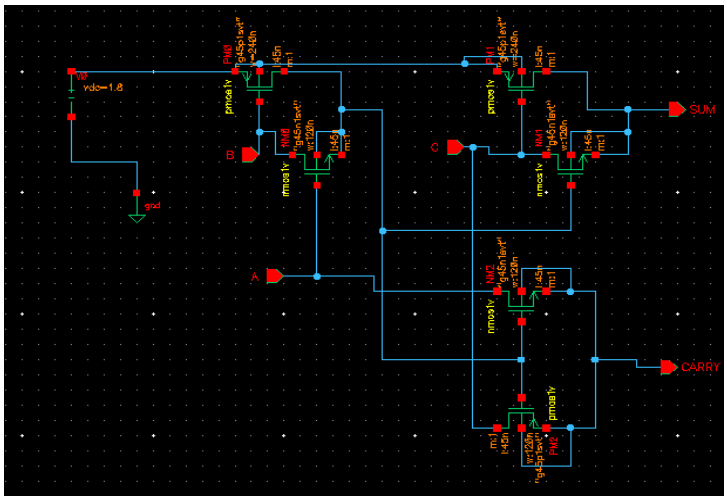
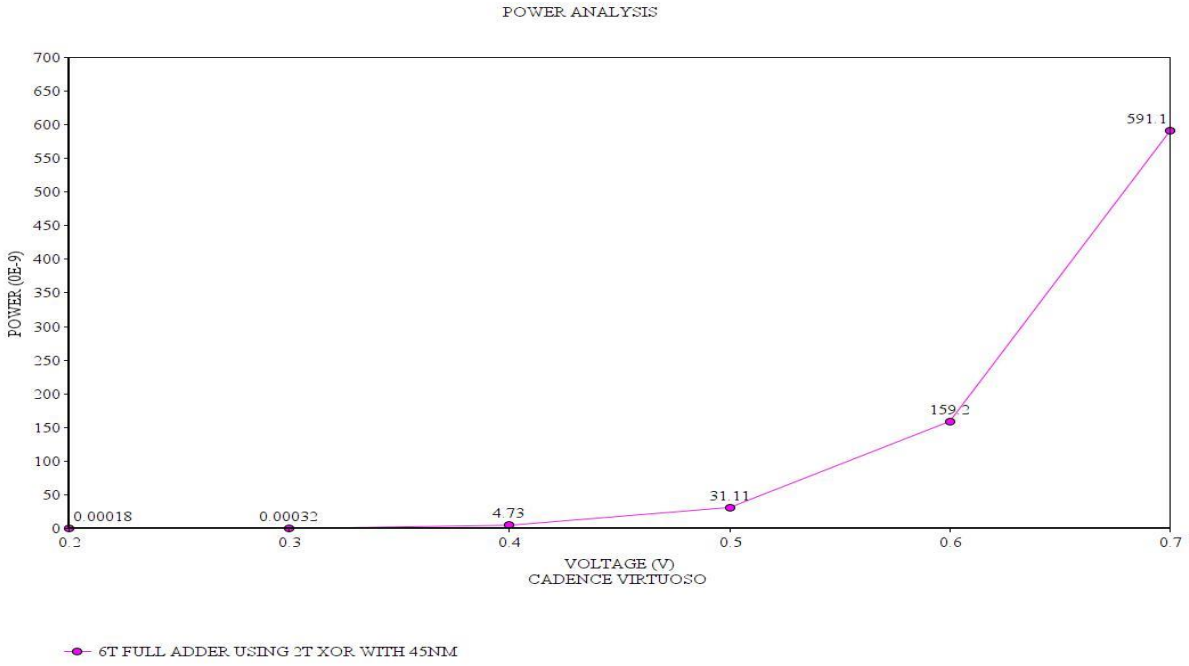


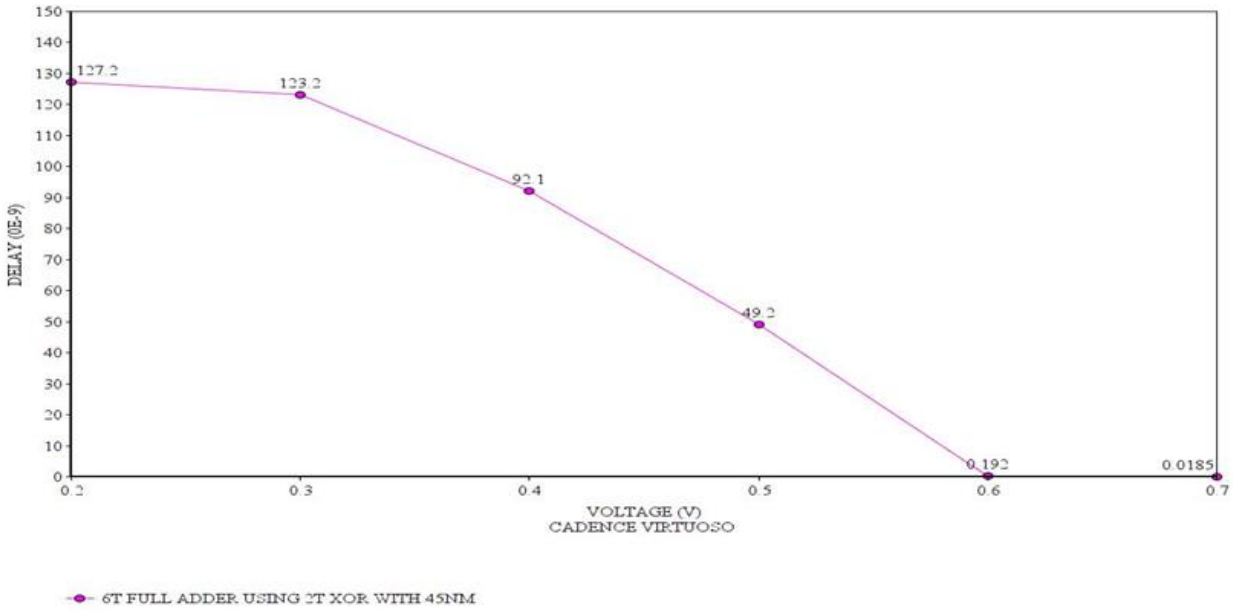
Figure 5.16 Schematic of 6T Full Adder in 45nm.

VOLTAGE(V)	POWER(W)	DELAY(S)
0.2	18.2(E-12)	127.2(E-9)
0.3	32.2(E-12)	123.2(E-9)
0.4	4.73(E-9)	92.1(E-9)
0.5	31.11(E-9)	49.2(E-9)
0.6	159.2(E-9)	192.2(E-9)
0.7	591.1(E-9)	18.5(E-12)

Table 5.17 Power and Delay table for different voltages of 6T Full Adder in 45nm.



Graph 5.18 Power Analysis Graph for different voltages of 6T Full Adder in 45nm.



Graph 5.19 Delay Graph for different voltages of 6T Full Adder in 45nm.

5.6 Simulation of Full Adder using DPL:

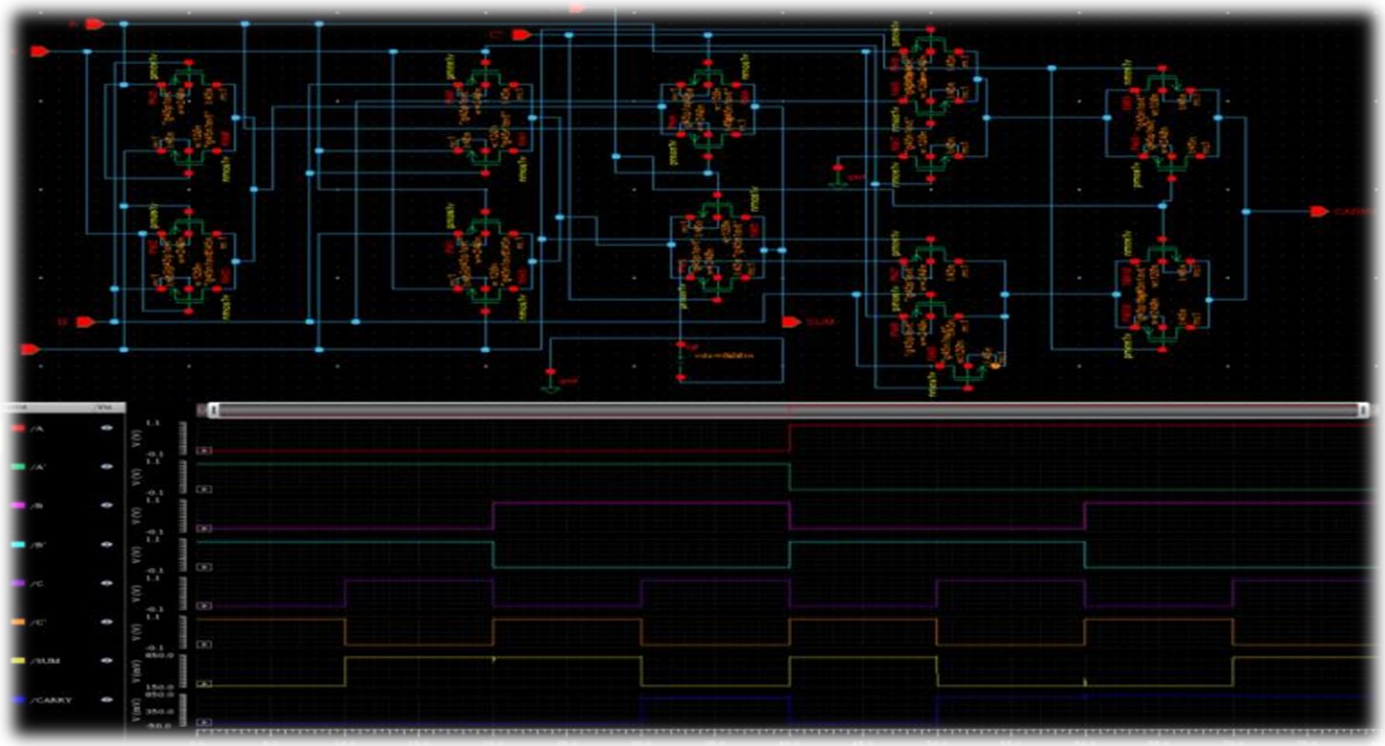
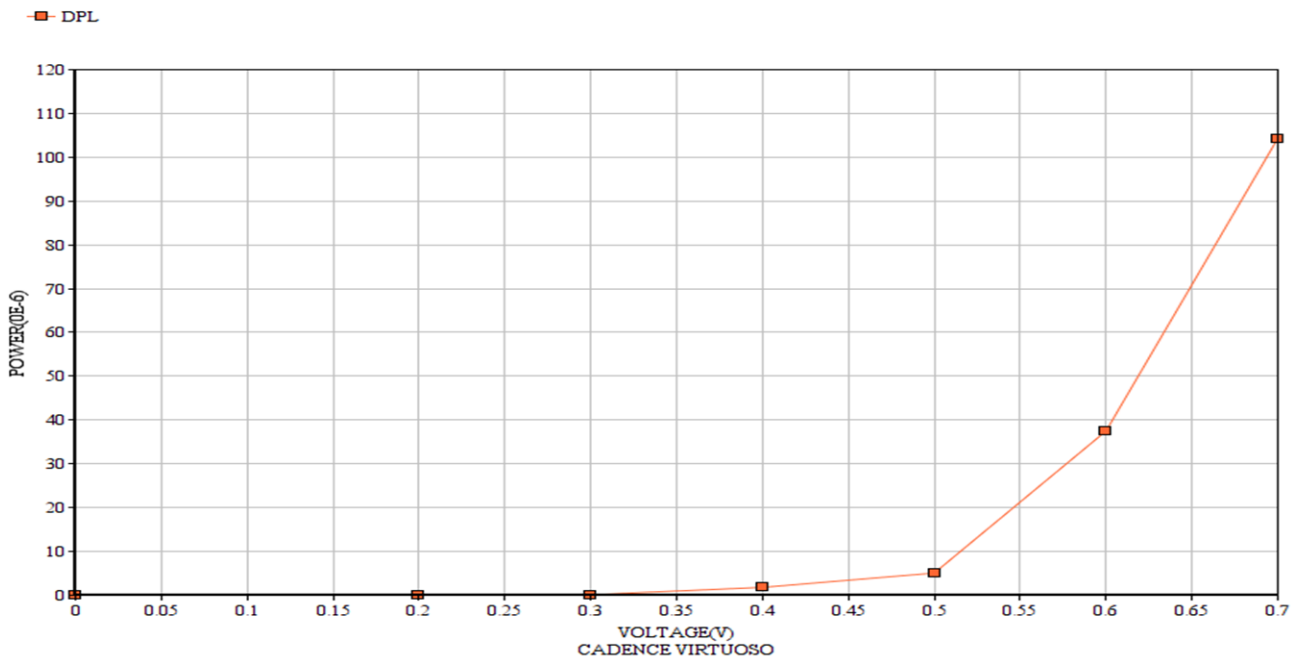


Figure 5.20 Output of Full Adder using DPL in 45nm.



Graph 5.21 Power Analysis Graph for DPL.

5.7 Simulation of Full Adder using SRC-PL:

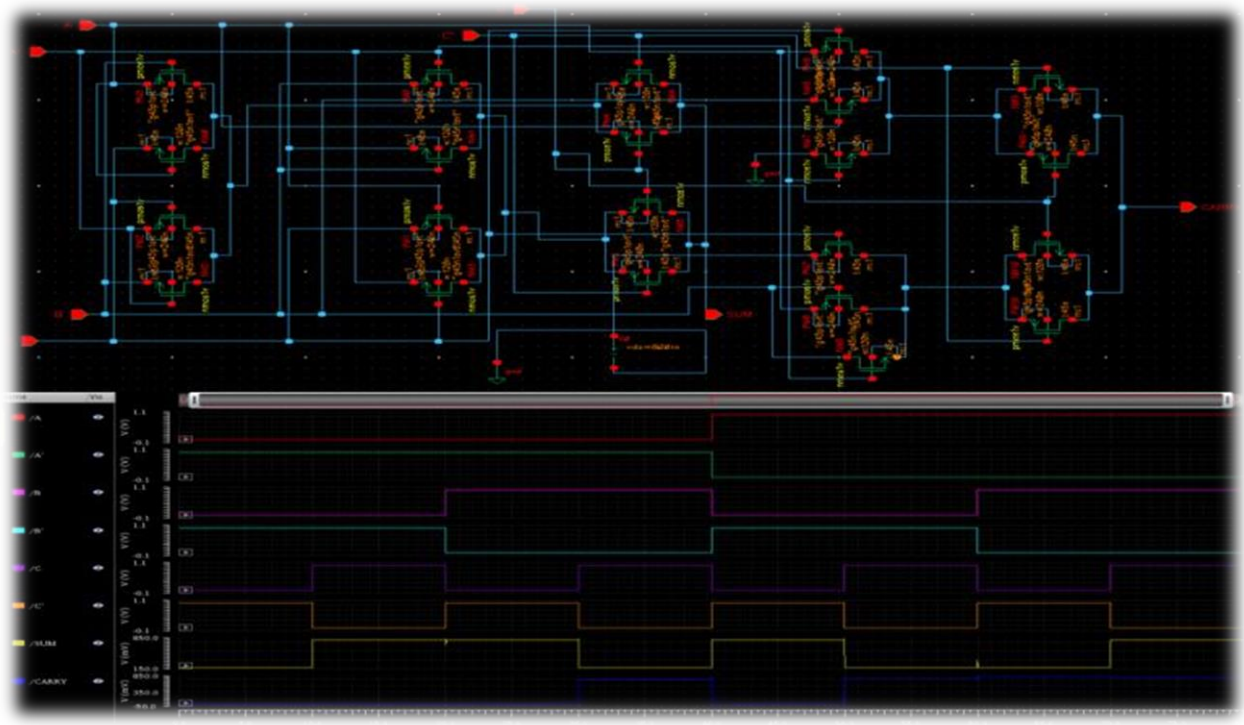
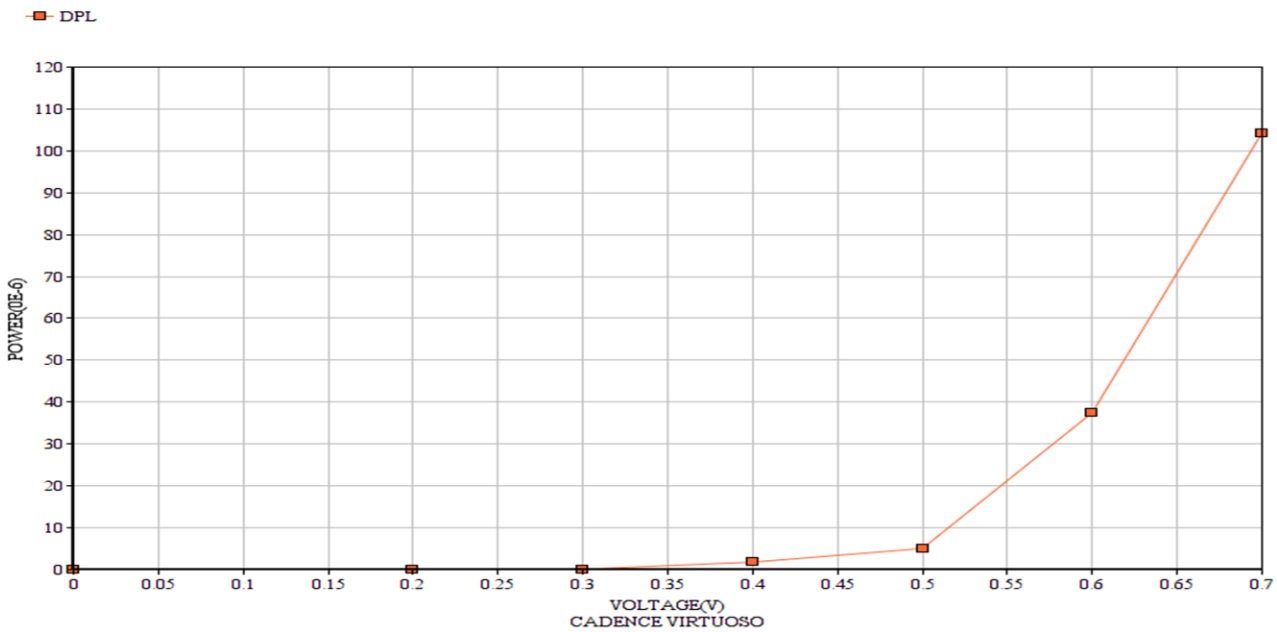


Figure 5.22 Output of Full Adder using SRC-PL in 45nm.



Graph 5.23 Power Analysis Graph for SR-CPL.

5.8 Simulation of full adder using pass transistor logic:

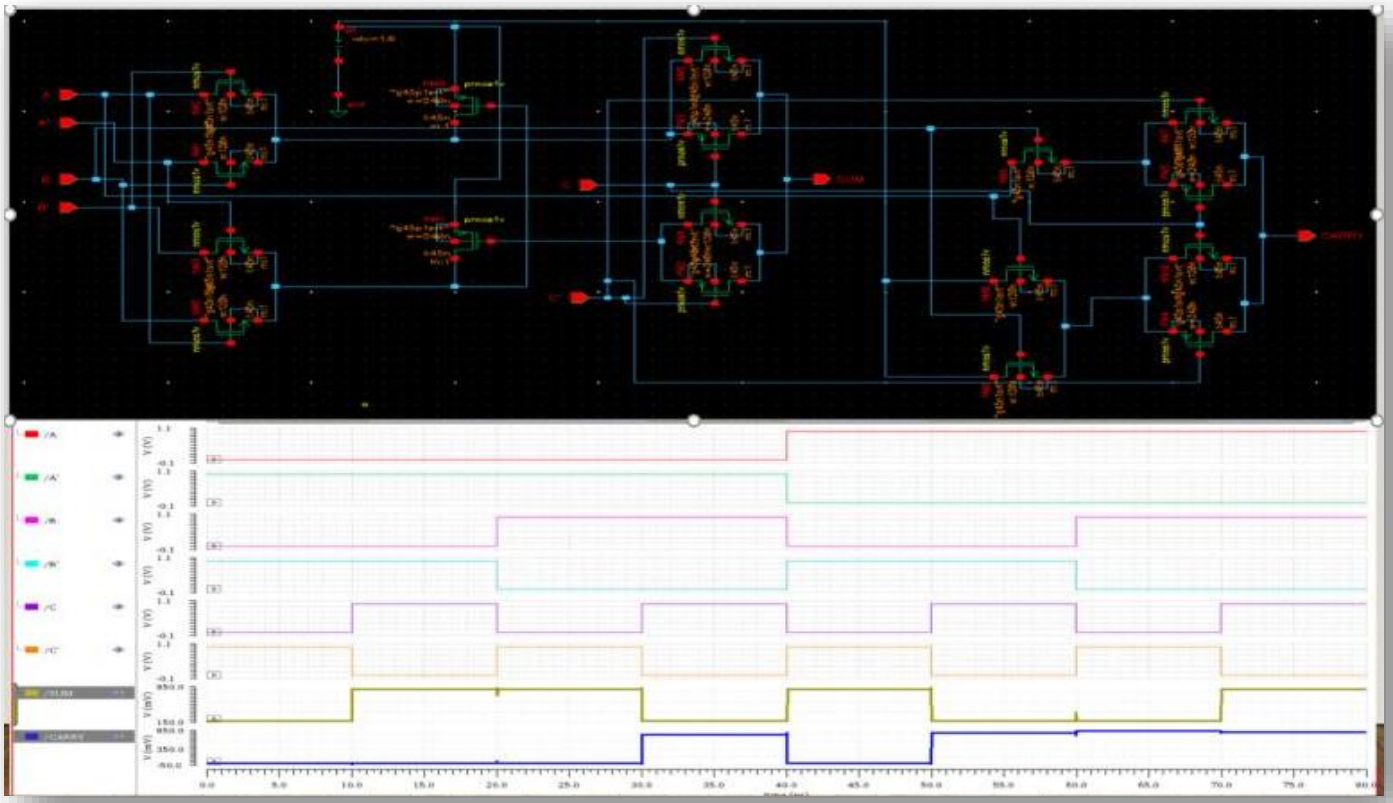
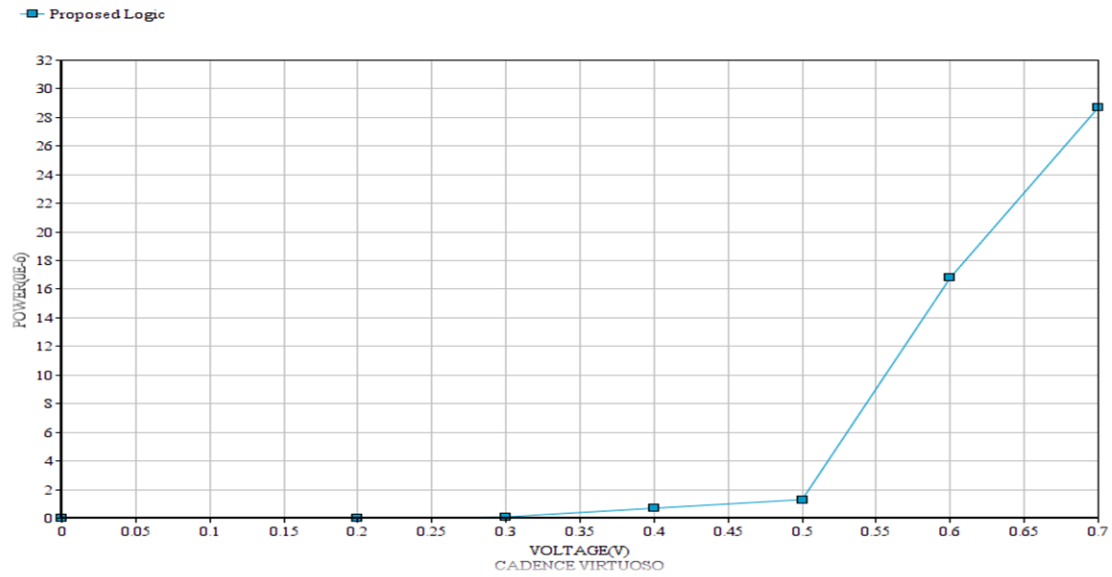
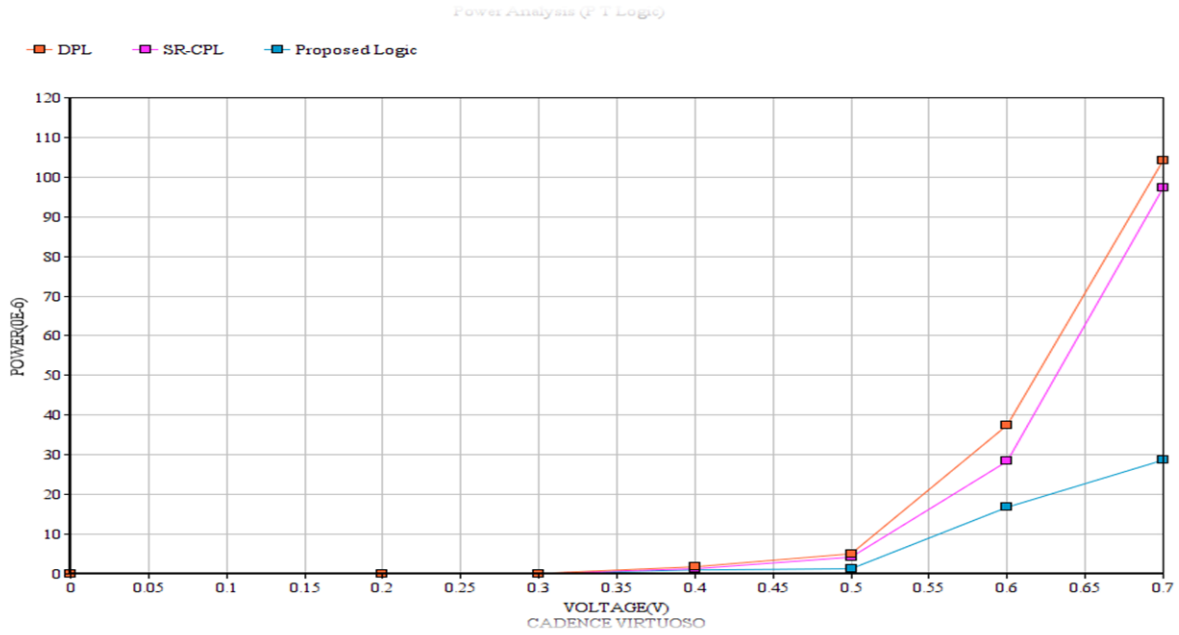


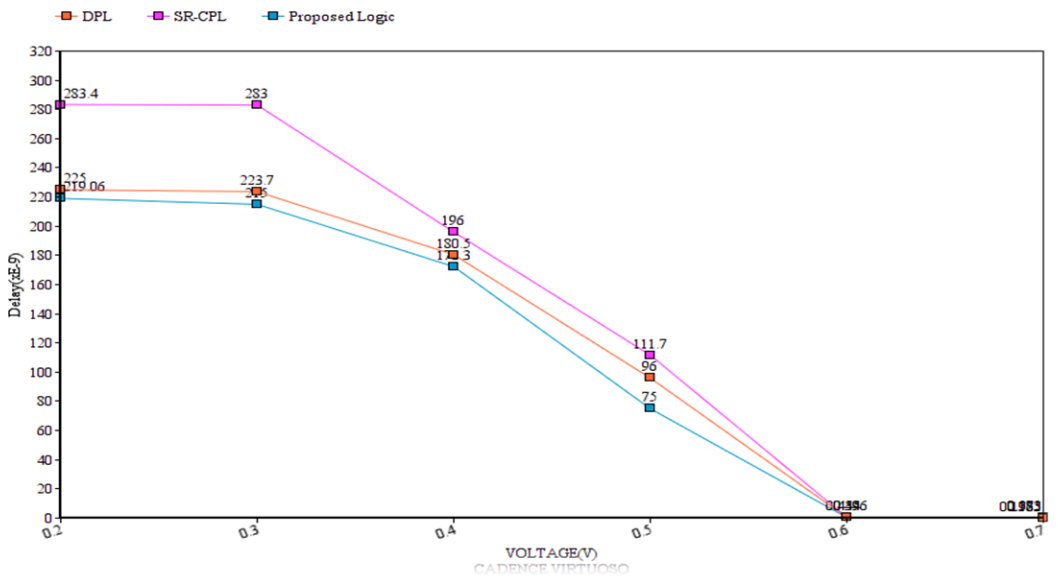
Figure 5.24 Output of Full Adder using PT logic in 45nm.



Graph 5.25 Power Analysis Graph For Pass transistor Logic.



Graph 5.26 Graphical Comparison of Power Consumed for DPL, SRC-PL, PT



Graph 5.27 Graphical Analysis of Delay for DPL, SRC-PL, PT

5.9 Simulation of full adder using transmission gates:

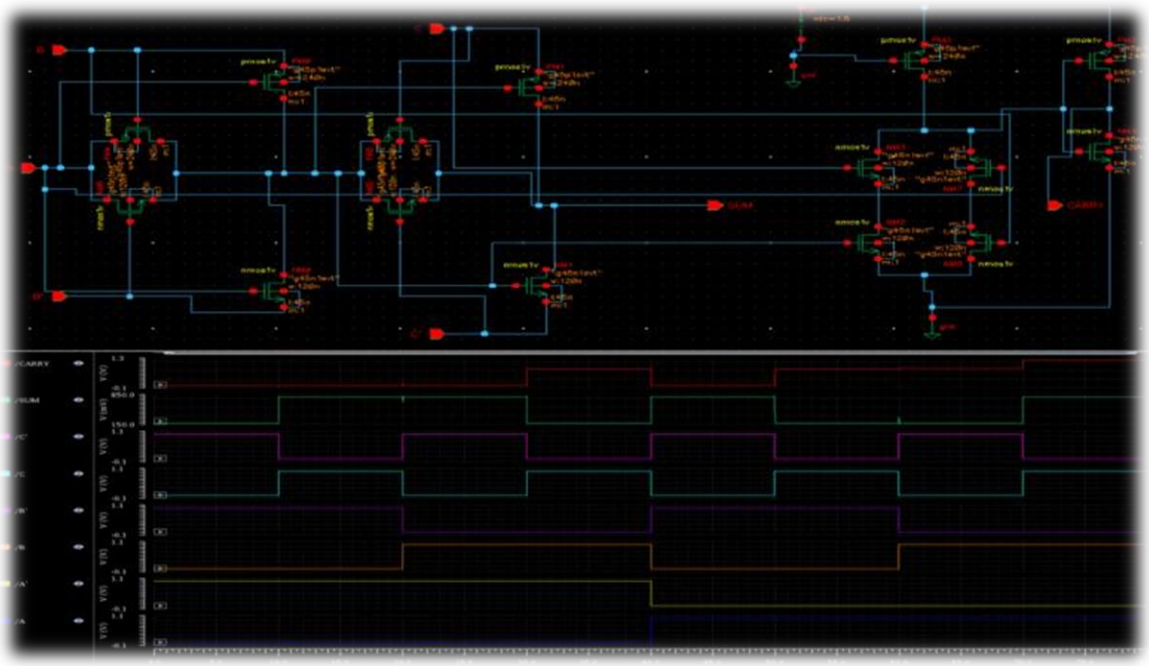
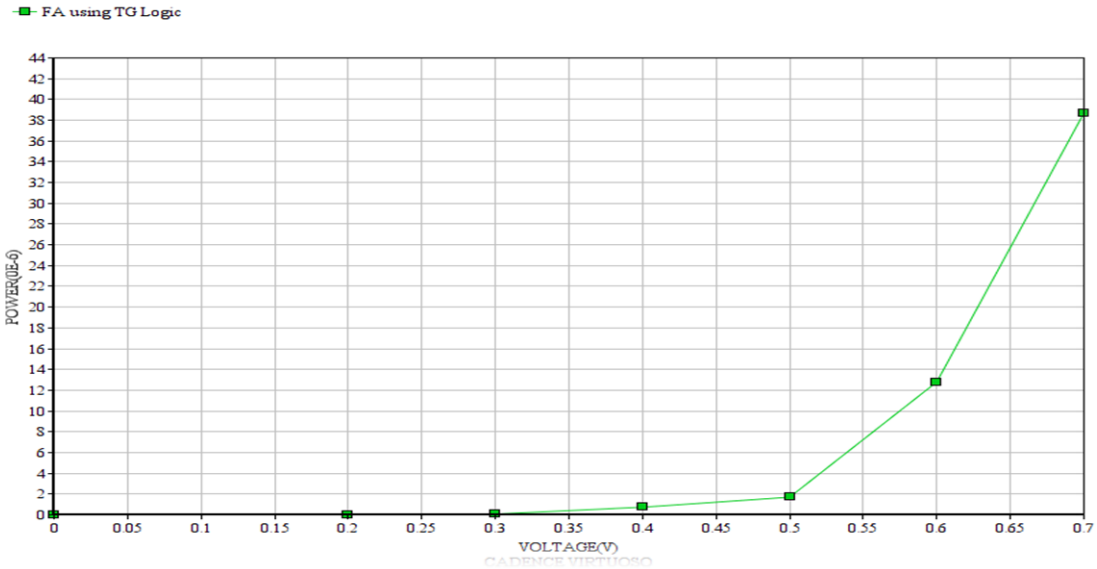
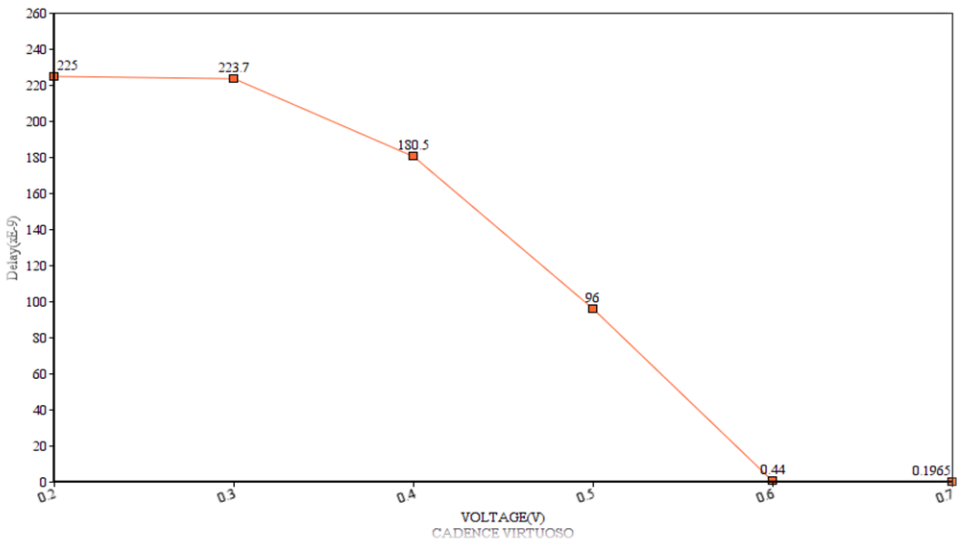


Figure 5.28 Output of Full Adder using transmission gates logic in 45nm.



Graph 5.29 Power Analysis Graph For transmission gate Logic.



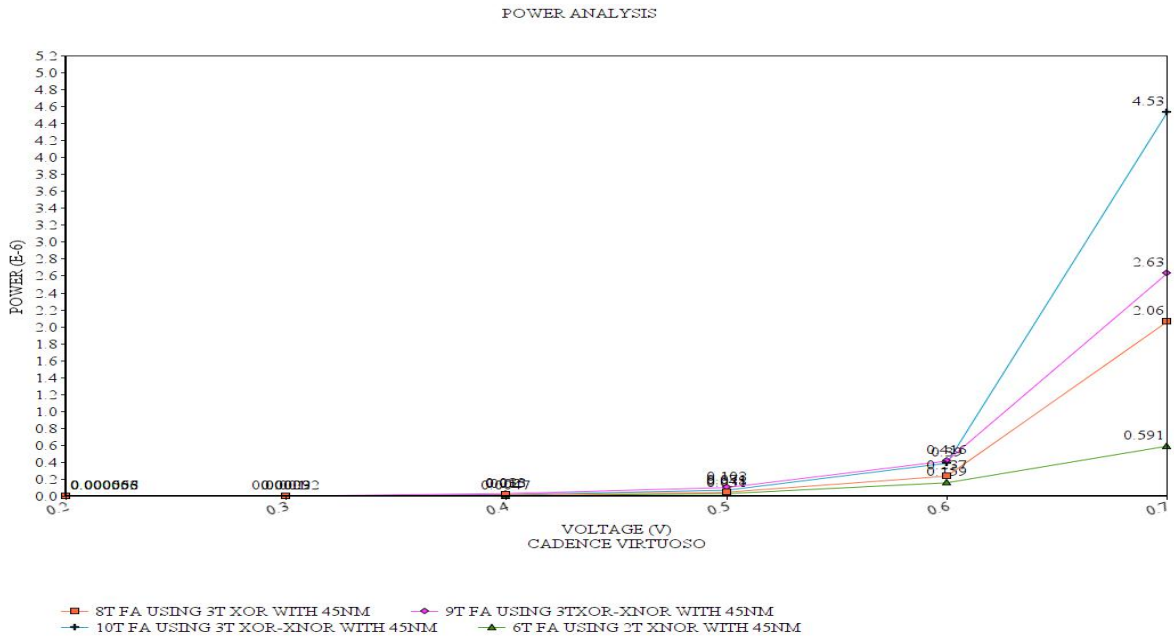
Graph 5.30 Graphical Analysis of Delay for transmission gates logic.

5.10 Comparative Analysis of Different Types of Full Adders:

FULL ADDER DESIGN	0.7	0.6	0.5	0.4	0.3	0.2
DPL LOGIC	104.3(E-6)	37.5(E-6)	5.07(E-6)	1.8(E-6)	130.4(E-9)	56.3(E-12)
SR-CPL	97.4(E-6)	28.4(E-6)	4.22(E-6)	1.0(E-6)	112.6(E-9)	45.6(E-12)
TRANSMISSION GATES	38.7(E-6)	12.8(E-6)	1.7(E-6)	0.73(E-6)	80.5(E-9)	30.03(E-12)
PASS TRANSISTOR LOGIC	28.7(E-6)	16.8(E-6)	1.3(E-6)	0.7(E-6)	88.9(E-9)	29.4(E-12)
10T USING 3T XNOR-XOR	4.53(E-6)	390.3(E-9)	71.4(E-9)	20.5(E-9)	2.2(E-9)	556.8(E-12)
9T USING 3T XNOR-XOR	2.63(E-6)	416.2(E-9)	102.9(E-9)	32.3(E-9)	2.94(E-9)	63(E-12)

8T USING 3T XOR	2.06(E-6)	237.6(E-9)	48.8(E-9)	15.7(E-9)	1.39(E-9)	56.9(E-12)
6T USING 2T XOR	591.1(E-9)	159.2(E-9)	31.11(E-9)	4.73(E-9)	32.2(E-12)	18.2(E-12)

Table 5.31 Power values for different voltages of all Full Adders in 45nm.

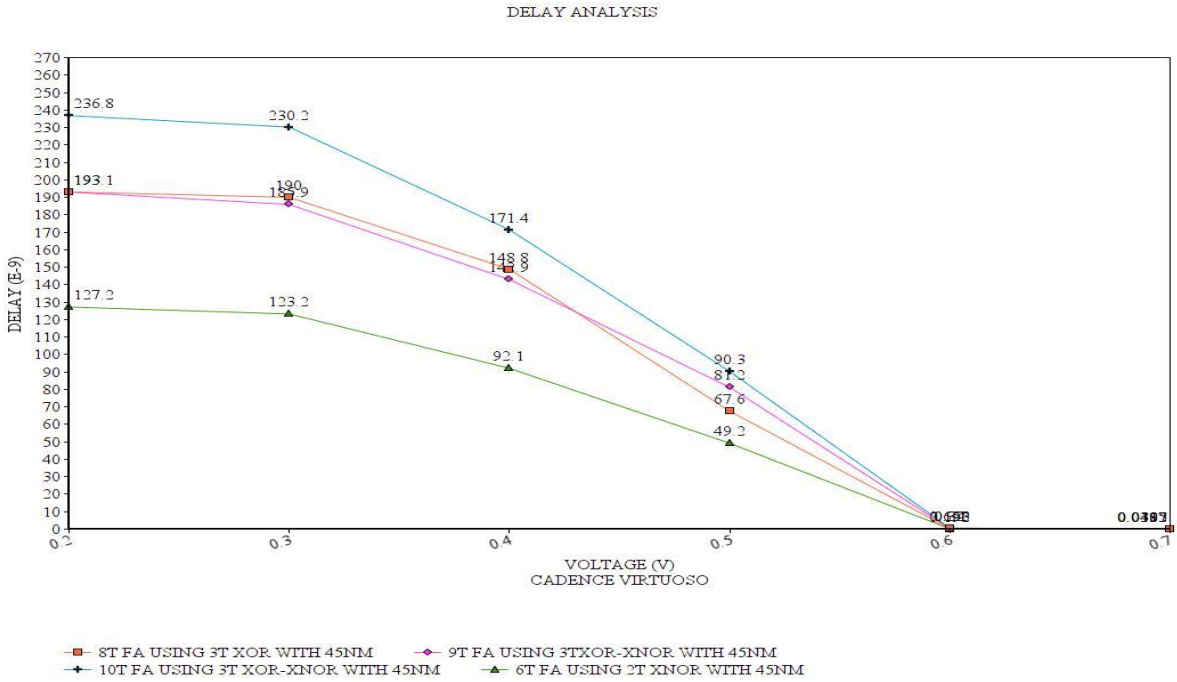


Graph 5.32 Power Graph for different voltages of all Full Adders in 45nm.

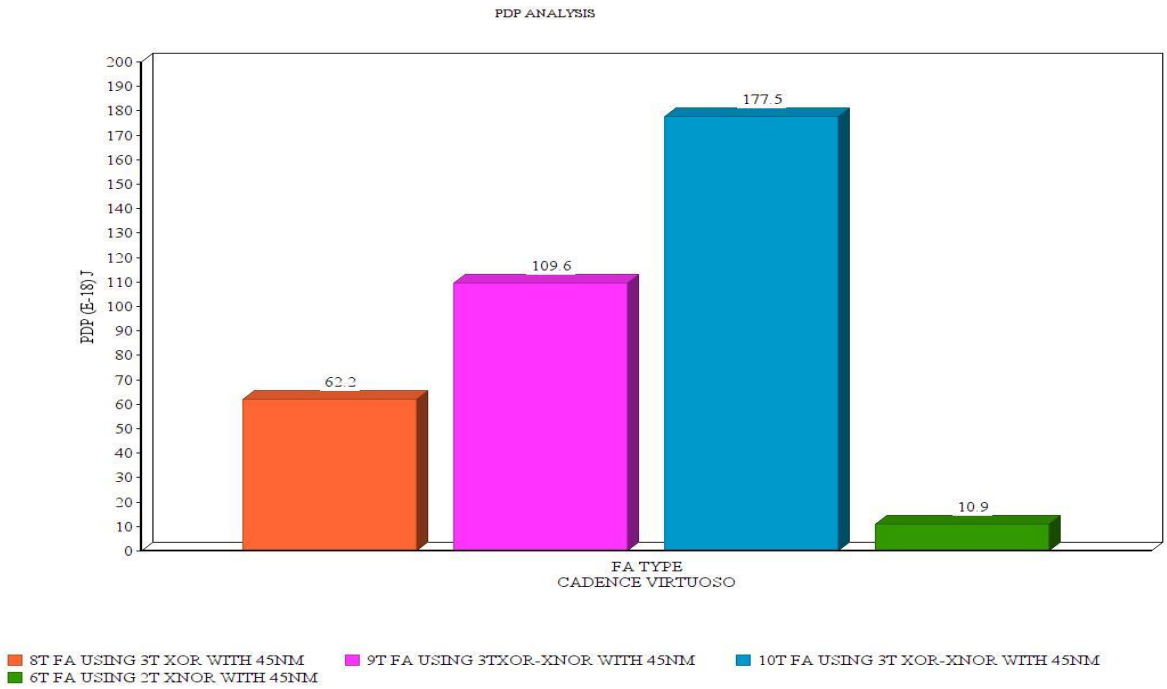
FULL ADDER DESIGN	0.7	0.6	0.5	0.4	0.3	0.2
DPL LOGIC	460.5(E-12)	716.5(E-12)	130(E-9)	203(E-9)	311.4(E-9)	315(E-9)
SR-CPL	373.6(E-12)	590(E-12)	111.7(E-9)	196(E-9)	283	283.4(E-9)
TRANSMISSION GATES	196.5(E-12)	440(E-12)	96(E-9)	180.5(E-9)	223.7(E-9)	225(E-9)

PASS TRANSISTOR LOGIC	182(E-12)	435.6(E-12)	75(E-9)	172.3(E-9)	215(E-9)	219.06(E-9)
10T USING 3T XNOR-XOR	39.2(E-12)	653.1(E-12)	90.3(E-9)	171.4(E-9)	230.2(E-9)	236.8(E-9)
9T USING 3T XNOR-XOR	41.7(E-12)	340.3(E-12)	81.2(E-9)	142.9(E-9)	185.9(E-9)	193(E-9)
8T USING 3T XOR	30.2(E-12)	320(E-12)	67.6(E-9)	148.8(E-9)	190(E-9)	193.1(E-9)
6T USING 2T XOR	18.5(E-12)	192.2(E-12)	49.2(E-9)	92.1(E-9)	123.2(E-9)	127.2(E-9)

Table 5.33 Delay values for different voltages of all Full Adders in 45nm.



Graph 5.34 Delay Graph for different voltages of all Full Adders in 45nm.



Graph 5.35 PDP Comparison for different voltages of all Full Adders in 45nm.

5.11 Summary:

All different types of full adders are simulated in Cadence Software using 45nm technology and corresponding power and delay values are noted and plotted into graphs. A comparative table is also made for all full adders for better understanding. And 6T Full Adder has the lowest PDP value.

CHAPTER 6
CONCLUSION AND FUTURE WORK

This chapter concludes the project on Performance analysis of low power hybrid CMOS full adders and suggests additional functionalities for future implantation.

6.1 Conclusion

In this project we have understood the various designing methods of full adders and implemented a new design of full adder which has the least transistor count and power consumption. In order to understand the advantages of different styles of full adders we have simulated every design in Cadence Software and compared each result and drawn their individual and overall graphs for power and delay as well.

we have observed that by reducing the power supply the power dissipation is reduced where as the delay is increased. And we also noticed that reducing transistor count also reduces the power consumption. It is to be noted that the newer designs have better performance than the older designs.

The performance of the proposed XOR–XNOR circuit and the Full Adder cells was tested by simulating them in virtuoso tool of cadence using GPDK 45 nm CMOS technology. The proposed XOR–XNOR circuit showed a reduction in terms of power, delay and PDP.

- A Minimum of 6T are used to design full adder using 2T XOR model and it had a power of 591.1nW , delay of 18.5ps and PDP of 10.9e^-18 J.
- For 8T FA simulated in cadence with 45nm technology a minimum of 2.06uW of power, delay of 30.2ps and PDP of 62.2e^-18 J.
- 9T had a power of 2.63uW, delay of 41.7ps and PDP of 109.6e^-18 J.
- 10T had a power of 4.53uW, delay of 39.2ps and PDP of 177.5e^-18 J.

6.2 Future work

In order to design a low power design there are various methodologies but in this project we used only voltage scaling method but in future we can implement the same project with other methods as well. In today's day there well be newer logic styles to design full adders such as GDI and many more. We can extend the same project for multiple bits as well. Low power designs always had a better future scope of work.

6.3 Video Presentation:

https://drive.google.com/file/d/1ePBuIXMxFDAD290oL7-o7dUQ3SRL3Fm_/view?usp=sharing

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