

2016



# EEE234 - Digital IC Design

PROJECT-1

SRIHARSHA JADHAV,

Email: sriharsha1994@outlook.com

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# 1. INVERTER

Parameters  $(W/L)_n = 1.8/0.18$  and  $(W/L)_p = 3.6/0.18$ .

input 

 output

vdd 

vss 

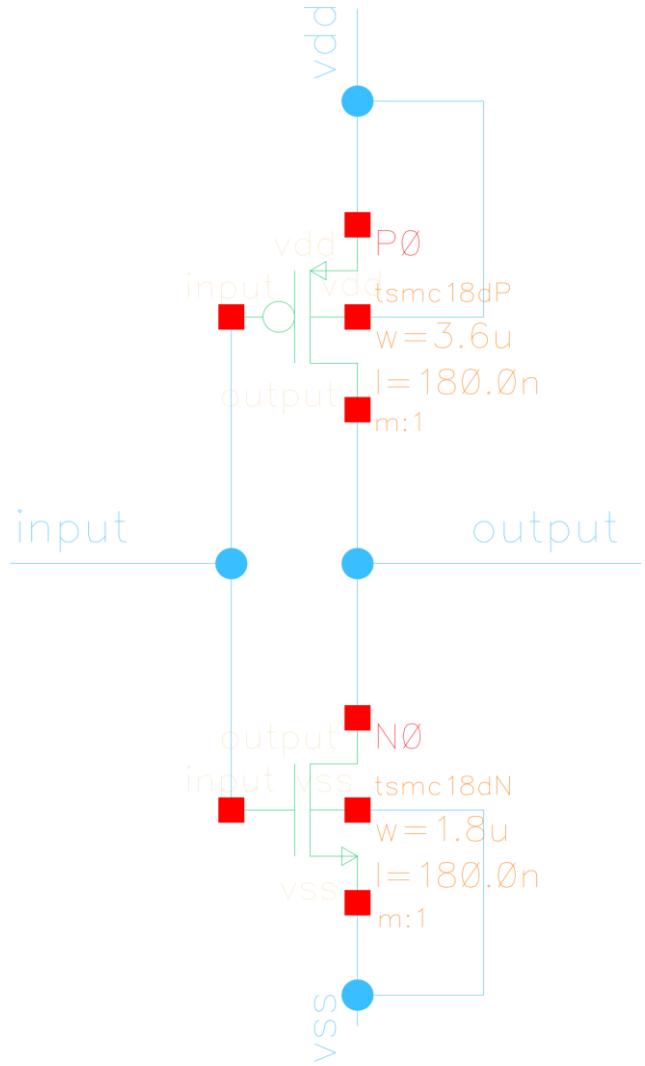
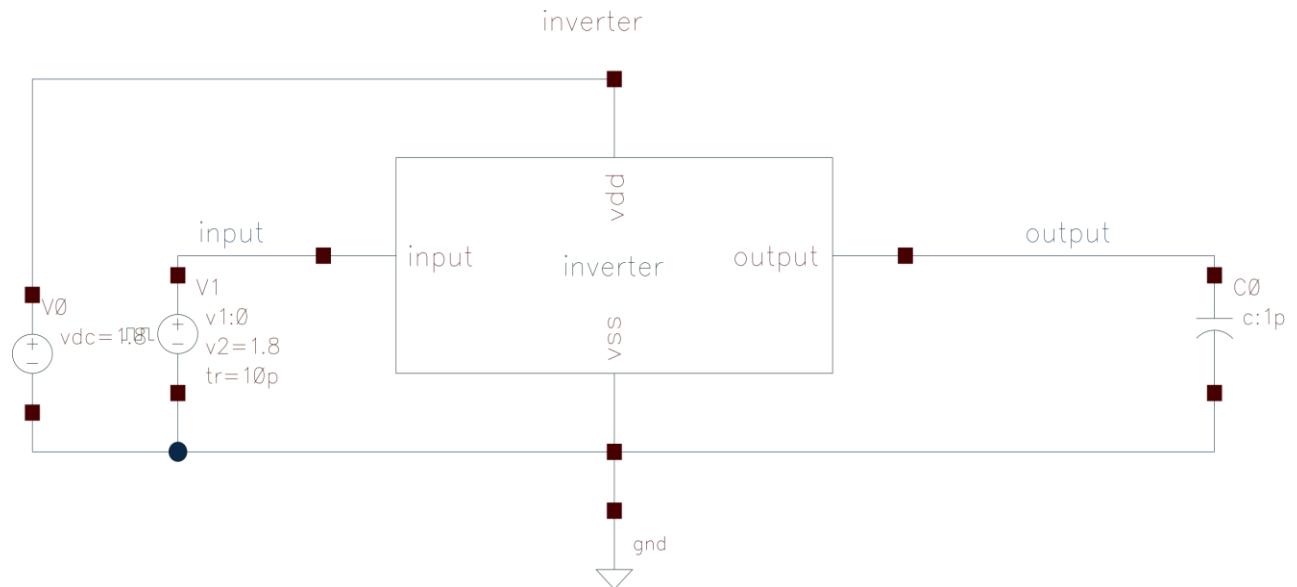


Fig 1.1: inverter schematic.

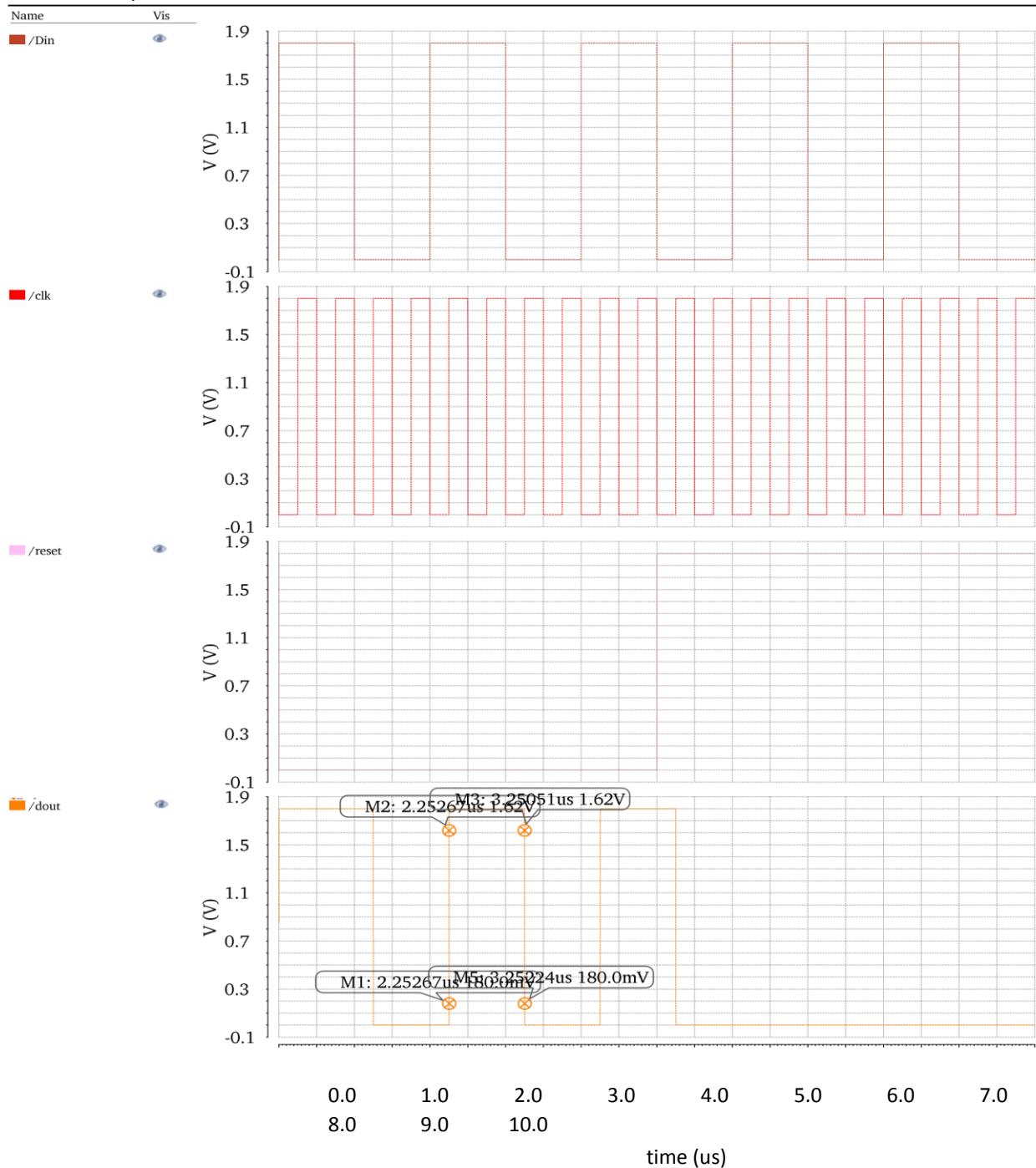


*Fig 1.2 inverter schematic test bench.*

2016

## Transient Response

Mon Oct 10 16:30:11 2016



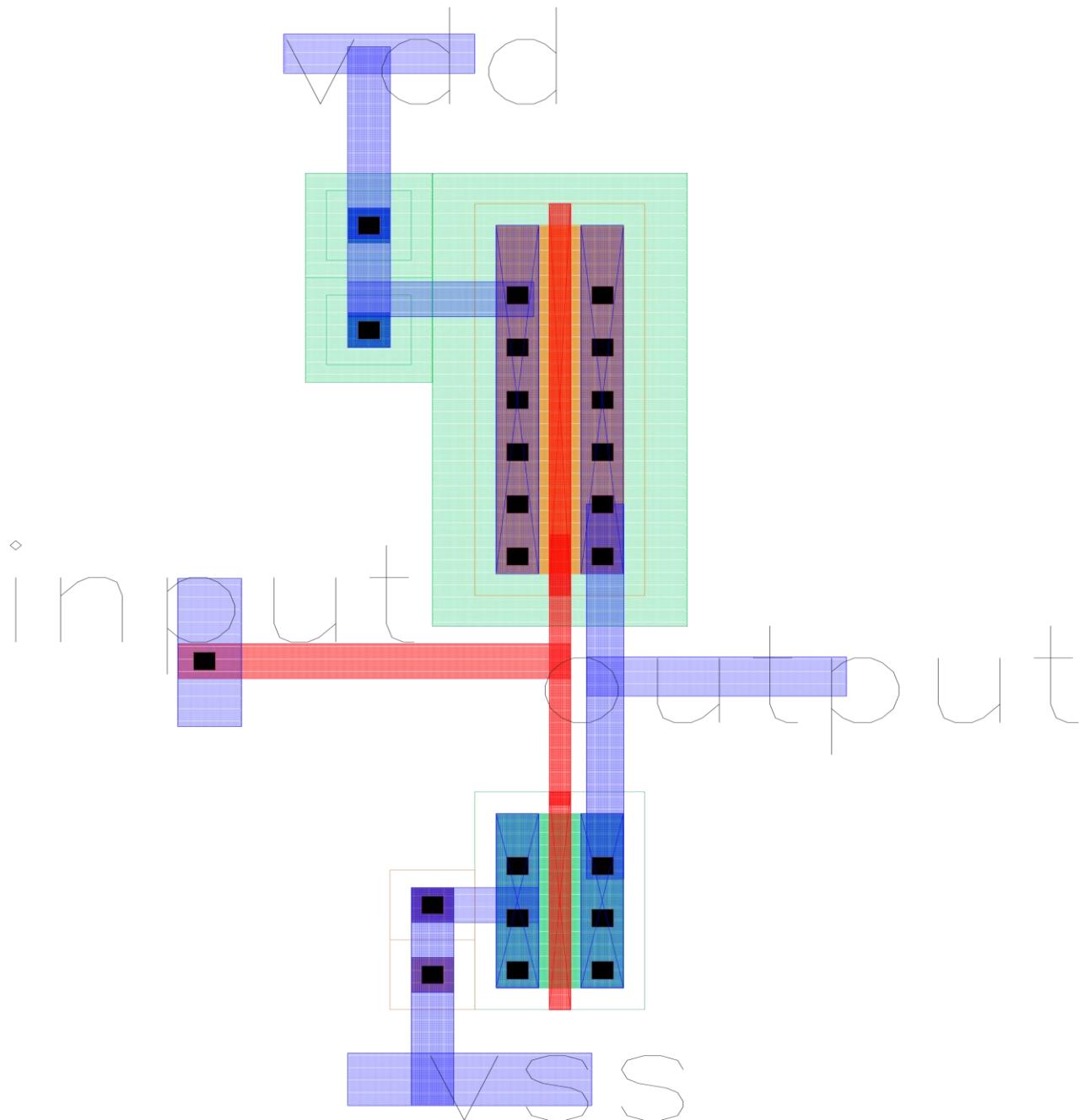


Fig 1.4: inverter layout.

## DRC REPORT:

The screenshot shows a window titled "Virtuoso® 6.1.6-64b - Log: /gaia/class/student/jadhavs/CDS.log.1". The menu bar includes "File", "Tools", "Options", and "Help". The main area displays a summary of rule violations for a cell named "inverterFIN-lay layout". It states "Total errors found: 0". The bottom status bar shows mouse coordinates and function keys: "mouse L: showClickInfo()", "M: setDRCForm()", and "R: \_lxHiMousePopUp()".

```
Virtuoso® 6.1.6-64b - Log: /gaia/class/student/jadhavs/CDS.log.1
File Tools Options Help
***** Summary of rule violations for cell "inverterFIN-lay layout" *****
Total errors found: 0
mouse L: showClickInfo()
M: setDRCForm()
R: _lxHiMousePopUp()
```

Fig 1.5: DRC no error report.

## LVS REPORT:

```
@(#) $CDS: LVS version 6.1.6-64b 09/01/2015 22:33 (sjfnl138) $  
  
Command line: /software/IC616/tools.lnx86/dfII/bin/64bit/LVS -dir  
/gaia/class/student/jadhavs/Desktop/harsha/LVS -l -s -t  
/gaia/class/student/jadhavs/Desktop/harsha/LVS/layout  
/gaia/class/student/jadhavs/Desktop/harsha/LVS/schematic  
Like matching is enabled.  
Net swapping is enabled.  
Using terminal names as correspondence points.  
Compiling Diva LVS rules...
```

```
Net-list summary for  
/gaia/class/student/jadhavs/Desktop/harsha/LVS/layout/netlist  
count  
4 nets  
0 terminals  
1 pmos  
1 nmos
```

```
Net-list summary for  
/gaia/class/student/jadhavs/Desktop/harsha/LVS/schematic/netlist  
count  
4 nets  
4 terminals  
1 pmos  
1 nmos
```

Devices in the rules but not in the netlist:  
cap nfet pfet nmos4 pmos4

The net-lists match.

	layout	schematic
	instances	instances
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	2	2
total	2	2

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	4	4
total	4	4

	terminals	
un-matched	0	0
matched but different type	0	0

total	0	4
-------	---	---

Probe files from /gaia/class/student/jadhavs/Desktop/harsha/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/jadhavs/Desktop/harsha/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

## 2. TWO-INPUT NAND GATE

Parameters (W/L)<sub>n</sub>=5.4/0.18 and (W/L)<sub>p</sub>= 3.6/0.18.

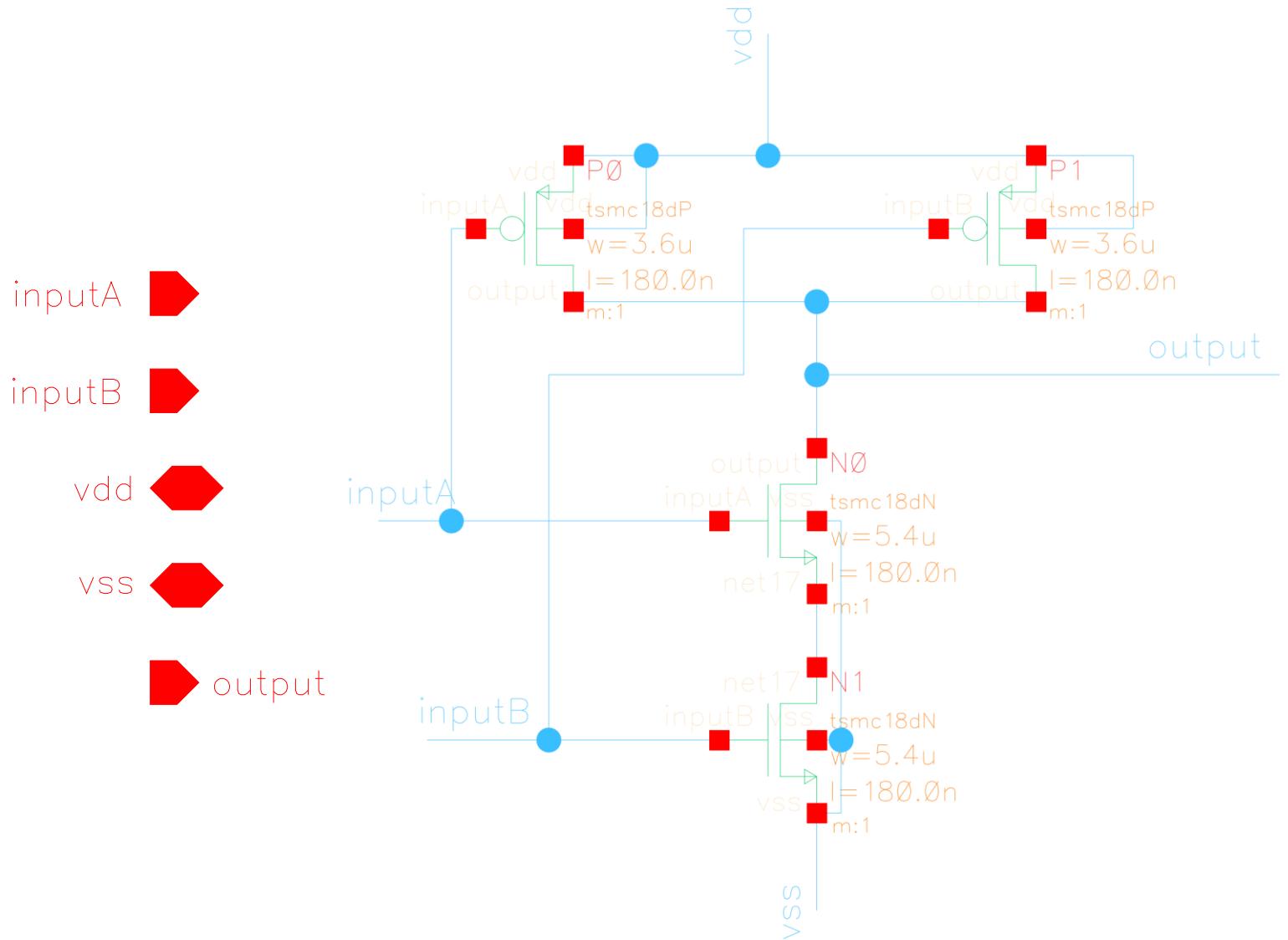


Fig 2.1: schematic diagram for 2 input NAND gate

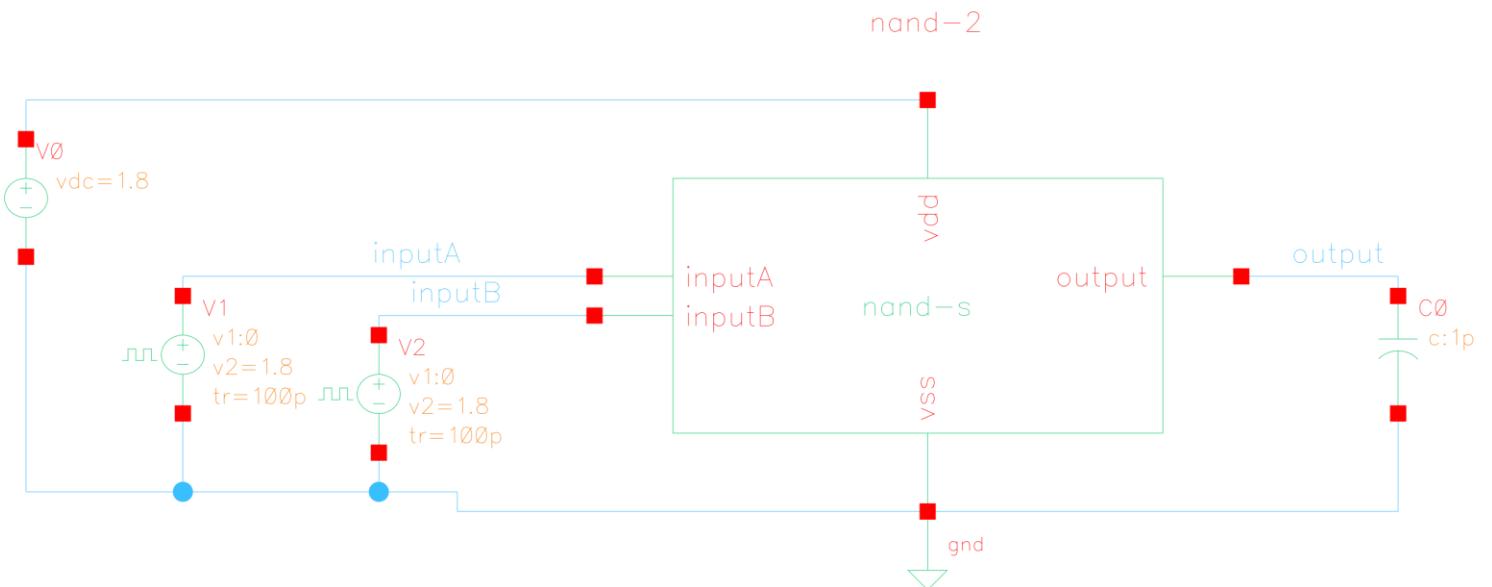
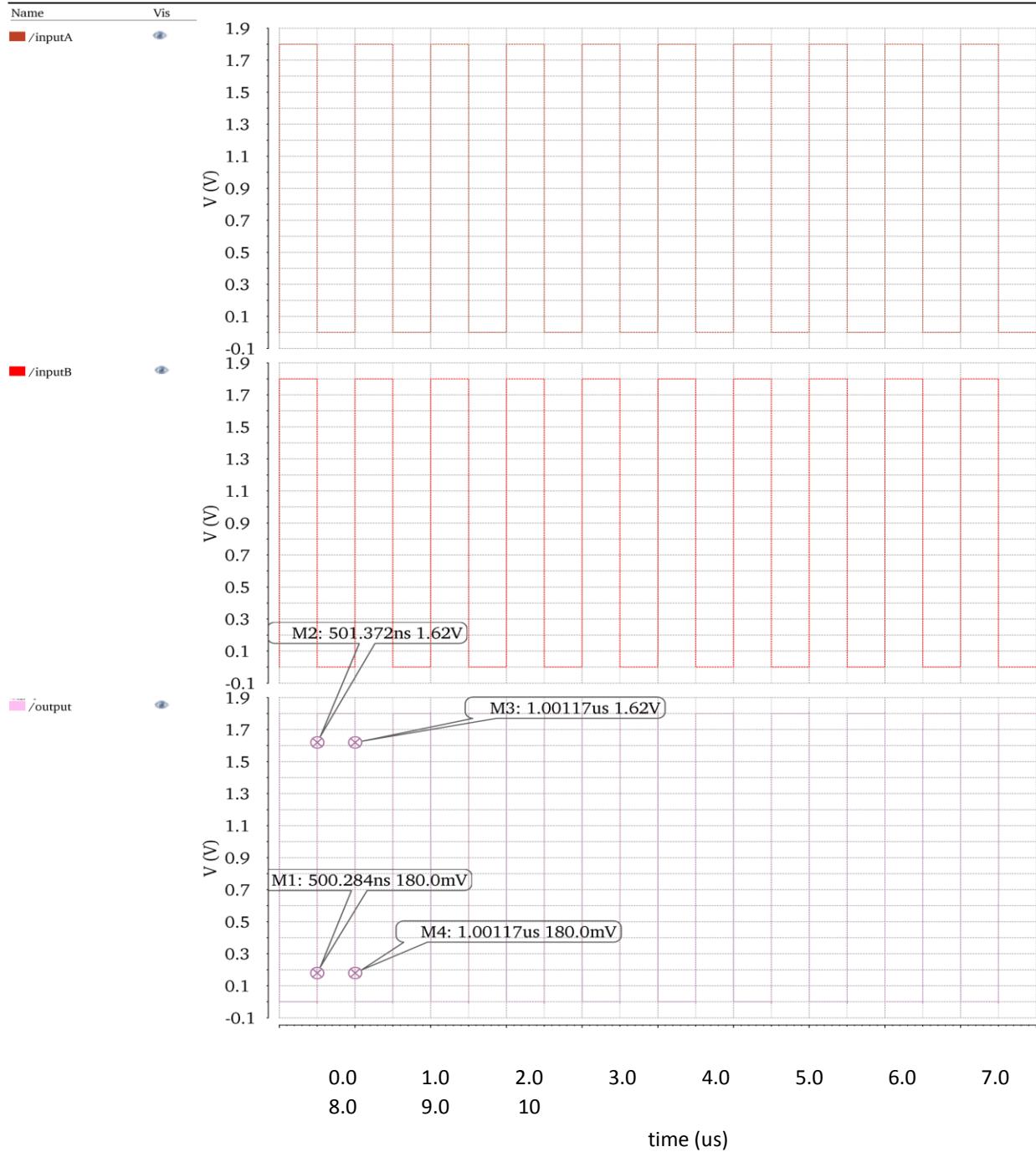


Fig 2.2: 2 input NAND gate test bench.

## Transient Response

Mon Oct 10 16:52:07 2016

*Fig 2.3: 2 input NAND output waveform.*

## LAYOUT:

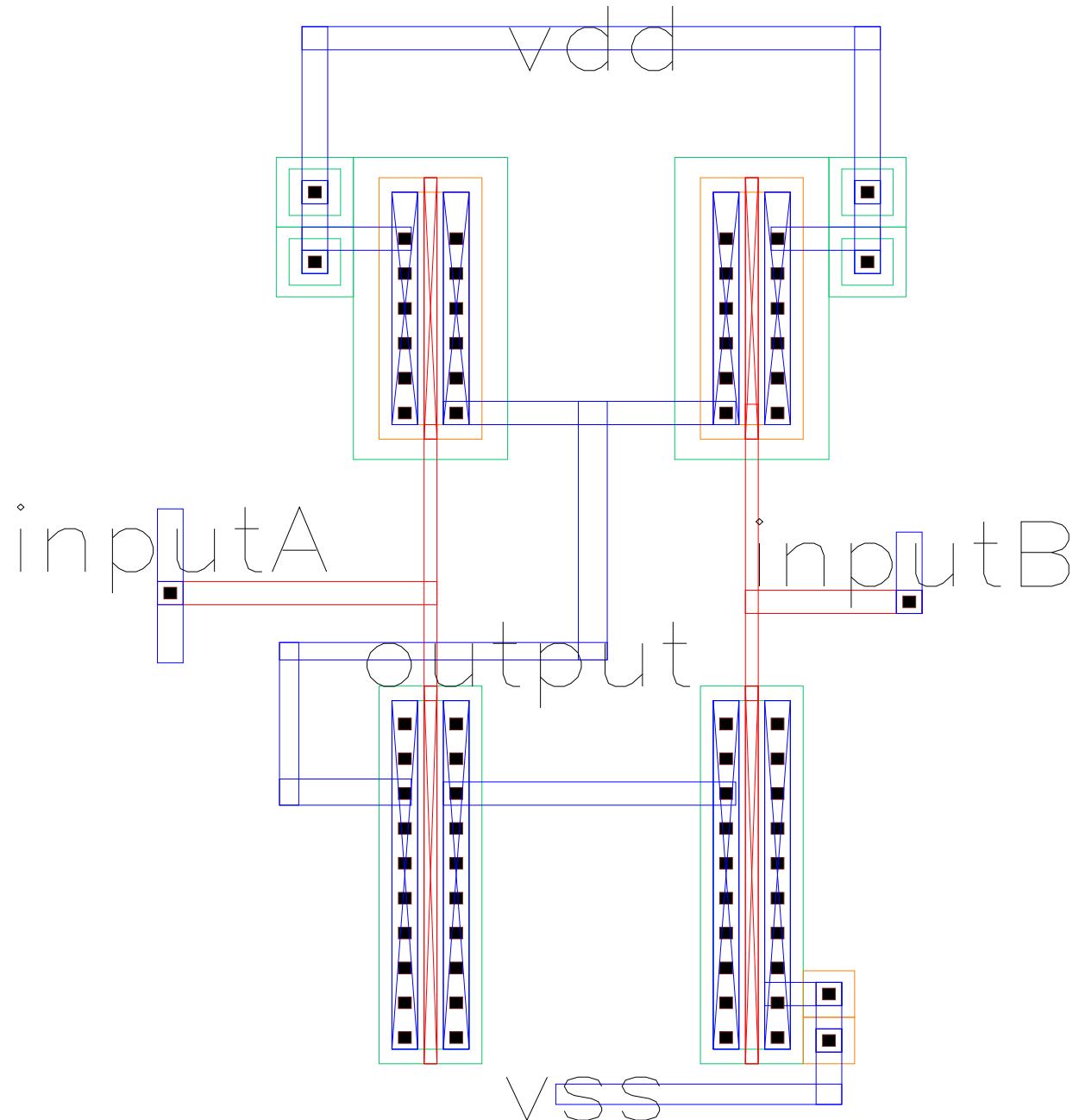


Fig 2.4: 2 input NAND gate layout diagram.

DRC REPORT:

The screenshot shows a window titled "Virtuoso® 6.1.6-64b - Log: /gaia/class/student/jadhavs/CDS.log.1". The menu bar includes "File", "Tools", "Options", and "Help". The main area displays a summary of rule violations for the cell "nand\_new-layout layout". It states "Total errors found: 0". Below this, there is a scrollable log area with entries: "L: showClickInfo()", "M: setDRCForm()", and "R: \_JxHiMousePopUp()".

Fig 2.5: DRC REPORT.

## LVS REPORT:

```
@(#) $CDS: LVS version 6.1.6-64b 09/01/2015 22:33 (sjfnl138) $  
Command line: /software/IC616/tools.lnx86/dfII/bin/64bit/LVS -dir  
/gaia/class/student/jadhavs/Desktop/harsha/LVS -l -s -t  
/gaia/class/student/jadhavs/Desktop/harsha/LVS/layout  
/gaia/class/student/jadhavs/Desktop/harsha/LVS/schematic  
Like matching is enabled.  
Net swapping is enabled.  
Using terminal names as correspondence points.  
Compiling Diva LVS rules...
```

```
Net-list summary for  
/gaia/class/student/jadhavs/Desktop/harsha/LVS/layout/netlist  
count  
6 nets  
0 terminals  
2 pmos  
2 nmos
```

```
Net-list summary for  
/gaia/class/student/jadhavs/Desktop/harsha/LVS/schematic/netlist  
count  
6 nets  
5 terminals  
2 pmos  
2 nmos
```

Devices in the rules but not in the netlist:

```
cap nfet pfet nmos4 pmos4
```

1 net-list ambiguity was resolved by random selection.

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	4	4
total	4	4

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	6	6
total	6	6

	terminals	
un-matched	0	0

matched but		
different type	0	0
total	0	5

Probe files from /gaia/class/student/jadhavs/Desktop/harsha/LVS/schematic  
devbad.out:  
netbad.out:  
mergenet.out:  
termbad.out:  
prunenet.out:  
prunedev.out:  
audit.out:

Probe files from /gaia/class/student/jadhavs/Desktop/harsha/LVS/layout  
devbad.out:  
netbad.out:  
mergenet.out:  
termbad.out:  
prunenet.out:  
prunedev.out:  
audit.out:

### 3. THREE INPUT NOR GATE:

Parameters (W/L)  $n = 1.8/0.18$  and (W/L)  $p = 7.2/0.18$ .

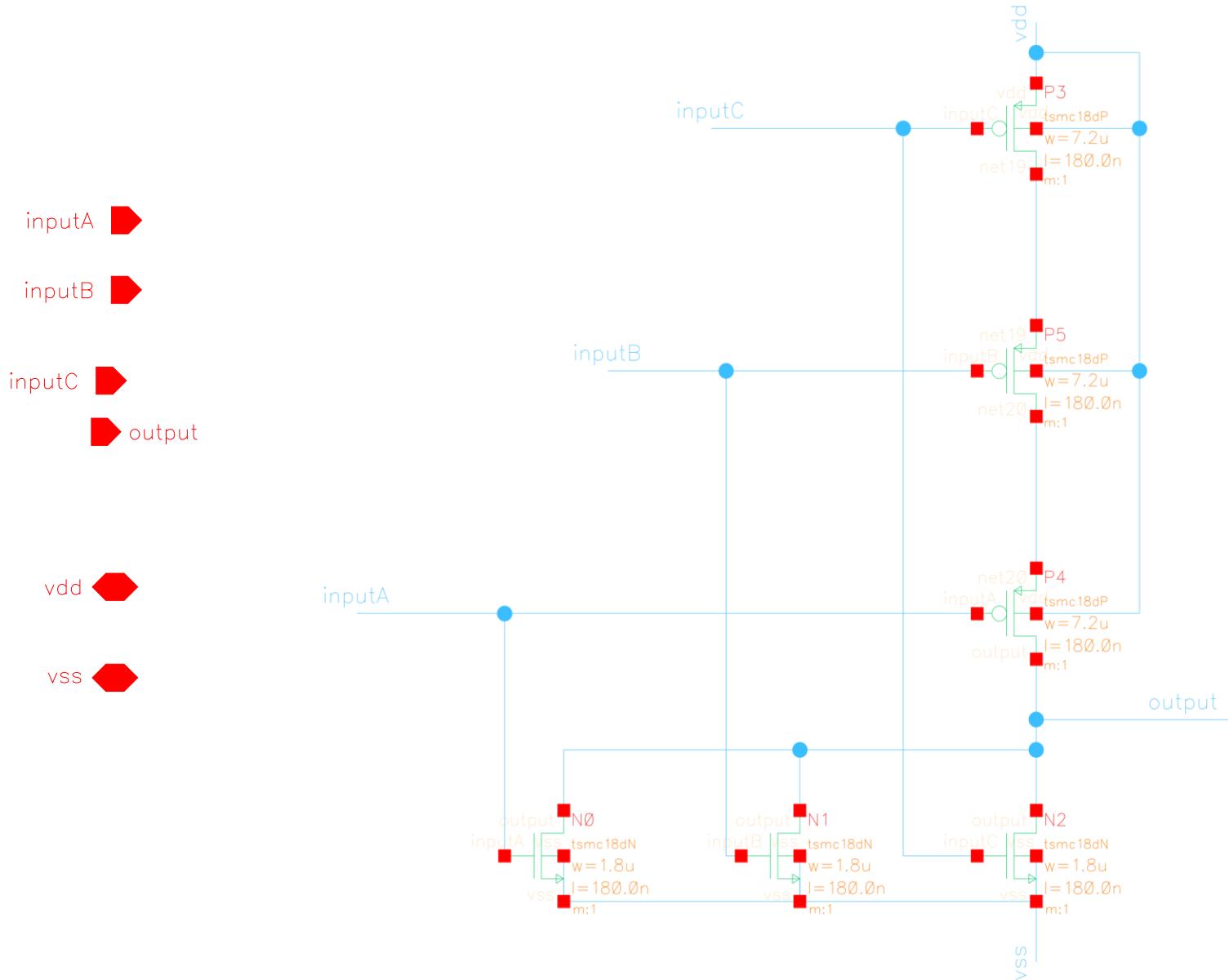


Fig 3.1: three input NOR gate schematic diagram.

## TESTBENCH SCHEMATIC:

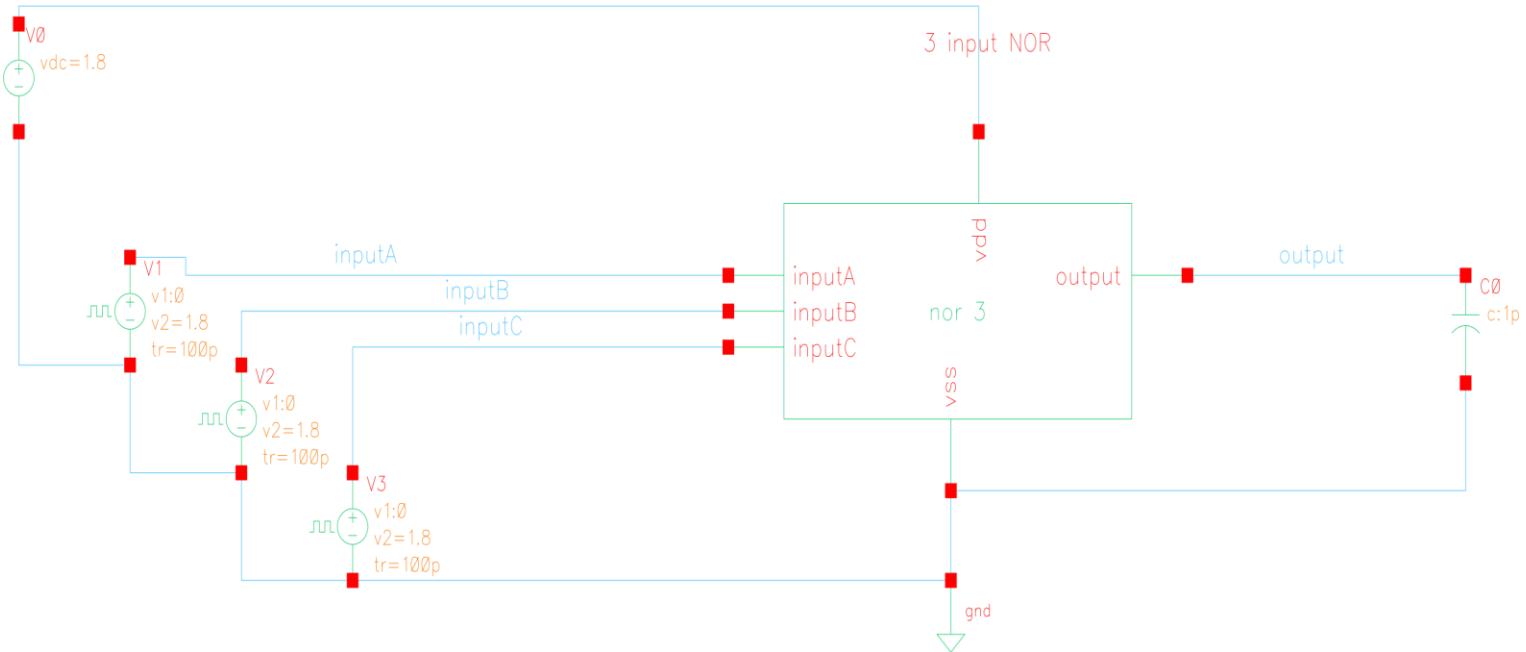


Fig 3.2: three input NOR gate test bench.

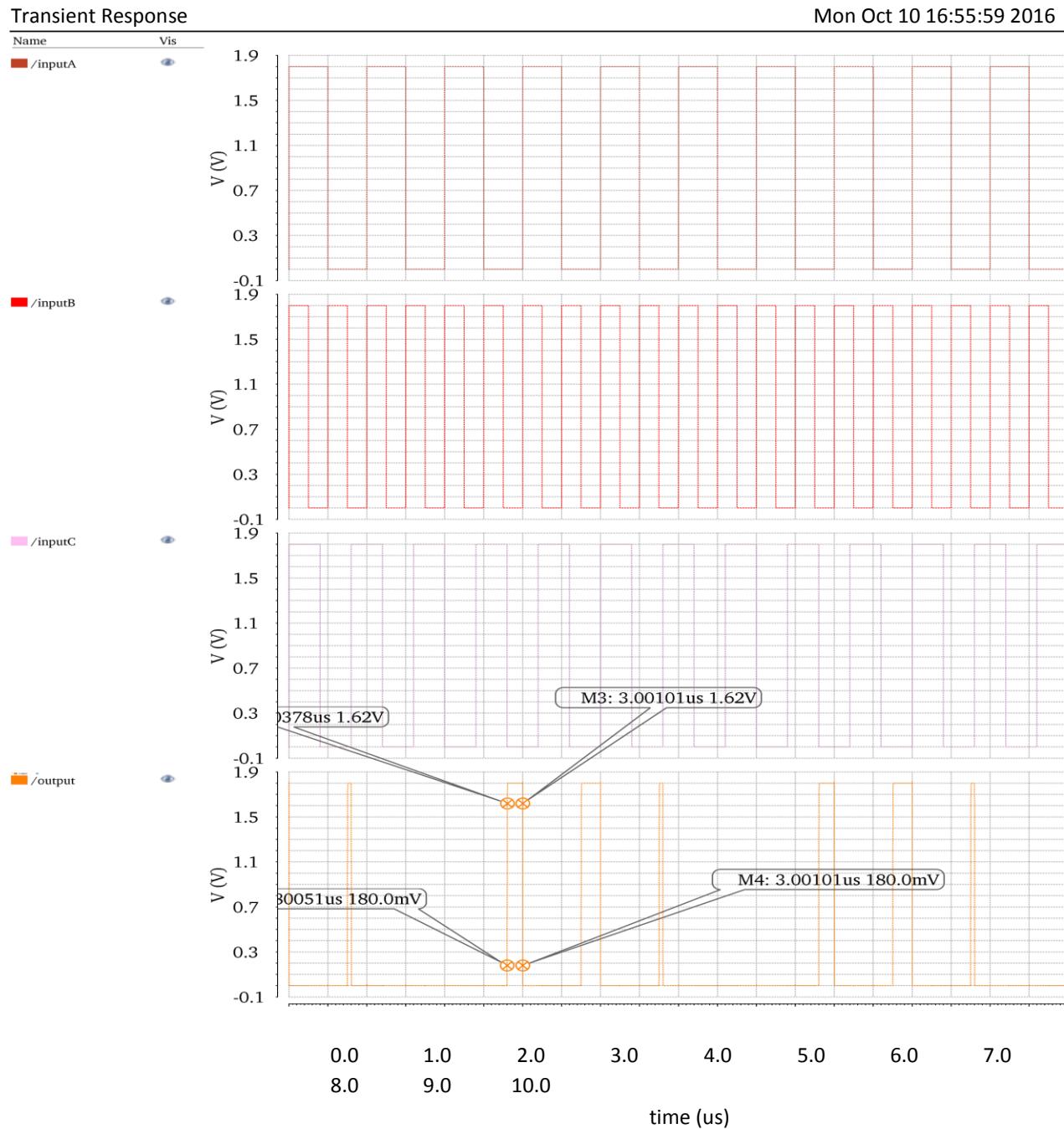


Fig 3.3: three input NOR output waveform

## LAYOUT:

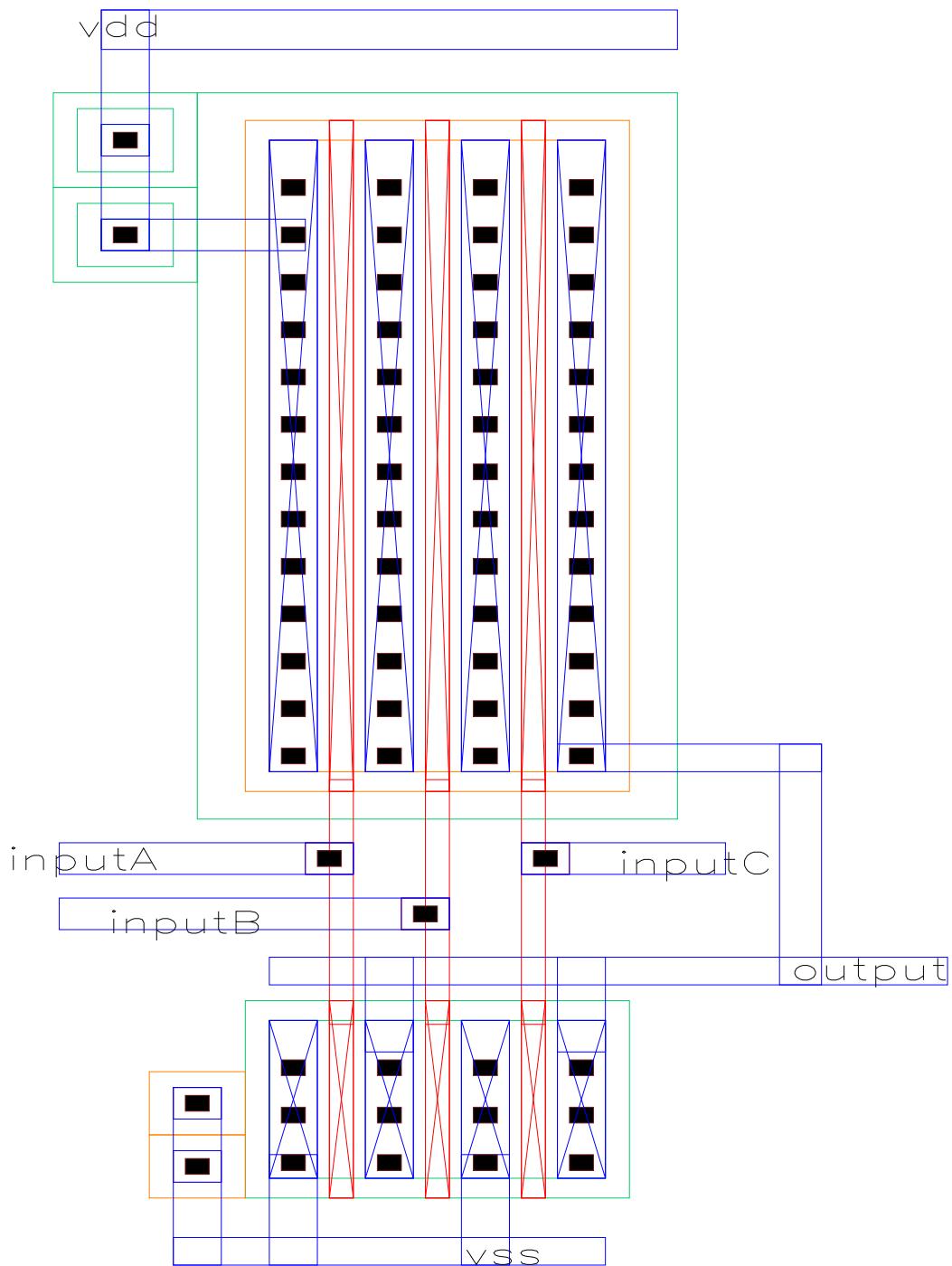


Fig 3.4: three input NOR gate layout.

DRC REPORT:

The screenshot shows a CADENCE software interface titled "Virtuoso® 6.1.6-64b - Log: /gaia/class/student/jadhavs/CDS.log.1". The menu bar includes "File", "Tools", "Options", and "Help". The main window displays a summary of rule violations for the cell "nor-3-layout layout". It states "Total errors found: 0". Below this, there is a status bar with the text "m:mouse L: showClickInfo()", "M: setDRCForm()", and "R: \_lxHiMousePopUp()". A scroll bar is visible on the right side of the main window.

Fig 3.4: DRC report.

## LVS REPORT:

```
@(#) $CDS: LVS version 6.1.6-64b 09/01/2015 22:33 (sjfnl138) $  
  
Command line: /software/IC616/tools.lnx86/dfII/bin/64bit/LVS -dir  
/gaia/class/student/jadhavs/LVS -l -s -t  
/gaia/class/student/jadhavs/LVS/layout  
/gaia/class/student/jadhavs/LVS/schematic  
Like matching is enabled.  
Net swapping is enabled.  
Using terminal names as correspondence points.  
Compiling Diva LVS rules...  
  
Net-list summary for /gaia/class/student/jadhavs/LVS/layout/netlist  
count  
  8      nets  
  0      terminals  
  3      pmos  
  3      nmos  
  
Net-list summary for /gaia/class/student/jadhavs/LVS/schematic/netlist  
count  
  8      nets  
  6      terminals  
  3      pmos  
  3      nmos  
  
Devices in the rules but not in the netlist:  
  cap nfet pfet nmos4 pmos4  
  
2 net-list ambiguities were resolved by random selection.  
  
The net-lists match.  
  
          layout schematic  
                  instances  
un-matched          0      0  
rewired            0      0  
size errors        0      0  
pruned             0      0  
active              6      6  
total               6      6  
  
          nets  
un-matched          0      0  
merged              0      0  
pruned              0      0  
active              8      8  
total               8      8  
  
          terminals  
un-matched          0      0  
matched but  
different type      0      0
```

total	0	6
-------	---	---

Probe files from /gaia/class/student/jadhavs/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/jadhavs/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

#### 4. TWO INPUT XOR GATE:

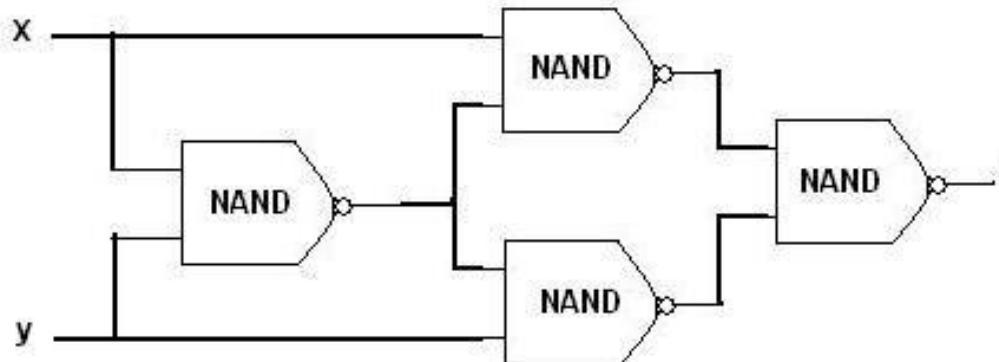


Fig 4.1: two input XOR gate using 4 - two input NAND gates:

A two input XOR gate can be realized using 4 two input NAND gates. The fig 4.1 shows the logical circuit diagram of XOR using NAND fig 4.2.

Parameters  $(W/L)_n = 3.6/0.18$  and  $(W/L)_p = 7.2/0.18$ .

#### SCHEMATIC FOR 2 INPUT NAND:

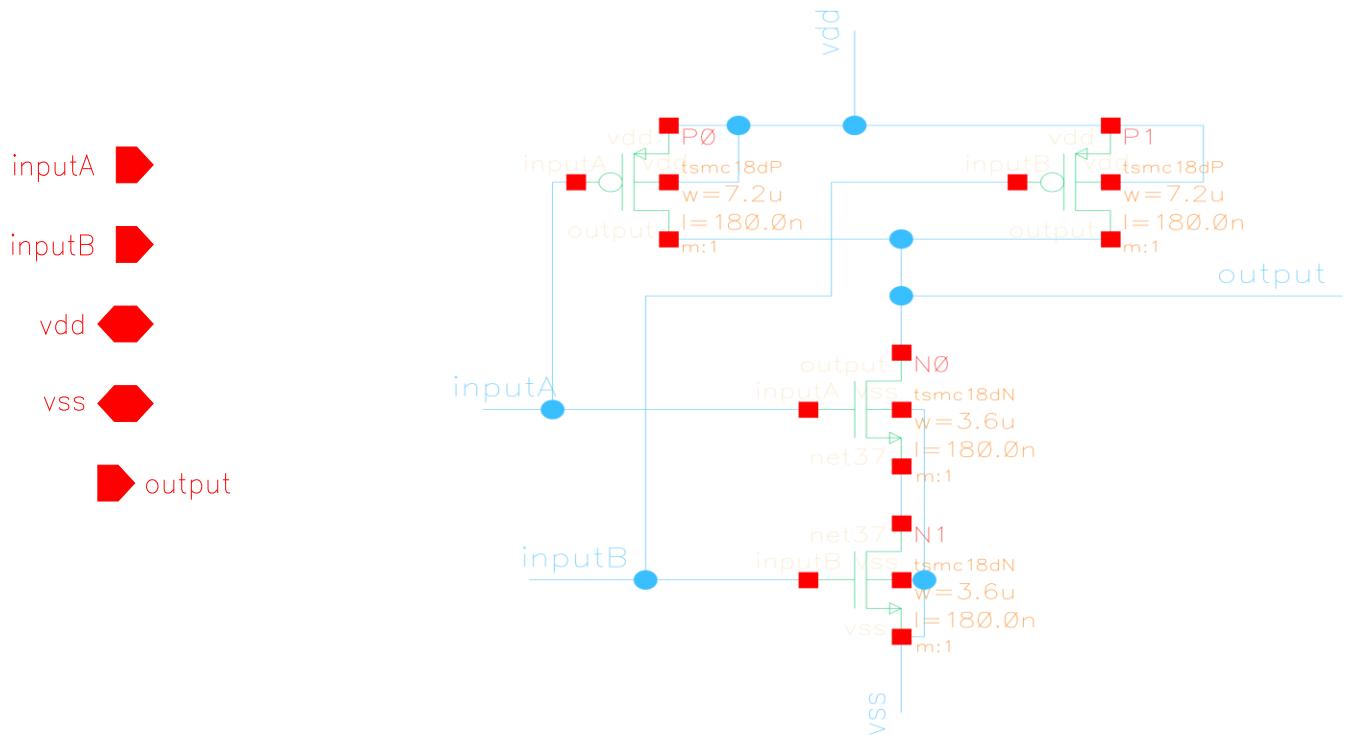
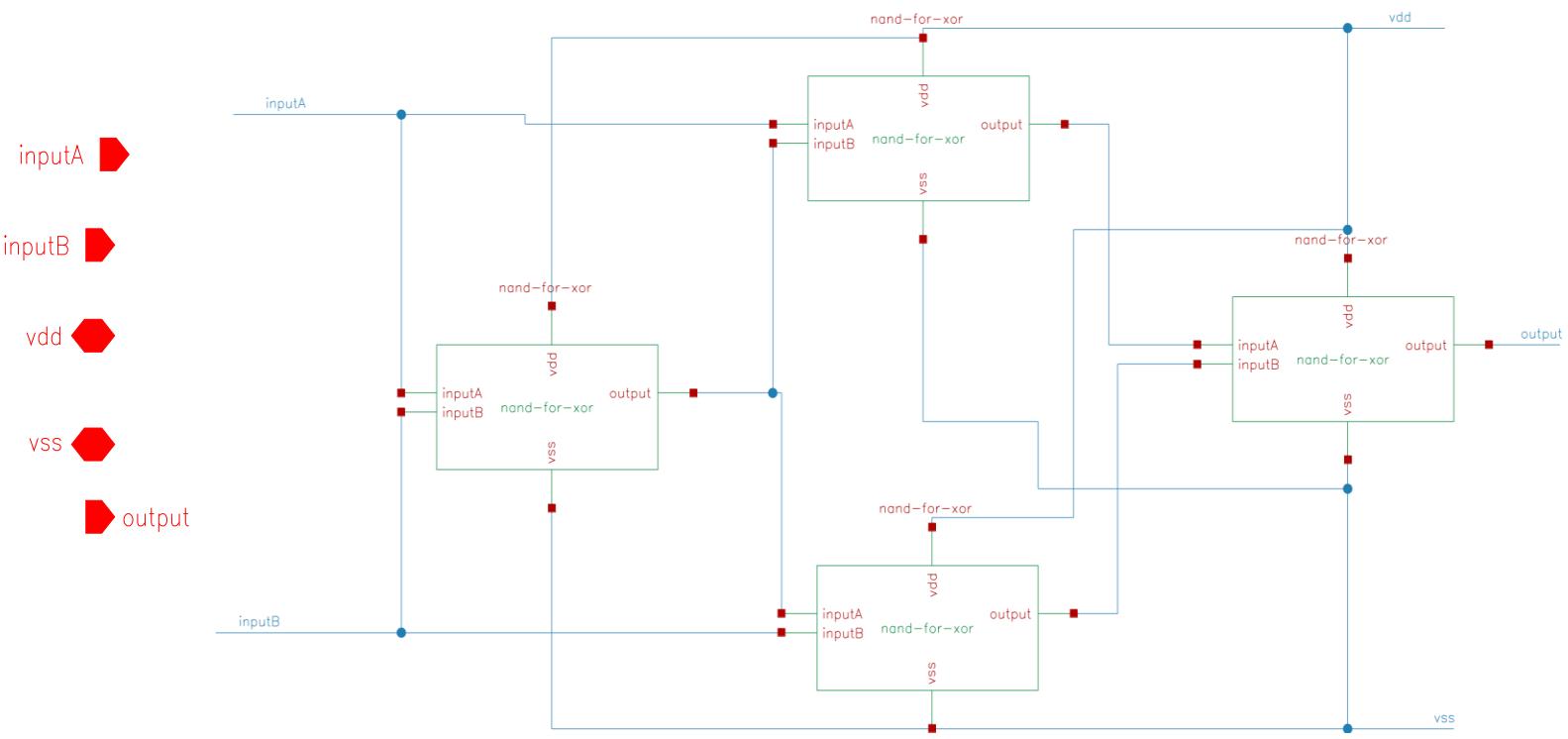


Fig 4.2: two input NAND gate.

## SCHEMATIC DIAGRAM:



*Fig 4.3 XOR gate schematic diagram.*

## TEST BENCH:

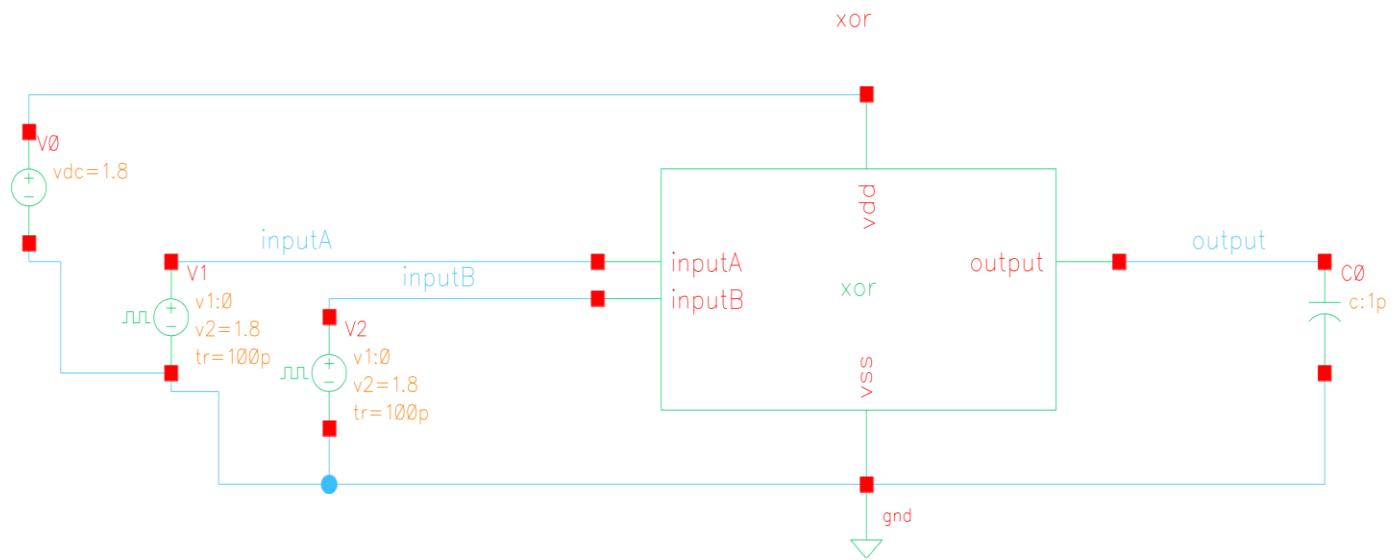


Fig 4.4: XOR gate testbench.

## TEST BENCH:

project-1:xor-2-tb:1 : project-1 xor-2-tb schematic 17:02:00 Mon Oct 10 2016

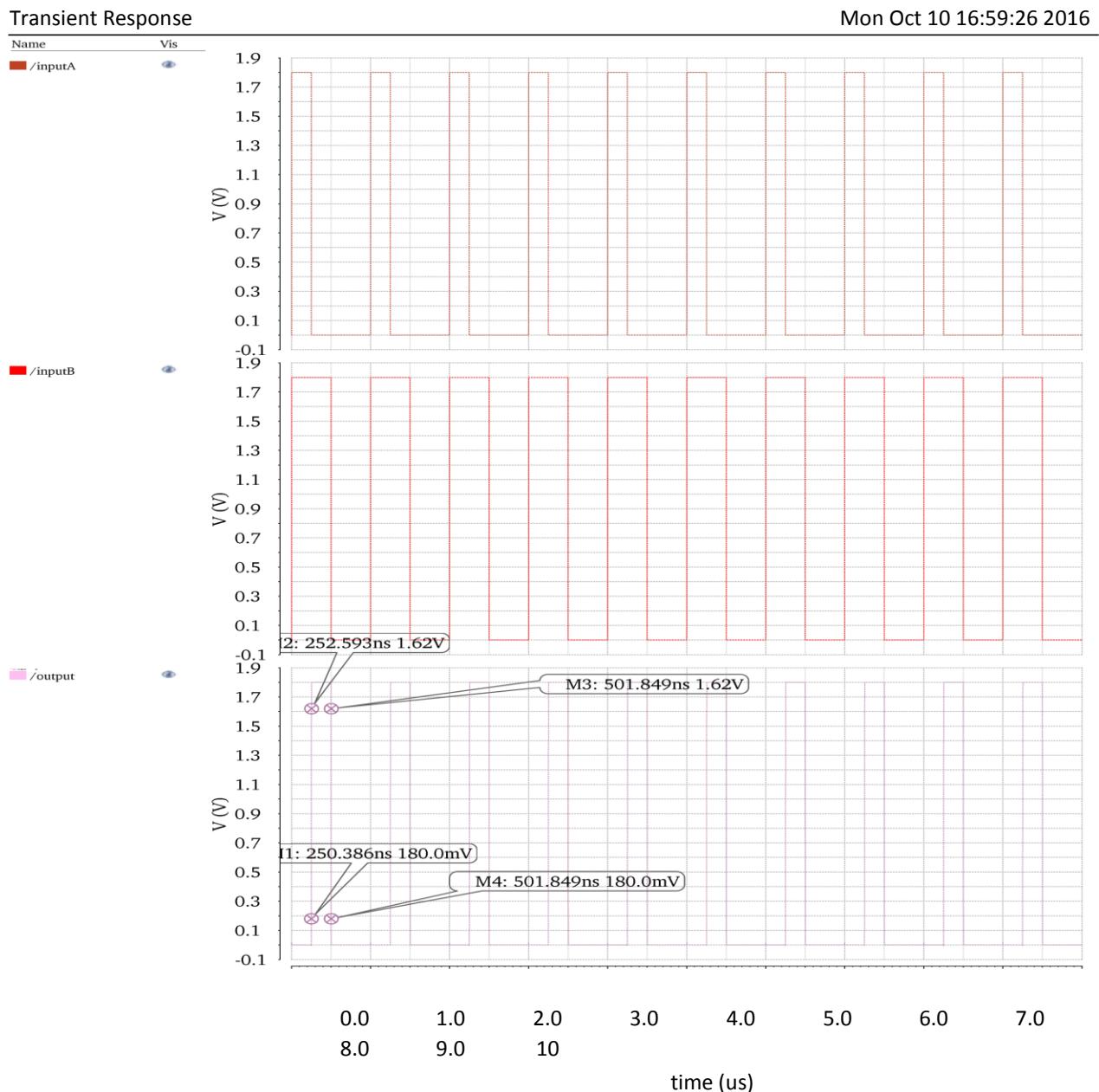


Fig 4.5: 2 input XOR wave form.

## LAYOUT:

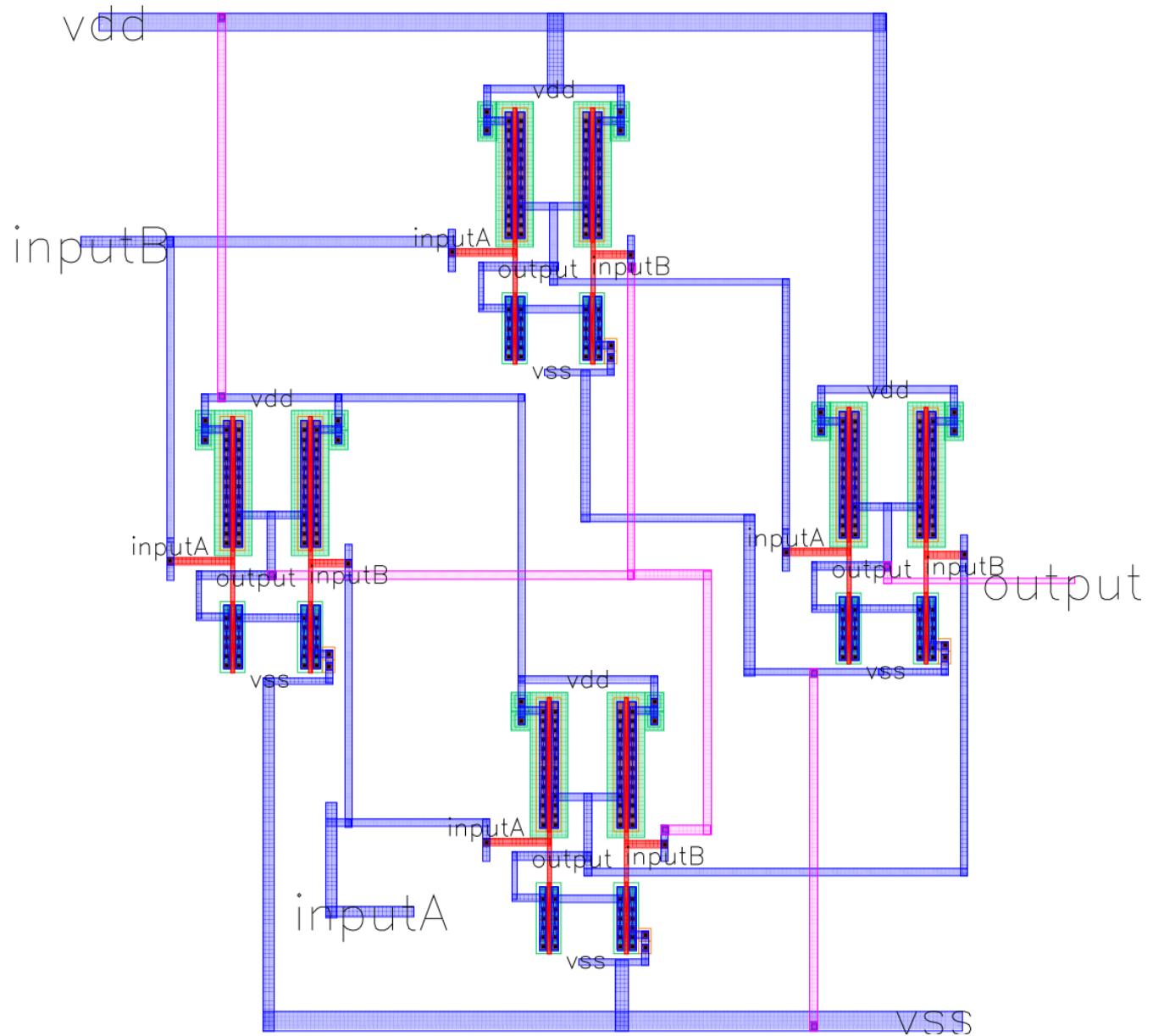
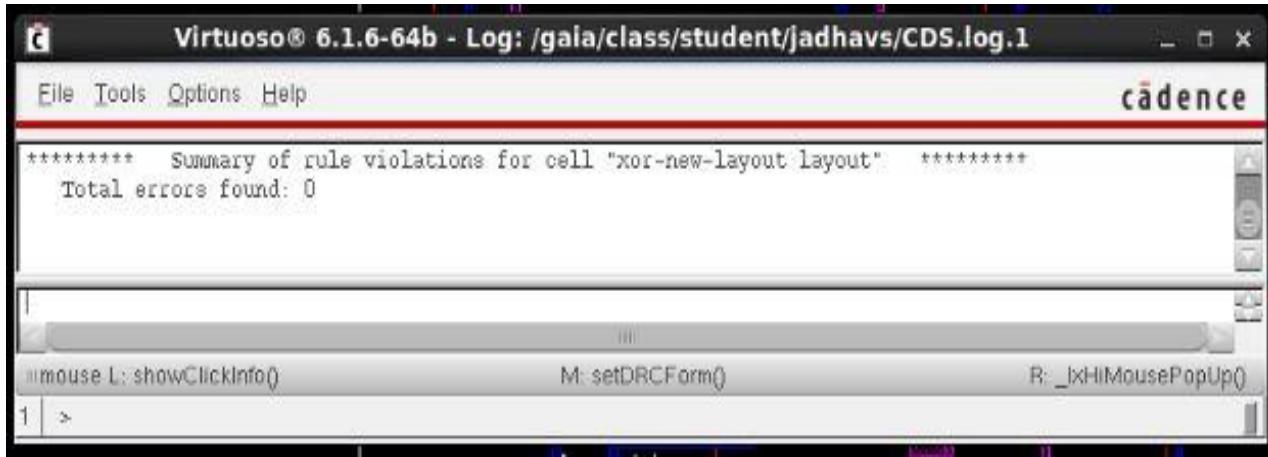


Fig 4.5: 2 input XOR layout.

DRC REPORT:



The screenshot shows a window titled "Virtuoso® 6.1.6-64b - Log: /gaia/class/student/jadhavs/CDS.log.1". The window has a menu bar with "File", "Tools", "Options", and "Help". The main area displays a summary of rule violations for a cell named "xor-new-layout layout". It states "Total errors found: 0". Below this, there is a scrollable list of log entries. The first entry is "Jxmouse L: showClickInfo()". The window is part of the Cadence software suite.

```
***** Summary of rule violations for cell "xor-new-layout layout" *****
Total errors found: 0

Jxmouse L: showClickInfo()
M: setDRCForm()
R: _JxHiMousePopUp()
```

Fig 4.7: DRC report.

## LVS REPORT.

```
@(#) $CDS: LVS version 6.1.6-64b 09/01/2015 22:33 (sjfnl138) $  
  
Command line: /software/IC616/tools.lnx86/dfII/bin/64bit/LVS -dir  
/gaia/class/student/jadhavs/LVS -l -s -t  
/gaia/class/student/jadhavs/LVS/layout  
/gaia/class/student/jadhavs/LVS/schematic  
Like matching is enabled.  
Net swapping is enabled.  
Using terminal names as correspondence points.  
Compiling Diva LVS rules...  
  
Net-list summary for /gaia/class/student/jadhavs/LVS/layout/netlist  
count  
12      nets  
0       terminals  
8       pmos  
8       nmos  
  
Net-list summary for /gaia/class/student/jadhavs/LVS/schematic/netlist  
count  
12      nets  
5       terminals  
8       pmos  
8       nmos  
  
Devices in the rules but not in the netlist:  
cap nfet pfet nmos4 pmos4  
  
1 net-list ambiguity was resolved by random selection.  
  
The net-lists match.  
  
          layout schematic  
                  instances  
un-matched        0      0  
rewired           0      0  
size errors       0      0  
pruned            0      0  
active            16     16  
total             16     16  
  
          nets  
un-matched        0      0  
merged            0      0  
pruned            0      0  
active            12     12  
total             12     12  
  
          terminals  
un-matched        0      0  
matched but  
different type     0      0
```

total	0	5
-------	---	---

Probe files from /gaia/class/student/jadhavs/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/jadhavs/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

## 5. SINGLE BIT FULL ADDER:

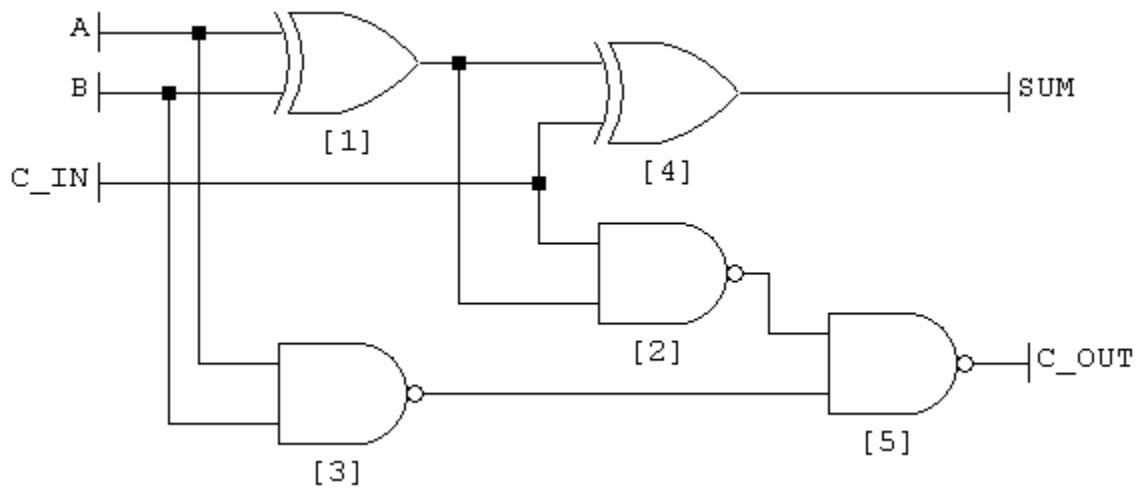


Fig 5.1: full adder using NAND and XOR gates:

A single bit full adder can be realized using 2 two input XOR gates and 3 two input NAND gates. The schematics of the NAND and XOR gates used are shown in fig 2.1 and fig 4.3

## SCHEMATIC OF FULL ADDER.

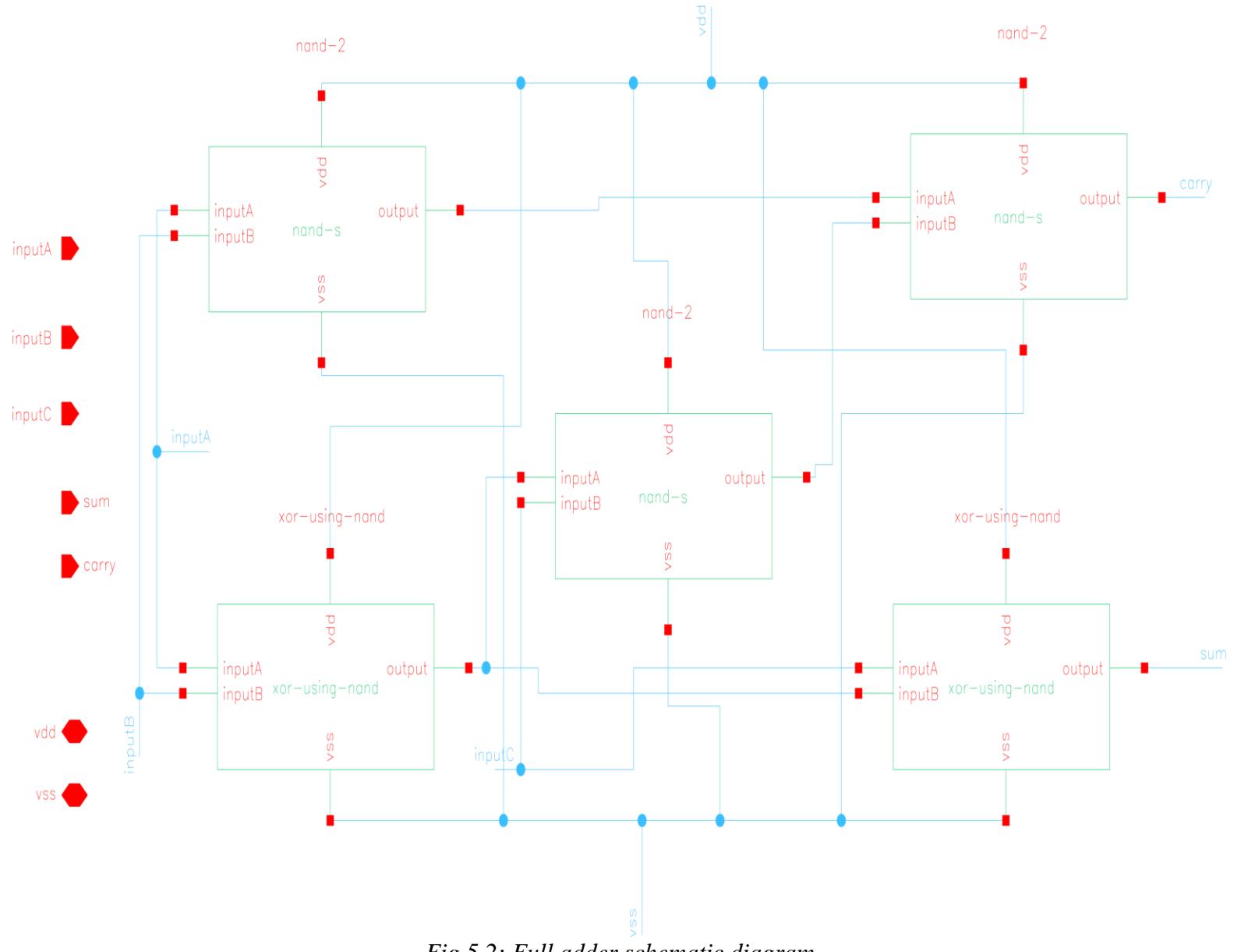
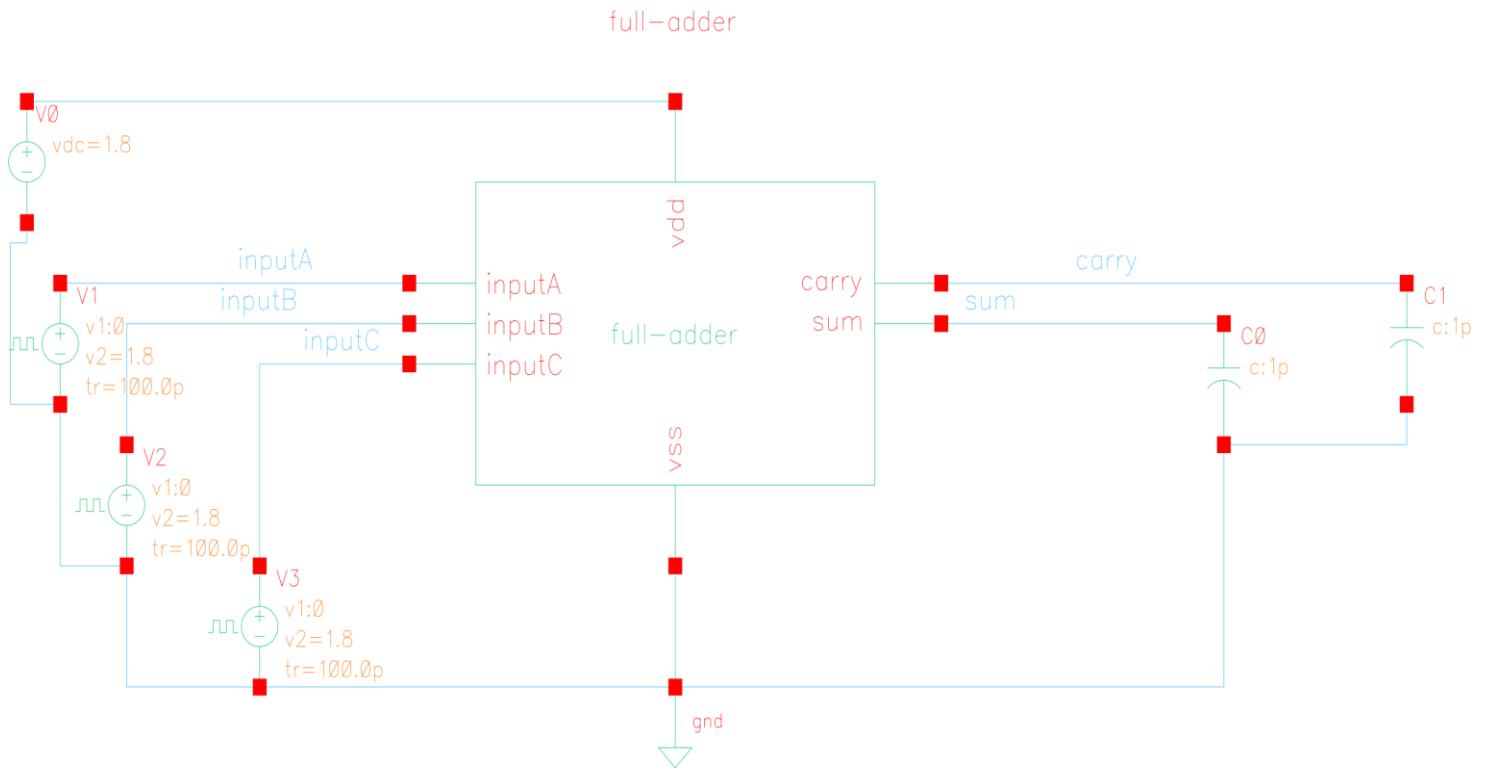


Fig 5.2: Full adder schematic diagram.

## FULL ADDER TEST BENCH.



*Fig 5.3 Full adder testbench*

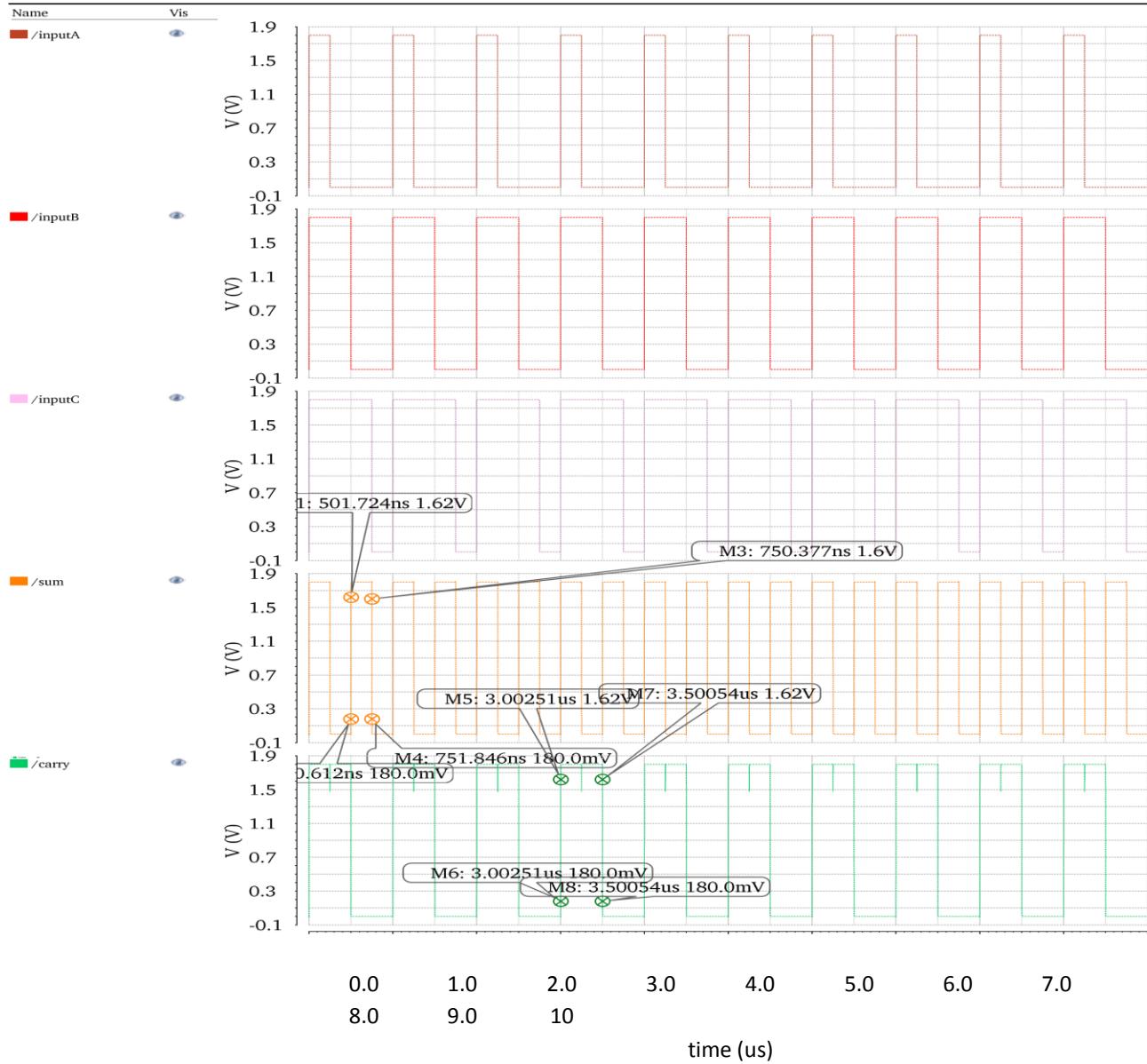
## WAVEFORM:

2016

project-1:fulladder-tb:1 : project-1 fulladder-tb schematic 16:44:04 Mon Oct 10

Transient Response

Mon Oct 10 16:37:23 2016



Printed on  
by jadhavas

Page 1 of 1

fig 5.4 :Full adder waveform

## LAYOUT:

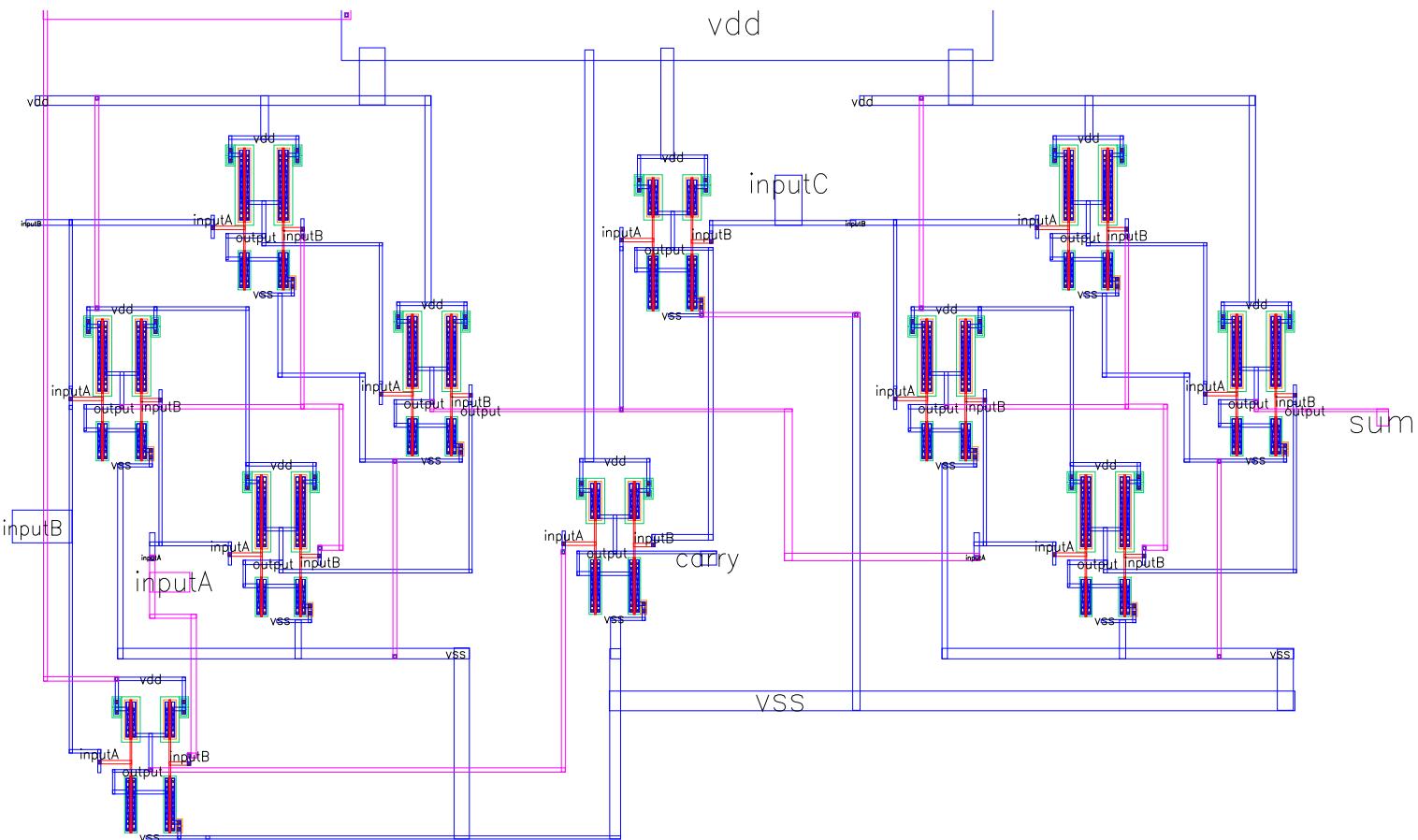


fig 5.5 :Full adder layout

DRC REPORT:

The screenshot shows a window titled "Virtuoso® 6.1.6-64b - Log: /gaia/class/student/jadhavs/CDS.log.1". The window has a menu bar with "File", "Tools", "Options", and "Help". The main area displays a log message: "\*\*\*\*\* Summary of rule violations for cell \"fulladder-layout layout\" \*\*\*\*\*" followed by "Total errors found: 0". Below this, there is a status bar with three items: "mouse L: showClickInfo()", "M: setDRCForm()", and "R: \_JxHiMousePopUp()". A small number "1" is visible in the bottom left corner of the status bar.

Fig 5.6: DRC report

## LVS REPORT:

```
@(#)$CDS: LVS version 6.1.6-64b 09/01/2015 22:33 (sjfnl138) $  
  
Command line: /software/IC616/tools.lnx86/dfII/bin/64bit/LVS -dir  
/gaia/class/student/jadhavs/Desktop/harsha/LVS -l -s -t  
/gaia/class/student/jadhavs/Desktop/harsha/LVS/layout  
/gaia/class/student/jadhavs/Desktop/harsha/LVS/schematic  
Like matching is enabled.  
Net swapping is enabled.  
Using terminal names as correspondence points.  
Compiling Diva LVS rules...  
  
Net-list summary for  
/gaia/class/student/jadhavs/Desktop/harsha/LVS/layout/netlist  
count  
27 nets  
0 terminals  
22 pmos  
22 nmos  
  
Net-list summary for  
/gaia/class/student/jadhavs/Desktop/harsha/LVS/schematic/netlist  
count  
27 nets  
7 terminals  
22 pmos  
22 nmos  
  
Devices in the rules but not in the netlist:  
cap nfet pfet nmos4 pmos4  
  
1 net-list ambiguity was resolved by random selection.  
  
The net-lists match.  
  
layout schematic  
instances  
un-matched 0 0  
rewired 0 0  
size errors 0 0  
pruned 0 0  
active 44 44  
total 44 44  
  
nets  
un-matched 0 0  
merged 0 0  
pruned 0 0  
active 27 27  
total 27 27  
  
terminals  
un-matched 0 0
```

matched but		
different type	0	0
total	0	7

Probe files from /gaia/class/student/jadhavs/Desktop/harsha/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/jadhavs/Desktop/harsha/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

## 6. D TYPE FLIP FLOP:

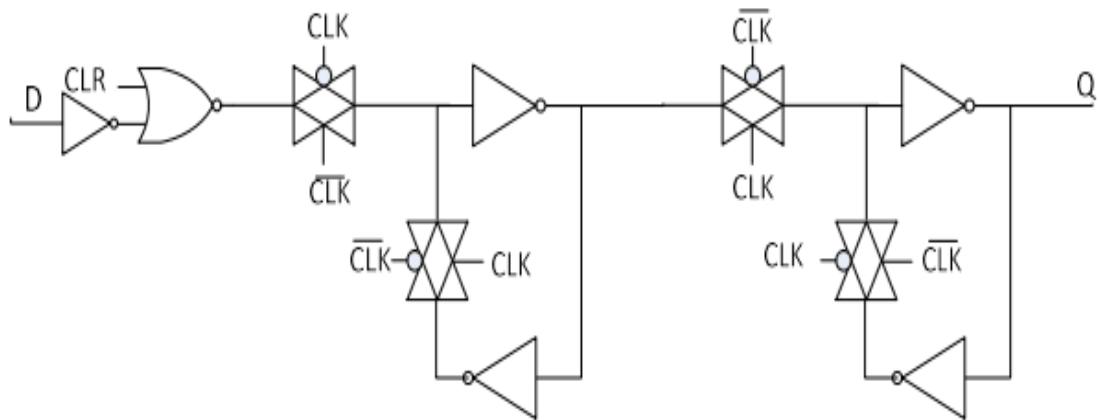


Fig 6.1: D type Flip Flop.

A D type flip flop can be realized using other gates like the inverter (NOT) gate , NOR gate and transmission gates.

## SCHEMATIC DIAGRAM.

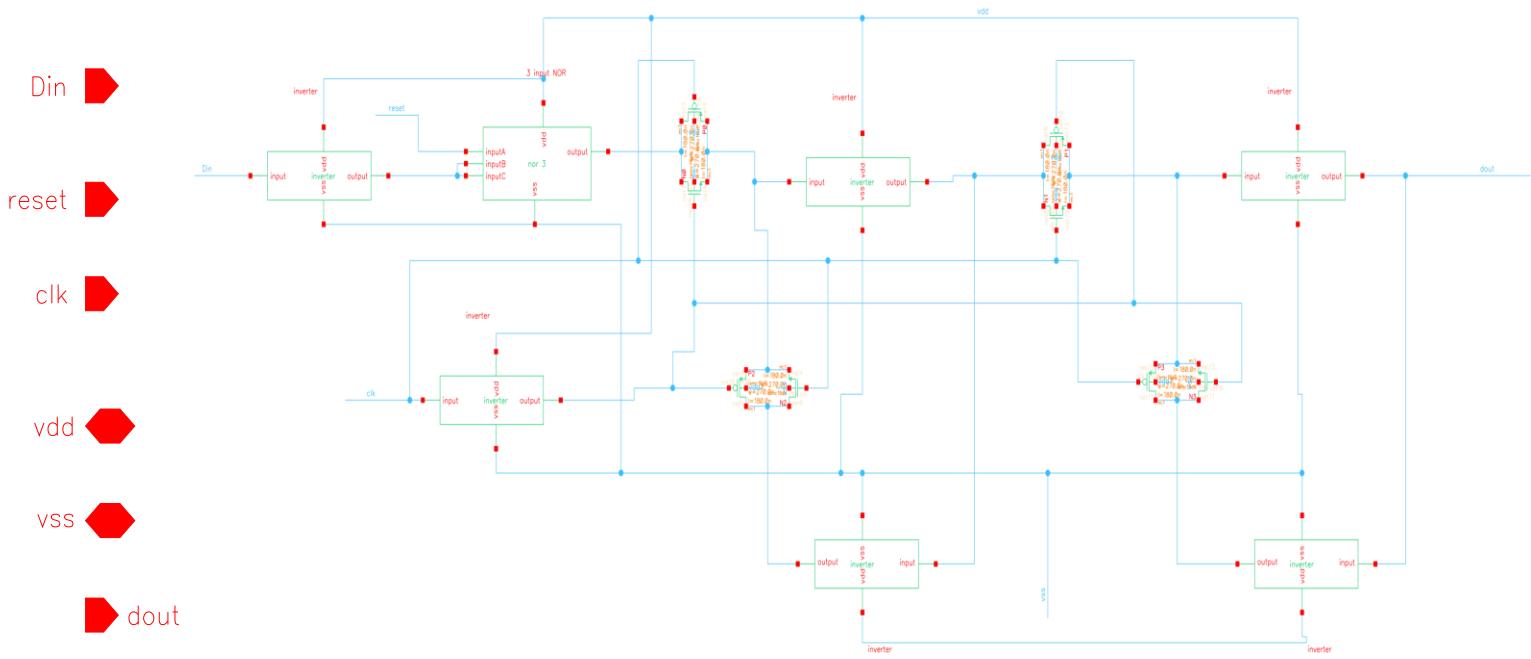


Fig 6.2 D flip flop schematic diagram

## D FLIP FLOP TEST BENCH

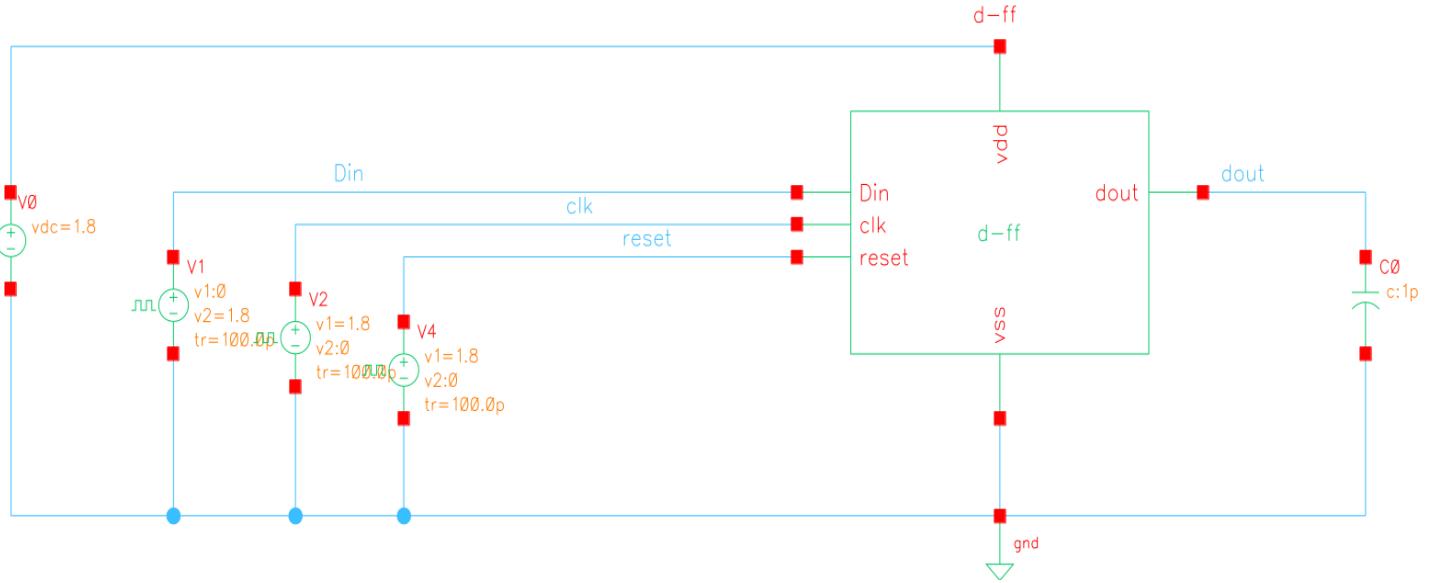


Fig 6.3: D flip flop test bench

## Transient Response

Mon Oct 10 16:30:11 2016

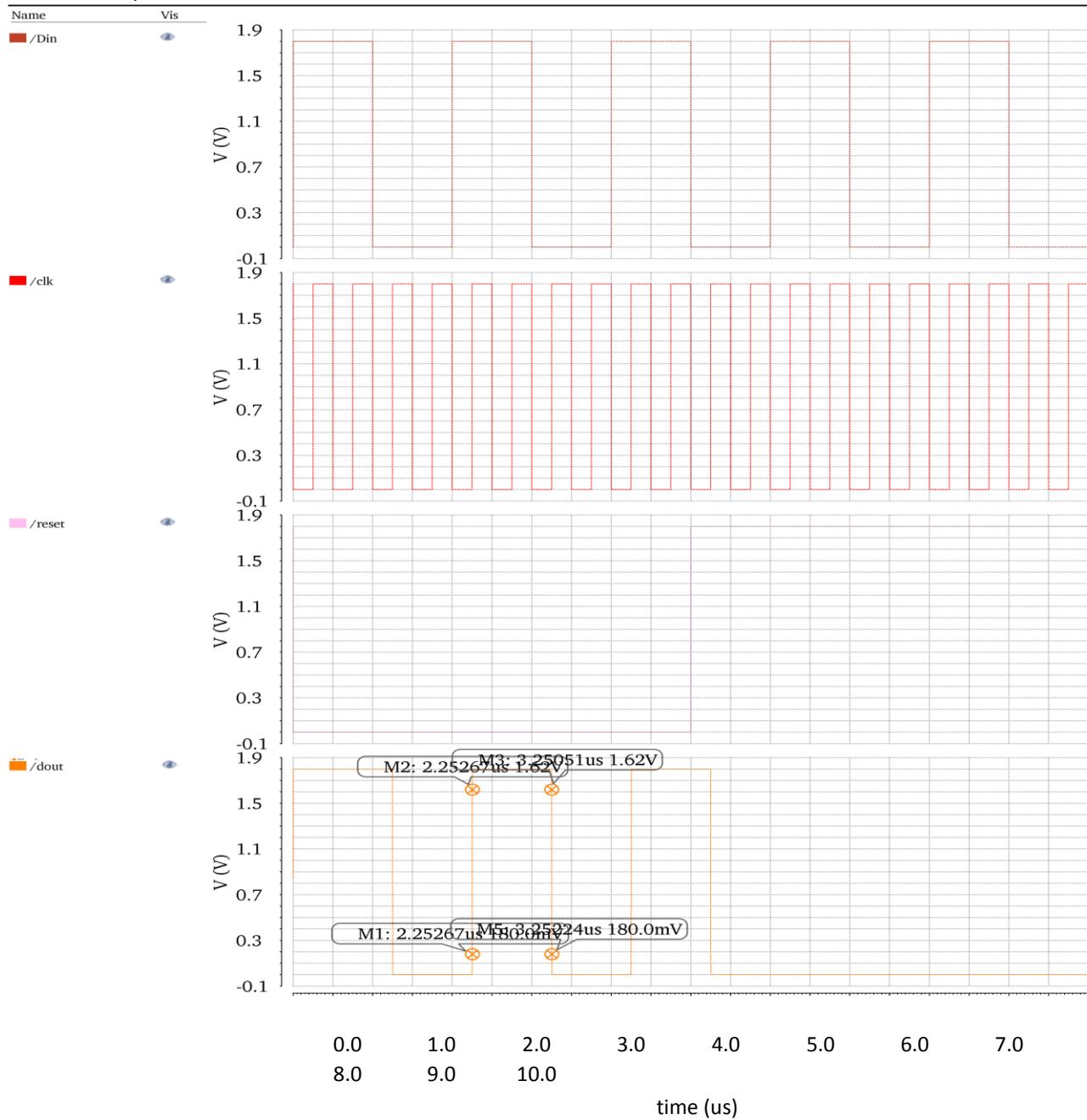


Fig 6.3: D flip flop waveform

## LAYOUT

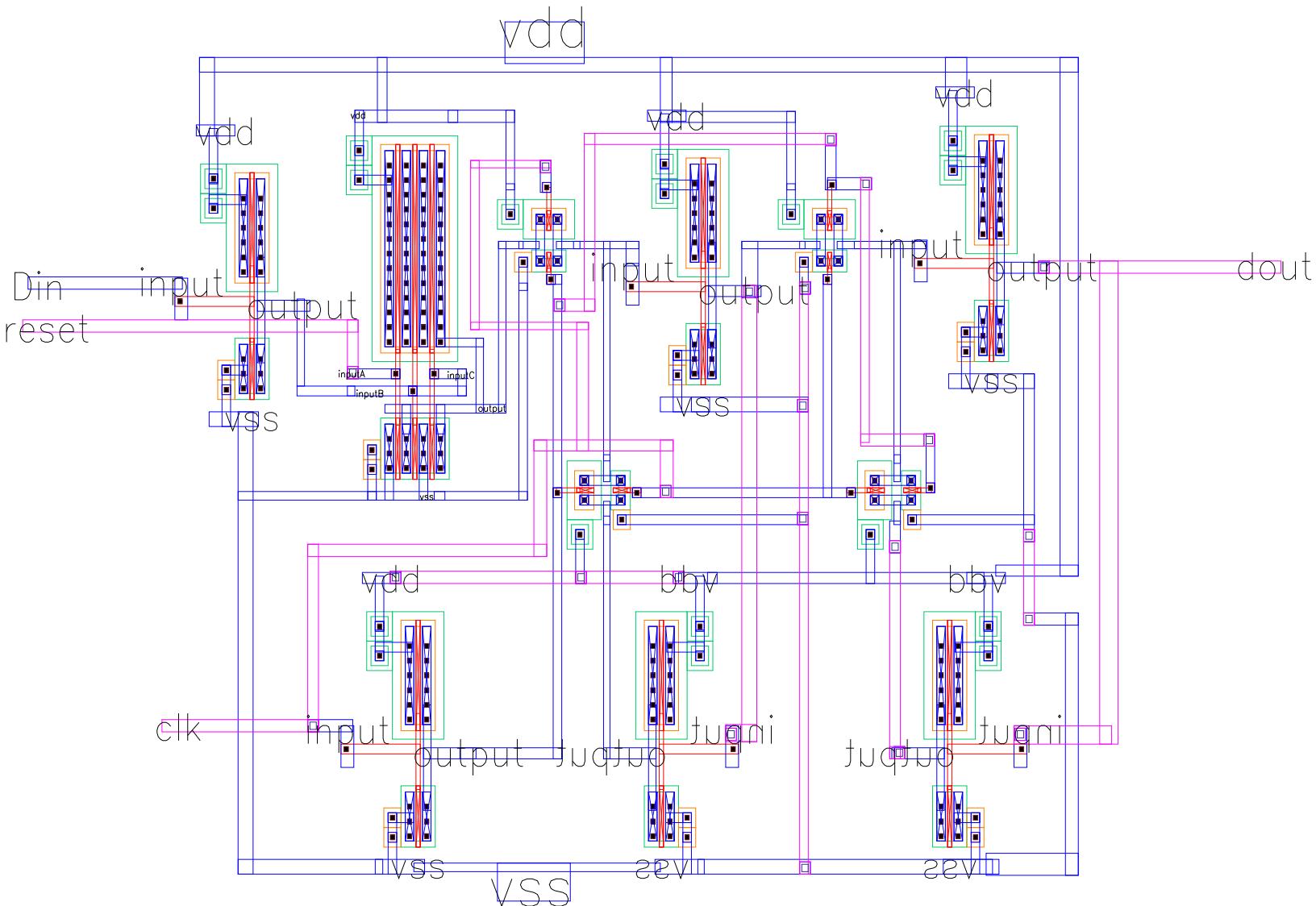


Fig 6.4 D flip flop layout

## DRC REPORT:

The screenshot shows a Virtuoso® 6.1.6-64b software window titled "Virtuoso® 6.1.6-64b - Log: /gaia/class/student/jadhavs/CDS.log.1". The menu bar includes File, Tools, Options, and Help. The main area displays a log message: "\*\*\*\*\* Summary of rule violations for cell \"d-ff-lay layout\" \*\*\*\*\*" followed by "Total errors found: 0". Below this, there is a status bar with the text "l:mouse L:showClickInfo()", "M: setDRCForm()", and "R: \_lxHiMousePopUp()".

Fig 6.5 DRC report

## LVS REPORT:

```
@(#) $CDS: LVS version 6.1.6-64b 09/01/2015 22:33 (sjfnl138) $  
Command line: /software/IC616/tools.lnx86/dfII/bin/64bit/LVS -dir  
/gaia/class/student/jadhavs/Desktop/harsha/LVS -l -s -t  
/gaia/class/student/jadhavs/Desktop/harsha/LVS/layout  
/gaia/class/student/jadhavs/Desktop/harsha/LVS/schematic  
Like matching is enabled.  
Net swapping is enabled.  
Using terminal names as correspondence points.  
Compiling Diva LVS rules...
```

```
Net-list summary for  
/gaia/class/student/jadhavs/Desktop/harsha/LVS/layout/netlist
```

count	
16	nets
0	terminals
13	pmos
13	nmos

```
Net-list summary for  
/gaia/class/student/jadhavs/Desktop/harsha/LVS/schematic/netlist
```

count	
16	nets
6	terminals
13	pmos
13	nmos

```
Devices in the rules but not in the netlist:  
cap nfet pfet nmos4 pmos4
```

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	26	26
total	26	26

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	16	16
total	16	16

	terminals	
un-matched	0	0
matched but		

different type	0	0
total	0	6

Probe files from /gaia/class/student/jadhavs/Desktop/harsha/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/jadhavs/Desktop/harsha/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

## OBSERVATIONS:

SL NO	DESCRIPTION	RISE TIME in ns	FALL TIME in ns	DELAY in ns
1	Inverter	0.1	0	0
2	NAND gate	1.09	0	0
3	NOR gate	3.19	0	0
4	XOR gate	2.2	0	0
5	1 bit full adder (sum)	1.11	1.47	0
	carry	0	0	0
6	D flip flop	0	17.3	0