ECE 546 - VLSI Systems Design

Project Introduction

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with significant material from Rabaey, Chandrakasan, and Nikolić

Announcements

- Deadlines
  - Due Today
    - Homework 7
    - Homework 6 Grading
  - Due in 9 days
    - Homework 8
    - Project Milestone 1
- Still 5 students without a project group
- Syllabus updated
  - Project performance grade reduced from 5% to 2% in final average (Physical Verification increased from 5% to 8%) to reduce incentive for re-design and total hours spent on project (in response to COVID19)

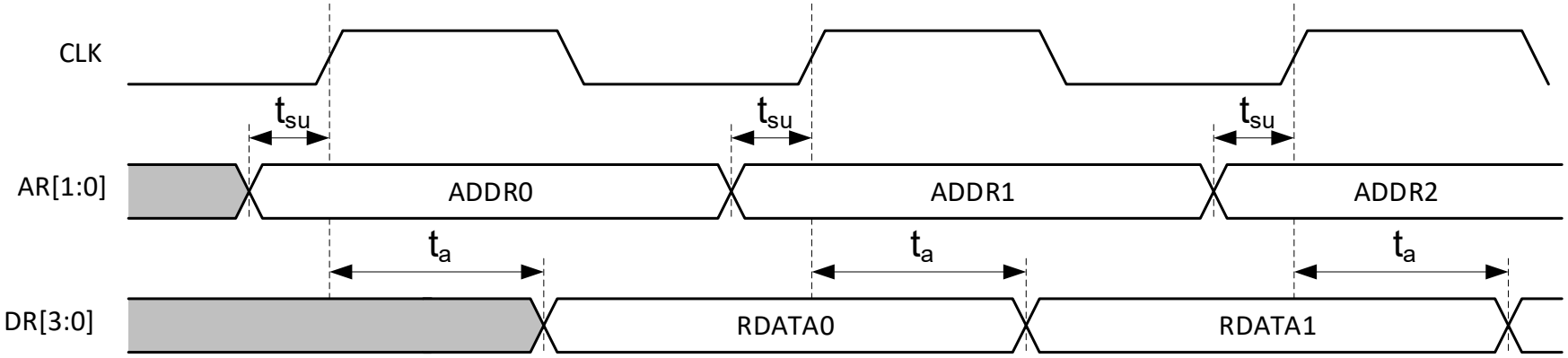
Today's Lecture

- Project Introduction
  - Specification
  - Requirements
  - Milestones
  - Grading
  - Project Groups

System Specification

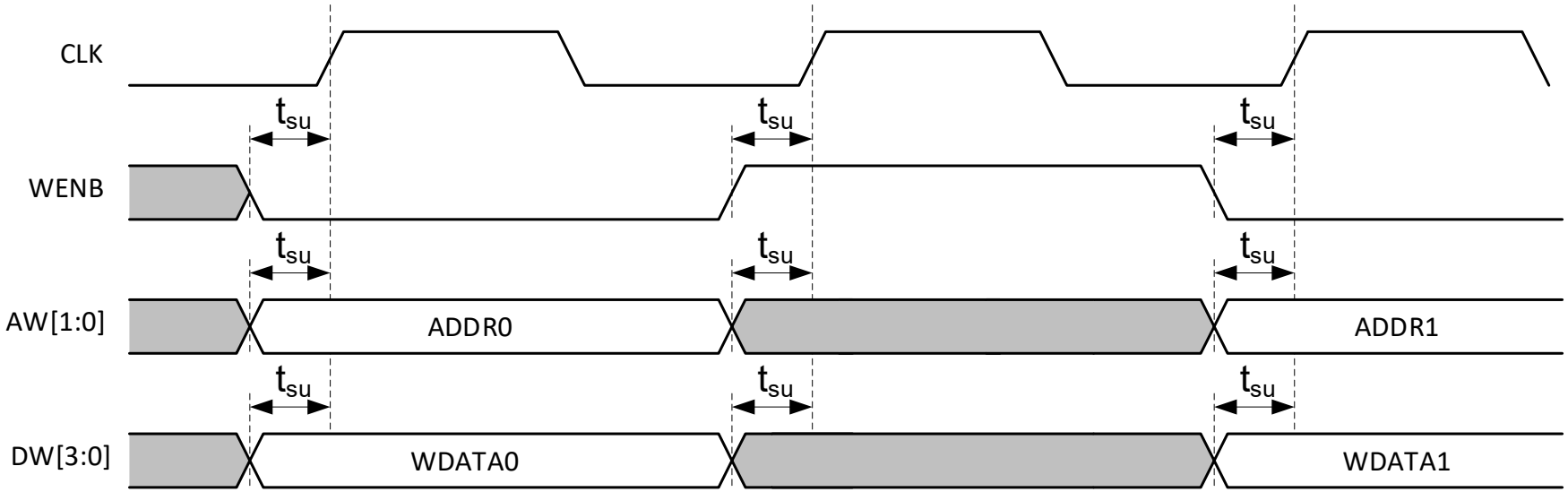
- **16 bit (4x4) 2-Port SRAM**
  - **1 write-port**
  - **1 read-port**
- **Inputs**
  - **AW[1:0], AR[1:0]** – address
  - **DW[3:0]** – write data
  - **WENB** – write-enable bar (low indicates write)
  - **CLK** – clock
- **Outputs**
  - **DR[3:0]** – read data

Read-Port Timing



- Output must be stored until next value arrives
- t_{su} – Setup time for your input vectors
- t_a – Read access time

Write-Port Timing



- Address and Write-Enable do not need to be stored (to reduce complexity)

Requirements (1 of 3)

- Functional Correctness
  - Your design will be judged functionally correct if it simulates the vectors provided with no errors. (extracted layout – C only)

- Optimization Metric
  - Optimize the design for minimum energy-delay-area product (EDA)
  - Highest marks will be given to the project group that minimizes this metric.
  - Delay must be measured as the minimum clock period for which the system is fully functional, according to the simulation vectors provided.
  - Energy must be measured as the total energy for the entirety of the functionality simulation above, using the same clock-period.
  - Area must be measured as the area of the bounding box around the entire layout.

Requirements (2 of 3)

- Inputs & Outputs
  - All inputs will be connected to buffers (two inverters) with NFIN=4 to model the output of the flip-flops at the previous stage of the pipeline. These buffers will be included in the *test_bench.sp* file provided.
  - Input vectors must be synchronized to the rising edge of the clock.
  - Output vectors may be delayed by any amount that allows successful simulation.
  - The output must be held steady until the next value arrives, with a maxiumum rise above GND (dip below VDD) of 100 mV.
  - Outputs must be loaded with 5 fF capacitors. These loads will be included in the the *test_bench.sp* file provided.
  - Input and Output pins must be on the boundary of the design.
  - The clock input will be buffered just as the other inputs. You must buffer the clock yourself, if necessary.

Requirements (3 of 3)

- Supply Voltage
  - Active Supply voltage must be 0.8 V
  - Input and output signals must be 0.8V signals

- Other Requirements
  - If initial conditions (.ic) are used in simulation, then they must be used for every bit, and every bit must be set to zero
  - Design must pass DRC & LVS Checks

Milestones (1 of 2)

1. Due Thu. Apr. 1 (9 days) –
   One person from each group should turn in a proposal with the following information:
   - Design options to be explored
     - Logic styles and circuit topologies for bit-cells, decoders, and flip-flops
     - Include a brief description, references, or schematics for each option
   - Rough floorplan
   - Division of labor in your group

2. Due Tues. Apr. 13 (12 days after Milestone 1) –
   One person from each group should turn in plots of complete schematics and simulated waveforms showing correct operation. Your final design does not need to match this design.

Milestones (2 of 2)

3. Apr. 20 and 22 - Each group should sign-up for a time-slot for the TA to observe a simulation of the extracted layout (with parasitics) that shows correct operation with your final energy, delay, and area.

4. Tue. Apr. 27 (2 weeks after Milestone 2) - Design Demonstrations. Each group must show a simulation that demonstrates correct operation with the energy, delay, and area claimed in the final report. Each group must also show LVS and DRC checks with no errors. Each group must also be prepared to share schematics and layout that demonstrate adherence to the project spec.

5. Fri. Apr. 30 - Final reports due.

Grading (1 of 3)

- 40% Total
- Correctness of Milestones 1 & 2 (2% and 3%)
- Correct Operation of Final Design (10%)
  - Design must generate correct output
- Correct Physical Verification of Final Design (8%)
  - Design must pass DRC and LVS checks.

Grading (2 of 3)

- Final Report (10%)
  - Documentation of logic design, physical layout, and verification in an ISSCC-style paper. Most of this portion of the grade will depend on technical depth, readability, and completeness of design documentation.
  - Be sure to gather data for your report in the early stages of your design to maximize your marks for technical depth

- Performance (2%)
  - Highest marks will be given to the group with the lowest E*D*A metric. Lower marks will be given to groups with larger metrics.

Grading (3 of 3)

- Partner Assessment (5%)
  - Group members will complete an online survey rating whether or not you
    - did what you promised to do
    - made it a priority to attend group meetings
    - did your fair share of the work
    - made a valuable contribution to the project

Project Groups

- You must work in groups of 3.
  Find two project partners from the class.

- Verify your group assignment on the Project Groups List (linked from the Project section of the course web-site)

- To share an AFS directory with your partners
  - Use the command “fs sa [path] [userid] rlidwk” to give read & write access to a directory
  - Ensure that you use the command “fs sa [path] [userid] l” for every parent directory that contains the shared directory