HARSHA RASTOGI

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OBJECTIVE

Seeking software engineering summer internship ’15 to get hands on experience with cutting edge technologies in the field of distributed systems, systems programming and applied machine learning

EDUCATION

Carnegie Mellon University, Pittsburgh, PA, USA Aug’14 - Dec’15
Master of Science in Electrical and Computer Engineering, GPA 3.78/4.0

Birla Institute of Technology and Science (BITS), Pilani, India Aug’09 - Aug’13
Bachelor of Engineering in Electrical and Electronics, GPA 9.55/10

TECHNICAL SKILLS

- **Relevant Courses:** Introduction to Computer Systems, Machine Learning, Distributed Systems*, Storage Systems*, Rapid Prototyping of Computer Systems*, Multimedia Databases and Data Mining*, Digital Electronics and Computer Organization, VLSI/Computer Architecture
- **Programming Languages:** C, Java, x86, ARM, Verilog HDL, Perl
- **Tools:** MATLAB, GitHub, GNU Debugger, Eclipse, QEMU
- **Operating Systems:** Linux, Mac OS, Microsoft Windows

PROFESSIONAL EXPERIENCE

Broadcom, Bangalore, India, IC Design Engineer, Mobile Platforms Group Aug’13 - Jul’14
- Enhanced mobile baseband SoC performance by identifying logical and functional flaws in the design and power management code

Intel Labs, Bangalore, India, Bachelor’s Thesis Project Feb ’13 - Jun’13
- Improved personal safety by designing a low power wearable tracking device as part of Intel’s Internet of Things (IoT) vision
- The device performs real time object tracking and sends user’s location coordinates to the predefined recipients in case of an emergency

Carnegie Mellon University, Pittsburgh, Summer Research Intern, Professor Onur Mutlu May’12 - Jul’12
- Increased system throughput by 1% and fairness by 5.9% in multi core systems via implementation of efficient memory scheduling algorithms at the memory controller.
- Performed exploratory work on Blacklisting Memory Scheduler presented at ICCD, 2014

PROJECTS

System Programming

- **Memory Allocator**
  Designed a general purpose dynamic memory allocator for C programs. Optimized its performance by implementing a segregated list with immediate coalescing, four byte pointers, footer elimination and combination of best and first fit placement policy

- **Cache Simulator**
  Coded a cache simulator that models hit/miss behavior of cache memory and outputs total number of hits, misses and evictions

- **Multi-threaded Proxy**
  Designed an HTTP proxy server program that supports caching of web objects and concurrent requests. Implemented multi-threading with appropriate locking mechanisms for accessing cache lines

- **Linux Shell**
  Designed an interactive command line interpreter in C supporting job control, signal handling and I/O redirection

Kernel Programming
- Designed a single-task mini-kernel that supports read, write and exit system calls and runs user space applications

Machine Learning
- Worked on designing novel image classifiers to perform a ten-class classification task on small color images in CIFAR-10 data set
- Configured a majority-voting algorithm (Accuracy 62%) that uses the results of best supervised classifiers to generate combined predictions

PUBLICATIONS

- Lavanya Subramanian, Donghyuk Lee, Vivek Seshadri, Harsha Rastogi and Onur Mutlu, “The Blacklisting Memory Scheduler: Achieving High Performance and Fairness at Low Cost” ,32nd IEEE International Conference on Computer Design (ICCD), Seoul, Korea, Oct. 2014

- Ashish Mishra, Nidhi Jayapalan, Harsha Rastogi and Tushar Agrawal , “Impact of Segmentation Distribution on Area and Delay in FPGA Routing Architectures”, 3rd IEEE International Advance Computing Conference, Ghaziabad, India, Feb. 2013

*Future Courses