Design, implementation of N bit UP/DOWN Counter

Verilog code

```
module nbud #(parameter N=8)(input clk,rst,swi,output[N-1:0]q);
reg[N-1:0]q;
always @(posedge clk or negedge rst)
begin
if(~rst)
q<=0;
else
 if(swi==1)
 q<=q+1;
 else
 q<=q-1;
end
endmodule
```

Open

```
module nbud_tb();
parameter N=8;
reg clk,rst,swi;
wire [N-1:0]q;
nbud n1(clk,rst,swi,q);
initial
begin
clk = 0;
rst=0;
swi=0;
end
always #5 clk = ~clk;
always #100 rst=~rst;
always #300 swi=~swi;
endmodule
```

Constraint

```
set sdc version 1.4
current_design nbud

create_clock -name clk -period 500 -waveform {0 1} [get_ports "clk"]
set_clock_transition -rise 0.4 [get_clocks "clk"]
set_clock_transition -fall 0.4 [get_clocks "clk"]
set_input_delay -min 0.2 [get_ports "rst"]
set_input_delay -max 0.4 [get_ports "swi"]
set_load 0.2 [all_outputs]
# set_input_transition 1 [all_inputs]
set_input_transition 1 [get_ports "rst"]
set_input_transition 1.5 [get_ports "swi"]
```

Optimized Constraint

```
set_units -capacitance 1000fF
set_units -time 1000ps

# Set the current design
current_design nbud

create_clock -name "clk" -period 500.0 -waveform {0.0 1.0} [get_ports clk]
set_clock_transition 0.4 [get_clocks clk]
set_load -pin_load 0.2 [get_ports {q[7]}]
set_load -pin_load 0.2 [get_ports {q[6]}]
set_load -pin_load 0.2 [get_ports {q[5]}]
set_load -pin_load 0.2 [get_ports {q[4]}]
set_load -pin_load 0.2 [get_ports {q[3]}]
set_load -pin_load 0.2 [get_ports {q[2]}]
set_load -pin_load 0.2 [get_ports {q[1]}]
set_load -pin_load 0.2 [get_ports {q[0]}]
set_clock_gating_check -setup 0.0
set_input_delay -add_delay -min 0.2 [get_ports rst]
set_input_delay -add_delay -max 0.4 [get_ports swi]
set_input_transition 1.0 [get_ports rst]
set_input_transition 1.5 [get_ports swi]
set_wire_load_mode "enclosed"
```

Report on area

Open

nbud_area.rep

~/harsha/synthesis/logisyn/output/nbitud1

```
=============================================================
  Generated by:           Genus(TM) Synthesis Solution 21.17-s066_1
  Generated on:           Aug 04 2024  10:16:19 am
  Module:                 nbud
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
=============================================================

Instance Module  Cell Count  Cell Area  Net Area   Total Area   Wireload
-----------------------------------------------------------------------------
nbud                     37    113.544     0.000      113.544 <none> (D)
  (D) = wireload is default in technology library
```

Report on power

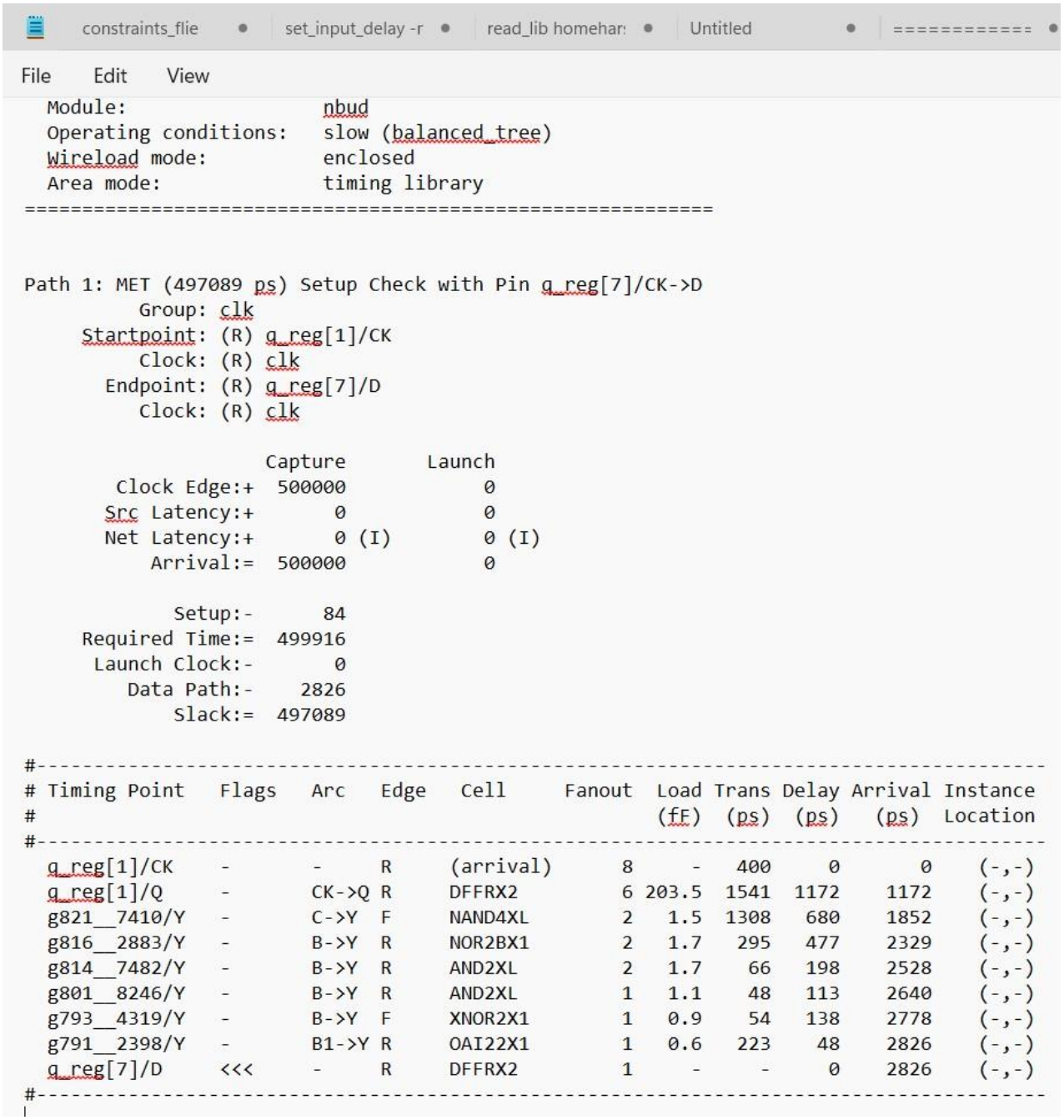
Open

nbud_power.rep

~/harsha/synthesis/logisyn/output/nbitud1

```
Instance: /nbud
Power Unit: W
PDB Frames: /stim#0/frame#0
  ------------------------------------------------------------------------
    Category         Leakage     Internal    Switching        Total     Row%
  ------------------------------------------------------------------------
       memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
     register     2.84842e-09  1.72832e-07  3.56543e-07  5.32224e-07  91.70%
        latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
        logic     2.28058e-09  3.19358e-08  6.19873e-09  4.04151e-08   6.96%
         bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
        clock     0.00000e+00  0.00000e+00  7.77600e-09  7.77600e-09   1.34%
          pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
           pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  ------------------------------------------------------------------------
     Subtotal     5.12900e-09  2.04768e-07  3.70518e-07  5.80415e-07 100.00%
   Percentage           0.88%       35.28%       63.84%      100.00% 100.00%
  ------------------------------------------------------------------------
```

Report on timing



constraints_flie • set_input_delay -r • read_lib homehar: • Untitled • ========== •

File Edit View

```
  Module:                 nbud
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
==========================================================


Path 1: MET (497089 ps) Setup Check with Pin q_reg[7]/CK->D
          Group: clk
     Startpoint: (R) q_reg[1]/CK
          Clock: (R) clk
       Endpoint: (R) q_reg[7]/D
          Clock: (R) clk

                     Capture       Launch
        Clock Edge:+  500000            0
       Src Latency:+       0            0
       Net Latency:+       0 (I)        0 (I)
           Arrival:=  500000            0

             Setup:-      84
     Required Time:=  499916
      Launch Clock:-       0
         Data Path:-    2826
             Slack:=  497089

#-------------------------------------------------------------------------------------------------
# Timing Point   Flags   Arc   Edge   Cell     Fanout  Load Trans Delay Arrival Instance
#                                                      (fF)  (ps)  (ps)   (ps)  Location
#-------------------------------------------------------------------------------------------------
  q_reg[1]/CK    -       -     R     (arrival)      8     -   400     0       0    (-,-)
  q_reg[1]/Q     -       CK->Q R     DFFRX2         6 203.5  1541  1172    1172    (-,-)
  g821__7410/Y   -       C->Y  F     NAND4XL        2   1.5  1308   680    1852    (-,-)
  g816__2883/Y   -       B->Y  R     NOR2BX1        2   1.7   295   477    2329    (-,-)
  g814__7482/Y   -       B->Y  R     AND2XL         2   1.7    66   198    2528    (-,-)
  g801__8246/Y   -       B->Y  R     AND2XL         1   1.1    48   113    2640    (-,-)
  g793__4319/Y   -       B->Y  F     XNOR2X1        1   0.9    54   138    2778    (-,-)
  g791__2398/Y   -       B1->Y R     OAI22X1        1   0.6   223    48    2826    (-,-)
  q_reg[7]/D     <<<     -     R     DFFRX2         1     -     -     0    2826    (-,-)
#-------------------------------------------------------------------------------------------------
```

Report on QoR

Updated Netlist

constraints_flie • set_input_delay -r • read_lib homehar: • Untitled •

File Edit View

```
module nbud(clk, rst, swi, q);
  input clk, rst, swi;
  output [7:0] q;
  wire clk, rst, swi;
  wire [7:0] q;
  wire UNCONNECTED, UNCONNECTED0, UNCONNECTED1, UNCONNECTED2,
       UNCONNECTED3, UNCONNECTED4, UNCONNECTED5, n_1;
  wire n_2, n_4, n_5, n_6, n_7, n_8, n_9, n_10;
  wire n_11, n_12, n_14, n_15, n_16, n_17, n_18, n_19;
  wire n_20, n_21, n_22, n_24, n_25, n_26, n_27, n_28;
  wire n_29, n_31, n_32, n_37, n_38;
  DFFRX2 \q_reg[7] (.RN (rst), .CK (clk), .D (n_32), .Q (q[7]), .QN
       (UNCONNECTED));
  DFFRX2 \q_reg[6] (.RN (rst), .CK (clk), .D (n_31), .Q (q[6]), .QN
       (UNCONNECTED0));
  OAI22X1 g791__2398(.A0 (swi), .A1 (n_28), .B0 (n_29), .B1 (n_27), .Y
       (n_32));
  OAI22X1 g794__5107(.A0 (swi), .A1 (n_26), .B0 (n_29), .B1 (n_22), .Y
       (n_31));
  DFFRX2 \q_reg[5] (.RN (rst), .CK (clk), .D (n_24), .Q (q[5]), .QN
       (UNCONNECTED1));
  DFFRX2 \q_reg[3] (.RN (rst), .CK (clk), .D (n_38), .Q (q[3]), .QN
       (UNCONNECTED2));
  XNOR2X1 g795__6260(.A (q[7]), .B (n_25), .Y (n_28));
  XNOR2X1 g793__4319(.A (q[7]), .B (n_17), .Y (n_27));
  AOI21XL g797__8428(.A0 (q[6]), .A1 (n_20), .B0 (n_25), .Y (n_26));
  OAI22X1 g799__5526(.A0 (swi), .A1 (n_18), .B0 (n_29), .B1 (n_15), .Y
       (n_24));
  DFFRX2 \q_reg[2] (.RN (rst), .CK (clk), .D (n_21), .Q (q[2]), .QN
       (UNCONNECTED3));
  DFFRX2 \q_reg[4] (.RN (rst), .CK (clk), .D (n_19), .Q (q[4]), .QN
       (UNCONNECTED4));
  XNOR2X1 g798__3680(.A (q[6]), .B (n_16), .Y (n_22));
  XNOR2X1 g812__1617(.A (q[2]), .B (n_12), .Y (n_21));
  NOR2X1 g802__2802(.A (q[6]), .B (n_20), .Y (n_25));
  XNOR2X1 g804__1705(.A (q[4]), .B (n_7), .Y (n_19));
  AOI21XL g805__5122(.A0 (q[5]), .A1 (n_9), .B0 (n_14), .Y (n_18));
  AND2XL g801__8246(.A (q[6]), .B (n_16), .Y (n_17));
  XNOR2X1 g808__7098(.A (q[5]), .B (n_8), .Y (n_15));
  INVX1 g809(.A (n_14), .Y (n_20));
  DFFRX2 \q_reg[1] (.RN (rst), .CK (clk), .D (n_6), .Q (q[1]), .QN
```

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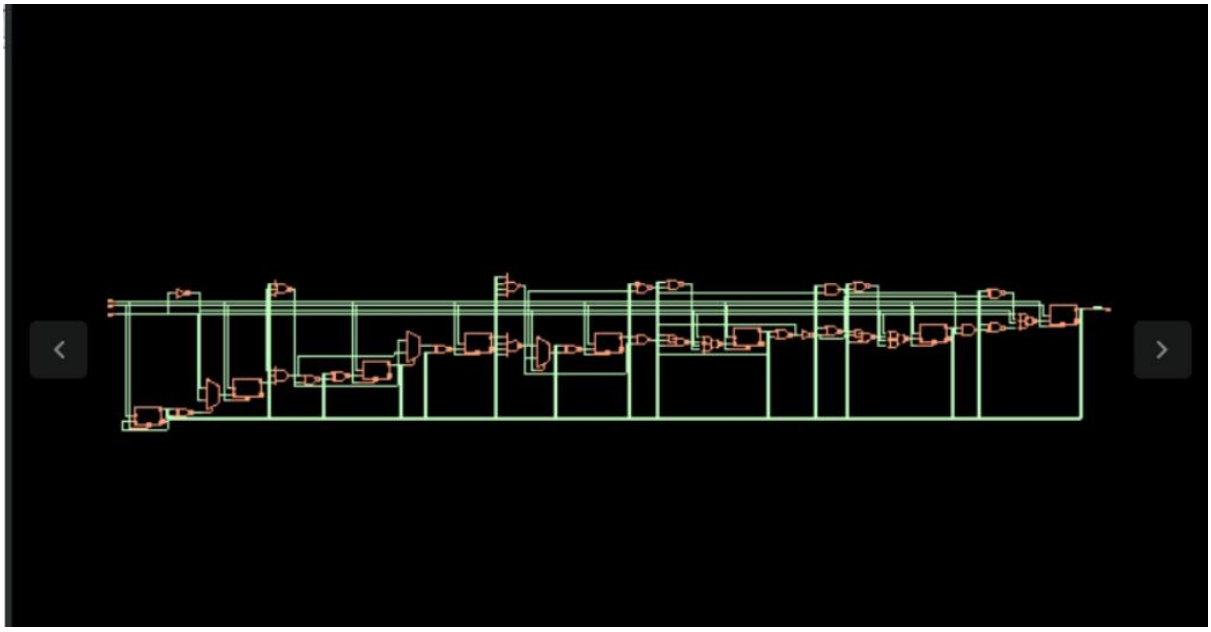
Schematic



Waveform