Design, implementation and synthesis of BCD 7 Segment display

BCD 7 Segment display

Verilog code

bcdseg7.v

```
module bs_7 (input[3:0]bn,input en, output [6:0]seg);
  reg [6:0] seg;
  always @(*)
begin
  if(~en)
  seg=1'bx;
else
    begin
      case (bn)
      4'b0000: seg = 7'b1111110;
      4'b0001: seg = 7'b0110000;
      4'b0010: seg = 7'b1101101;
      4'b0011: seg = 7'b1111001;
      4'b0100: seg = 7'b0110011;
      4'b0101: seg = 7'b1011011;
      4'b0110: seg = 7'b1011111;
      4'b0111: seg = 7'b1110000;
      4'b1000: seg = 7'b1111111;
      4'b1001: seg =7'b1111011;
      default:seg = 7'b000000;
      endcase
    end
end
endmodule
```

```
module bs_7_tb;
reg [3:0] bn; reg en;
wire [6:0]seg;
bs_7 a1(bn,en,seg);
initial
begin
en=0; #10;
en=1; #10;
bn[0]=0;bn[1]=0;bn[2]=0;bn[3]=0; #10;
bn[0]=1;bn[1]=0;bn[2]=0;bn[3]=0; #10;
bn[0]=0;bn[1]=1;bn[2]=0;bn[3]=0; #10;
bn[0]=1;bn[1]=1;bn[2]=0;bn[3]=0; #10;
bn[0]=0;bn[1]=0;bn[2]=1;bn[3]=0; #10;
bn[0]=1;bn[1]=0;bn[2]=1;bn[3]=0; #10;
bn[0]=0;bn[1]=1;bn[2]=1;bn[3]=0; #10;
bn[0]=1;bn[1]=1;bn[2]=1;bn[3]=0; #10;
bn[0]=0;bn[1]=0;bn[2]=0;bn[3]=1; #10;
end
endmodule
```

Constraint

bcdseg7.sdc

```
set sdc_version 1.4
current_design bs_7

set_input_transition 0.3 [get_ports bn]
set_input_transition 0.2 [get_ports en]
set_max_capacitance 20 [all_outputs]

set_load 0.10 [all_outputs]
set_max_fanout 20.00 [current_design]
```

Optimized Constraint

constraints_flie • set_input_delay -r • read_lib homehar: • Untitled • ==========

File Edit View

```
# ####################################################################

#  Created by Genus(TM) Synthesis Solution 21.17-s066_1 on Sat Aug 03 17:21:41 UTC 2024

# ####################################################################

set sdc_version 2.0

set_units -capacitance 1000fF
set_units -time 1000ps

# Set the current design
current_design bs_7

set_load -pin_load 0.1 [get_ports {seg[6]}]
set_load -pin_load 0.1 [get_ports {seg[5]}]
set_load -pin_load 0.1 [get_ports {seg[4]}]
set_load -pin_load 0.1 [get_ports {seg[3]}]
set_load -pin_load 0.1 [get_ports {seg[2]}]
set_load -pin_load 0.1 [get_ports {seg[1]}]
set_load -pin_load 0.1 [get_ports {seg[0]}]
set_clock_gating_check -setup 0.0
set_max_fanout 20.000 [current_design]
set_max_capacitance 20.0 [get_ports {seg[6]}]
set_max_capacitance 20.0 [get_ports {seg[5]}]
set_max_capacitance 20.0 [get_ports {seg[4]}]
set_max_capacitance 20.0 [get_ports {seg[3]}]
set_max_capacitance 20.0 [get_ports {seg[2]}]
set_max_capacitance 20.0 [get_ports {seg[1]}]
set_max_capacitance 20.0 [get_ports {seg[0]}]
set_input_transition 0.3 [get_ports {bn[3]}]
set_input_transition 0.3 [get_ports {bn[2]}]
set_input_transition 0.3 [get_ports {bn[1]}]
set_input_transition 0.3 [get_ports {bn[0]}]
set_input_transition 0.2 [get_ports en]
set_wire_load_mode "enclosed"
```

Ln 36, Col 30 | 1,307 characters

28°C Partly sunny Search

Report on area

Open bcd_area.rep ~/harsha/synthesis/logisyn/output/bcdseg7

```
====================================================================
  Generated by:           Genus(TM) Synthesis Solution 21.17-s066_1
  Generated on:           Aug 03 2024  05:19:08 pm
  Module:                 bs_7
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
====================================================================

Instance Module  Cell Count  Cell Area  Net Area   Total Area   Wireload
--------------------------------------------------------------------------
bs_7                    22      35.568     0.000       35.568 <none> (D)
  (D) = wireload is default in technology library
```

Report on power

Open ▾ bcd_power.rep ~/harsha/synthesis/logisyn/output/bcdseg7 Save

```
Instance: /bs_7
Power Unit: W
PDB Frames: /stim#0/frame#0
  ------------------------------------------------------------------------
    Category         Leakage     Internal    Switching        Total    Row%
  ------------------------------------------------------------------------
       memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
     register     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
        latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
        logic     1.40976e-09  8.11885e-07  7.78480e-06  8.59809e-06 100.00%
         bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
        clock     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
          pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
           pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  ------------------------------------------------------------------------
    Subtotal     1.40976e-09  8.11885e-07  7.78480e-06  8.59809e-06 100.00%
  Percentage           0.02%        9.44%       90.54%      100.00% 100.00%
  ------------------------------------------------------------------------
```

Report on timing

Open ▾ bcd_timing.rep ~/harsha/synthesis/logisyn/output/bcdseg7 Save

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 21.17-s066_1
  Generated on:           Aug 03 2024  05:18:49 pm
  Module:                 bs_7
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

Some unconstrained paths have not been displayed.
Use -unconstrained or set the root attribute 'timing_report_unconstrained' to 'true' to see only
these unconstrained paths.
```

Report on QoR

```
    Module:                     bs_7
    Operating conditions:       slow (balanced_tree)
    Wireload mode:              enclosed
    Area mode:                  timing library
  ==================================================================

  Timing
  -------
    Cost     Critical           Violating
   Group    Path Slack  TNS      Paths
  ------------------------------------
  default     No paths    0.0
  ------------------------------------
  Total                   0.0           0

  Instance Count
  --------------
  Leaf Instance Count              22
  Physical Instance count           0
  Sequential Instance Count         0
  Combinational Instance Count     22
  Hierarchical Instance Count       0

  Area
  ----
  Cell Area                              35.568
  Physical Cell Area                     0.000
  Total Cell Area (Cell+Physical)        35.568
  Net Area                               0.000
  Total Area (Cell+Physical+Net)         35.568

  Max Fanout                             6 (bn[1])
  Min Fanout                             1 (n_2)
  Average Fanout                         2.3
  Terms to net ratio                     2.8519
  Terms to instance ratio                3.5000
  Runtime                                20.959726 seconds
  Elapsed Runtime                        527 seconds
  Genus peak memory usage                1452.18
  Innovus peak memory usage              no_value
  Hostname                               ip-10-0-6-35.ap-south-1.compute.internal
```

Ln 44, Col 76 1,545 characters

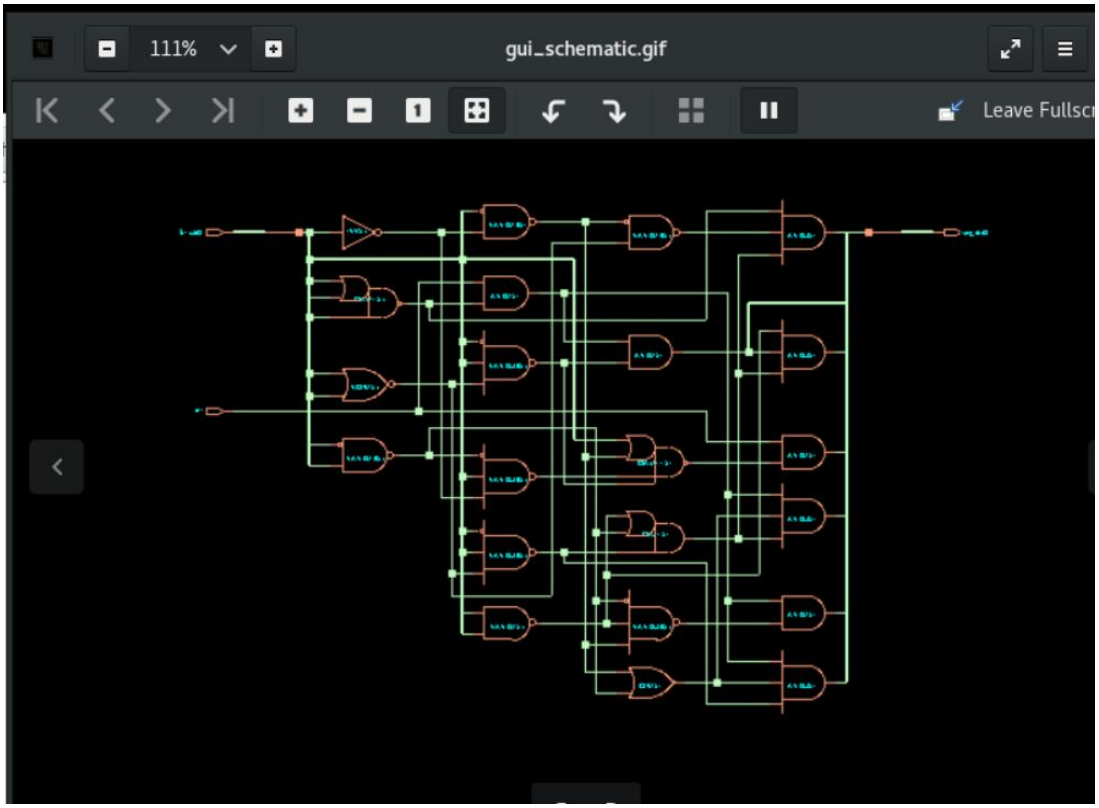
Updated Netlist

```
// Generated by Cadence Genus(TM) Synthesis Solution 21.17-s066_1
// Generated on: Aug  3 2024 17:21:23 UTC (Aug  3 2024 17:21:23 UTC)

// Verification Directory fv/bs_7

module bs_7(bn, en, seg);
  input [3:0] bn;
  input en;
  output [6:0] seg;
  wire [3:0] bn;
  wire en;
  wire [6:0] seg;
  wire n_1, n_2, n_3, n_4, n_5, n_7, n_8, n_9;
  wire n_10, n_11, n_12, n_14, n_15, n_18, n_28;
  AND3X1 g524__2398(.A (n_15), .B (n_14), .C (n_18), .Y (seg[3]));
  AND2X1 g522__5107(.A (en), .B (n_12), .Y (seg[2]));
  AND3X1 g523__6260(.A (n_10), .B (seg[4]), .C (n_18), .Y (seg[1]));
  AND3X1 g527__4319(.A (n_3), .B (n_4), .C (n_18), .Y (seg[0]));
  AND3X1 g526__8428(.A (n_15), .B (n_14), .C (n_9), .Y (seg[6]));
  AND2X1 g529__5526(.A (n_15), .B (n_8), .Y (seg[5]));
  OAI211X1 g525__6783(.A0 (bn[2]), .A1 (n_28), .B0 (n_2), .C0 (n_11),
       .Y (n_12));
  AND2X1 g528__3680(.A (n_15), .B (n_11), .Y (seg[4]));
  OA21X1 g530__1617(.A0 (n_10), .A1 (n_7), .B0 (n_9), .Y (n_18));
  NAND3BXL g531__2802(.AN (n_7), .B (n_10), .C (n_28), .Y (n_8));
  NAND3BXL g535__1705(.AN (bn[0]), .B (bn[1]), .C (n_5), .Y (n_11));
  NAND3BXL g534__5122(.AN (bn[1]), .B (bn[0]), .C (n_5), .Y (n_9));
  NAND2BXL g537__8246(.AN (n_28), .B (n_5), .Y (n_4));
  OR2X1 g536__7098(.A (n_28), .B (n_7), .Y (n_14));
  AND2X1 g532__6131(.A (en), .B (n_3), .Y (n_15));
  NAND3BXL g533__1881(.AN (n_7), .B (bn[1]), .C (n_1), .Y (n_2));
  OAI21XL g538__7482(.A0 (bn[2]), .A1 (bn[1]), .B0 (bn[3]), .Y (n_3));
  NOR2XL g542__4733(.A (bn[2]), .B (bn[3]), .Y (n_5));
  NAND2XL g541__6161(.A (bn[0]), .B (bn[1]), .Y (n_10));
  NAND2BXL g540__9315(.AN (bn[3]), .B (bn[2]), .Y (n_7));
  INVXL g543(.A (bn[0]), .Y (n_1));
  NAND2BX1 g2(.AN (bn[1]), .B (n_1), .Y (n_28));
endmodule
```

Schematic



Waveform