**RAM Verification Architecture in SV**

**TOP**

**TEST**

**ENV**

GENERATOR

Ref\_

Model

Score

board

Write\_

Monitor

Write\_

Driver

Read\_

Monitor

Read\_

Driver

Interface

**DUV**

**(A Class Based Layered TB)**

rd\_enb

reset

clk

**Sync.**

**RAM**

**16 x 8**

4\

rd\_addr

wr\_enb

8

4

rd\_data

wr\_addr

8

wr\_data