

Ref link for literature paper

[1] Görkem Nişancı ,Paul G. Flikkema and Tolga Yalçın “Symmetric Cryptography on RISC-V: Performance Evaluation of Standardized Algorithms”.

<https://www.mdpi.com/2410-387X/6/3/41>

[2] Ben Marshall, G. Richard Newell, Dan Page, Markku-Juhani O. Saarinen and Claire Wolf “The design of scalar AES Instruction Set Extensions for RISC-V “

<https://eprint.iacr.org/2020/930.pdf>

[3] Huimin Li, Nele Mentens and Stjepan Picek “Maximizing the Potential of Custom RISC-V Vector Extensions for Speeding up SHA-3 Hash” {<https://eprint.iacr.org/2022/868.pdf>}

[4] Sen Yang, Lian Shao ,Junke Huang and Wanghui Zou “ Design and Implementation of Low-Power IoT RISC-V Processor with Hybrid Encryption Accelerator “ {<https://www.mdpi.com/2079-9292/12/20/4222>}.

[5] A Adams, P Gupta “Cryptography Acceleration in a RISC”

https://carrv.github.io/2021/papers/CARRV2021_paper_87_Adams.pdf}.
\href{

[6] W wang, J Han, X Cheng, X Zeng “An energy-efficient crypto-extension design for RISC-V” {<https://dl.acm.org/doi/abs/10.1016/j.mejo.2021.105165>}.

[7] Jianwang Zhai, Chen Bai, Binwu Zhu, Yici Cai, Qiang Zhou, Bei Yu

“ **McPAT-Calib: A RISC-V BOOM Microarchitecture Power Modeling Framework**”

{<https://ieeexplore.ieee.org/document/9761982> }

[8] N. Bruschi, G. Haugou, G. Tagliavini, F. Conti, L. Benini, D. Rossi

“ A Highly Configurable, Fast and Accurate Full-Platform Simulator for RISC-V based IoT Processors {<https://arxiv.org/abs/2201.08166>}

[9] Ko Stoffelen “Efficient Cryptography on the RISC-V Architecture”

{<https://eprint.iacr.org/2019/794>}

[10] <https://roallogic.github.io/RV12/DATASHEET.html>