OBJECTIVE

Design of cascode amplifier and cascode current mirror in schematic and layout using LT Spice and Magic tools in 180 nm (supply 1.8 V) technology and only schematic of cascode amplifier, beta multiplier and cascode current mirror in 22 nm (supply 0.8 V) technology node to see the effect of lowering the technology node.

180 nm Technology

PROCEDURE

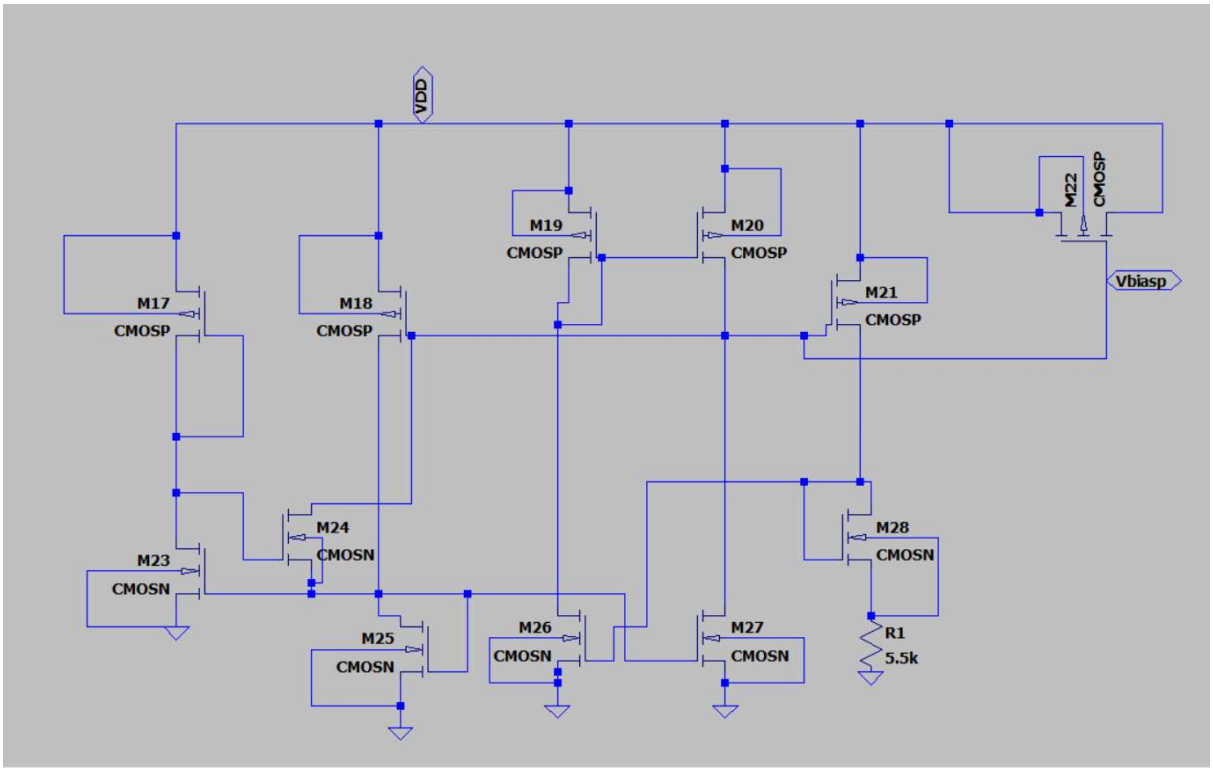


Fig: Beta Multiplier for 180 nm technology

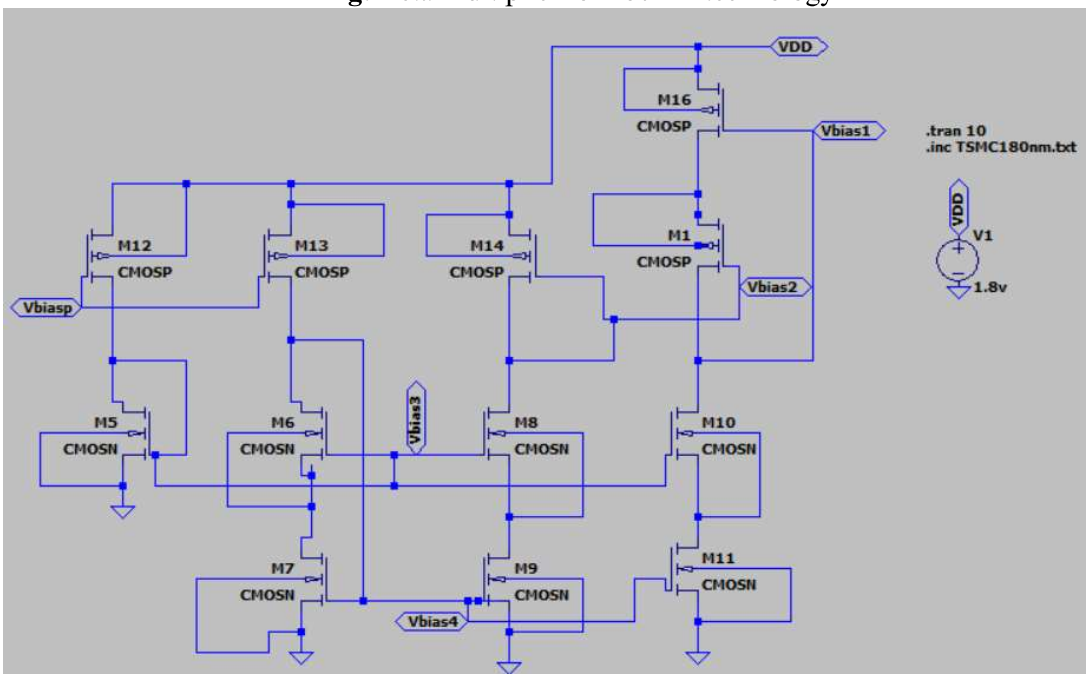


Fig: Current mirror implementation for 180 nm technology

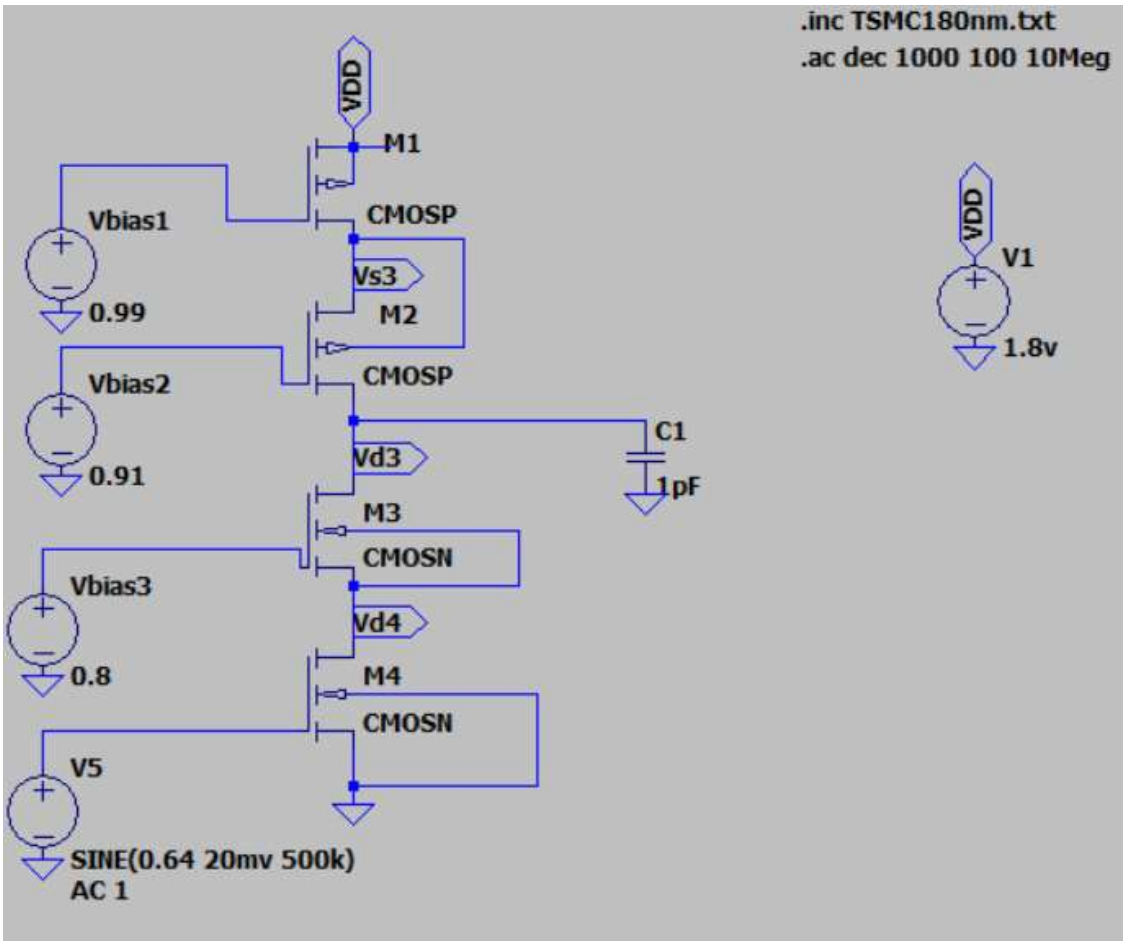


Fig: Cascode amplifier 180 nm technology

CALCULATIONS

Calculations

The expected frequency response of that of cascode amplifier is like integrator.

$\therefore$ Location of pole $f = \frac{1}{2\pi R_{out} C}$

Assuming pole to be at 1 MHz

$\therefore R_{out} = \frac{1}{2\pi \times 10^6 \times 10^{-12}}$

$= 159.154 k\Omega //$

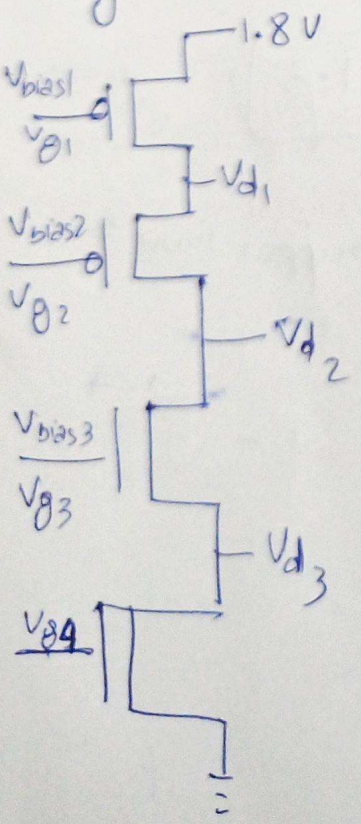
Given gain = 20

$\therefore 20 = g_m R_{out}$

$\therefore g_m = \frac{20}{159.154 \times 10^3} = 125.664 S //$

$\Delta g_m = \mu_n C_{ox} \frac{W}{L} \times (V_{gs} - V_{th}) \longrightarrow$ Eqn (2)

Now lets ~~took~~ drive all the mosfets into saturation region.



Following condition should be satisfied to drive all of them to saturation

$V_{g4} - 0 < V_{d3} - 0 + 0.5$

$\boxed{V_{g4} < V_{d3} + 0.5}$ — (1)

Then

$V_{g3} - V_{d3} - 0.5 < V_{d2} - V_{d3}$

$\boxed{V_{g3} < V_{d2} + 0.5}$ — (2) & $V_{g3} - V_{d3} > 0.5$

$\boxed{V_{g3} > 0.5 + V_{d3}}$ — (3)

then

$V_{g_2} - V_{d_1} - V_{thp} > V_{d_2} - V_{d_1}$

$V_{g_2} > V_{d_2} + V_{thp} \rightarrow V_{g_2} > V_{d_2} - 0.5$ → (4)

&

$V_{g_2} - V_{thp} < V_{d_1}$

$V_{g_2} < V_{d_1} + V_{thp} \rightarrow V_{g_2} < V_{d_1} - 0.5$ → (5)

then

$V_{g_1} - 1.8 - V_{thp} > V_{d_1} - 1.8$

$V_{g_1} > V_{d_1} + V_{thp} \rightarrow V_{g_1} > V_{d_1} - 0.5$ → (6)

& $V_{g_1} - 1.8 - V_{thp} < 0$

$V_{g_1} < 1.8 + V_{thp} \rightarrow V_{g_1} < 1.8 - 0.5 = 1.3$ → (7)

& if we move from VDD to ground we expect following inequality to be followed

$V_{d_3} < V_{d_2} < V_{d_1} < 1.8$ → (8)

→ one promising result we got is $V_{g_1} < 1.3$

Upon solving eq (4) (7) & (8)

we get V_{g_2} → upper limit < V_{g_1} → upper limit

Let say that $V_{d_3} = 0.2V$

then $V_{g_4} < 0.7$

And we know that $V_{d_2} > V_{d_3} = 0.2$

$\therefore V_{g_3} > V_{d_3} + 0.5 = 0.7$ //.

→ Upon exploiting above inequalities & after several trial & error the Bias voltages that satisfies saturation is

$V_{g4} = 0.64$	$V_{d3} = 0.2$
$V_{g3} = 0.8$	$V_{d2} = 1.4$
$V_{g2} = 0.91$	~~$V_{d2} = 1.67$~~
$V_{g3} = 0.99$	$V_{d1} = 1.6$

To attain the specified gain we have to specify W/L which can be calculated using this formula

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{tn})$$

$\mu_n C_{ox} = 175.4 \rightarrow$ nmos
$35.6 \rightarrow$ pmos

$g_m = 125.664S$

But theoretical W/L values does n't satisfies the specified goal, because we have not considered non idealities. After several trial and errors the target is achieved whose detail is given below,

Mosfet Number {Current Mirror}	W/L
M16	180n/540n
M1	180n/270n
M10	180n/240n
M11	180n/245n
M9	540n/180n
M8	540n/180n
M14	180n/509.5n
M13	540n/180n
M6	540n/180n
M7	270n/180n
M12	1558.198n/180n
M5	180n/720n

Mosfet Number {Cascode amplifier}	W/L
M1	1620n/180n
M2	1620n/180n
M3	1260n/180n
M4	1260n/180n

Bias Voltage	Values
Vbias1	0.99V
Vbias2	0.91V
Vbias3	0.8V
Offset source voltage	0.64V

Responses

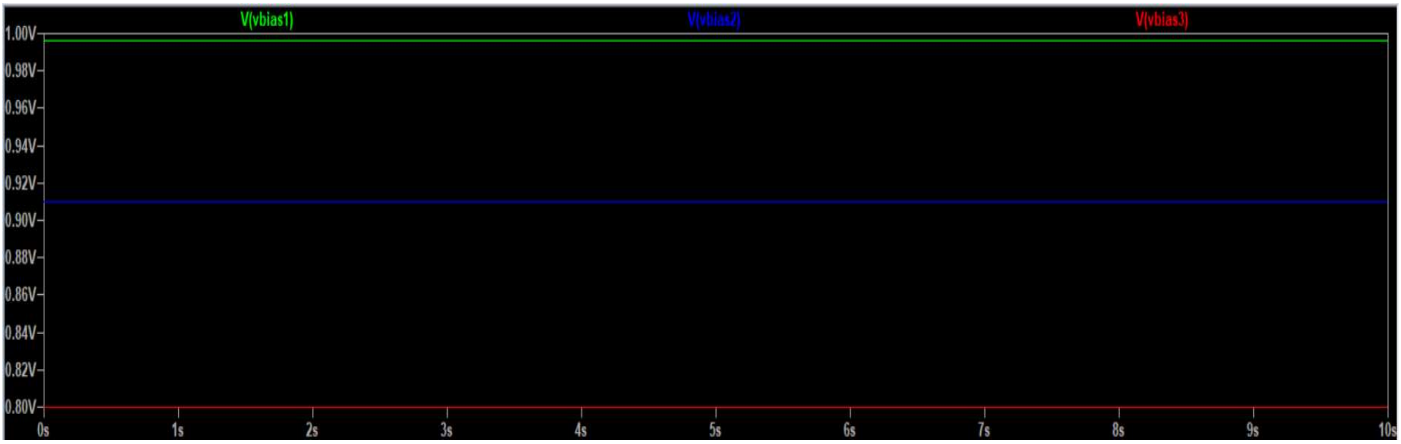


Fig: Bias Voltages

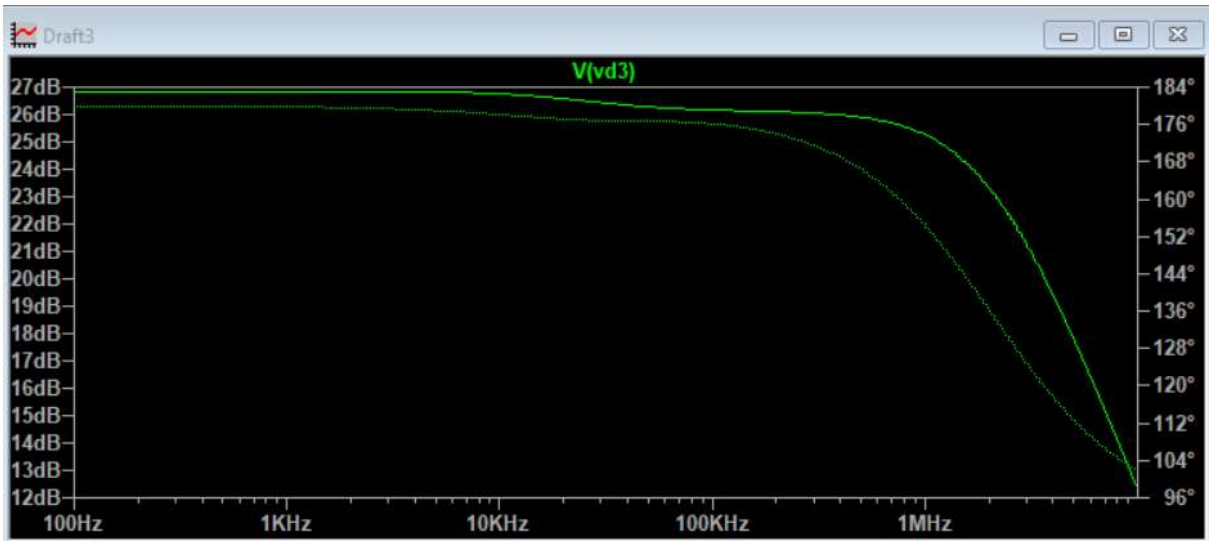


Fig: Frequency Response of Vout

22nm Technology

Procedure

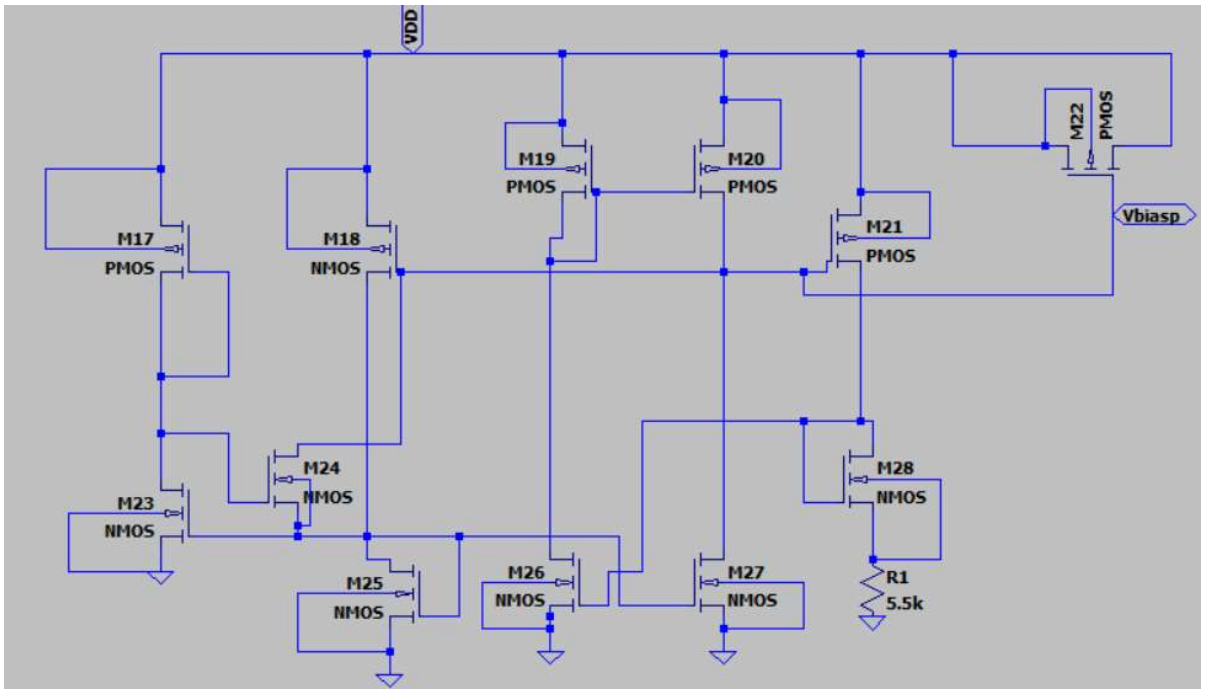


Fig: Beta Multiplier for 22 nm technology

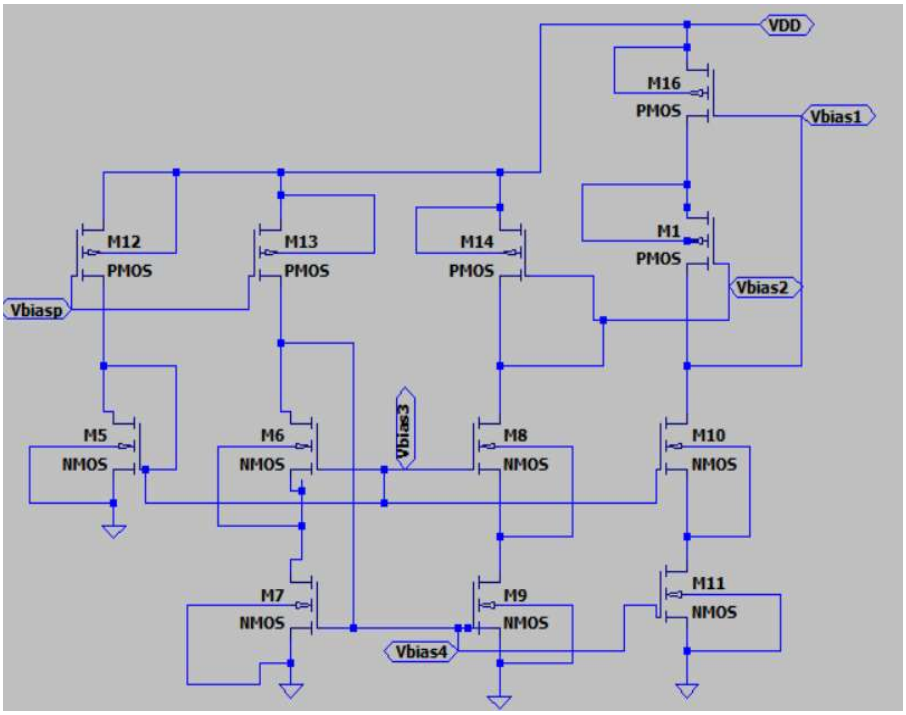


Fig: Current mirror implementation for 22 nm technology

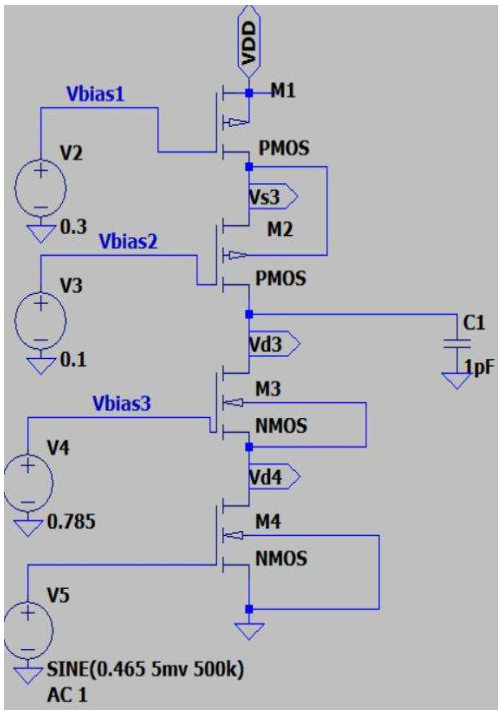
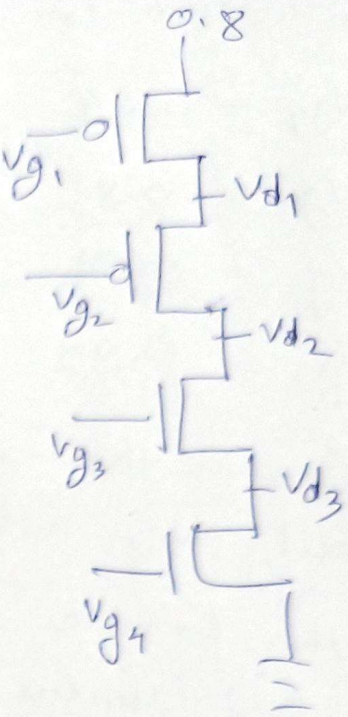


Fig: Cascode amplifier

For 22nm same approach is adopted

Following inequalities is what we get

To drive all the mosfet in saturation we get these inequalities.



$$V_{g_4} < V_{d_3} + 0.3 \quad \rightarrow (1)$$

$$V_{g_3} < V_{d_2} + 0.3 \quad \rightarrow (2)$$

$$V_{g_3} > 0.3 + V_{d_3} \quad \rightarrow (3)$$

$$V_{g_2} > V_{d_2} - 0.3 \quad \rightarrow (4)$$

$$V_{g_2} < V_{d_1} - 0.3 \quad \rightarrow (5)$$

$$V_{g_1} > V_{d_1} - 0.3$$

$$V_{g_1} \leq 0.8 - 0.3 = 0.5$$

After taking similar approach as that of 180nm we get following bias voltages that achieve our target.

$V_{g_1} = 0.3\ V$

$V_{g_2} = 0.1\ V$

$V_{g_3} = 0.785\ V$

$V_{g_4} = 0.465\ V$

To calculate W/L I adpoted the similar approach as that of 180nm where

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})$$

where $g_m = 87.964 \times 10^{-6}$ } $f = 700\,kHz$ }

But theoritical calculation doesn't achieve our goal because of not considering non-idealities hence after several trial and error we get this results.

Mosfet Number {Current Mirror}	W/L
M16	58n/44n
M1	44n/22n
M10	88n/22n
M11	1530n/44n
M9	660n/44n
M8	540n/180n
M14	55n/44n
M13	440n/44n
M6	540n/44n
M7	270n/44n
M12	778n/22n
M5	22n/990n

Mosfet Number {Cascode amplifier}	W/L
M1	819n/44n
M2	819n/44n
M3	820.52n/44n
M4	820.52n/44n

Bias Voltage	Values
Vbias1	0.3V
Vbias2	0.1V
Vbias3	0.785V
Offset source voltage	0.465V

Responses

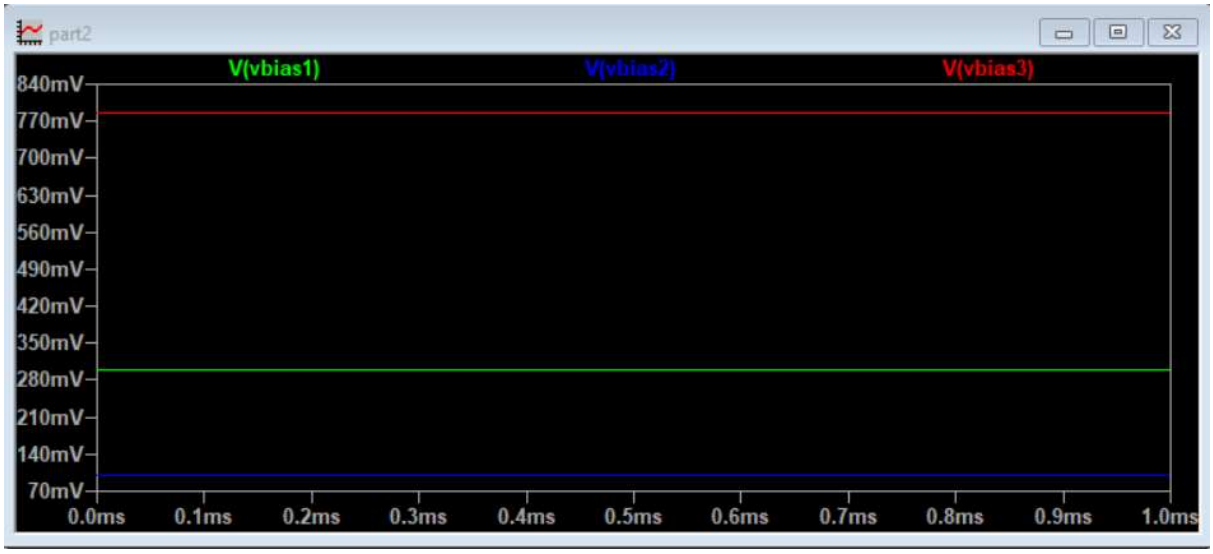


Fig: Bias Voltages

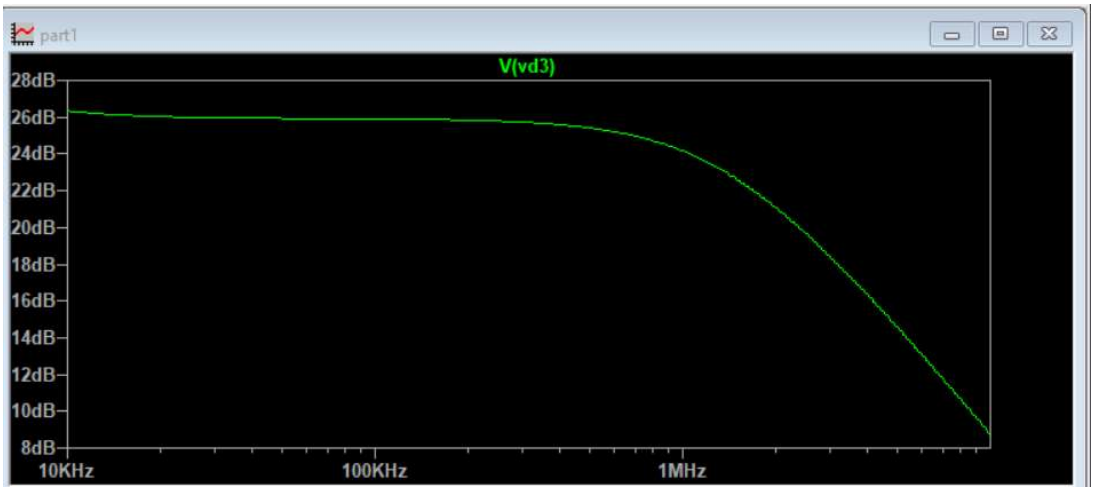


Fig: Frequency response of Vout

Layout in Magic for 180 nm:

- Magic layout was designed according to the given parameters. Each block in the magic corresponded to 90nm.)
- Metal 1 was used to made the connections and Vdd and ground.
- Polysilicon was used to lay the gate.
- Design Rule Check was obtained zero

Layout Schematics

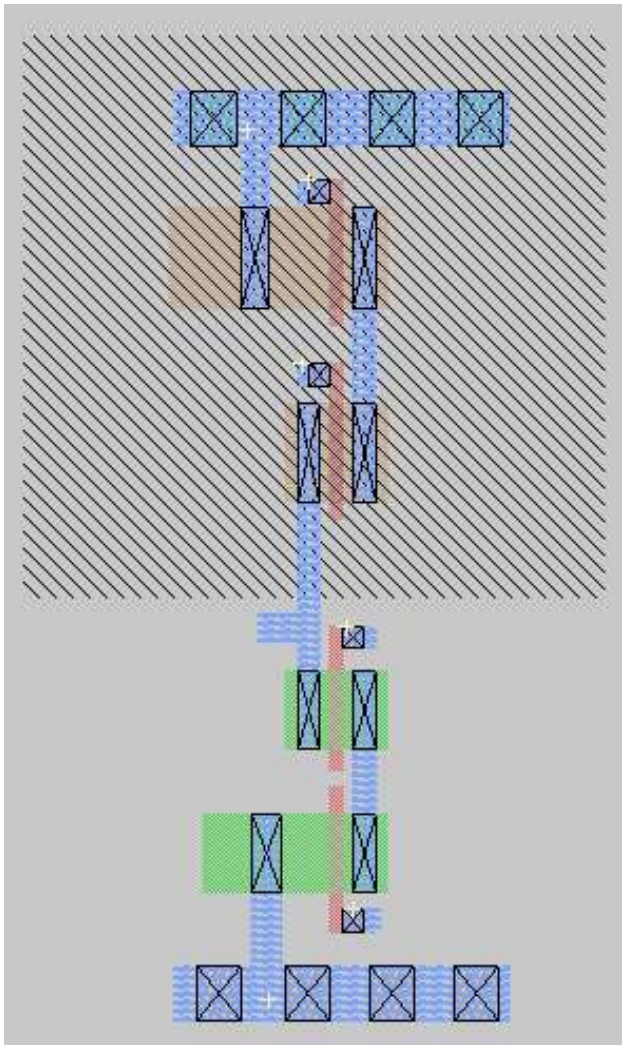


Fig: Cascode amplifier

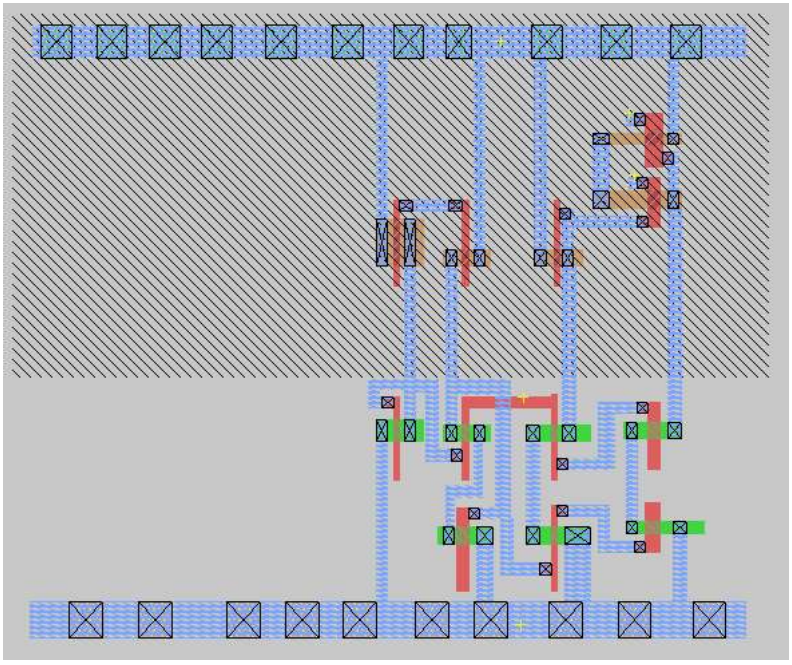


Fig: Current Mirror