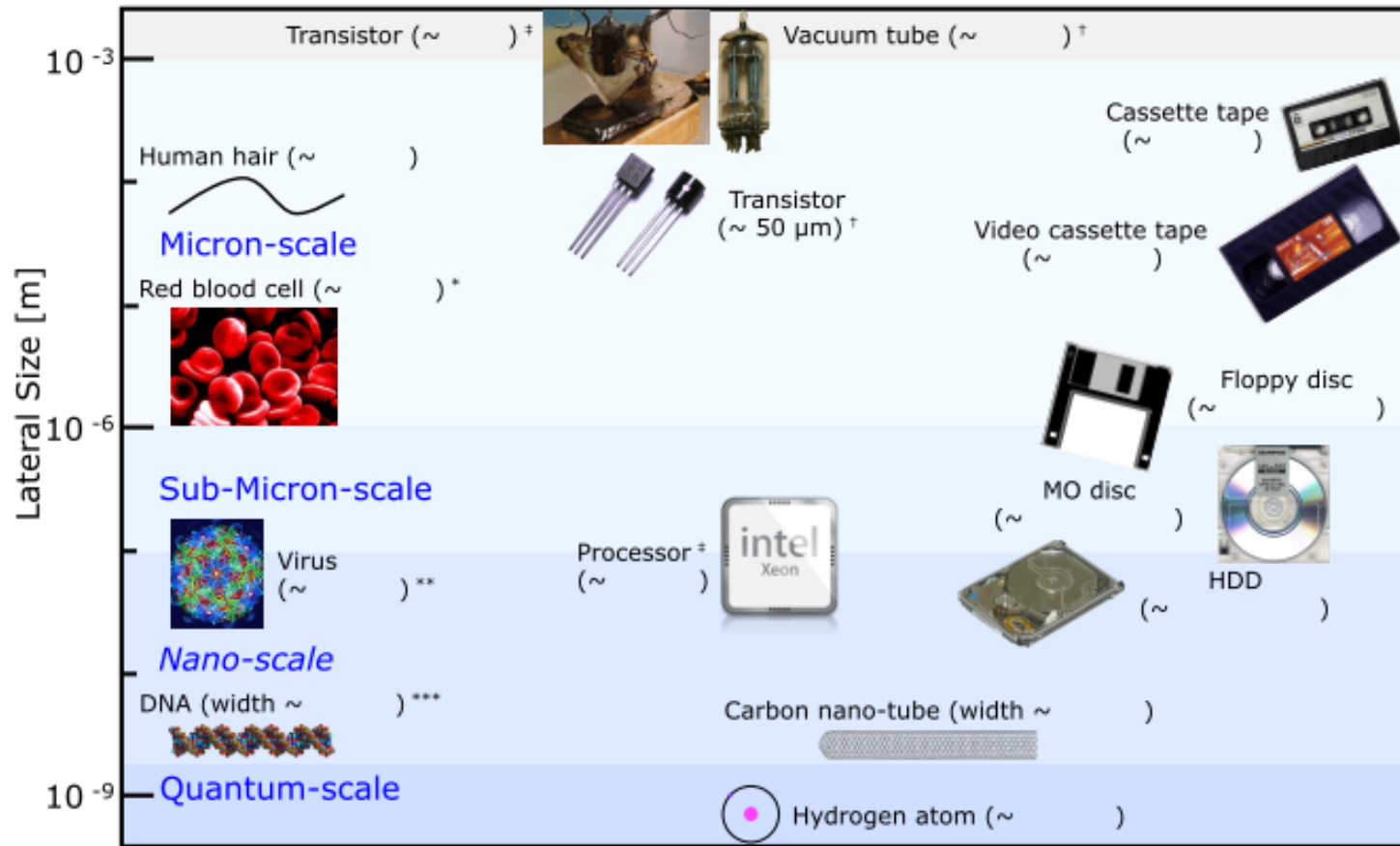


# Lecture 1 contents

Topic name	Content	Chapters / Sections
<b>Physical and Technological Limitations of nano CMOS Devices to the End of the Roadmap and Beyond</b>	International Technology Roadmap of Semiconductors Acceleration and Issues Limitations and Showstoppers Coming from CMOS Scaling Technological Options to MOSFET Optimization	Book: Silicon Nanoelectronics edited by Oda and Ferry Sections : 2.1, 2.2, 2.3, 3.1 Videos on MOSFET fabrication and working <b>ppt file: EL453_Nano_1</b>



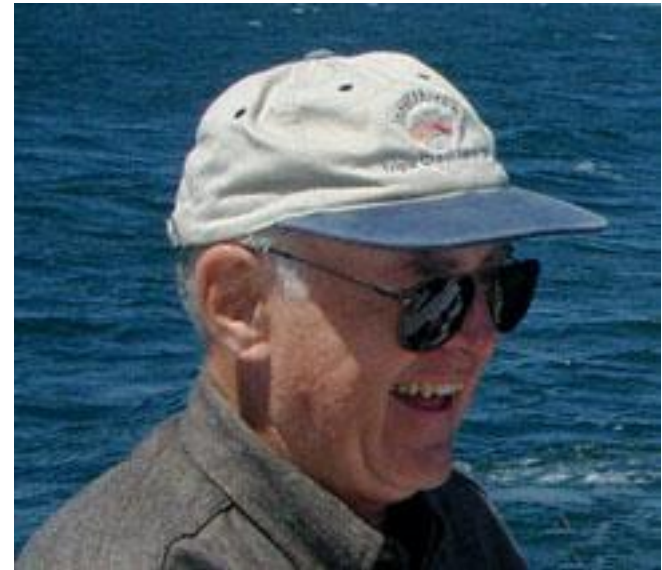
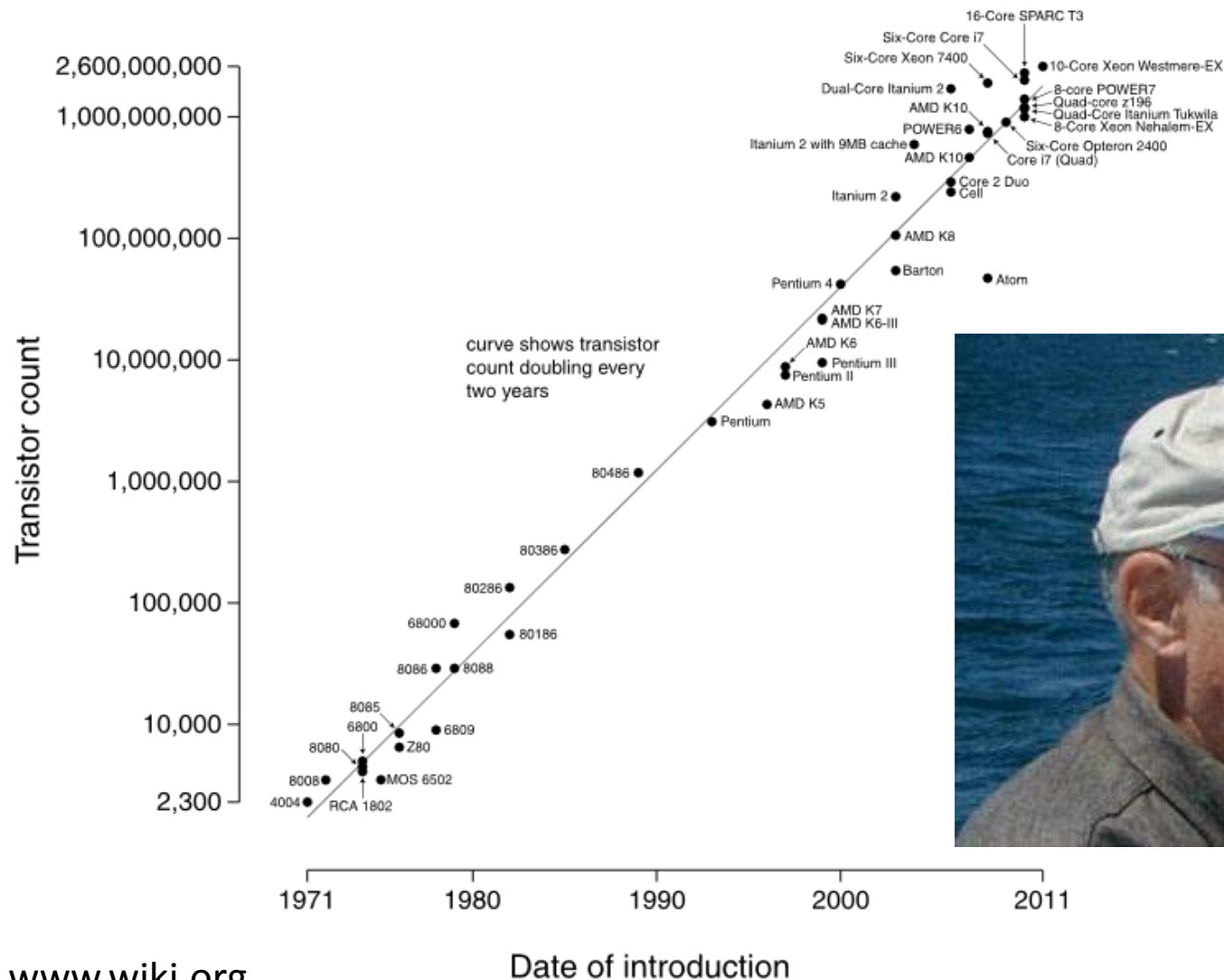
## Go into Nano-Scale



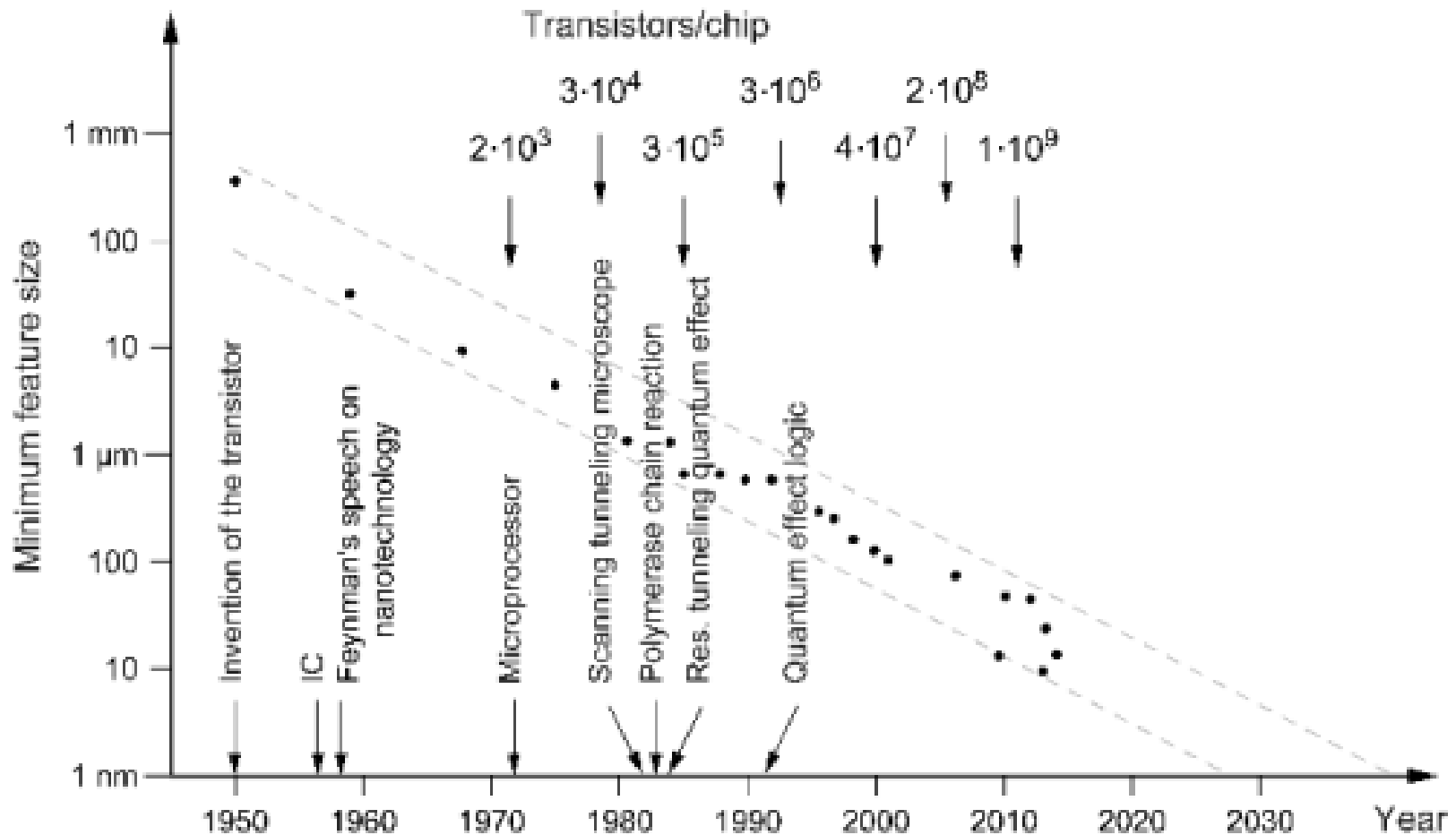
The term nanoelectronics encompasses developments in electronics that entail device physics and structures below the 100 nm level. Research in nano-electronics envisions extending CMOS and proposes new devices and technologies that perform either processor or memory functions or both in universal devices.

# Miniaturization and Integration in Semiconductor Devices

## Microprocessor Transistor Counts 1971-2011 & Moore's Law

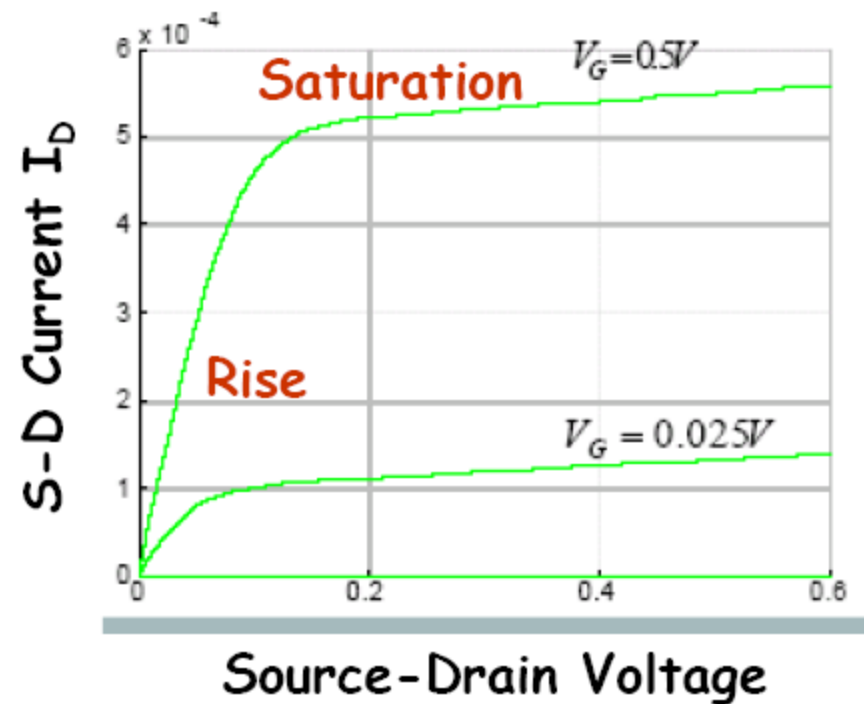
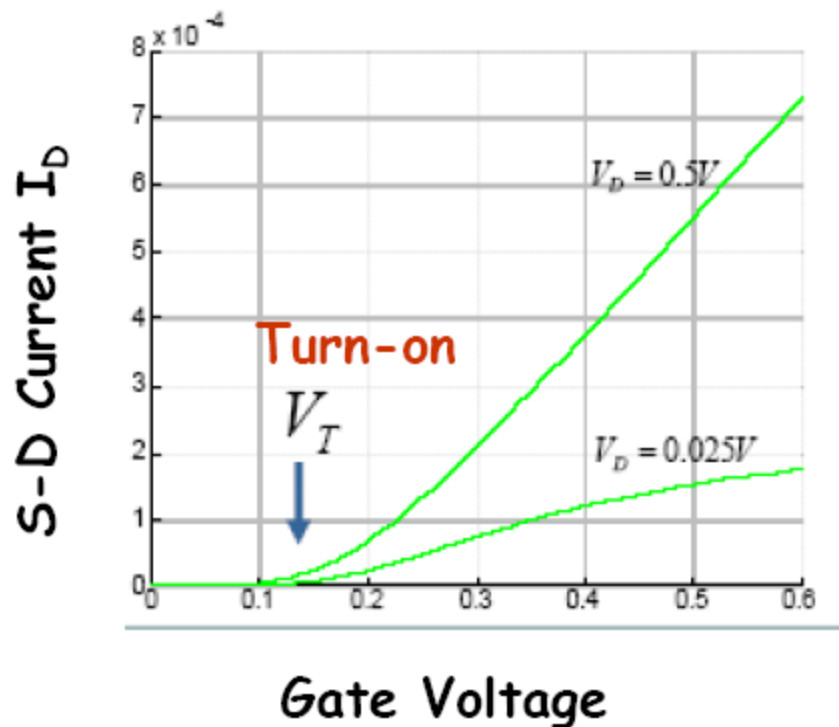
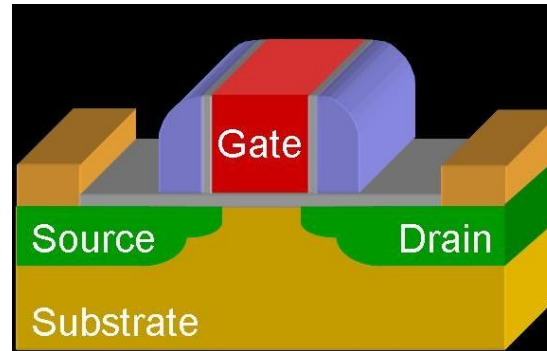


# Moore's Law



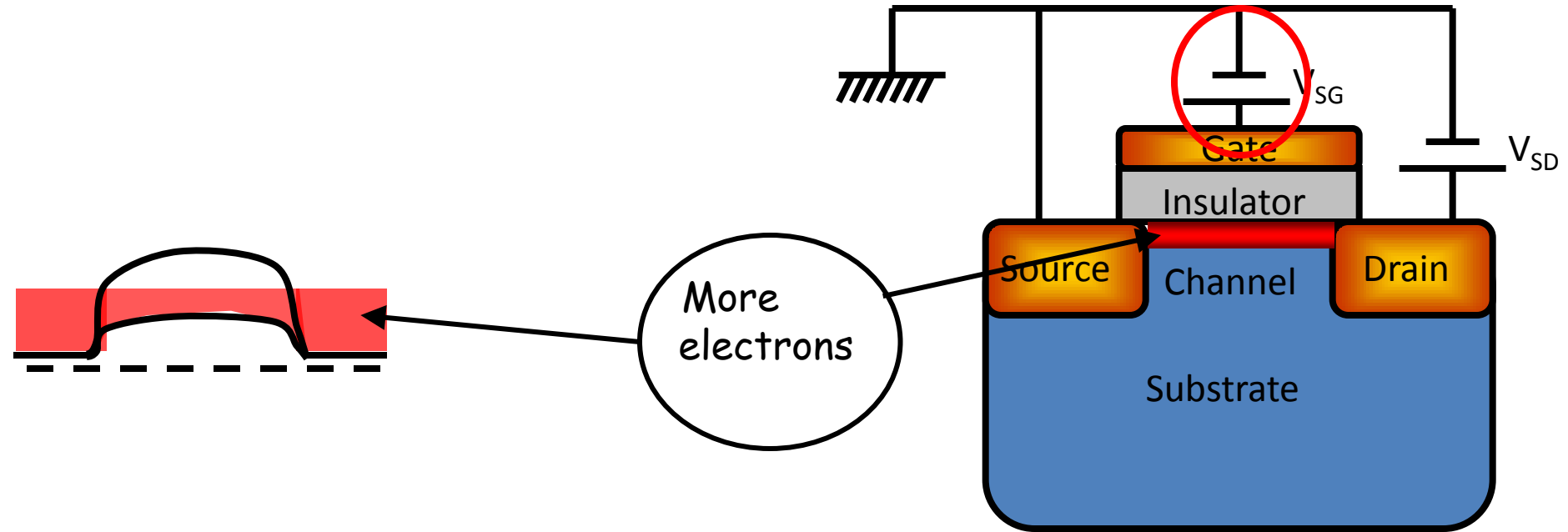
Nanotechnology and Nanoelectronics Materials, Devices, Measurement Techniques,  
W. R. Fahrner (Editor), Springer

# MOSFET I-Vs



# Operation of a transistor

$V_{SG} > 0$   
n type operation

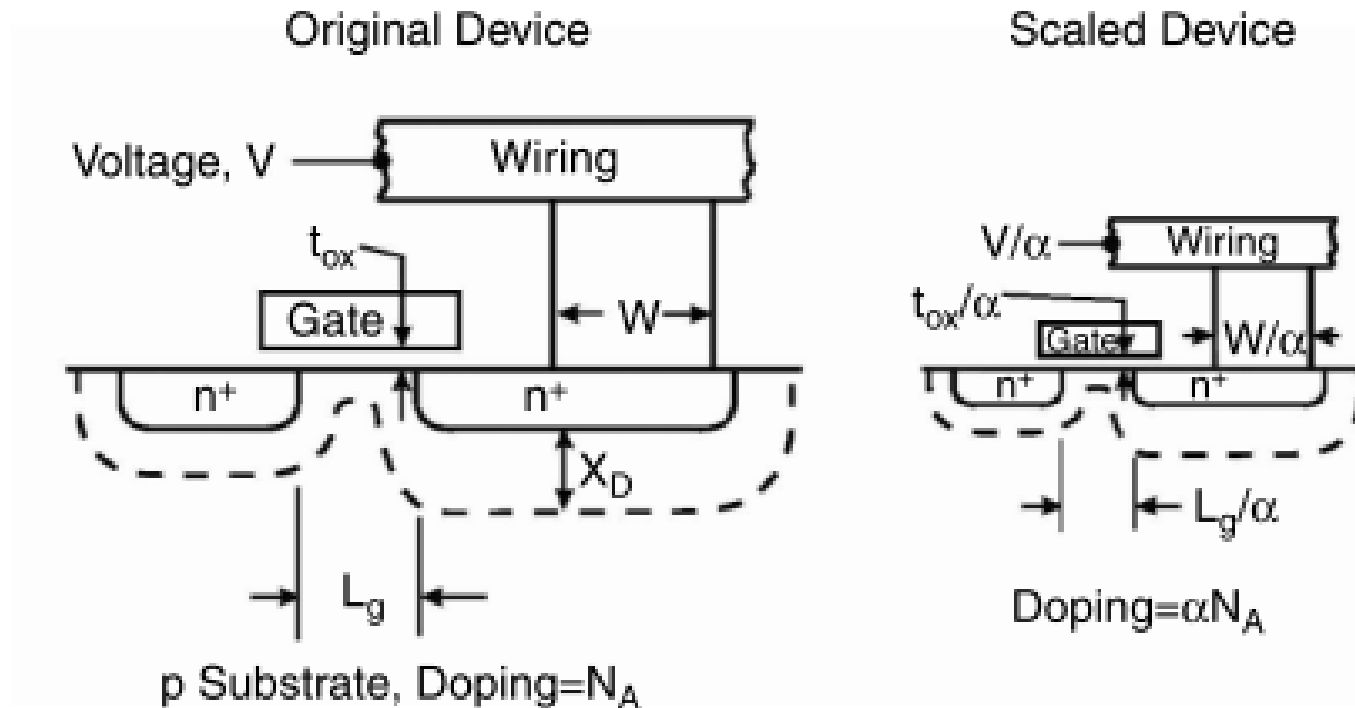


Positive gate bias attracts electrons into channel  
Channel now becomes more conductive

# ITRS Projections

<b>Year of Production</b>	<b>2013</b>	<b>2016</b>	<b>2019</b>	<b>2022</b>	<b>2025</b>
<b>Technology Node (nm) (DRAM Half pitch)</b>	<b>28</b>	<b>20</b>	<b>14.2</b>	<b>10</b>	<b>7.1</b>
<b>Transistor Gate Length in Microprocessors circuits (nm)</b>	<b>20</b>	<b>15.3</b>	<b>11.7</b>	<b>8.9</b>	<b>6.6</b>
<b>Wafer diameter (inch)</b>	<b>12</b>	<b>18</b>	<b>18</b>	<b>18</b>	<b>18</b>
<b>Transistors density in Microprocessor (billion/ cm<sup>2</sup>)</b>	<b>1.59</b>	<b>3.19</b>	<b>6.38</b>	<b>12.77</b>	<b>25.54</b>
<b>Number of interconnect wiring levels in the Microprocessor</b>	<b>12</b>	<b>13</b>	<b>14</b>	<b>15</b>	<b>16</b>
<b>Operating voltage (V)</b>	<b>0.85</b>	<b>0.77</b>	<b>0.71</b>	<b>0.64</b>	<b>0.59</b>

## Schematic illustration of the scaling of Si technology by a factor alpha



Oda, S. et Ferry, D. (2006), Silicon Nanoelectronics.

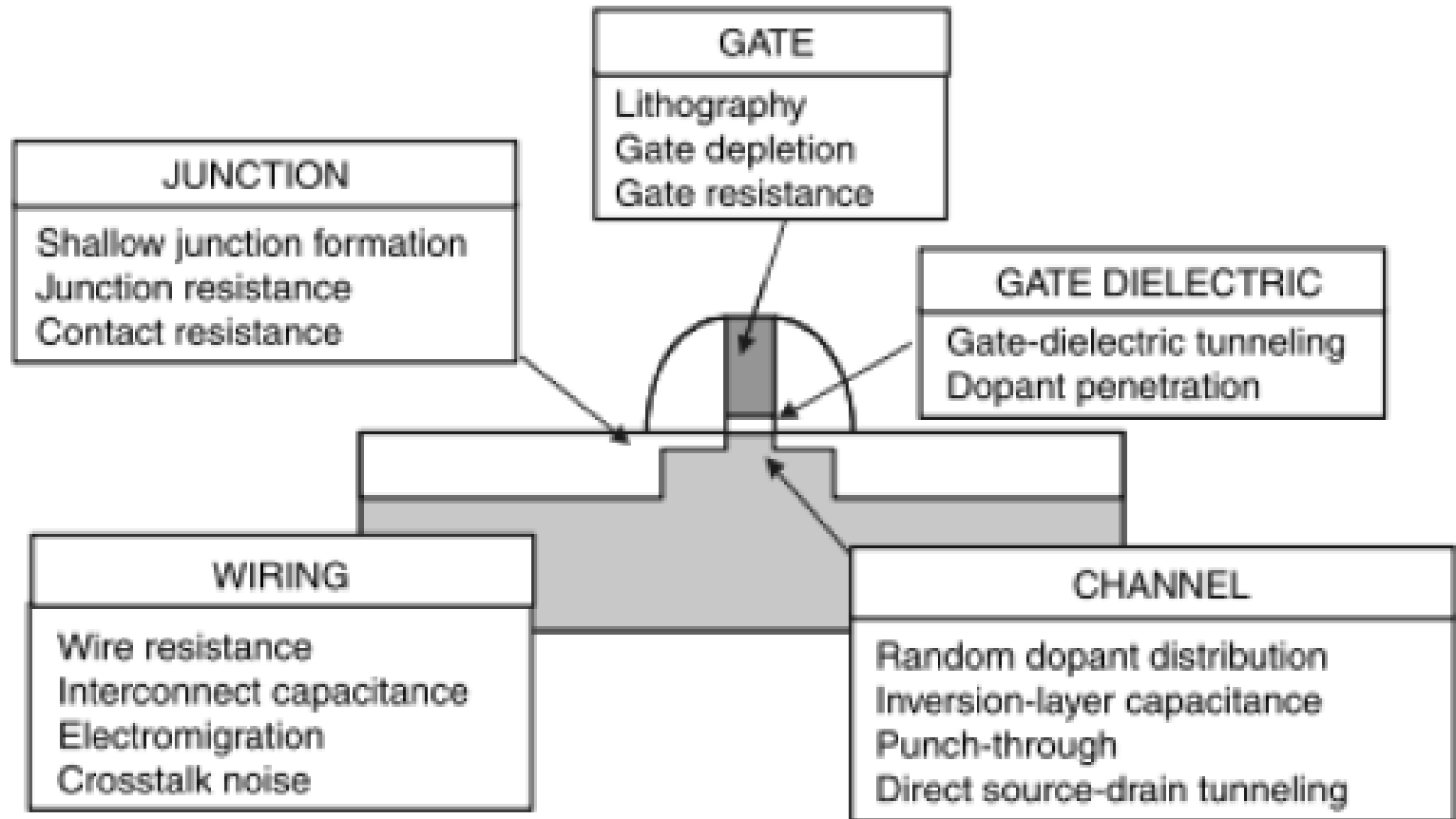


## Technology Scaling Rules for Three Types of Scaling

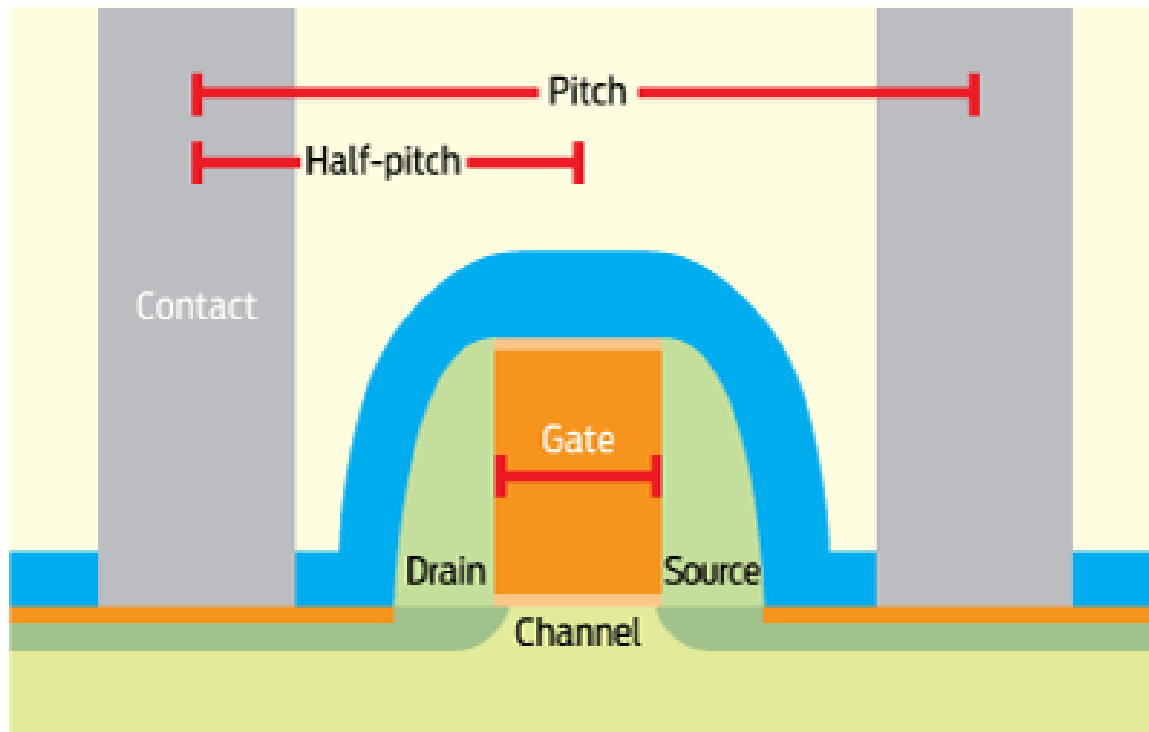
Physical Parameter	Constant-Electric Field Scaling Factor	Generalized Scaling Factor	Generalized Selective Scaling Factor
Channel length, insulator thickness	$1/\alpha$	$1/\alpha$	$1/\alpha_d$
Wiring width, channel width	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
Electric field in device	1	$\epsilon$	$\epsilon$
Voltage	$1/\alpha$	$\epsilon/\alpha$	$\epsilon/\alpha_d$
On-current per device	$1/\alpha$	$\epsilon/\alpha$	$\epsilon/\alpha_w$
Doping	$\alpha$	$\epsilon\alpha$	$\epsilon\alpha_d$
Area	$1/\alpha^2$	$1/\alpha^2$	$1/\alpha_w^2$
Capacitance	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
Gate delay	$1/\alpha$	$1/\alpha$	$1/\alpha_d$
Power dissipation	$1/\alpha^2$	$\epsilon^2/\alpha^2$	$\epsilon^2/\alpha_w\alpha_d$
Power density	1	$\epsilon^2$	$\epsilon^2\alpha_w/\alpha_d$

Oda, S. et Ferry, D. (2006), Silicon Nanoelectronics.

# Problems in the Scaling of MOSFETs

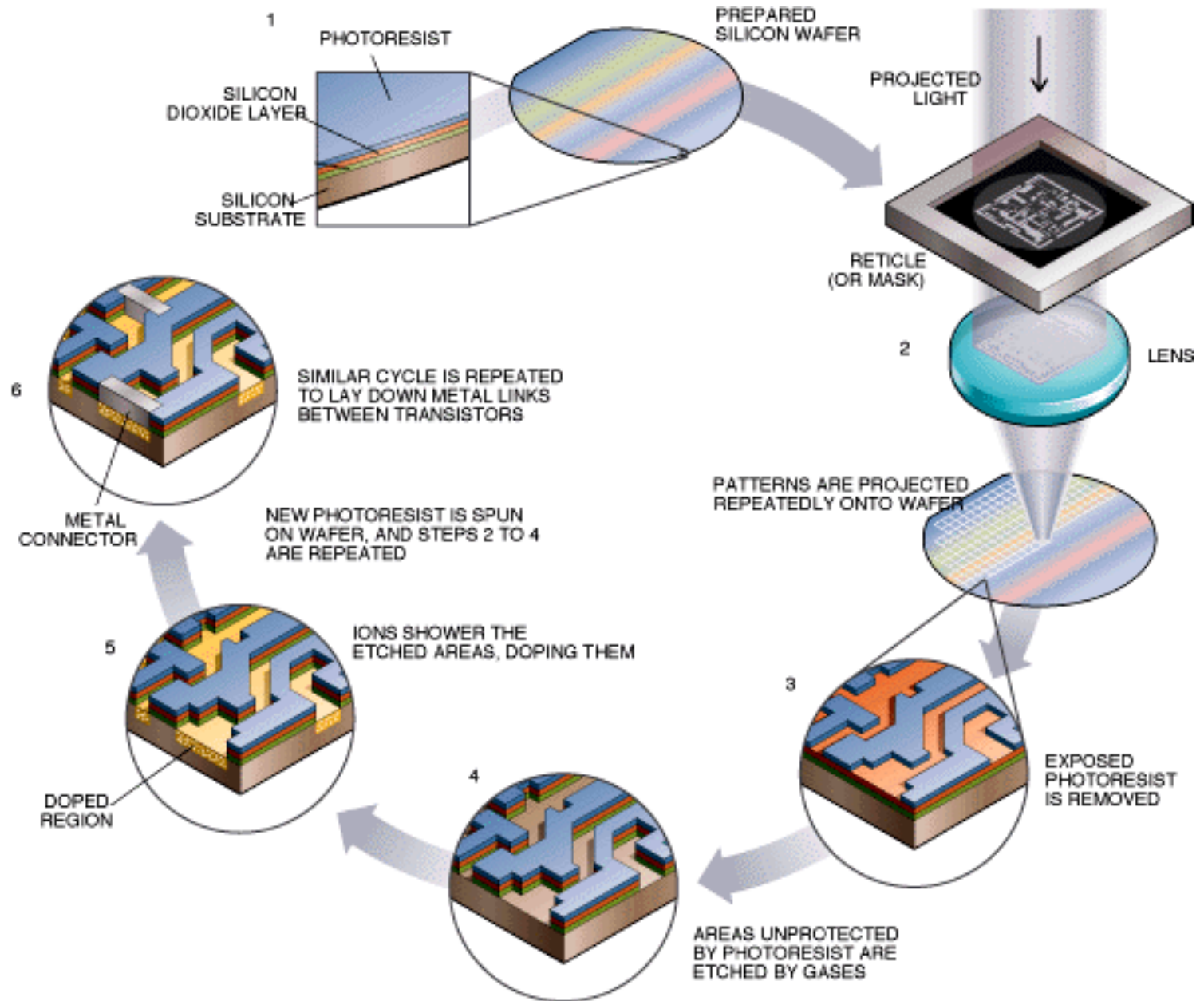


Oda, S. et Ferry, D. (2006), Silicon Nanoelectronics.



The half-pitch of the first wiring layer is the defining feature for memory chips, while the gate length is the gauge for logic manufacturers.

# IC fabrication process



# Home-work

1. Describe micro fabrication process with proper diagrams.
2. Describe short channel effects in MOSFETs

Good Luck !