Phase Change Memory

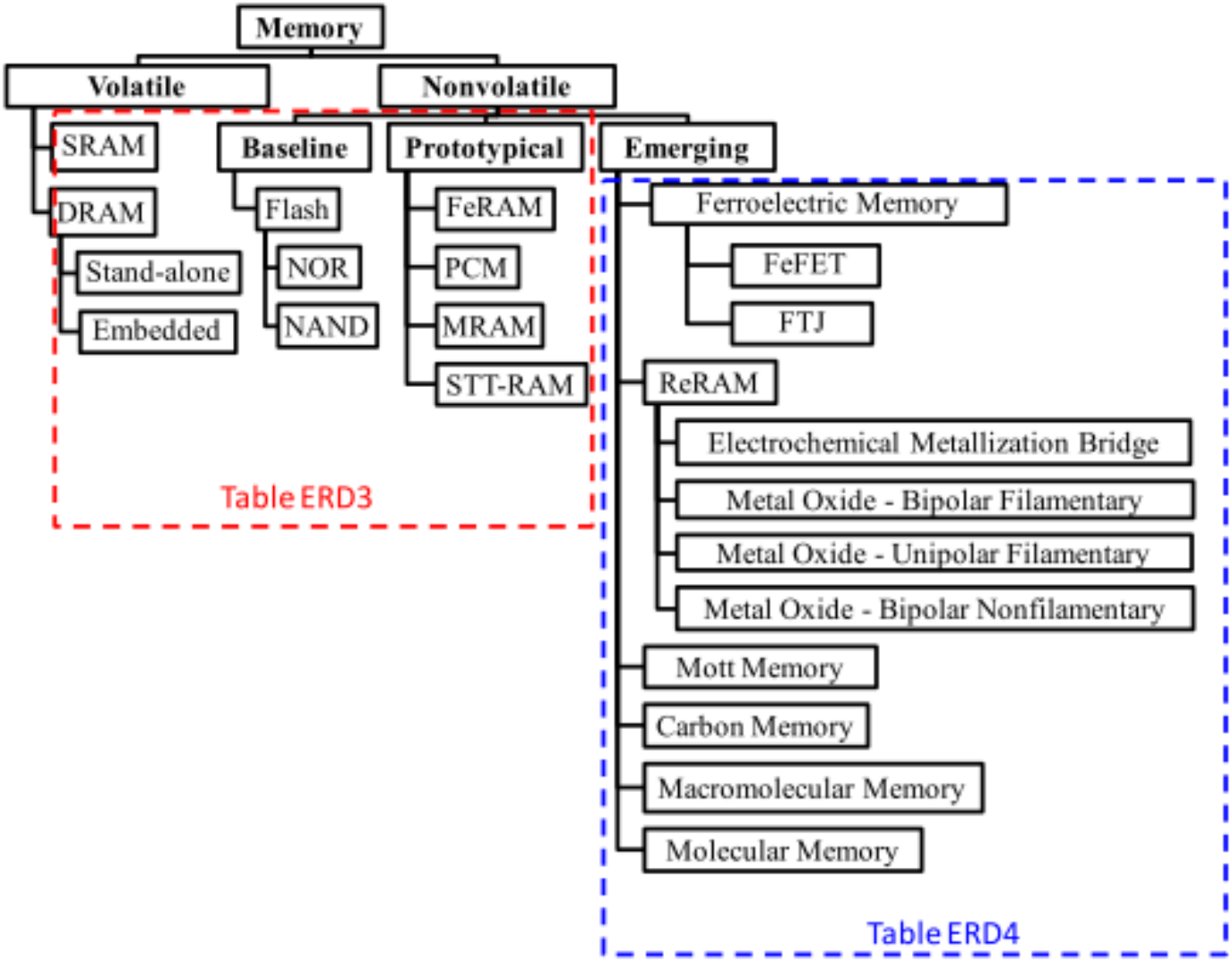
A New Era Emerging for Memory?

Convergence of many factors/pressures:

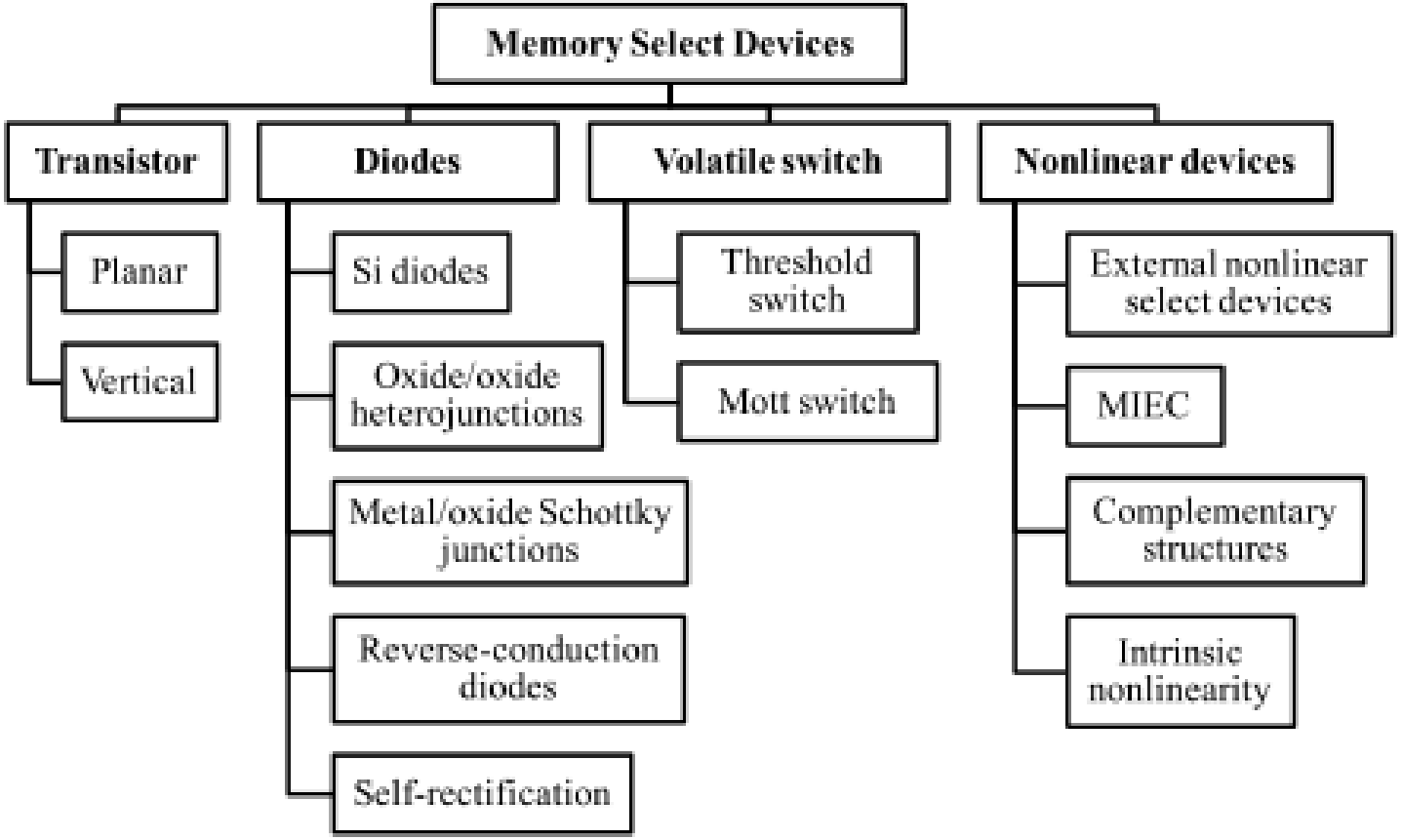
- Increasing importance of memory to user experience
  - Our lives are becoming one big shared database, with IOPs becoming more important than MIPs
- Both NAND and DRAM facing scaling challenges
  - No hard "wall," but increasing complexity
- Explosion of "new" memory storage concepts
  - New storage physics are enabling new usage models
- Evolving memory hierarchy
  - New features, relentless cost reduction, and need for I/O performance are remaking the memory hierarchy

Memory is moving from a support role to a defining system role

Taxonomy of emerging memory devices



Taxonomy of memory select devices



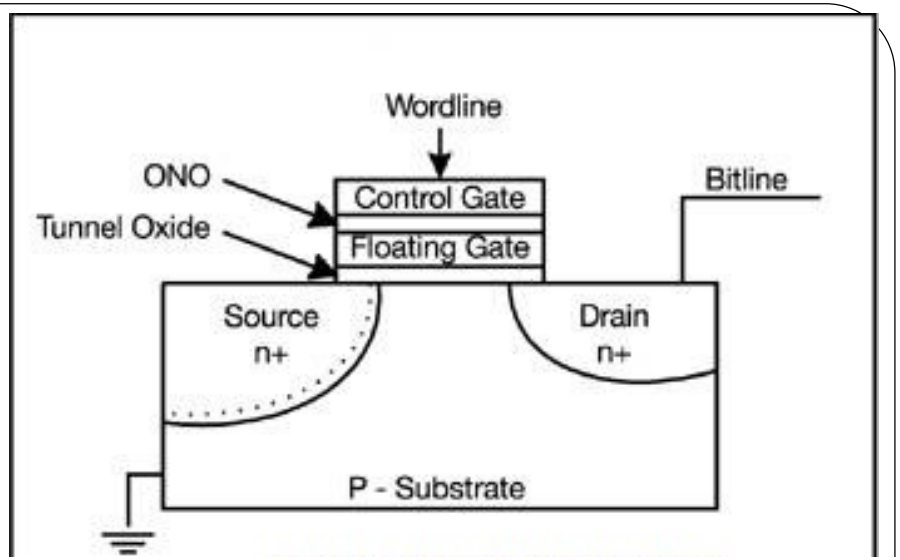
Memory Scaling Challenges

Just as memory usage becomes "interesting"…

- "Planar" nonvolatile (NVM) technology scaling is becoming difficult:
  - MOS transistor-based cell; charge-storage memory effect
  - Starting to encounter physical scaling limitations
  - Manifesting first as reliability → endurance/retention
  - Increasing degree of memory management required for functionality → memory abstraction
- No scaling "brick wall," but complexity is increasing the level of management required to maintain added functionality

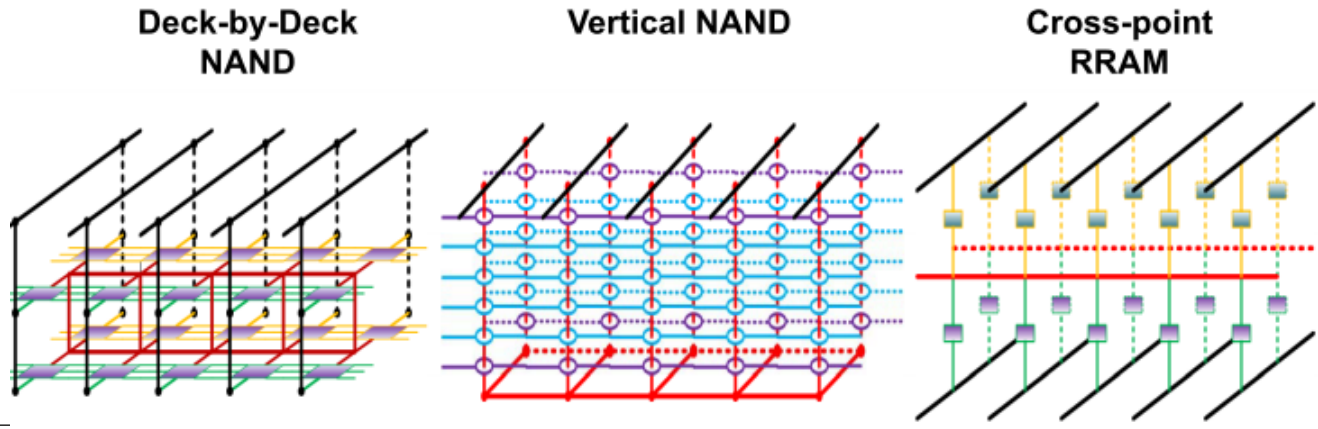
Flash Cell Scaling Challenges

Main scaling issues: 1. Few-electron problem 2. Tunnel and interpoly charge retention 3. Voltage isolation 4. Parasitic charge trapping 5. Read and write noise



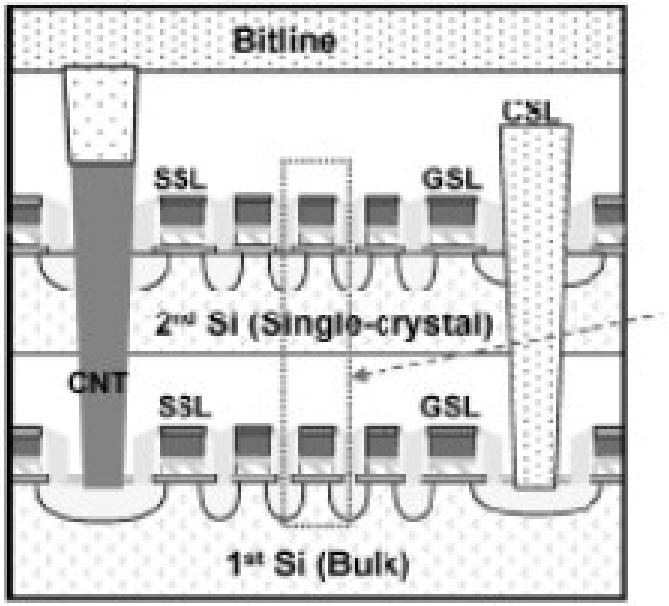
Going 3-D → Three Major Options

- **Deck-by-deck NAND** – SOI for upper decks
- **Vertical NAND** – Vertical cells arranged in vertical strings
- **Cross-point** – RRAM (resistive RAM) cells

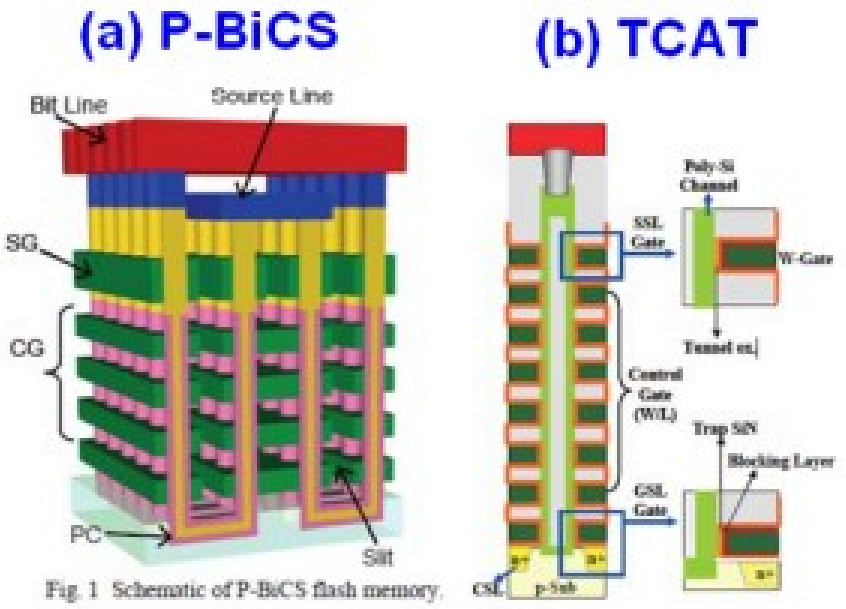


Flash Memory SUMMIT

3-D NAND Highlights



Deck-by-Deck: Dual-Deck



Vertical NAND

- Significant industry effort on 3-D NAND development
- Conference publications showing promising results
- Possibility to extend NAND roadmap for several generations

Phase Change Memory Case Study

- Of the emerging RRAMs, PCM is the most mature:
  - Already in low-volume production
  - Demonstrated at Gb density vs. other EM at Mb density
  - Announced by multiple memory companies
- PCM has been heavily studied for 10+ years:
  - Widely published – lots of good-quality technical content
  - Chalcogenide-based material understanding is fairly mature
  - Many active researchers in both industry and academia
- Provides insight into other emerging-materials systems:
  - Many of the RRAMs share similar attributes with PCM

Current Baseline and Prototypical Memory Technologies

		Baseline Technologies					Prototypical Tech	
		DRAM		SRAM [C]	Flash		FeRAM	STT-MRAM
		Stand-alone [A]	Embedded [C]		NOR Embedded [C]	NAND Stand-alone [A]		
Storage Mechanism		Charge on a capacitor		Inter-locked state of logic gates	Charge trapped in floating gate or in gate insulator		Remnant polarization on a ferroelectric capacitor	Magnetization of ferromagnetic layer
Cell Elements		1T1C		6T	1T		1T1C	1(2)T1R
Feature size F, nm	**2011**	36	65	45	90	22	180	65
	2024	9	20	10	25	8	65	16
Cell Area	**2011**	$6F^2$	$(12–30)F^2$	140 F^2	10 F^2	4 F^2	$22F^2$	$20F^2$
	2024	$4F^2$	$(12–50)F^2$	140 F^2	10 F^2	4 F^2	$12F^2$	$8F^2$
Read Time	**2011**	<10 ns	2 ns	0.2 ns	15 ns	0.1ms	40 ns [G]	35 ns [J]
	2024	<10 ns	1 ns	70 ps	8 ns	0.1ms	<20 ns [H]	<10 ns
W/E Time	**2011**	<10 ns	2 ns	0.2 ns	1μs/10ms	1/0.1 ms	65 ns [G]	35 ns {J]
	2024	<10 ns	1 ns	70 ps	1μs/10ms	1/0.1 ms	<10 ns[H]	<1 ns
Retention Time	**2011**	64 ms	4 ms	[D]	10 y	10 y	10 y	>10 y
	2024	64 ms	1 ms	[D]	10 y	10 y	10 y	>10 y
Write Cycles	**2011**	>1E16	>1E16	>1E16	1E5	1E4	1E14	>1E12
	2024	>1E16	>1E16	>1E16	1E5	5E3	>1E15	>1E15
Write Operating Voltage (V)	**2011**	2.5	2.5	1	10	15	1.3-3.3	1.8
	2024	1.5	1.5	0.7	9	15	0.7–1.5	<1
Read Operating Voltage (V)	**2011**	1.8	1.7	1	1.8	1.8	1.3–3.3	1.8
	2024	1.5	1.5	0.7	1	1	0.7–1.5	<1
Write Energy (J/bit)	**2011**	4E-15 [B]	5.00E-15	5.00E-16	1E-10 [E]	>2E-16 [F]	3E-14 [I]	2.5E-12 [A]
	2024	2E-15 [B]	2.00E-15	3.00E-17	1E-11 [E]	>2E-17 [F]	7E-15 [I]	1.5E-13 [A]

ITRS 2012 update

PCM benefits

- scalable
- multiple bits per cell
- Non volatile meaning significant leakage power saving, low power consumption than RAM
- Flexibility
  - No erase, bit alterable, continuous writing
- Techniques to reduce redundant writes, reduces energy consumption as well as increase system lifetime [1].
- Extended endurance

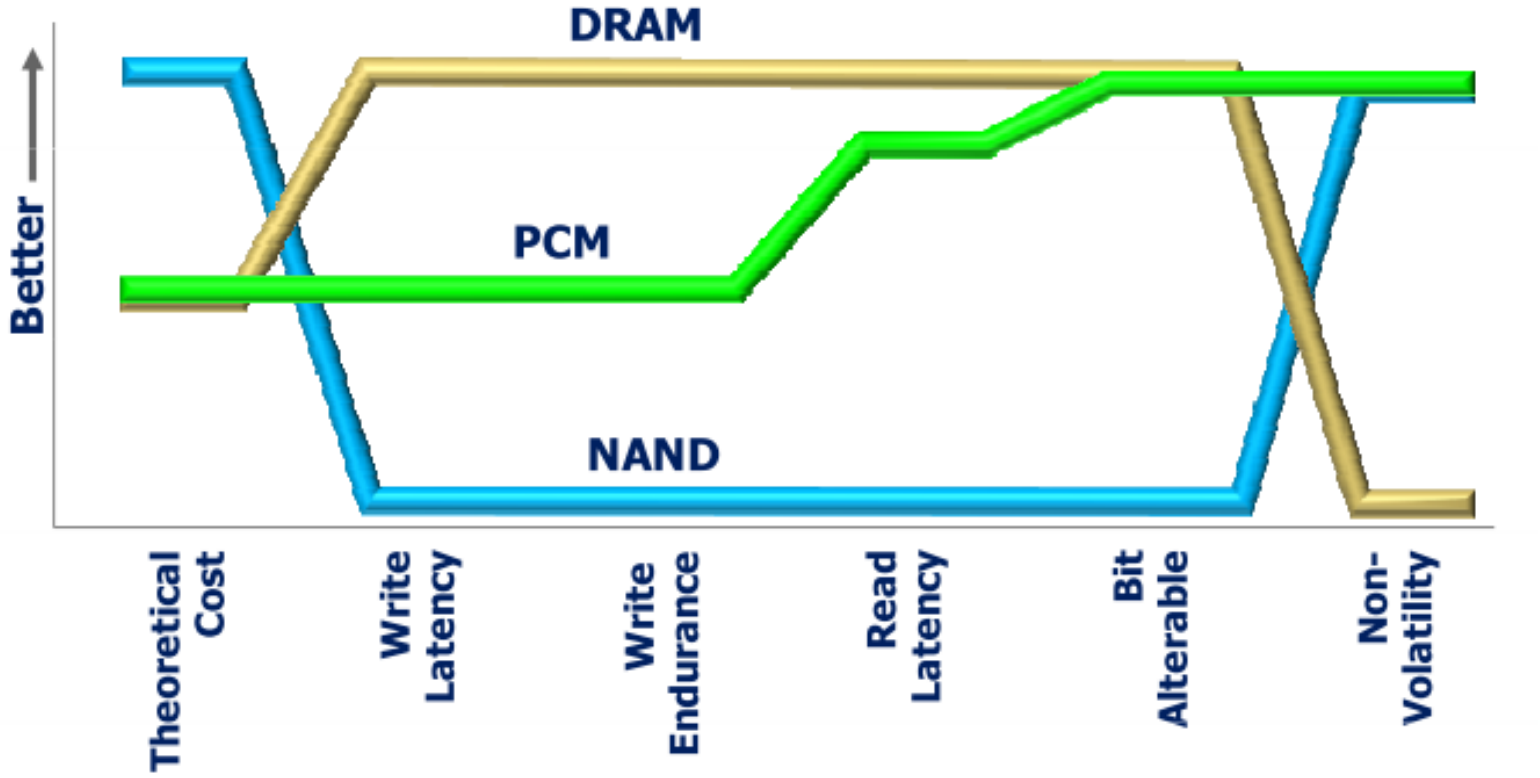
PCM Challenges

- Higher read latency (2x-4x slower than DRAM)
- higher write latency and energy
- limited write endurance

PCM combines components of DRAM and NVM

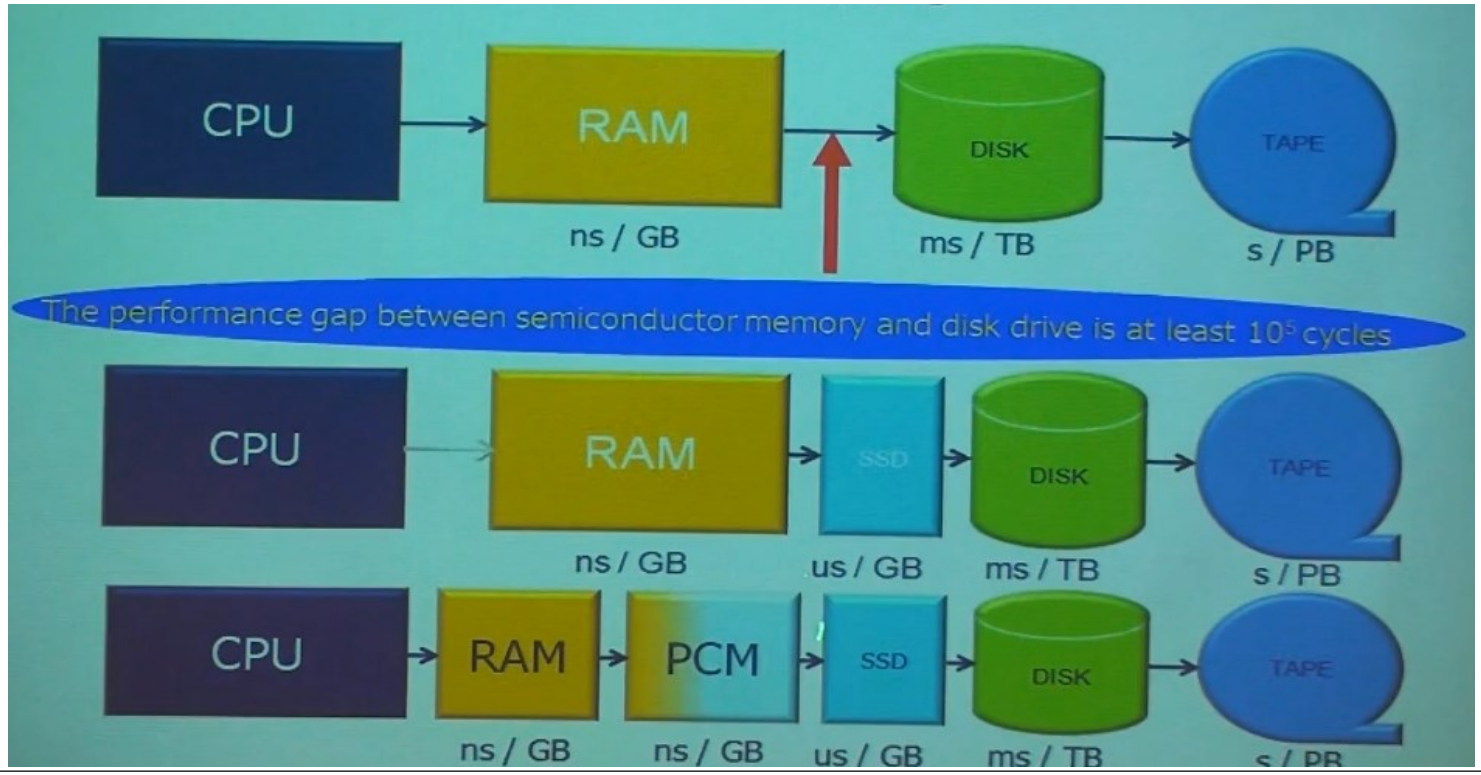
Characteristics

PCM combines the merits of NAND and RAM

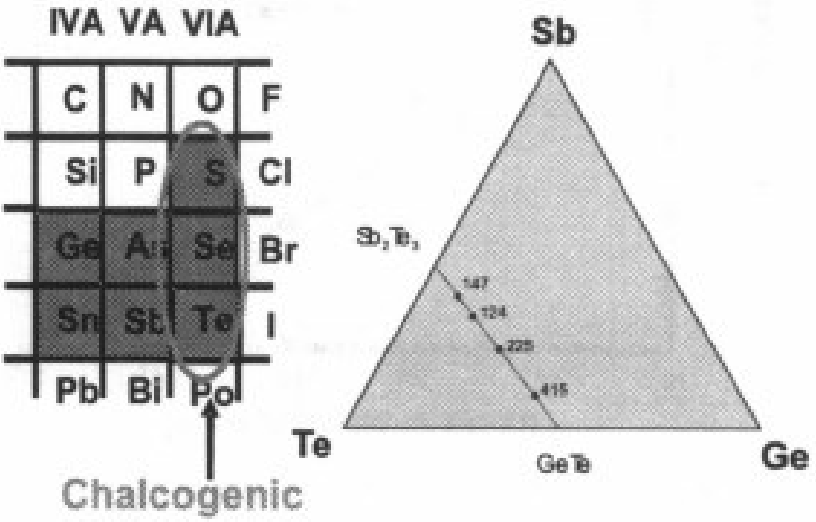


PCM applications

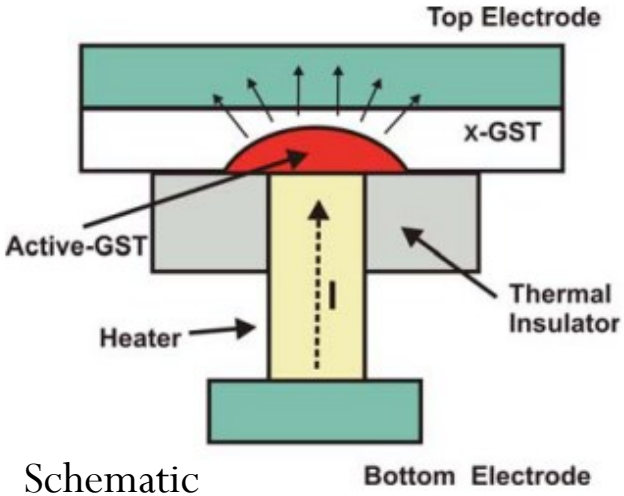
- **Wireless systems** to store XiP, semi-static data and files
  - Direct write memory due to bit alterability
- **Solid state storage** to store frequently accessed pages
  - Caching with PCM will improve performance and reliability
- **Computing platforms** with advantage of non-volatility to reduce power, offers endurance and write latency for a number of new applications



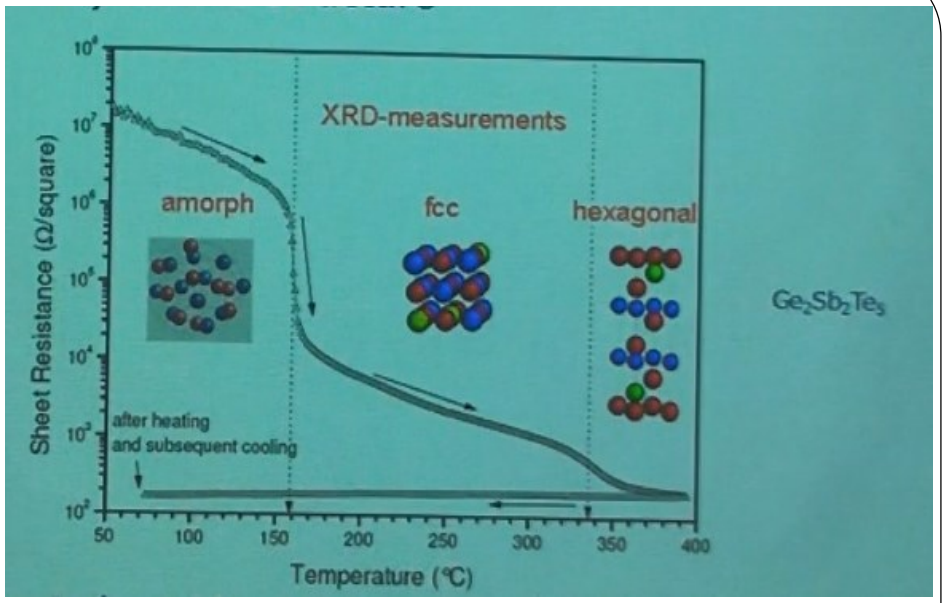
PCM Concept



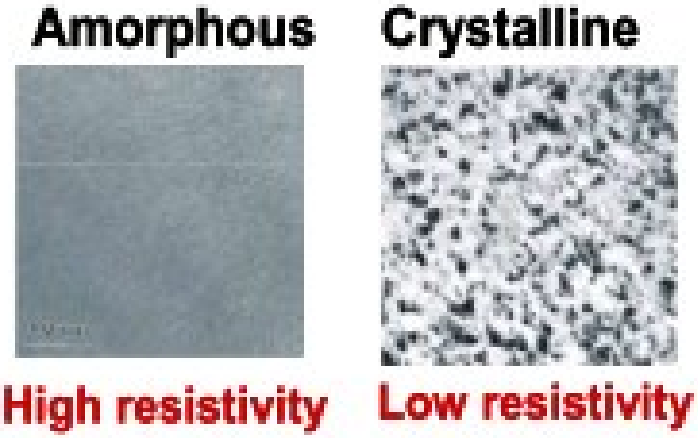
GST Chalcogenide alloys



Schematic



Phase transition



Data storing mechanism

Amorphous or poly-crystalline phases of a chalcogenide alloy, $Ge_2Sb_2Te_5$ (GST)

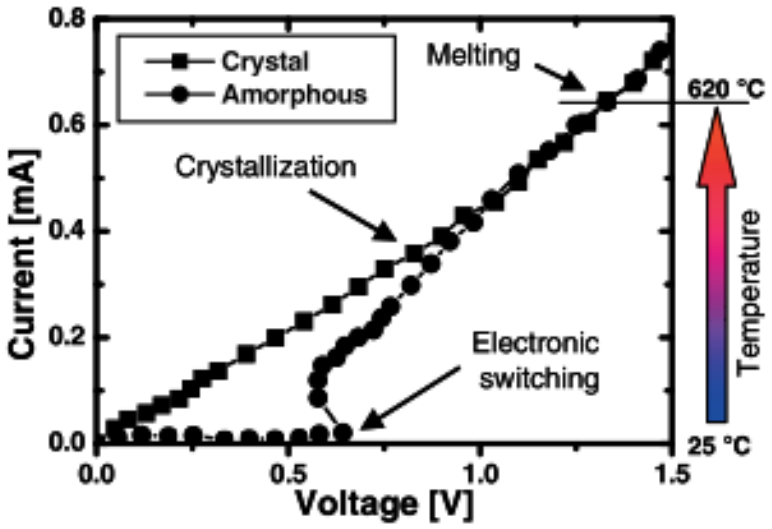
PCM Concept

Reading mechanism

By reading the current we know the state

Amorphous – high resistance -low current- RESET state

Crystalline-low resistance-high current-SET state



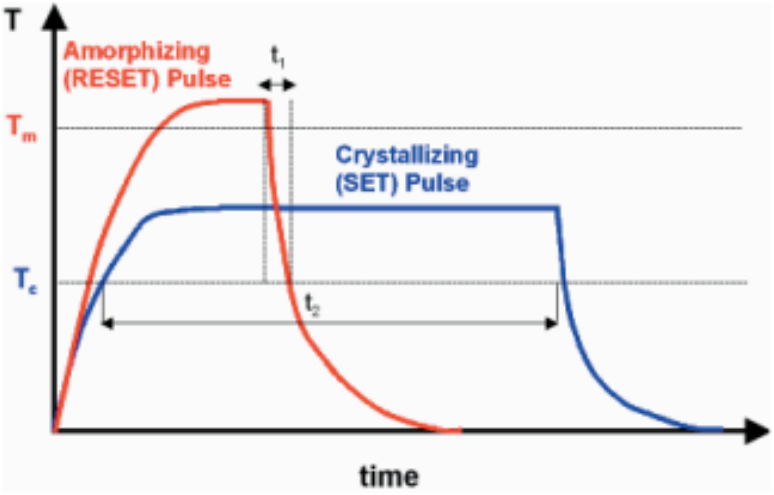
I–V curves of crystalline & amorphous state

Writing mechanism

Joule heating due to current flow

Current pulse t_1 = 50 -100 ns heats up the GST to melting temperature (620 ^{O}C), falling edge of the current pulse, freezes the material into amorphous phase

Current pulse t_2 (100 ns), lower in amplitude (results in temperatures above crystallization temperature), is used for amorphous-to-crystalline transition



Thermal induced phase change of the material

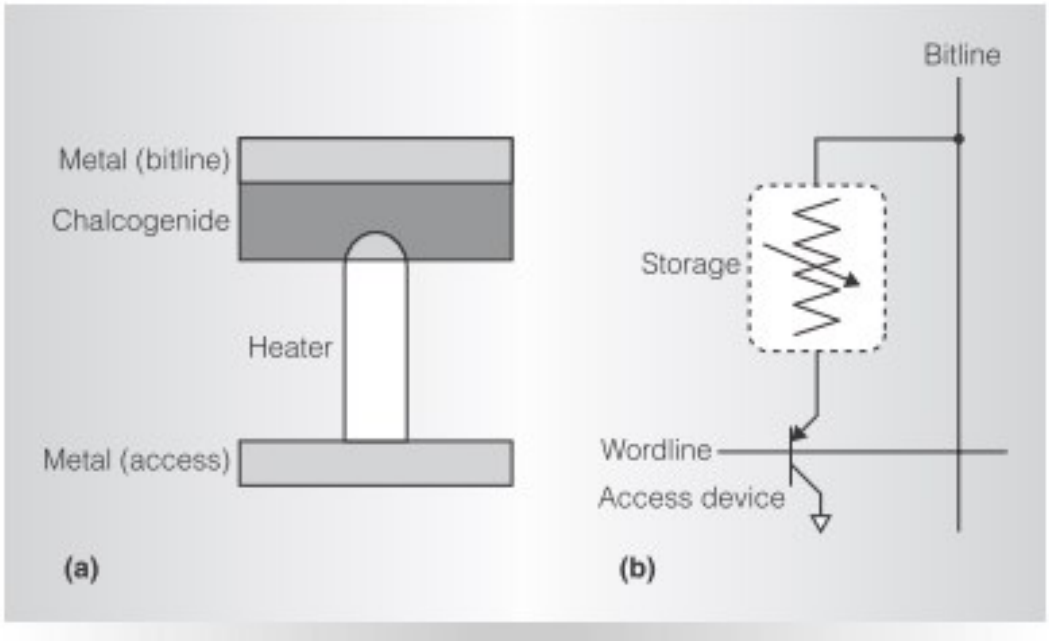
PCM cell - Read and Write

Writes : Access transistor thermally induces phase change by injecting current pulse into the storage medium.

By controlling the chalcogenide states of partial amorphous and partial crystalline it is possible to store multiple resistance level and hence multi level bits operation.

Reads: Bitline is charged to one before the cell is read. For a BJT transistor the word line is active low.

If the cell is in crystalline phase the bitline is discharged through BJT or the cell is in amorphous phase limiting the current through the access device.



(a) PCM cell (b) storage element and bipolar junction transistor [5]

45 nm PCM process flow

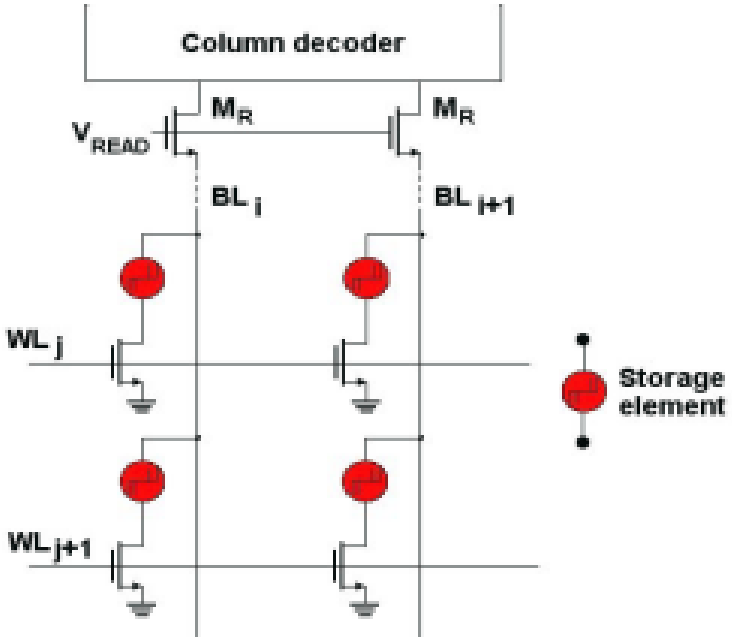
FEOL	Standard CMOS process •Define shallow trench isolation •Wells and gate oxides of LV and HV circuitry BJT array definition CMOS & BJT junction + salicidation
PCM	Wall storage element
BEOL	Cu line1 for array BLs and circuitry Base contact + Cu line2 for array WLs and ckt Final metals and passivation

1 Gbit 45nm PCM product in market

Chip area 37.5mm^2
Power supply range 1.7V, 2.0V
Temperature range -40^O C to +85^O C

Initial access speed 85 ns
Max read throughput 266MB/s
Program throughput 9MB/s

PCM memory



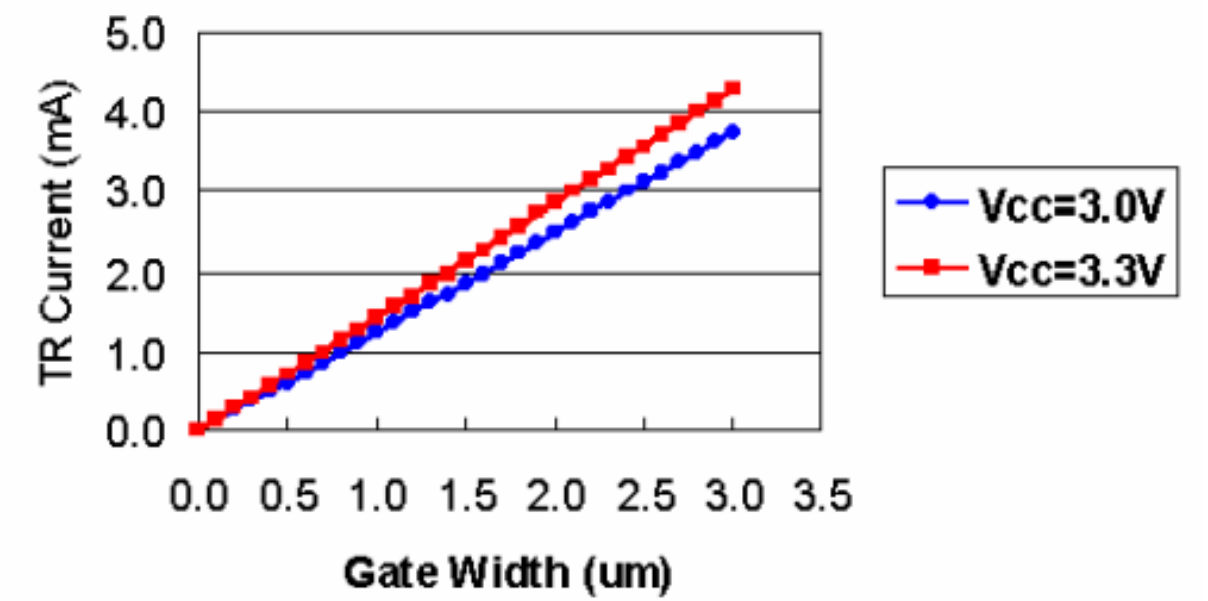
Memory Array [6]

		READ		SET		RESET	
		V(V)	I(μA)	V(V)	I(μA)	V(V)	I(μA)
WL	Sel	1.8	0	3	0	3	0
	No Sel	0	0	0	0	0	0
BL	Sel	0.4	0-80	1.5	300	2.7	600
	No Sel	0	0	0	0	0	0

Voltage and current for selected and unselected cells [7]

Programming Current

- **One of the main problems of PCM is the large programming current**
  - Larger (device width) access transistor → cell area larger
  - Higher power consumption
- **Programming current should scale down with memory cell size (transistor gate width)**



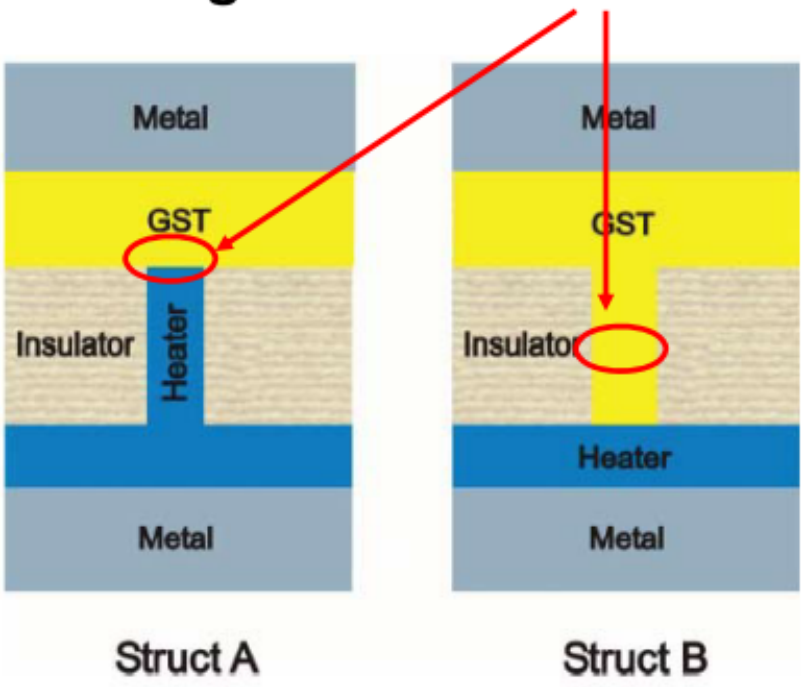
Y. N. Hwang, S. H. Lee, S. J. Ahn, S. Y. Lee, K. C. Ryoo, H. S. Hong, H. C. Koo, F. Yeung, J. H. Oh, H. J. Kim, W. C. Jeong, J. H. Park, H. Horii, Y. H. Ha, J. H. Yi, G. H. Koh, G. T. Jeong, H. S. Jeong, and K. Kim, "Writing current reduction for high-density phase-change RAM," *IEDM Tech. Dig.*, pp. 893 - 896, December 2003.

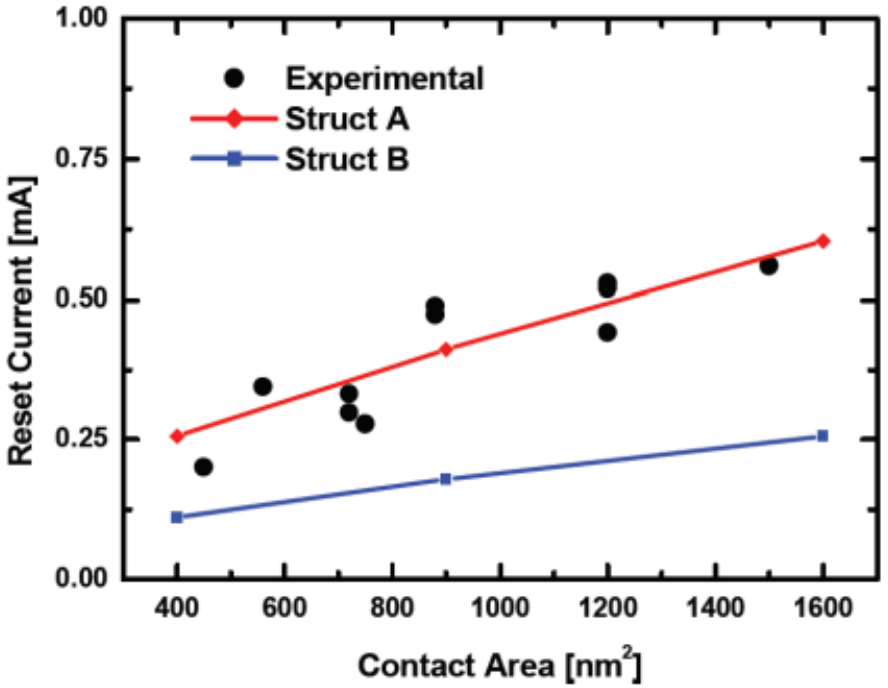
Reset Current Reduction

- **Reducing reset current is one of the most important issues of phase change memory**
  - Reduce contact area (brute force)
  - Engineer the device structure to achieve highest heating for a certain current
  - Engineer the interface thermal and electrical resistance of the GST / electrode interface
  - Engineer the electrical and thermal properties of the phase change material

Thermal Engineering of Cell Structure

- **Engineer the heated area to confine the heat**

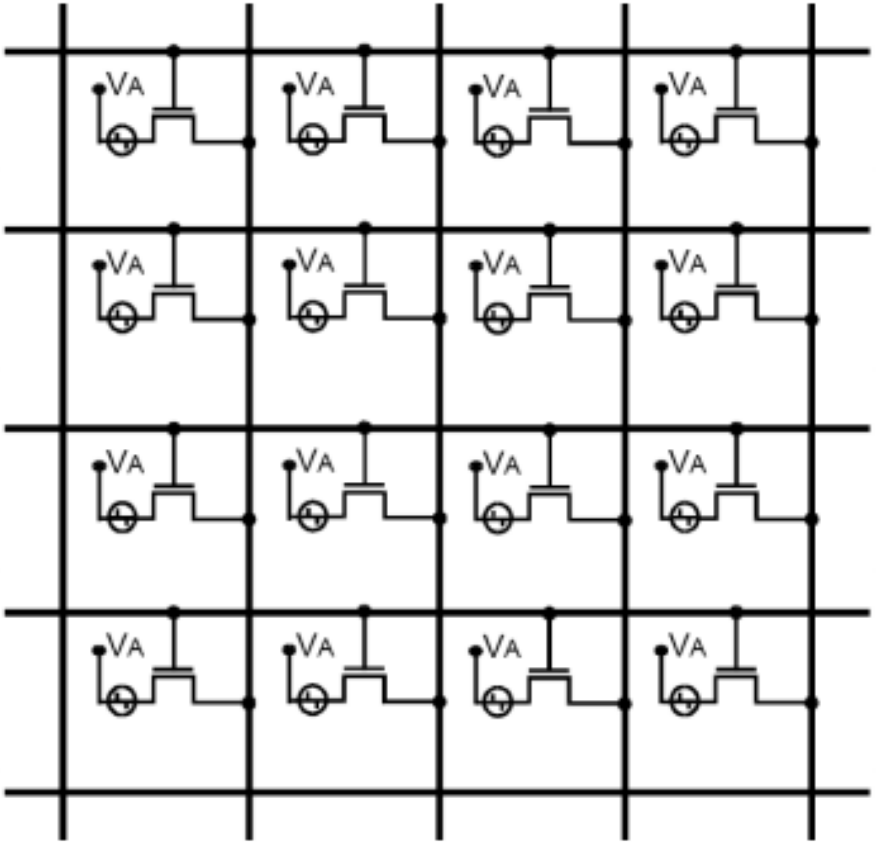




A. Pirovano, A. L. Lacaita, A. Benvenuti, F. Pellizzer, S. Hudgens, and R. Bez, "Scaling analysis of phase-change memory technology," *IEDM Tech. Dig.*, pp. 699 - 702, December 2003.

Array Configurations (FET)

- **Select transistor provides the set/reset current**
- **Because high reset current required (100's of uA), select transistor is larger than minimum width**



S. Lai, "Current status of the phase change memory and its future," *IEDM Tech. Dig.*, pp. 255 - 258, December 2003.

PCM Development Status

Company	Intel	Samsung		STMicroelectronix		IBM/Infineon/ Macronix
Source	ISSCC'02	ISSCC'04	VLSI'05	VLSI'04	VLSI'06	VLSI'06
Technology Node [nm]	180	180	120	180	90	180
Density	4Mb	64Mb	256Mb	4Mb/8Mb	-	-
Cell size [μm^2-F^2]	0.25- 7.7	0.5-16	0.16-16	1.3-40/ 0.32-10	0.097-12	n.a.-n.a.
Material	GST	GST	N-doped GST	GST	GST	N-doped GST
Cell type	Pore	Lance	Ring	µTrench	µTrench	Pore
Selector type	Diode	MOSFET	Tri-MOSFET	MOSFET/BJT	BJT	MOSFET
Current/bit [mA]	1	2	0.6	0.6	0.4	0.9
Operation voltage [V]	3.3	3.0	3.0	3.3	3.0	-
Write time [ns]	100	120	-	150	-	300 (MLC)
Endurance [cycles]]	10^8	-	10^9	10^{11}	10^8	10^6

A. Pirovano, "Emerging Non-Volatile Memories," *IEDM Short Course*, 2006.

What next ?

- Scaling
- Exploring new chalcogenide alloys for new application
- Vertical stacking of more than one memory layer