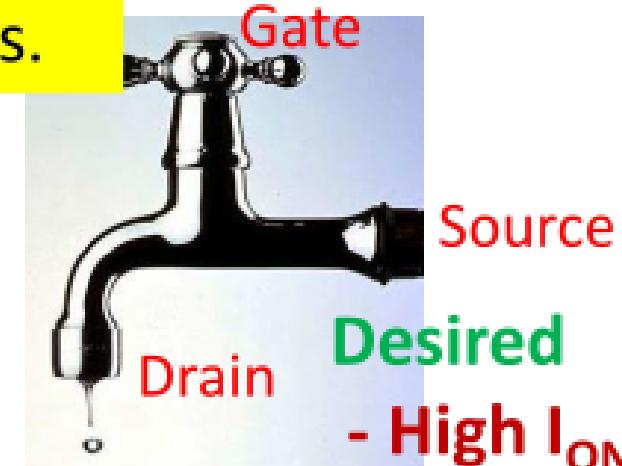
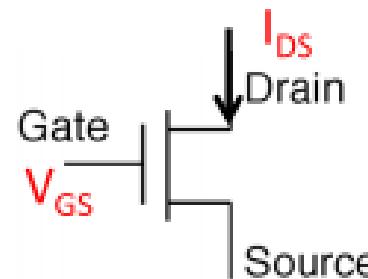
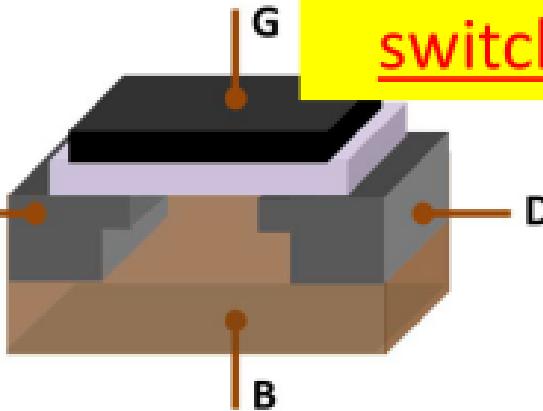


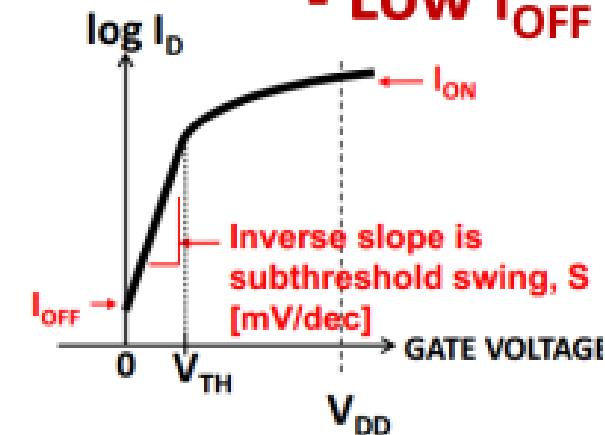
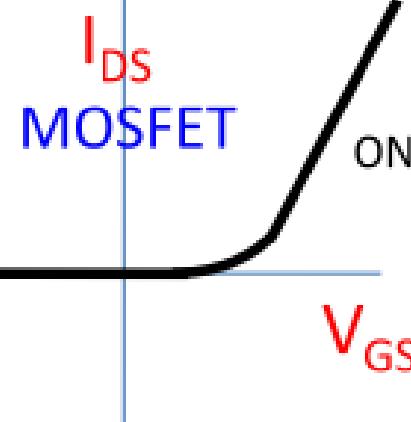
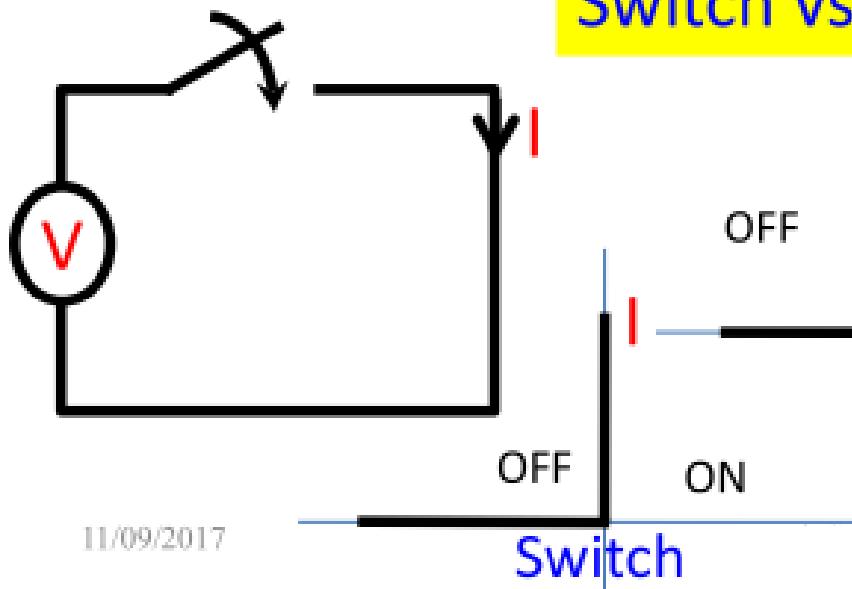
Nano CMOS

Transistor – The Driving Force

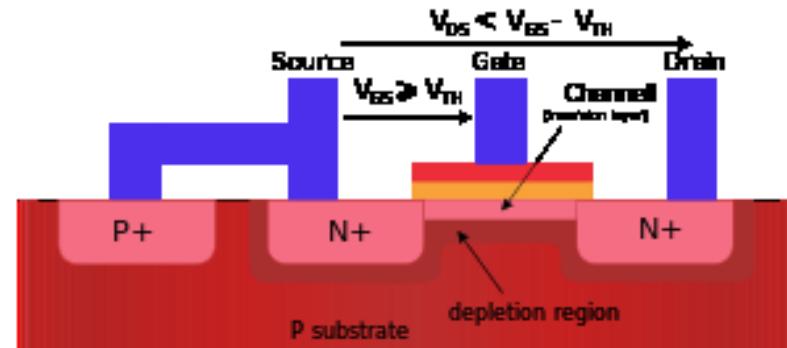
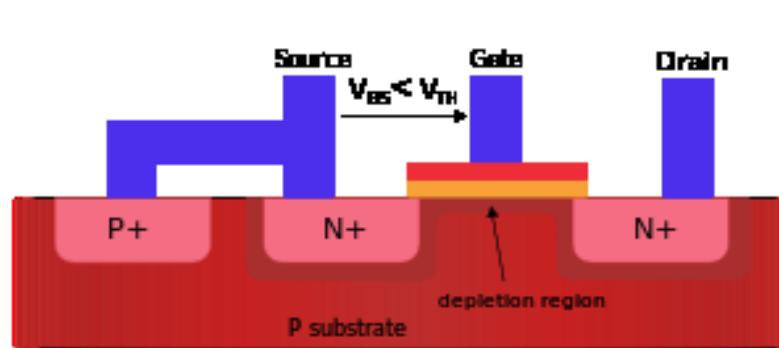
MOSFET is a transistor used for switching electronic signals.



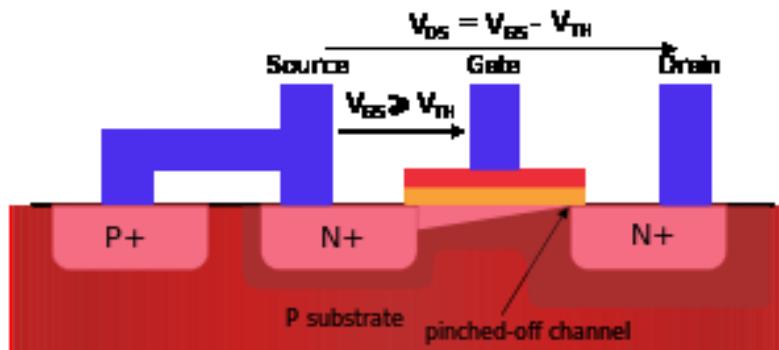
Switch vs. MOSFET



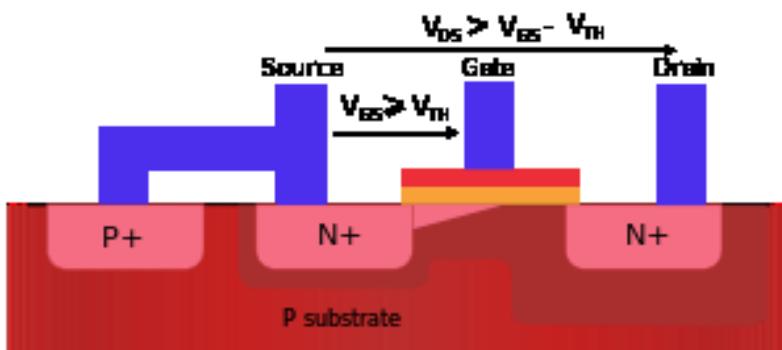
MOSFET



Linear operating region (ohmic mode)



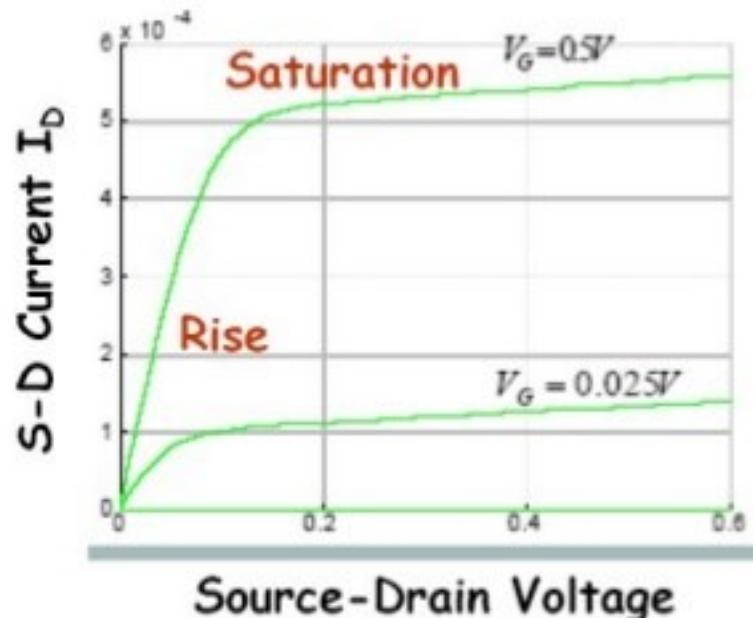
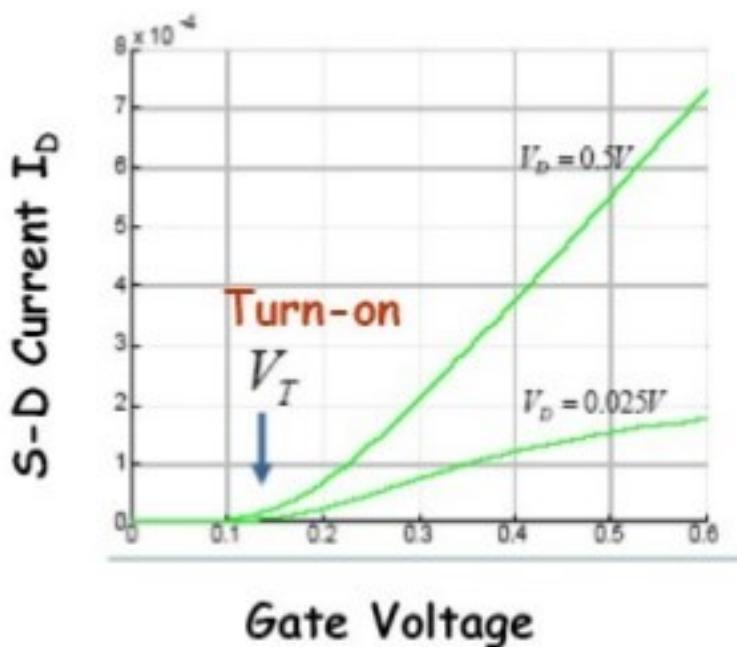
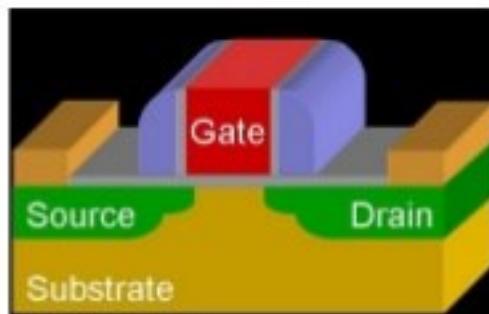
Saturation mode at point of pinch-off

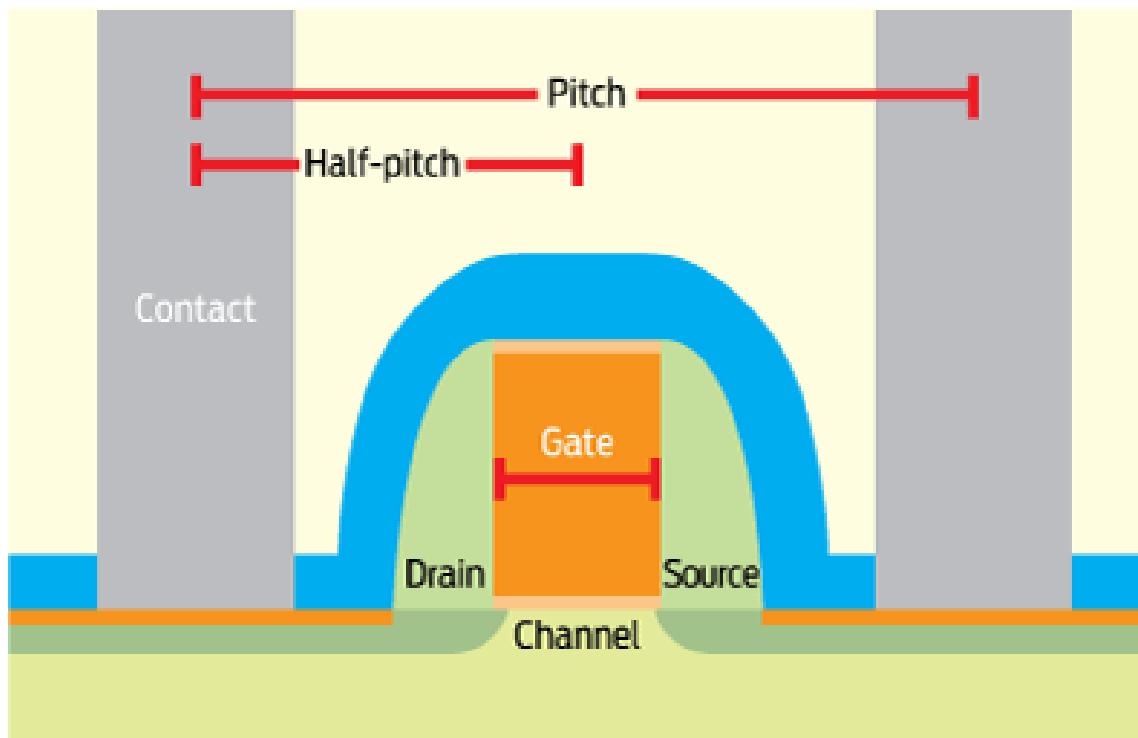


Saturation mode

Ohmic contact to body to ensure no body bias; top left:subthreshold, top right:Ohmic mode, bottom left:Active mode at onset of pinch-off, bottom right: Active mode well into pinch-off – channel length modulation evident

MOSFET I-Vs



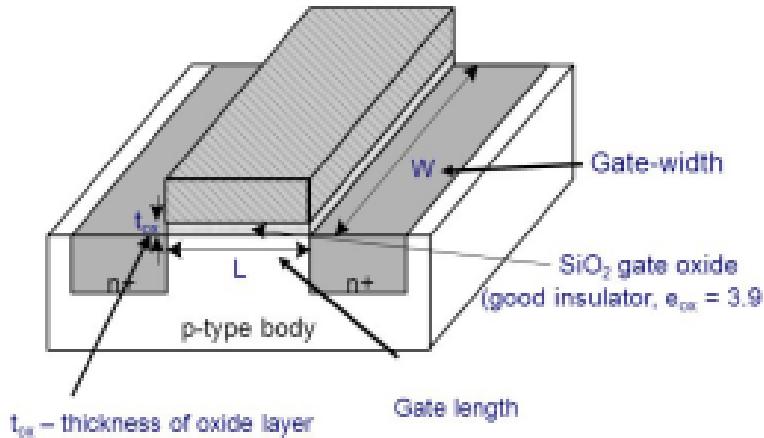


The half-pitch of the first wiring layer is the defining feature for memory chips, while the gate length is the gauge for logic manufacturers.

Bulk MOSFET

- Drain current in MOSFET (ON operation)

$$I_{ON} = \mu \frac{W}{L} C_{ox} (V_{DD} - V_{TH})^2$$



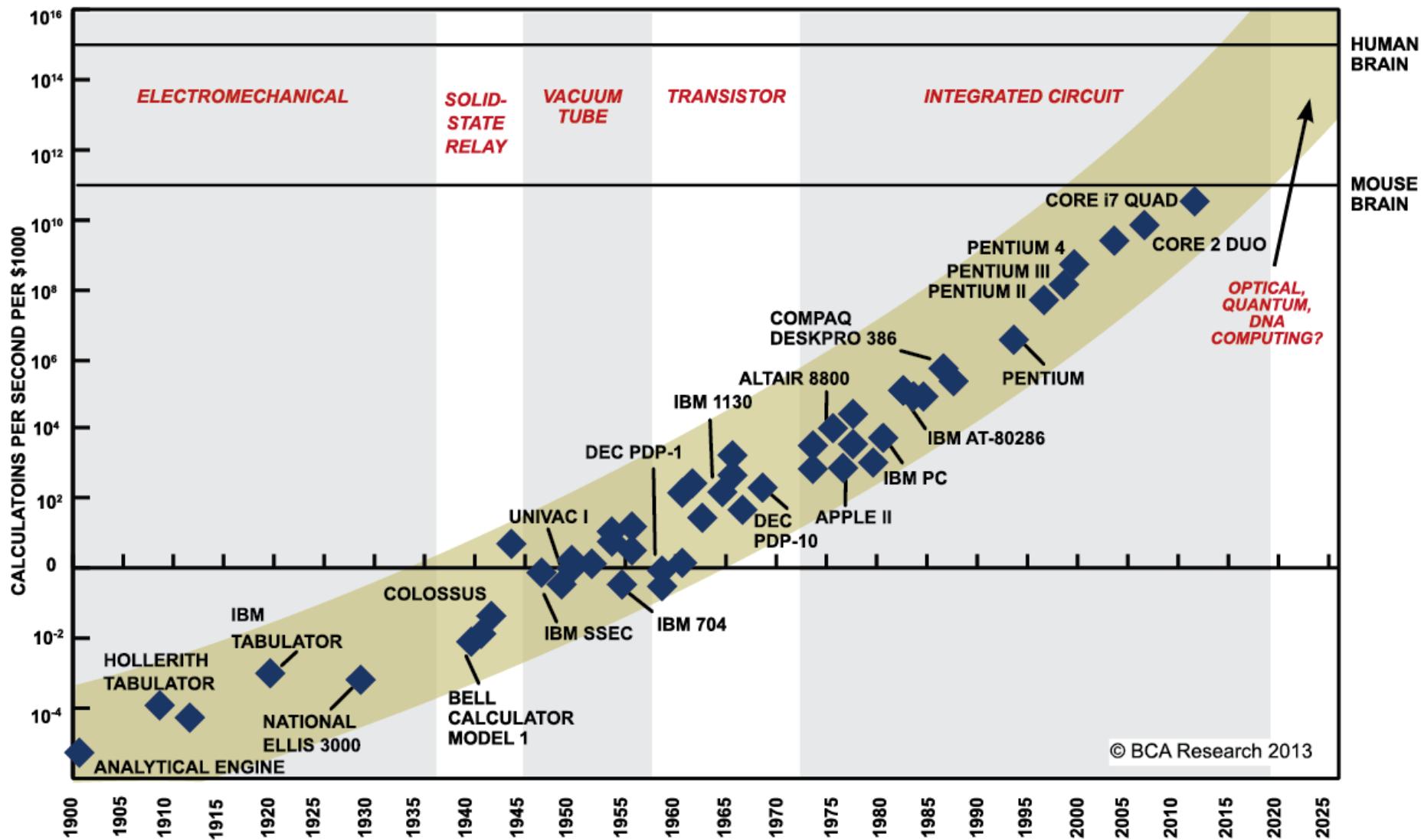
- Drain current in MOSFET (OFF operation)

$$I_{OFF} \propto 10^{\left(\frac{V_{GS}-V_{TH}}{S}\right)}$$

$C_{ox} = \epsilon_{ox}/t_{ox}$ = oxide cap.
S – Subthreshold slope

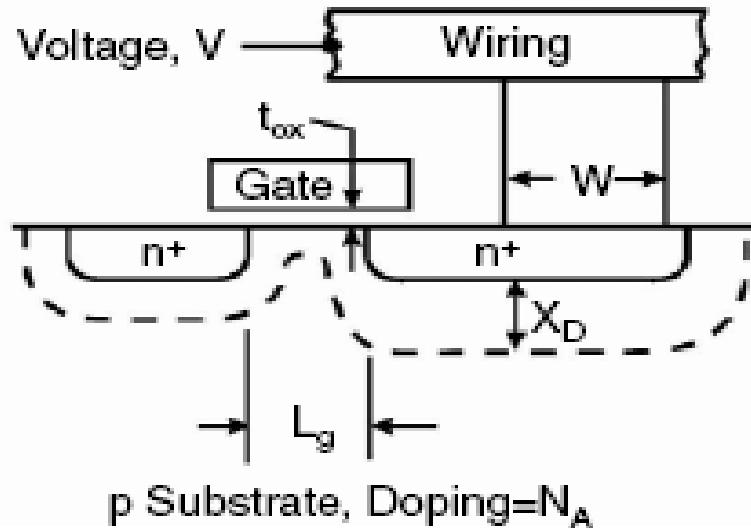
- **High I_{ON}** ($\downarrow L$, $\uparrow C_{ox}$, $\uparrow V_{DD} - V_{TH}$)
- **Low I_{OFF}** ($\uparrow V_{TH}$, $\uparrow S$)

Moores Law

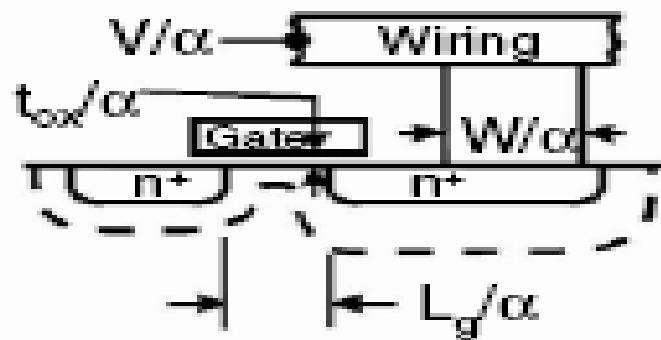


SOURCE: RAY KURZWEIL, "THE SINGULARITY IS NEAR: WHEN HUMANS TRANSCEND BIOLOGY", P.67, THE VIKING PRESS, 2006. DATAPoints BETWEEN 2000 AND 2012 REPRESENT BCA ESTIMATES.

Original Device



Original Device

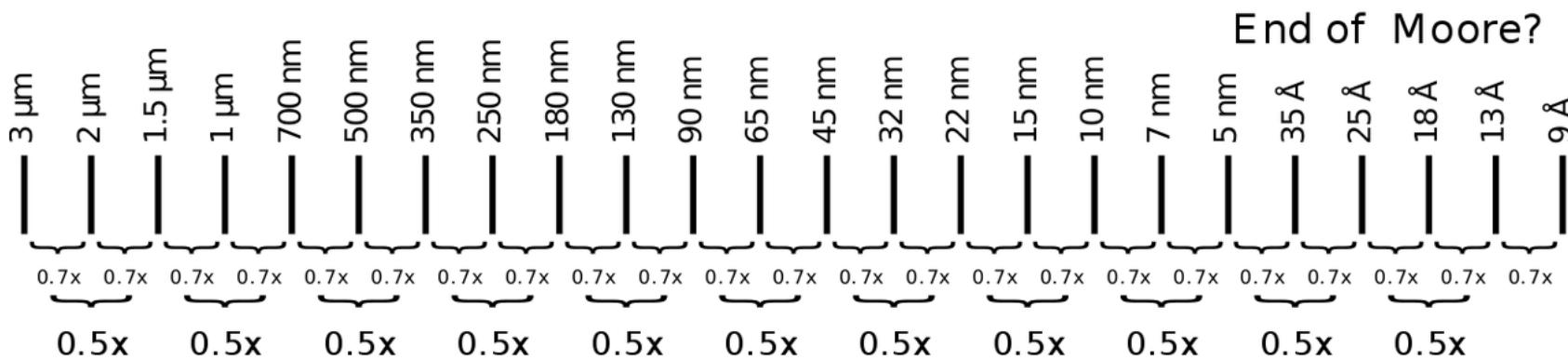
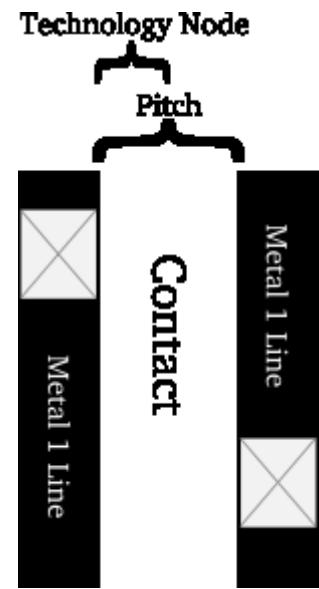


Doping=αN_A

Scaled Device

Technology Scaling

- Scaling – At each new node, all geometrical features are reduced in size to 70% of the previous node.
- Reward – Reduction of *circuit size by half*. (~50% reduction in area, i.e., $0.7 \times 0.7 = 0.49$.)
 - Twice number of circuits on each wafer
 - Cost per circuit is reduced significantly.
- Ultimately – **Scaling drives down the cost of ICs.**



MOS Scaling

Quantity	Sensitivity	Constant Field	Constant Voltage
Scaling Parameters			
Length	L	$1/S$	$1/S$
Width	W	$1/S$	$1/S$
Gate Oxide Thickness	t_{ox}	$1/S$	$1/S$
Supply Voltage	V_{dd}	$1/S$	1
Threshold Voltage	V_{T0}	$1/S$	1
Doping Density	N_A, N_D	S	S^2
Device Characteristics			
Area (A)	WL	$1/S^2$	$1/S^2$
β	W/Lt_{ox}	S	S
D-S Current (I_{DS})	$\beta(V_{dd} - V_T)^2$	$1/S$	S
Gate Capacitance (C_g)	WL/t_{ox}	$1/S$	$1/S$
Transistor On-Resistance (R_{tr})	V_{dd}/I_{DS}	1	S
Intrinsic Gate Delay (τ)	$R_{tr}C_g$	$1/S$	$1/S$
Clock Frequency	f	f	f
Power Dissipation (P)	$I_{DS}V_{dd}$	$1/S^2$	S
Power Dissipation Density (P/A)	P/A	1	S^3

ITRS Projections

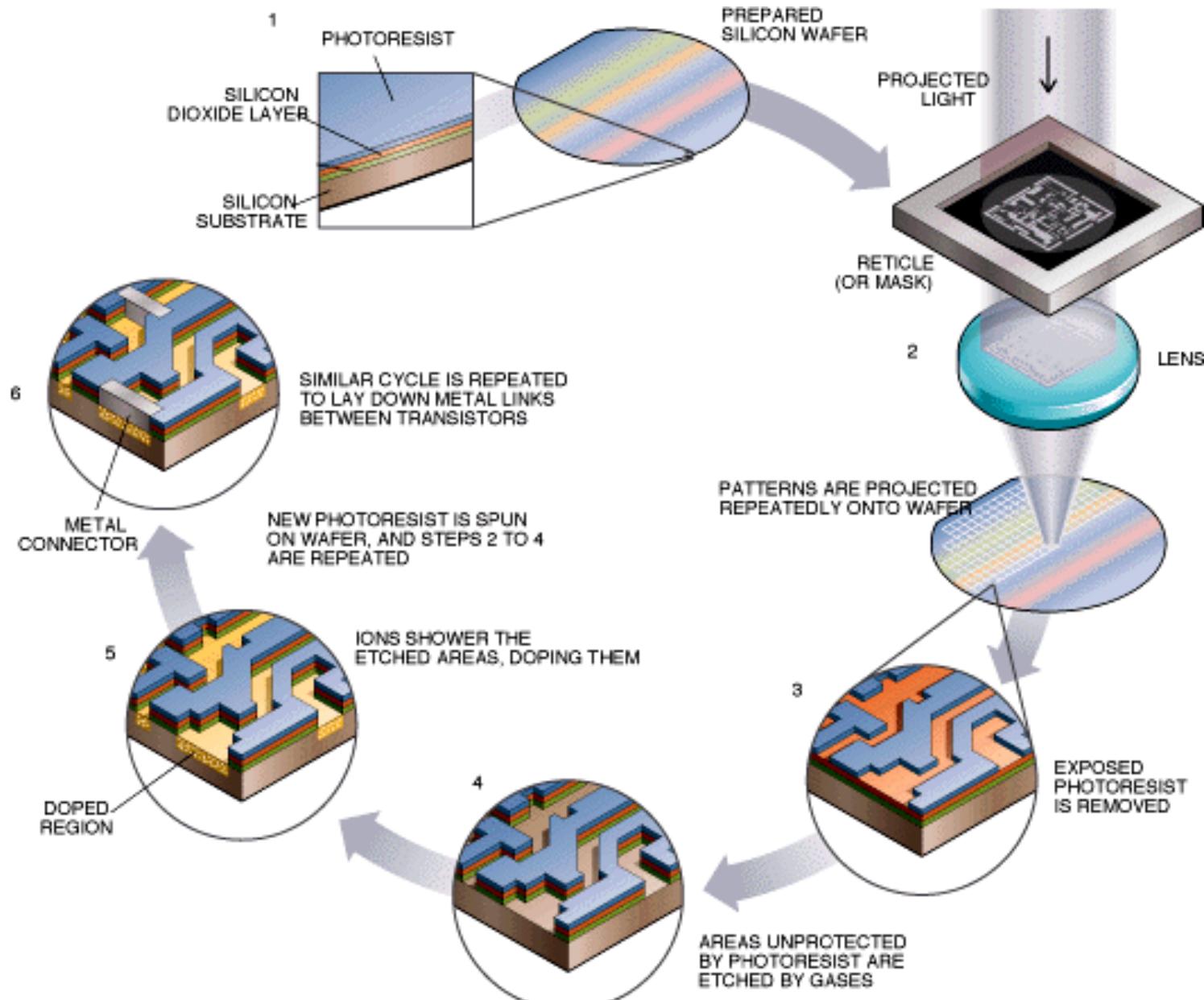
Year of Production	2013	2016	2019	2022	2025
Technology Node (nm) (DRAM Half pitch)	28	20	14.2	10	7.1
Transistor Gate Length in Micropocessors circuits (nm)	20	15.3	11.7	8.9	6.6
Wafer diameter (inch)	12	18	18	18	18
Transistors density in Micropocessor (billion / cm ²)	1.59	3.19	6.38	12.77	25.54
Number of interconnect wiring levels in the Microprocessor	12	13	14	15	16
Operating voltage (V)	0.85	0.77	0.71	0.64	0.59



2013 ITRS

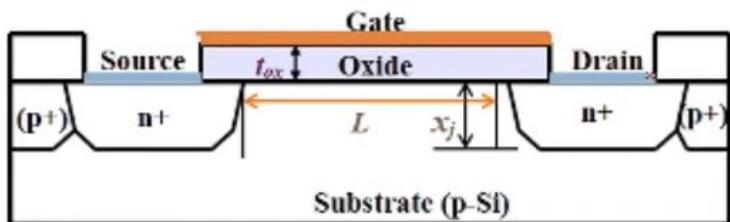
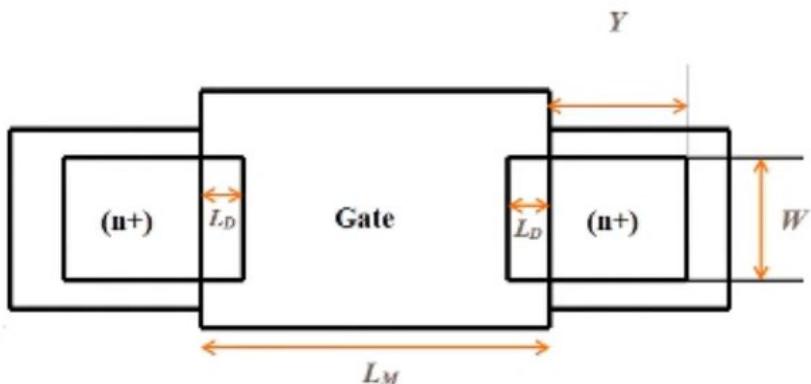
1. System Drivers
2. Design
3. Test & Test Equipment
4. Process Integration, Devices, & Structures
5. RF and A/MS Technologies
6. Emerging Research Devices
7. Emerging Research Materials
8. Front End Processes
9. Lithography
10. Interconnect Interconnect
11. Factory Integration
12. Assembly & Packaging
13. Environment, Safety, & Health
14. Yield Enhancement
15. Metrology
16. Modeling & Simulation
17. MEMs

IC fabrication process



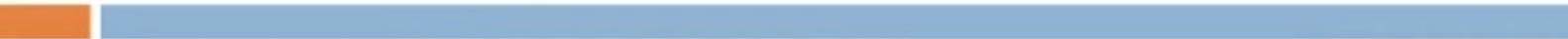
Short Channel Effects in MOSFET

MOSFET Transistor Dimensions



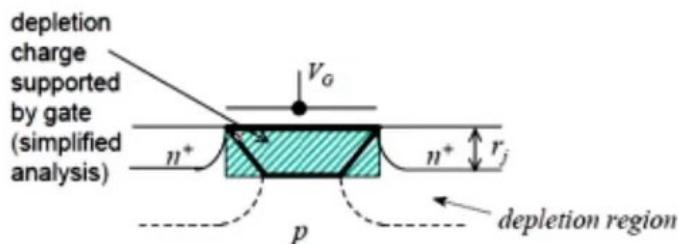
- L_M : mask length of the gate
- L : actual channel length
- L_D : gate-drain overlap
- Y : typical diffusion length
- W : length of the source and drain diffusion region

Various Scaling Issues

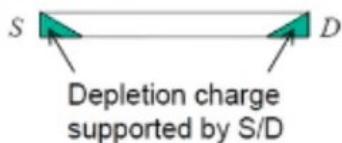


- Charge sharing
- Drain Induced Barrier Lowering
- Punchthrough
- Mobility Degradation
- Velocity Saturation
- Hot Electron Effect

Charge Sharing



Large L:



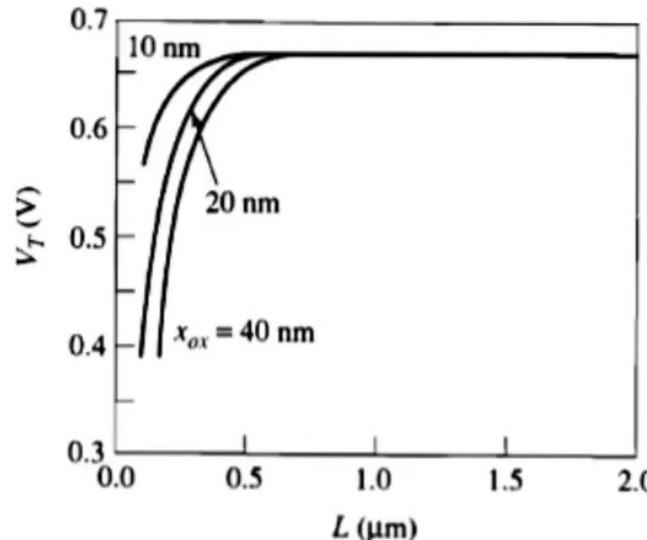
Small L:



- The smaller the L , the greater percentage of charge balanced by the S/D PN junctions
- At the source and drain ends of the channel, channel depletion region charge is actually depletion charge for the source and drain

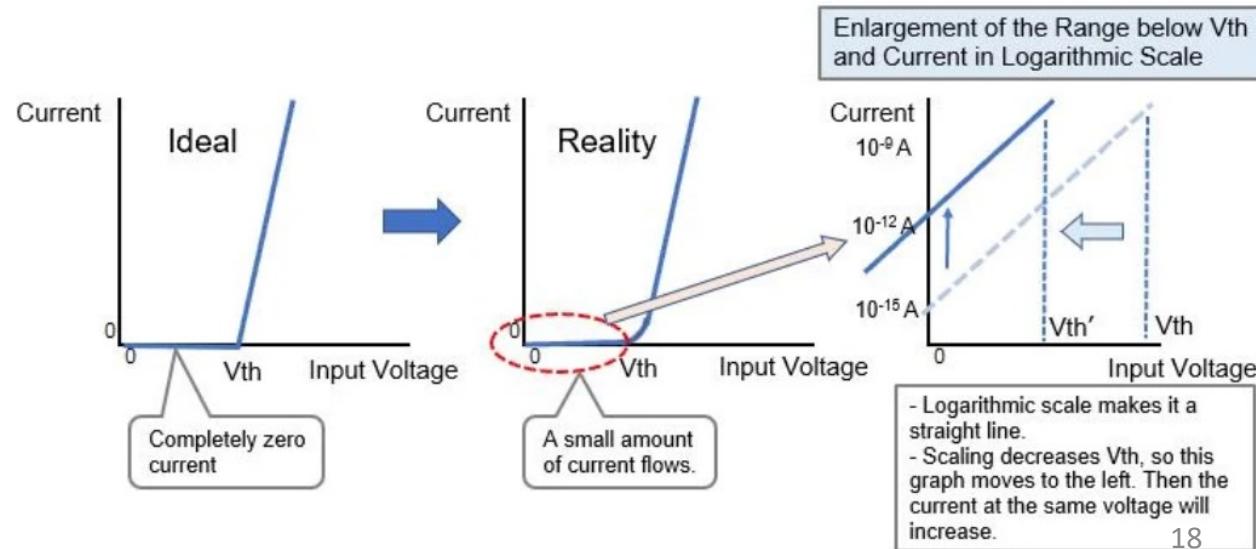
Charge Sharing

- Reduces the magnitude of V_T needed for inversion.
- Effect is more serious with thick gate oxides.
- Make thin oxides for avoiding this problem



Leakage Current?

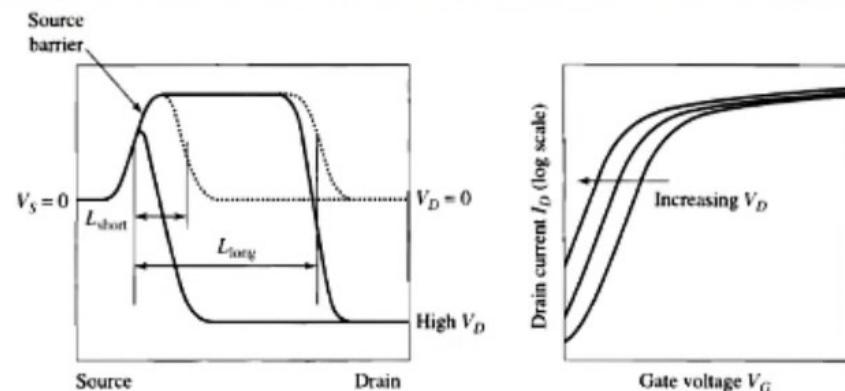
The MOS transistor tries to reduce the current rapidly when the input voltage falls below the threshold voltage (V_{th}), but when the threshold voltage (V_{th}) is reduced by scaling and gets closer to 0 V, the current cannot be decreased completely even when the input voltage reaches 0 V.



Drain induced barrier lowering

For long-channel devices, the source-channel potential barrier is determined primarily by the voltage applied to the gate.

As the source & drain get closer, they become electrostatically coupled, so that the drain bias can affect the potential barrier to carrier flow at the source junction



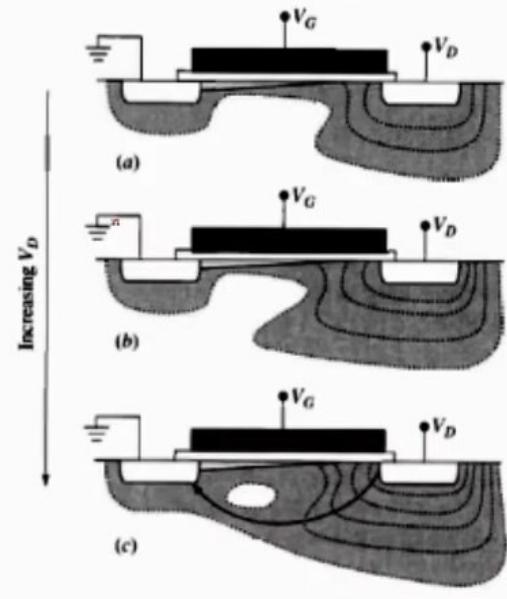
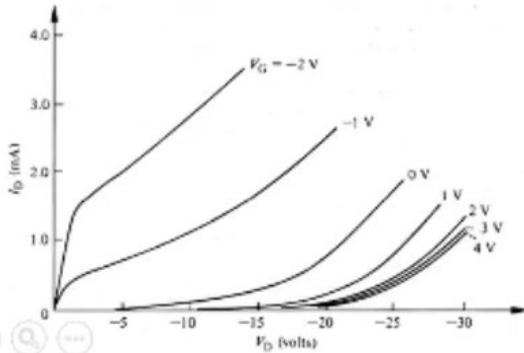
Allows electron flow between S and D even at $V_{GS} < V_{TO}$

Punchthrough

Merging of depletion regions of the source and drain

In short-channel n-channel MOSFETs, the surface p-region is more heavily doped than the bulk, making the junction-depletion region wider below the surface than in the channel region.

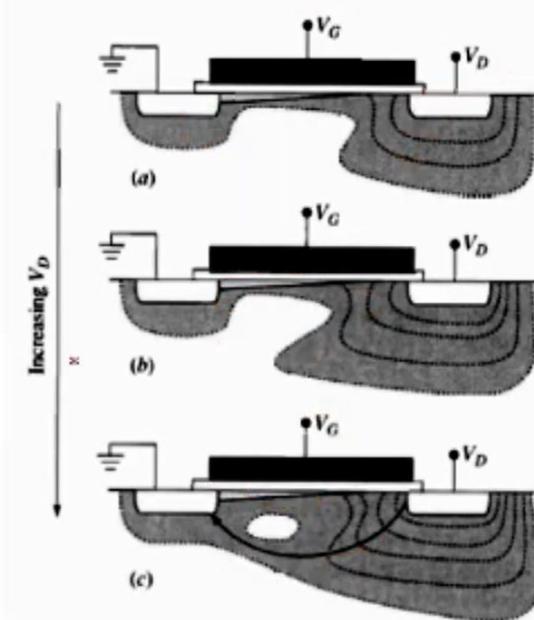
It is possible for the drain-substrate depletion region to reach the source-substrate depletion region at a sufficiently high drain bias



Punchthrough

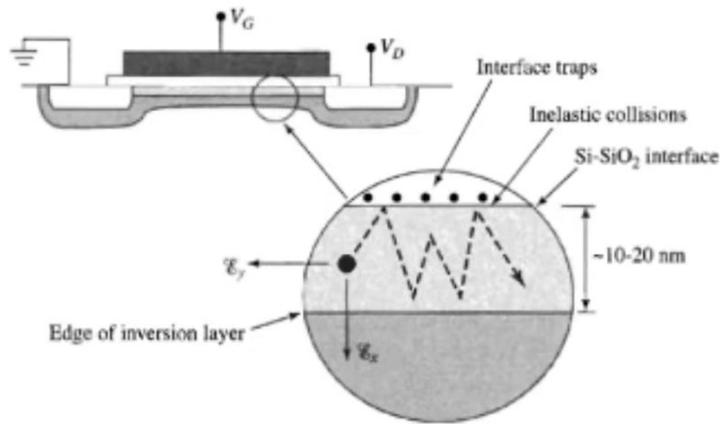
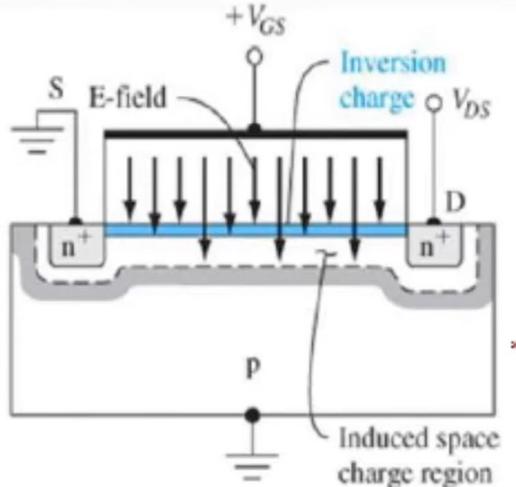
General “Cure” – high dose implant in substrate region to make narrower depletion widths

Higher substrate doping increases parasitic capacitances



Mobility Degradation

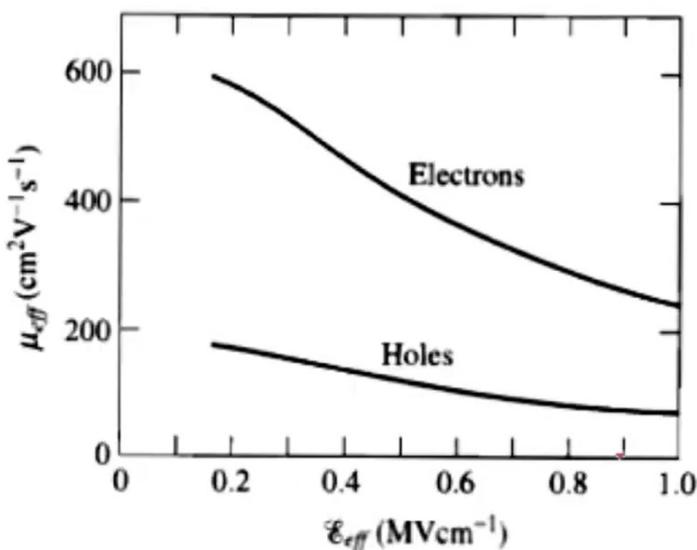
- Due to short channel effects, vertical electric field increases and mobility becomes field dependent.
- Surface scattering occurs.
- Average surface mobility decreases.



- Mobility degrades as gate oxide is thinner

Mobility = velocity / electric field

Mobility Degradation



$$\mu_{eff} = \frac{\mu_0}{1 + (\epsilon_{eff}/\epsilon_0)^\nu}$$

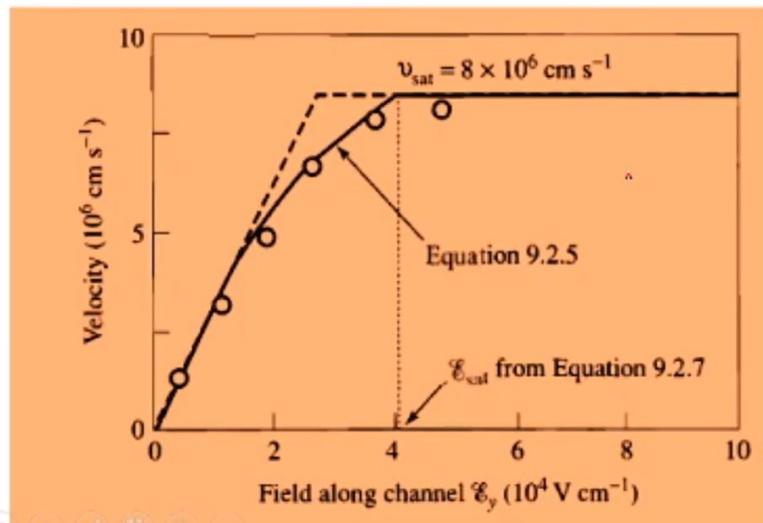
TABLE 9.3 Parameters for effective mobility
© 1986 IEEE [13]

	Unit	Electron (surface)	Hole (surface)	Hole (subsurface)
μ_0	$\text{cm}^2/\text{V}\cdot\text{s}$	670	160	290
ϵ_0	MV/cm	0.67	0.7	0.35
ν		1.6	1.0	1.0

If the mobility is reduced then the drain current is also reduced

Velocity saturation

Drift velocity of carriers in a semiconductor does not continue to increase linearly with electric field at higher fields. On the contrary, the velocity, plotted as a function of field, starts to level off, and finally saturates at a value v_{sat} .



$$v = \frac{\mu_{eff} \mathcal{E}}{(1 + \mathcal{E}/\mathcal{E}_{sat})} \quad \mathcal{E} < \mathcal{E}_{sat} \quad (9.2.5)$$

$$\mathcal{E}_{sat} = \frac{2v_{sat}}{\mu_{eff}} \quad (9.2.7)$$

If the velocity saturates then the current also saturates.

Hot Electron Effect

High electric fields in both the channel and pinch-off region for short channel lengths occur for small L .

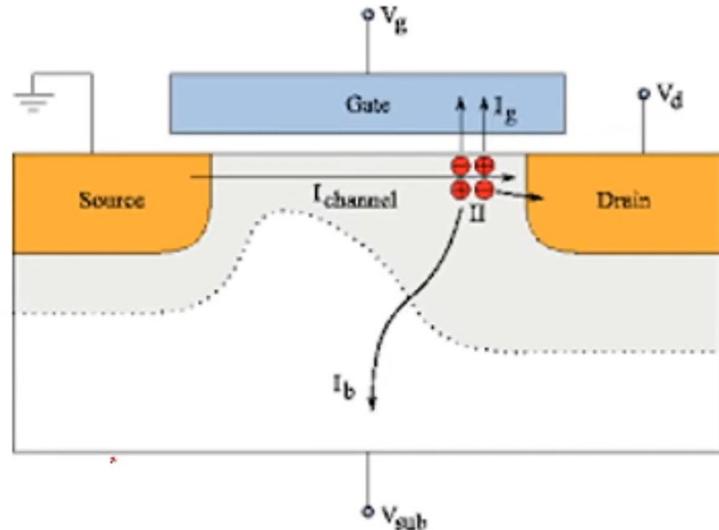
High electric fields accelerate electrons which have sufficient energy with the accompanying vertical field to be injected into the oxide (**Oxide Charging**) and are trapped in defect sites or contribute to interface states.

These are called **hot electrons**.

Resulting trapped charge increases V_T and otherwise affects transconductance, reducing the drain current.

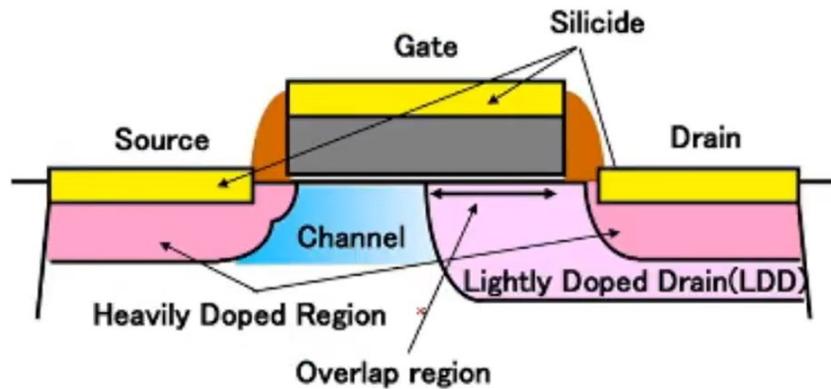
Effect further aggravated by **impact ionization**.

$$E = V/L$$

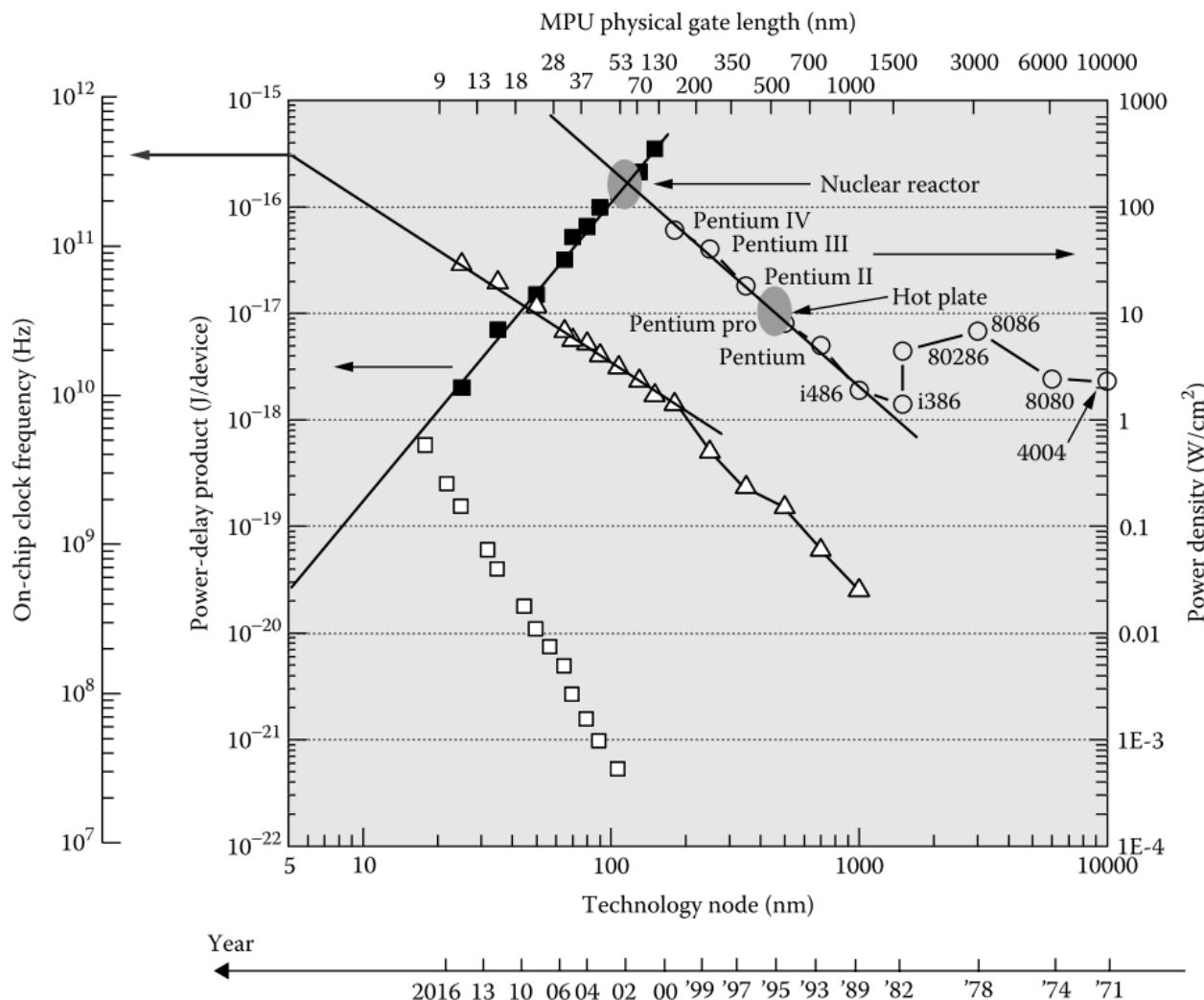


Hot Electron Effect

Reduced N gradient – smaller electric field near drain – fewer “hot” electrons into oxide

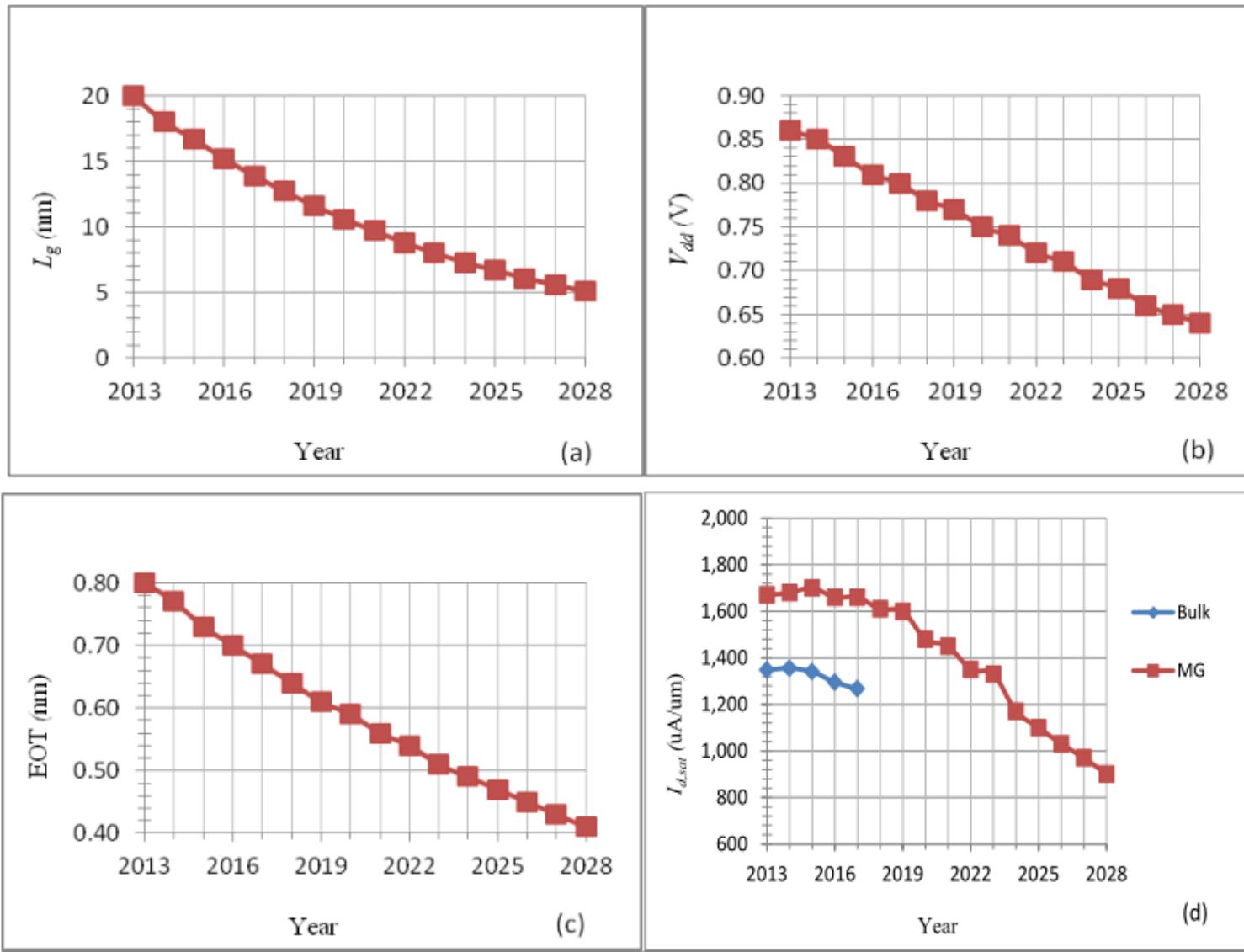


n⁻ to avoid large fields and hot electrons, n⁺ to get Ohmic contacts (still need to avoid punch-through)



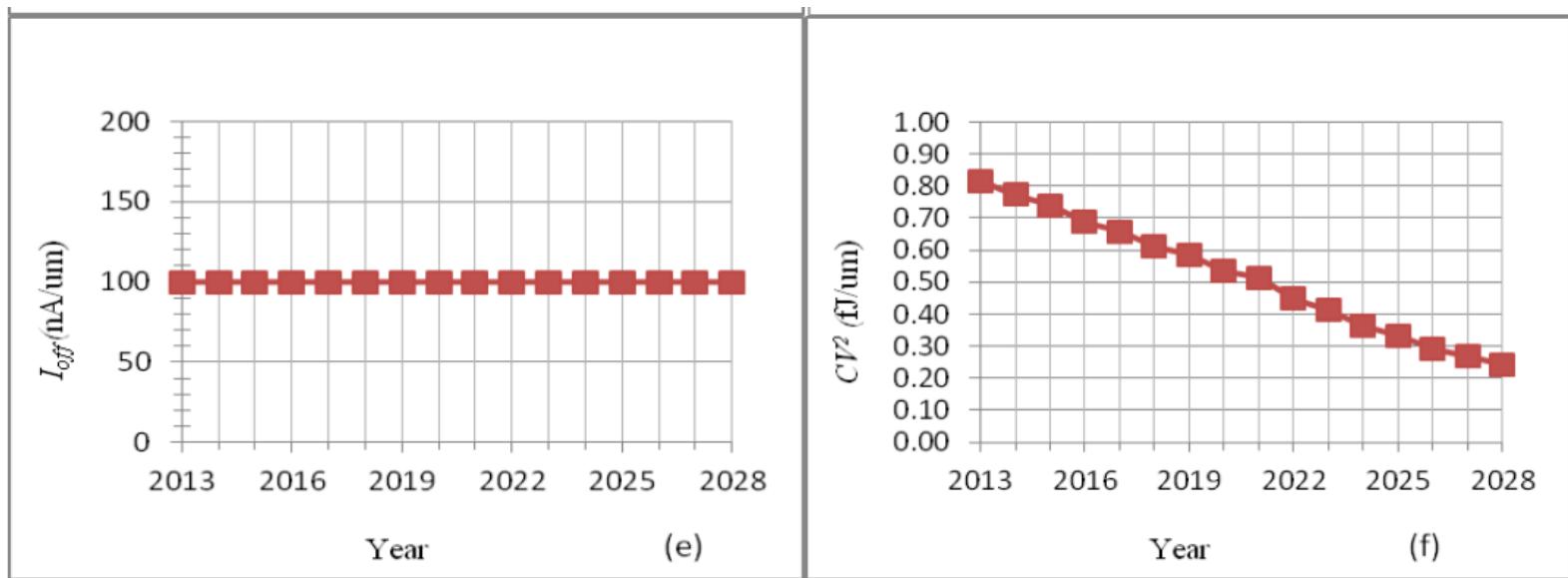
Power dissipation as a function of generation node. Power density on the surface of current and past microprocessor generations (*open circles*), on-chip clock frequency (*open triangles*), power-delay products for a single device (*solid squares*), estimated power density for the basic switch with linear driving function (*open squares*). (From Strukov, D.B. and K.K. Likharev, *Nanotechnology*, 2005, 16(1):137–148; Coey, J.M.D. and M. Venkatesan, *J Appl Phys*, 2002, 91(10):8345–8350; Unsal, O.S. and I. Koren, *Proc IEEE*, 2003, 91(7):1055–1069. With permission.)

Scaling Trend of Logic HP Transistors.

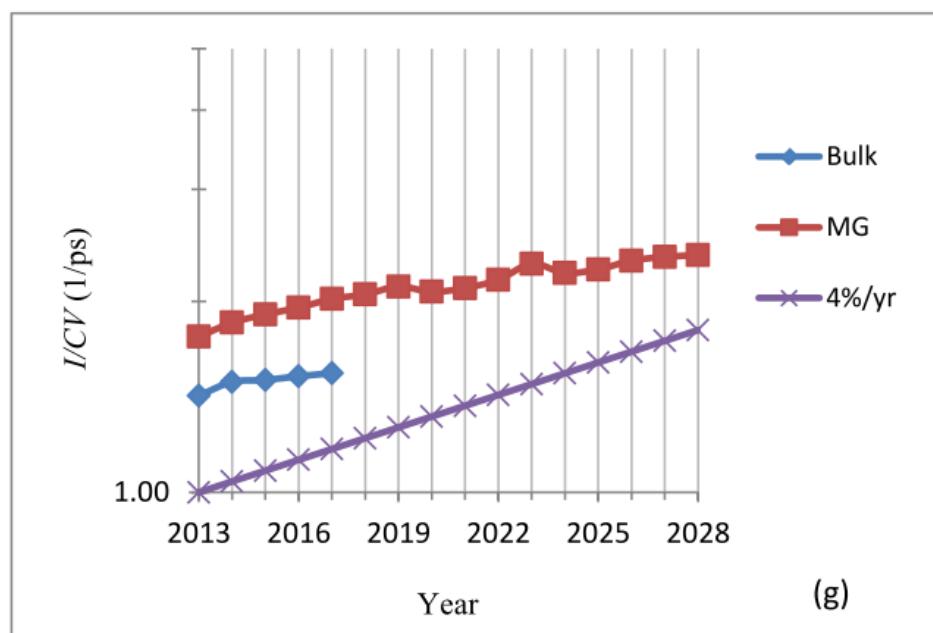


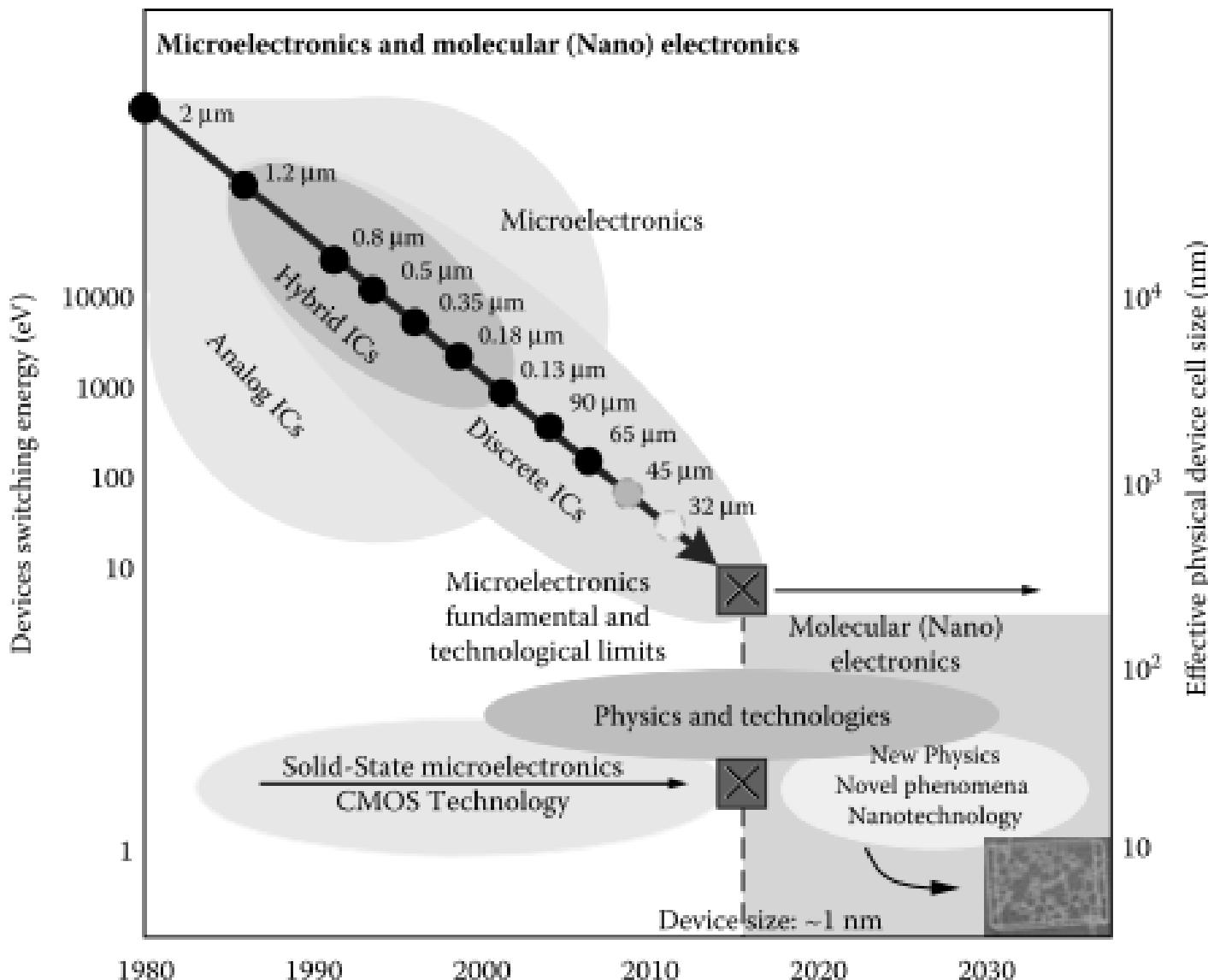
(a) Gate length, (b) Supply voltage, (c) EOT, (d) On-current

Scaling Trend of Logic HP Transistors



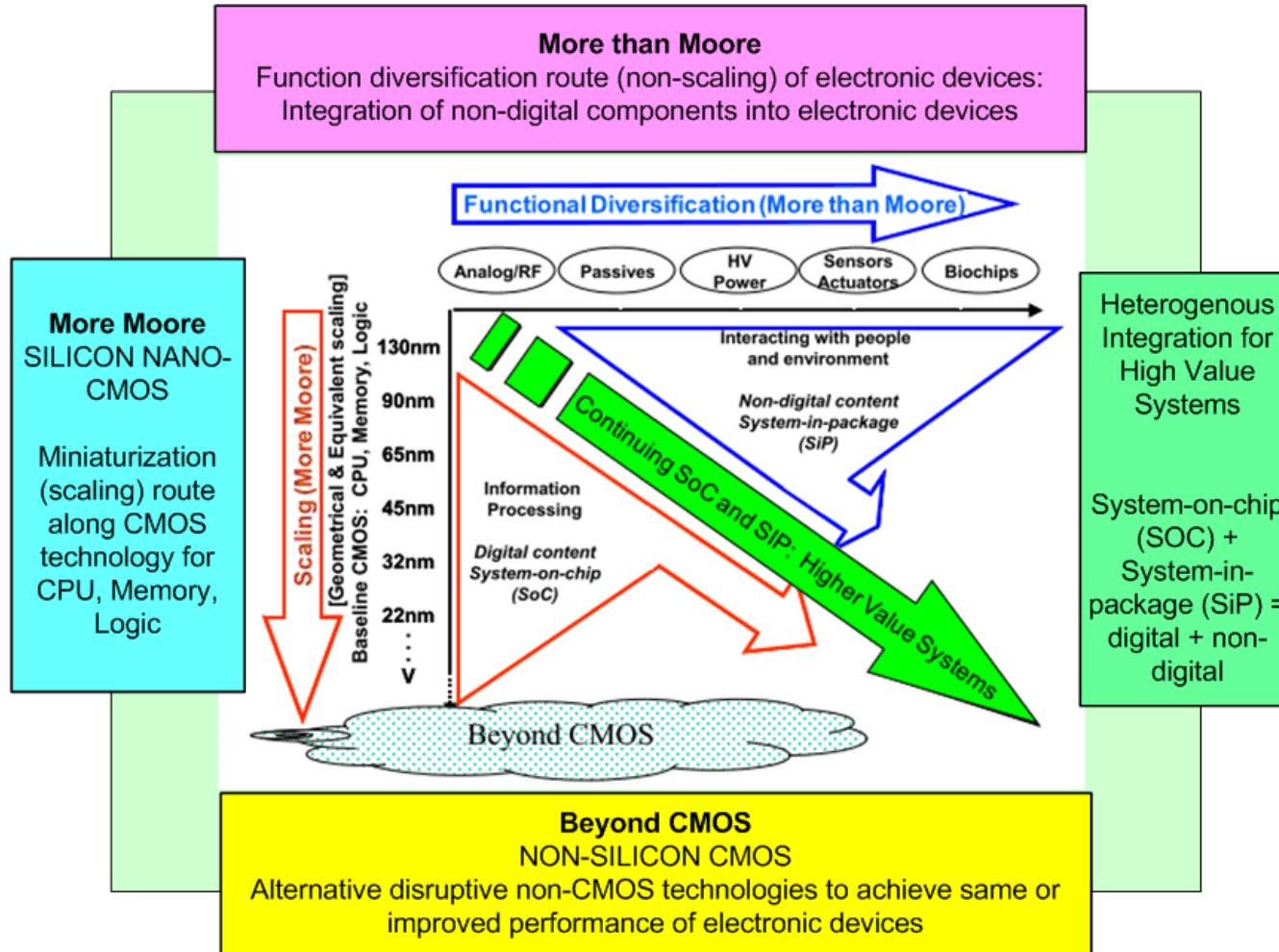
(e) Off-current I_{off} , (f)
Dynamic power CV^2 , and
(g) Intrinsic speed (I/CV)





Envisioned molecular (nano) electronics advancements and microelectronics trends.

Future of microelectronics and nanoelectronics



Nanoelectronics Technology Development Paths .

A Taxonomy for Nano Information Processing Technologies

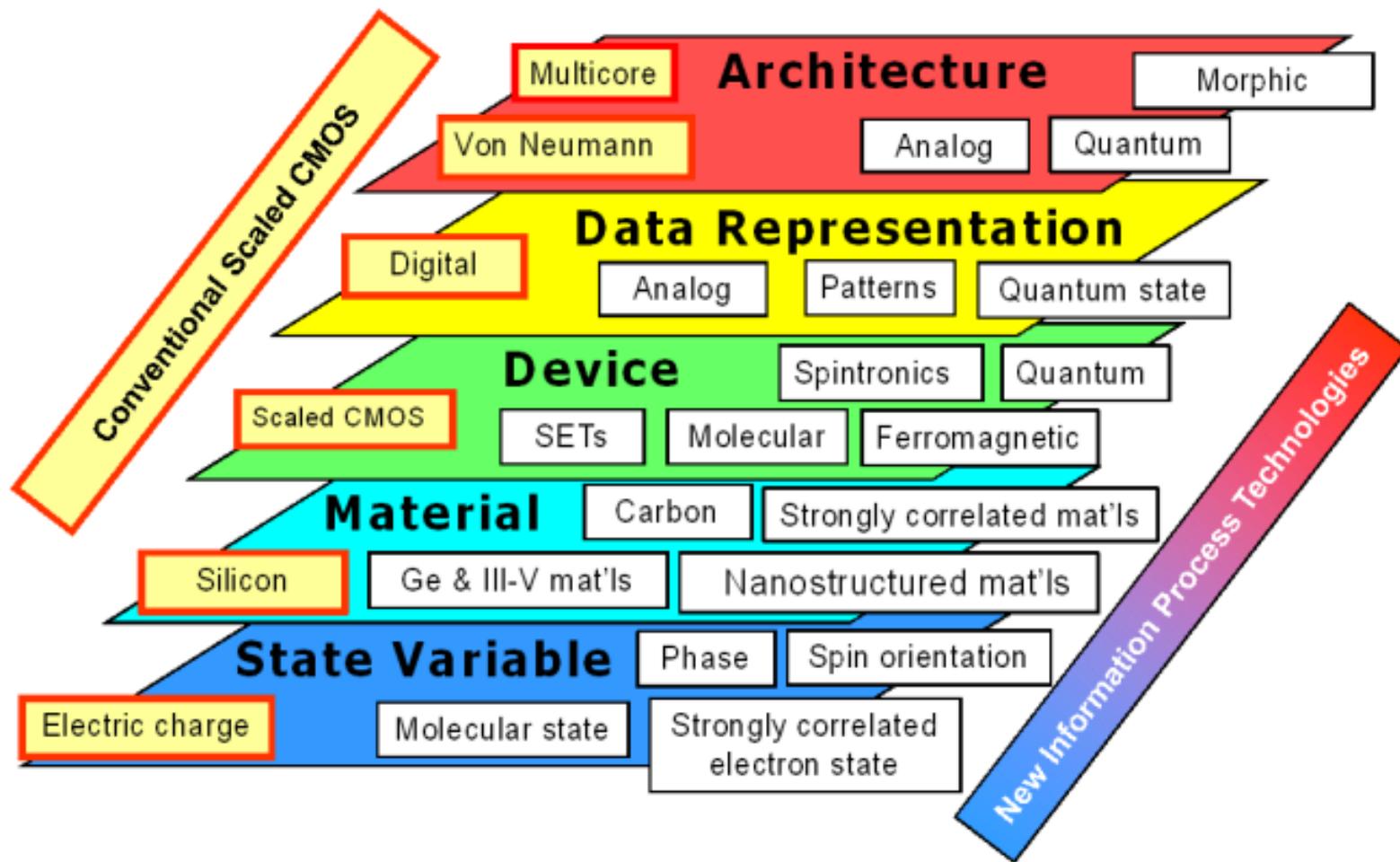


Figure ERD2 A Taxonomy for emerging research information processing devices (The technology entries are representative but not comprehensive.)

Logic Technology Tables

Table 1 – Extending MOSFETs to the End of the Roadmap

CNT FETs
Graphene nanoribbons
III-V Channel MOSFETs
Ge Channel MOSFETs
Nanowire FETs
Non-conventional Geometry Devices

Table 2- Unconventional FETS, Charge-based Extended CMOS

Tunnel FET
I-MOS
Spin FET
SET
NEMS switch
Negative Cg MOSFET

Table 3 - Non-FET, Non Charge-based ‘Beyond CMOS’ devices

Collective Magnetic Devices
Moving domain wall devices
Atomic Switch
Molecular Switch
Pseudo-spintronic Devices
Nanomagnetic (M:QCA)

Taxonomy of emerging memory devices

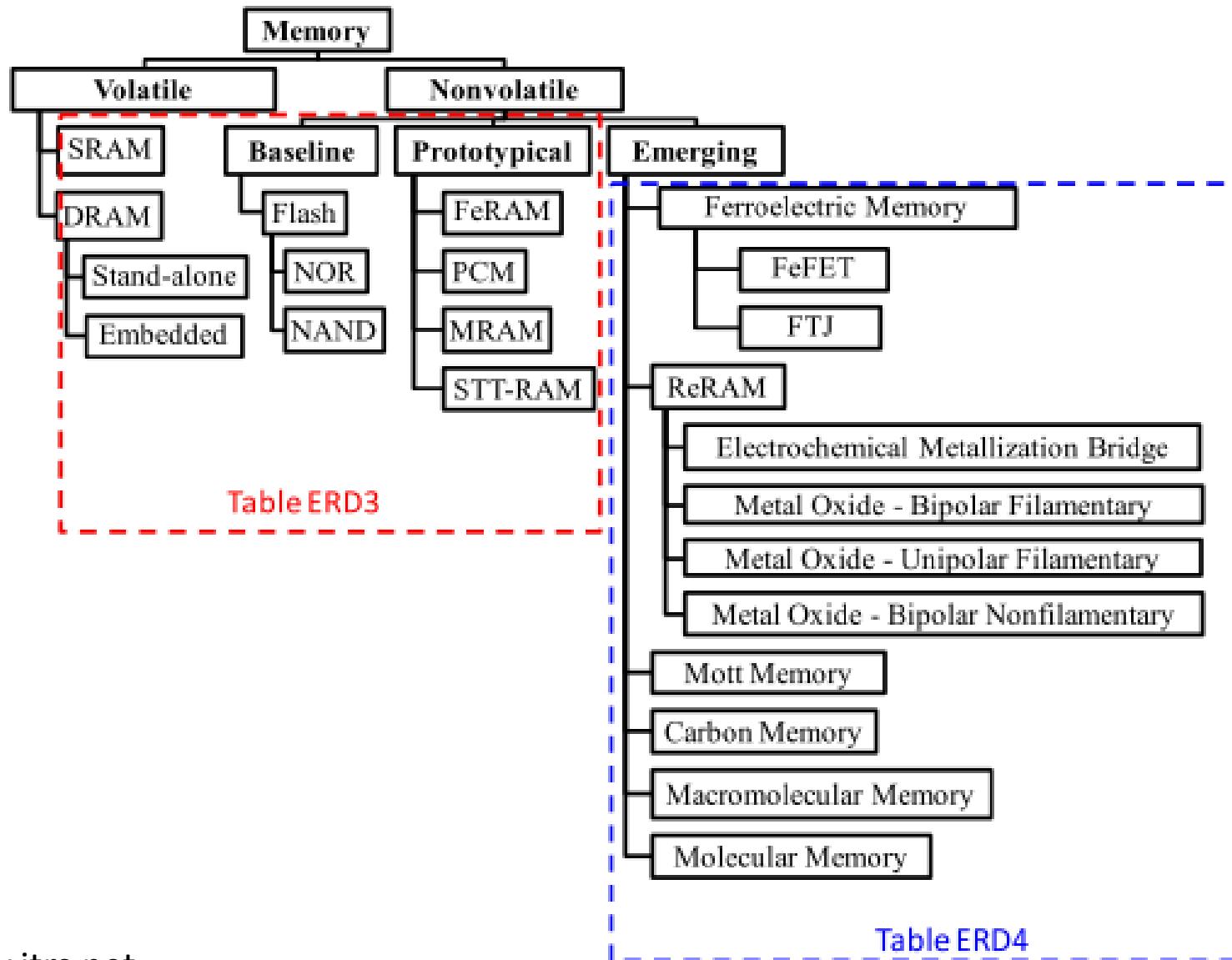


Table ERD3

Table ERD4

Interconnect Hierarchical Cross Sections

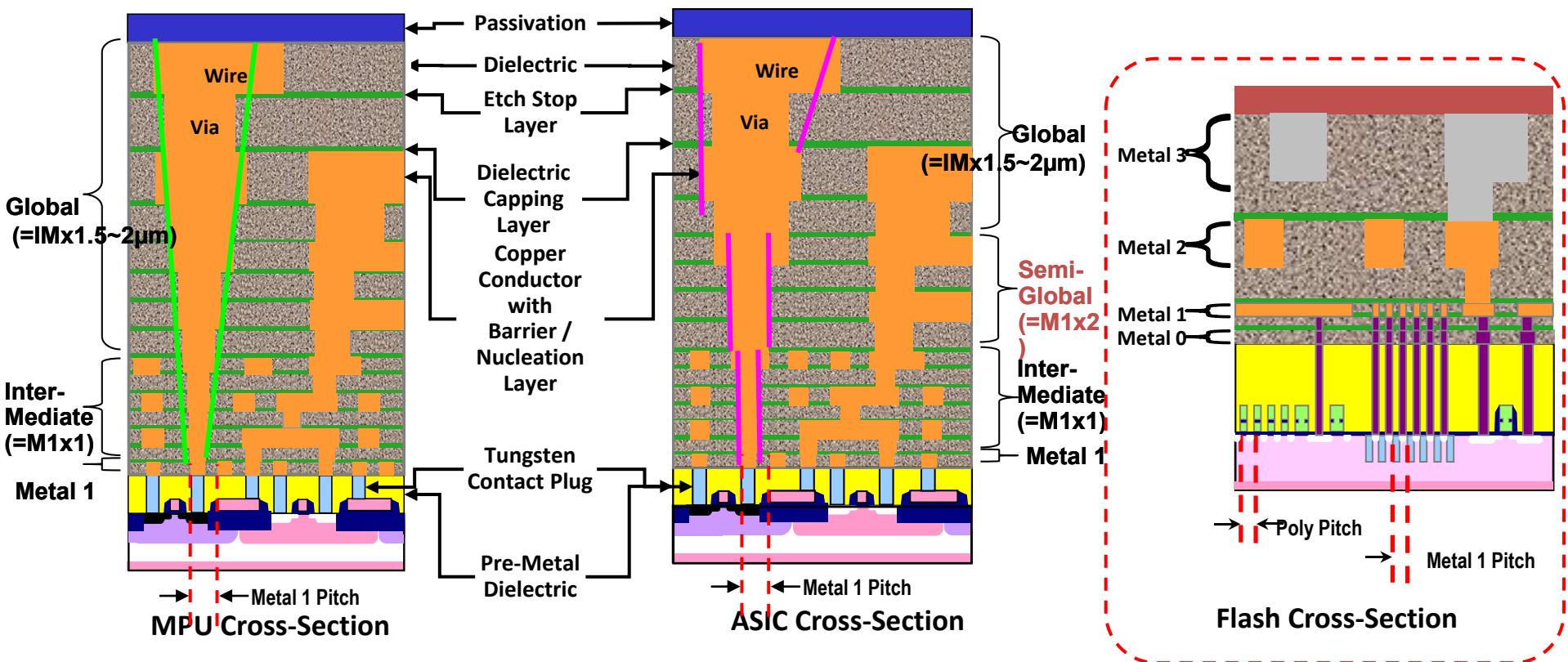


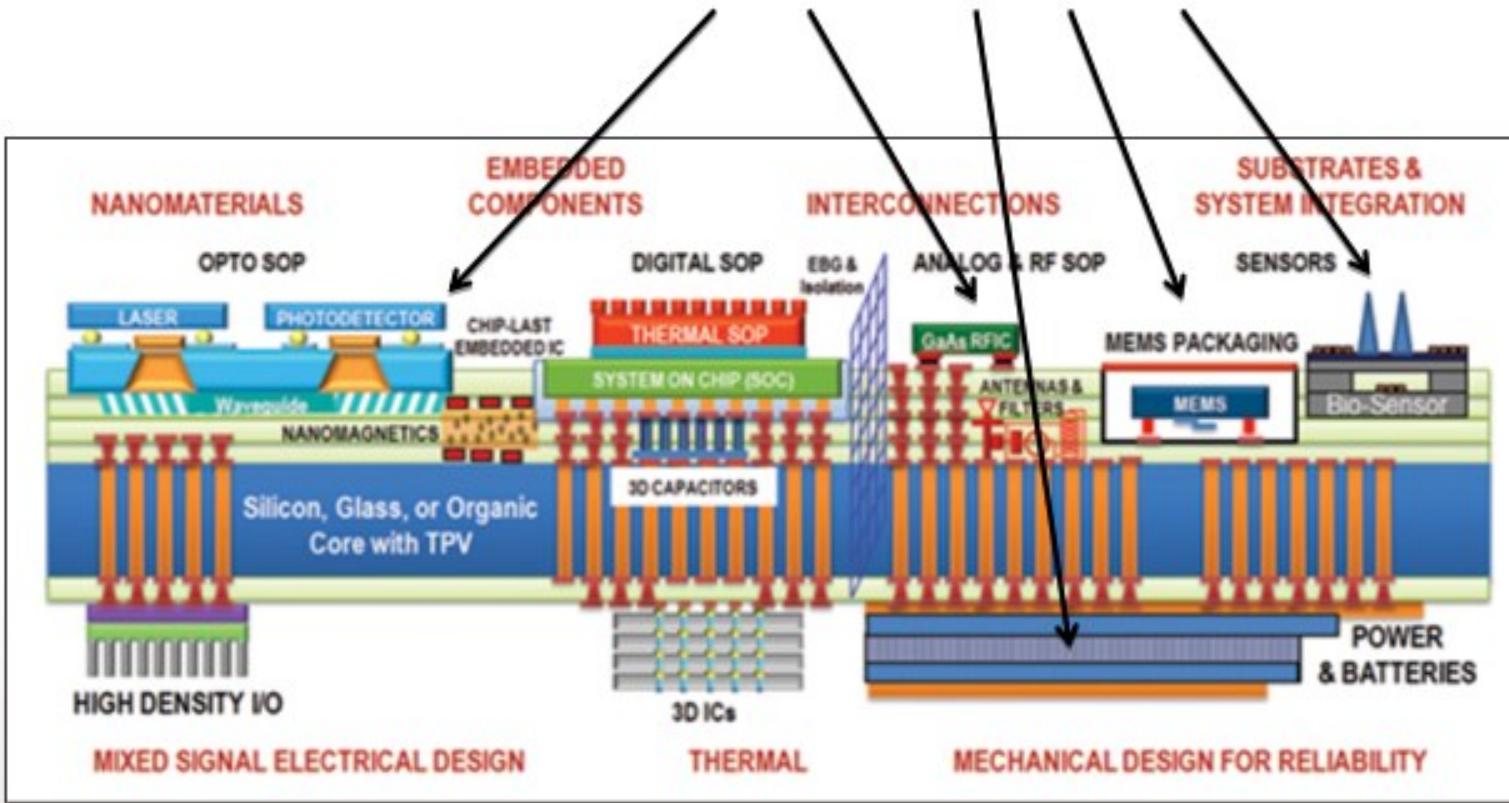
Table ERD 10a MOSFETs: Extending MOSFETs to the End of the Roadmap

Device		FET [A]	Carbon-based Nanoelectronics		Nanowire FETs	Tunnel FET	n-type alternate channel material FET	p-type alternate channel material FET
<i>Typical example devices</i>		Si CMOS	CNT FET	Graphene Nanoribbon FET	Ge/Si Nanowire FET	All Si, Ge and silicide source, VLS nanowire	n-Ge FET	Ga(In)Sb
<i>Cell Size (spatial pitch) [B]</i>	Projected	100 nm	100 nm	100 nm	40 nm [N]	20 nm		TBD
	Demonstrated	590 nm	1.4μm[A]	1.4μm[I]	300 nm [N]	sub 60 nm[V], 60nm[W]	80 nm	80 nm
<i>Density (device/cm²)</i>	Projected	1.00E+10	1.00E+10	1.00E+10	5.9E+10 [N]	channel down to 20nm [X,Y]: 1E10	not known	not known
	Demonstrated	2.80E+08	5.10E+07	5.10E+07	5.2E+07 [N]	not known	1.50E+10	1.60E+10
<i>Switch Speed</i>	Projected	12 THz	6.3 THz [B]	7 THz [J]	9.5 THz [O]	Si /InAs TFET: 60GHz/3THz [Z]	14 THz [EE]	270 GHz [HH]
	Demonstrated	1.5 THz	153 GHz [C]	300GHz [K]	250 GHz [P]	not known	140GHz [FF]	160 GHz [II]
<i>Circuit Speed</i>	Projected	61 GHz	100 GHz [D]	not known	100 GHz [P]	Si/InAs TFET inverter: 20GHz, 1THz [E]	not known	not known
	Demonstrated	5.6 GHz	52 MHz [E]	22 MHz [L]	108 MHz [Q]	not known	not known	not known
<i>Switch Energy, J</i>	Projected	3.00E-18	not known	not known	4E-20 [R]	CGG*VDD^2 (J/um) < 2E-17 [AA]	10 ⁻¹⁸ J	not known
	Demonstrated	1.00E-16	1E-11[F]	not known	2.0E-17 [S]	CGG*VDD^2 (J/um) = 1E-16 [AA]	N/A	not known
<i>Circuit Energy, J</i>	Projected	1.20E-17	1.5E-18 [G]	6.25E-18 [M]	2.0E-16 [T]	1.5E-16 [BB]	not known	not known
	Demonstrated	4.00E-16	not known	not known	not known	not known	not known	not known
<i>Subthreshold Slope, mV/dec</i>	Projected	60 mV/dec	60	60	60	20 [CC]	60	71 [HH]
	Demonstrated	60 mV/dec	60 [H]	not known	61 [U]	21 [DD]	90 [GG]	90 [II]
<i>Operational Temperature</i>		RT	RT	RT	RT	RT	RT	RT
<i>Material Challenges</i>		Si	CNT density, contacts	dielectrics, substrates, in situ mobility, contacts	assembly, directed placement	not known	gate insulator-Ge interfaces, metal-Ge contact	TBD ³⁶

Table ERD 10b Charge-Based Beyond CMOS: Non-Conventional FETs and Other Charge-Based Information Carrier Devices

Device		FET [A]	Spin FET and Spin MOSFET	NEMS	Atomic Switch	Mott FET	Neg Cap Ferroelectric
<i>Typical example devices</i>		Si CMOS	Spin MOSFET	2-terminal [D] 3-terminal [E] 4-terminal [F]		MottFET	
<i>Cell Size (spatial pitch) [B]</i>	Projected	100 nm	100nm [A]	100nm	40 nm	10nm[O]	100 nm
	Demonstrated	590 nm	Not known	sub-1000nm	65 nm [M]	1 μm x 150 μm [P]	150μm [T]
<i>Density (device/cm²)</i>	Projected	1.00E+10	1.00E+10	1.00E+10	1.00E+11	1.00E+12	Similar to Si CMOS
	Demonstrated	2.80E+08	Not known	~1E5 [G]	Not known	6.67E+05	Not known
<i>Switch Speed</i>	Projected	12 THz	12 THz or less [B]	~1GHz [H]	Not known	2THz (0.5ps) [Q]	500 GHz[U]
	Demonstrated	1.5 THz	Not known	0.18GHz [I]	1 ns [N]	13.3THz-0.1GHz(75fs-9ns) [Q]	Not known
<i>Circuit Speed</i>	Projected	61 GHz	61 GHz or less [B]	~1GHz [J]	Not known	Not known	Similar to Si CMOS
	Demonstrated	5.6 GHz	Not known	25 KHz [K]	Not known	Not known	Not known
<i>Switch Energy, J</i>	Projected	3.00E-18	~3E-18 [B]	<1E-17 [L]	Not known	0.1uW [R]	3.00E-19
	Demonstrated	1.00E-16	Not known	Not known	Not known	Not known	Not known
<i>Circuit Energy, J</i>	Projected	1.20E-17	1.2E-17 [B]	<1E-17 [L]	Not known	Not known	Not known
	Demonstrated	4.00E-16	Not known	Not known	Not known	Not known	Not known
<i>Subthreshold Slope, mV/dec</i>	Projected	60 mV/dec	~60 mV/dec [B]	0.00E+00	Not known	<= 60 mV/dec [S]	26 mV/dec [V]
	Demonstrated	60 mV/dec	~90 mV/dec [C]	0.00E+00	Not known	Not known	46 mV/dec [T]

Heterogeneous Components



Source: Georgia Tech PRC, <http://www.prc.gatech.edu/overview/images/etpc.jpg>

Heterogeneous Components — describes devices that do not necessarily scale according to “Moore’s Law,” and provide additional functionalities, such as sensing and actuating, or power generation and management.

After definition by: A. B. Kahng,

Mobile devices

Sensors

Accelerometer
Magnetometer
Gyroscope
Ambient Light
Pressure
Touch
Haptic
Fingerprint
Health
Environmental
UV & RGB
Humidity
Microphone



Applications

Motion Characterization
Contextual Awareness
Health & Fitness
Smart TV Remote
Gestures
Navigation
Biometrics Unlock
Heart Rate
Blood Sugar
CO and Pollutants
Multimedia
Haptic Feedback
Building Floor

Adapted from "Sensors System Integration Challenges, Len Sheynblat, M2M Forum, May 2012"

Wearables

Devices

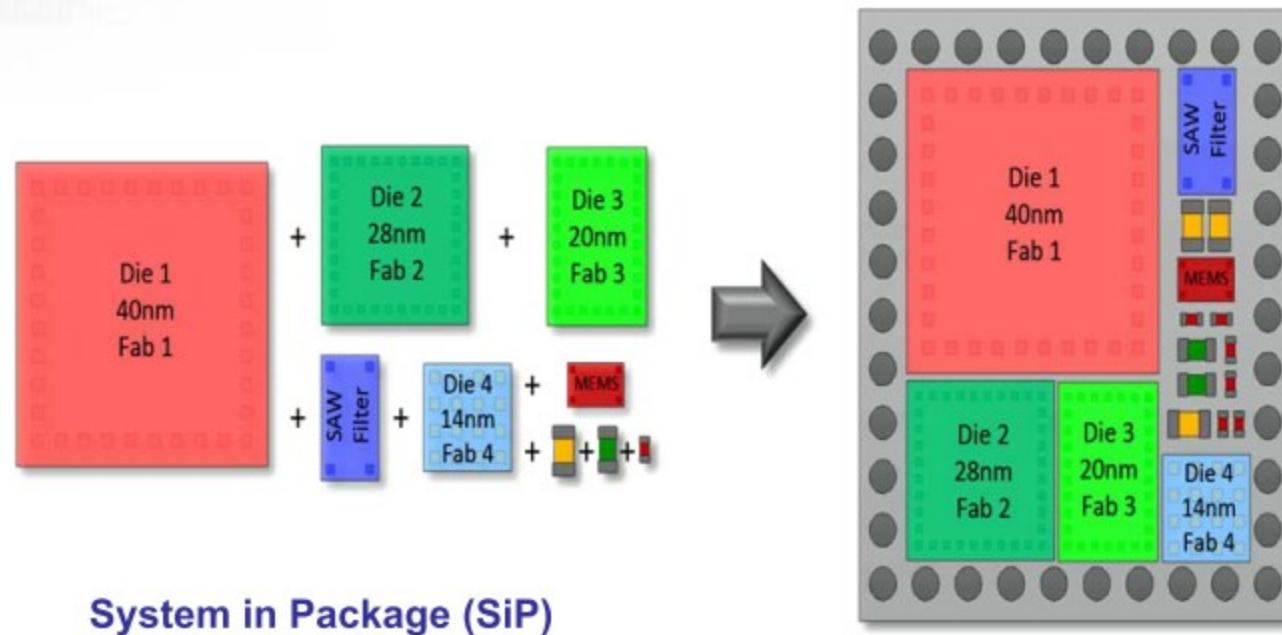
Accelerometer
Gyroscope
Magnetometer
Pressure
Microphone
Temperature
Conductivity
Camera/Optical Sensor
Micro Speakers
eNose
pH
Humidity
Galvanic Skin Response



Applications

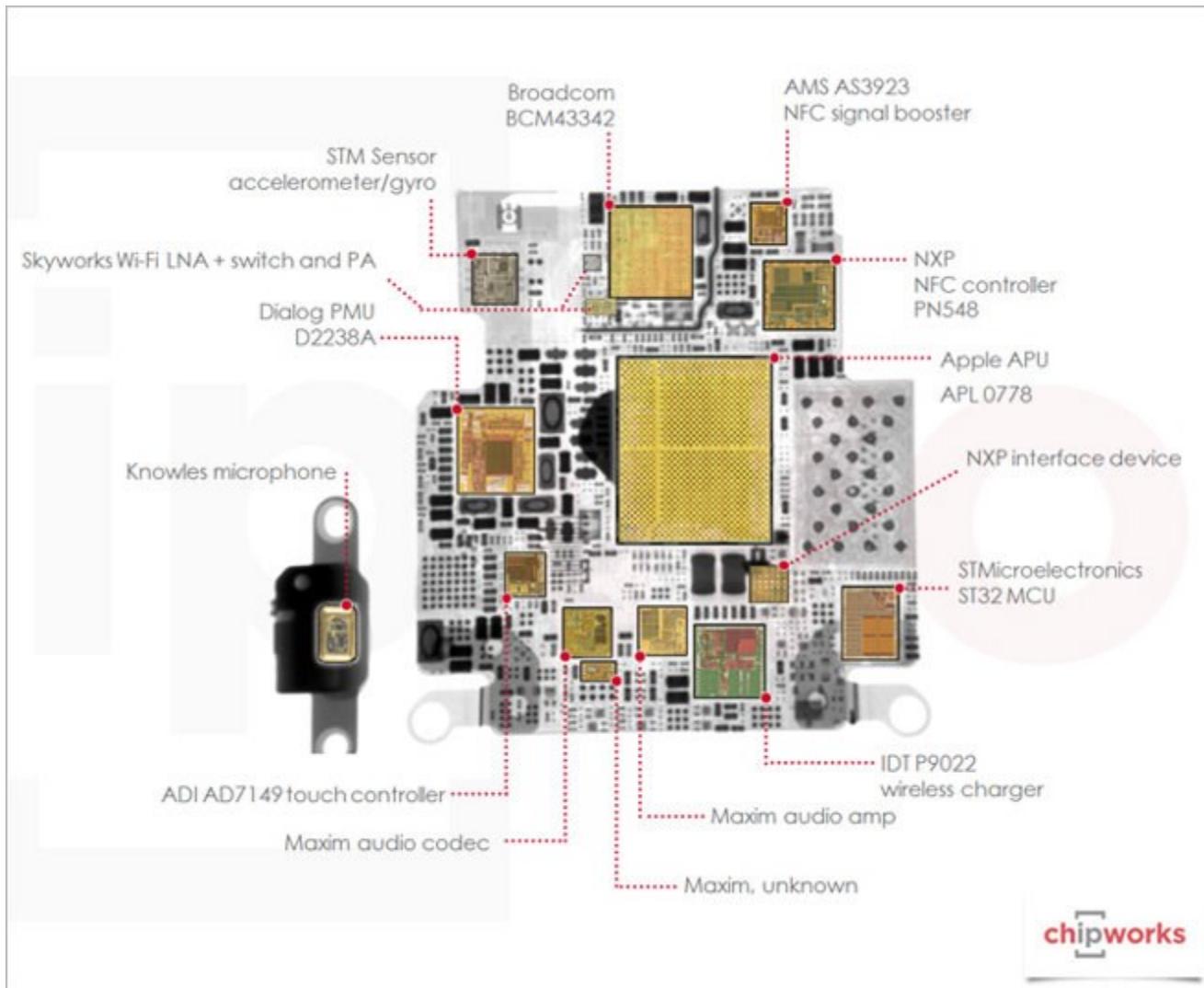
Caloric Consumption
Exercise Intensity
Exercise Safety
Sleep Patterns
Heart Rate
Blood Pressure
Walking Directions
Gas Monitor
Altitude
Motion
Shock
Messaging
Emergency Response

SiP Heterogeneous Integration



This is what we mean by Heterogeneous Integration

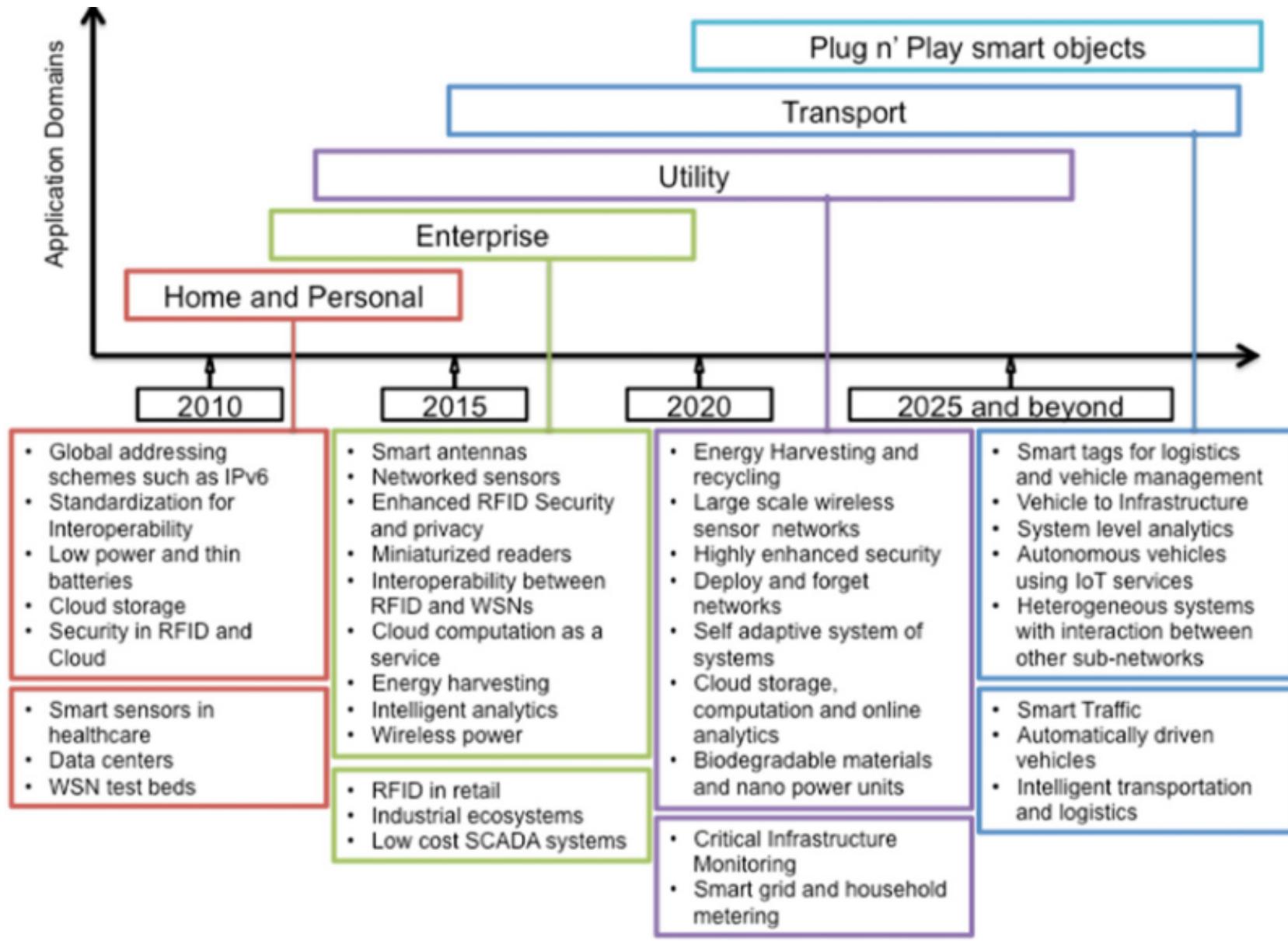
Apple watch S1 SiP



Internet of Things schematic showing the end users and application areas based on data.



Roadmap of key technological developments in the context of IoT application domains envisioned



FET devices for Nanocircuits

FD SOI, Fin FET, Multi Gate FETs

Outline

- Introduction
- MOSFET scaling and its impact
- Material and process approaches and solutions
- Non-classical CMOS
- Conclusions

Introduction

- IC Logic technology: following Moore's Law by rapidly scaling into deep submicron regime
 - Increased speed and function density
 - Lower power dissipation and cost per function
- The scaling results in major MOSFET challenges, including:
 - Simultaneously maintaining satisfactory I_{on} (drive current) and I_{leak}
 - High gate leakage current for very thin gate dielectrics
 - Control of short channel effects (SCEs) for very small transistors
 - Power dissipation
 - Etc.
- Potential solutions & approaches:
 - Material and process (front end): high-k gate dielectric, metal gate electrodes, strained Si, ...
 - Structural: non-classical CMOS device structures
 - *Many innovations needed in rapid succession*

International Technology Roadmap for Semiconductors (ITRS)

- Industry-wide effort to map IC technology generations for the next 15 years
 - Over 800 experts from around the world
 - From companies, consortia, and universities
 - For each calendar year
 - Projects scaling of technology characteristics and requirements, based on meeting key Moore's Law targets
 - Assesses key challenges and gaps
 - Lists best-known potential solutions
 - Projections are based on modeling, surveys, literature, experts' technical judgment

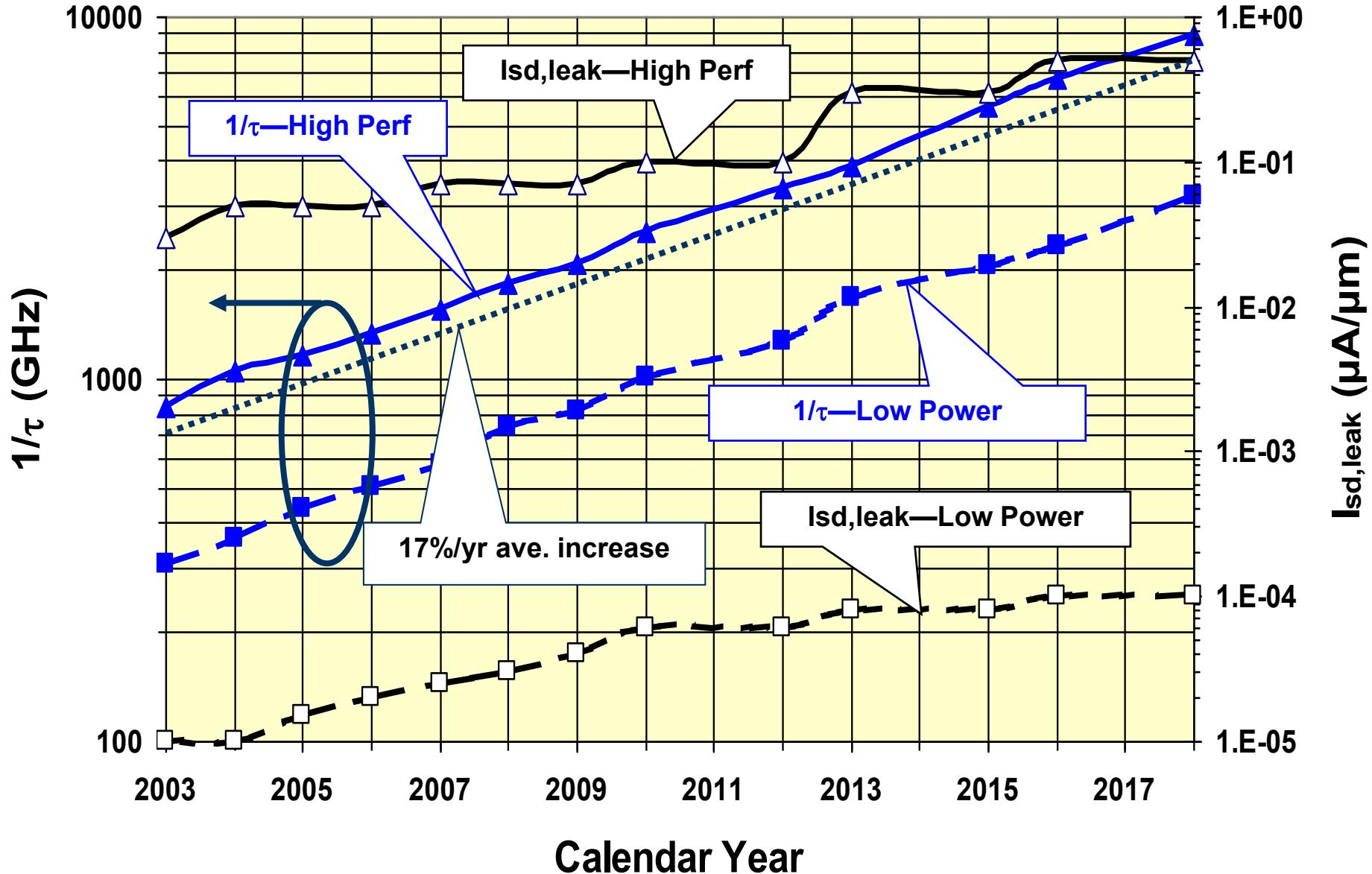
MOSFET Scaling Approach: 2005 ITRS

- MASTAR computer modeling software is used:
detailed, analytical MOSFET models with key
MOSFET physics included
 - Initial choice of scaled MOSFET parameters is made
 - Using MASTAR, MOSFET parameters are iteratively
varied to meet ITRS targets for either
 - Scaling of transistor speed OR
 - Specific (low) levels of leakage current

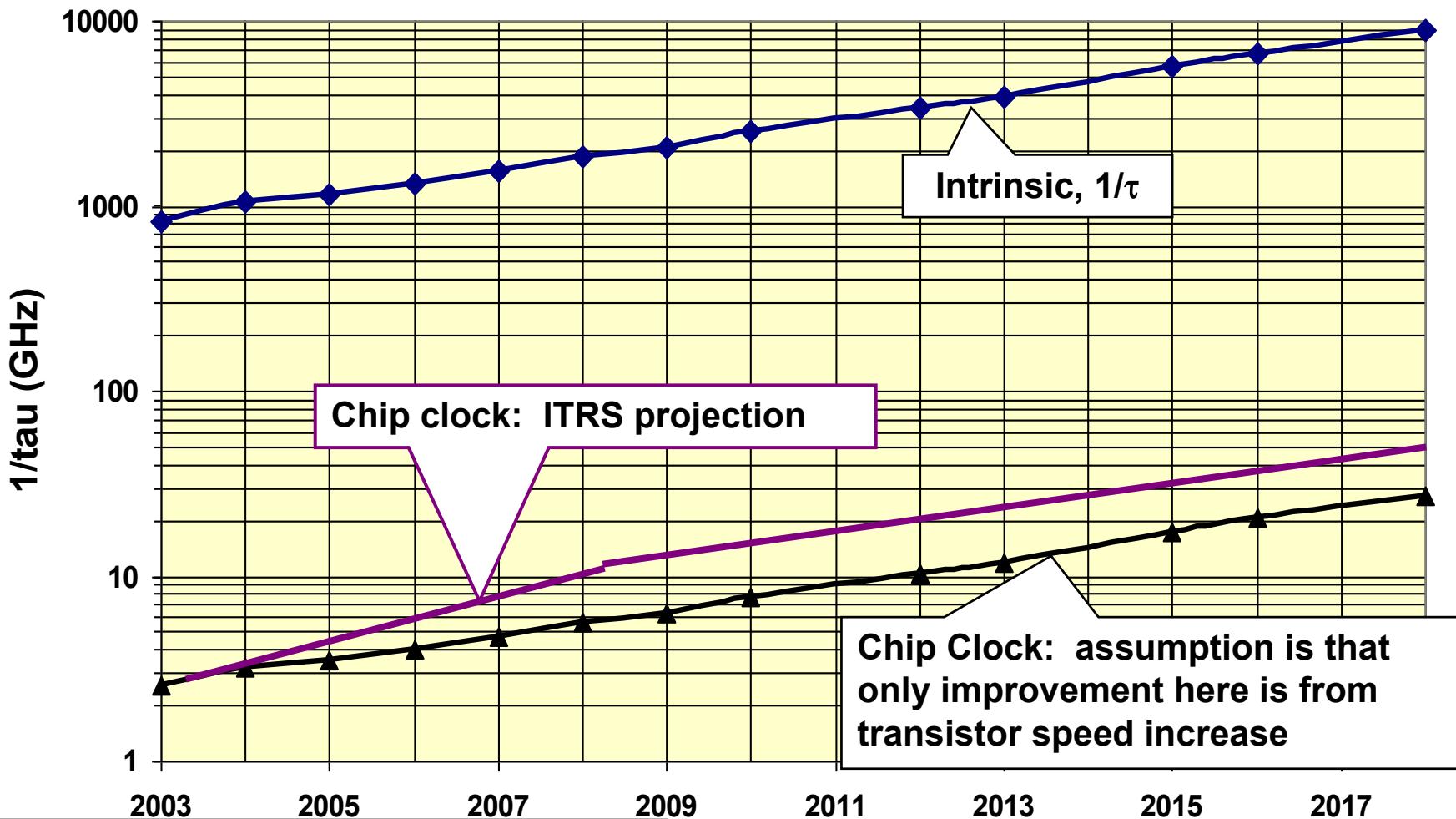
ITRS Drivers for Different Applications

- High-performance chips (MPU, for example)
 - Driver: maximize chip speed → maximize transistor performance (metric: τ , transistor intrinsic delay [or, equivalently, $1/\tau$])
 - Goal of ITRS scaling: $1/\tau$ increases at $\sim 17\%$ per year, historical rate
 - Must maximize I_{on}
 - Consequently, I_{leak} is relatively high
- Low-power chips (mobile applications)
 - Driver: minimize chip power (to conserve battery power)
→ minimize I_{leak}
 - Goal of ITRS scaling: low levels of I_{leak}
 - Consequently, $1/\tau$ is considerably less than for high-performance logic
- This talk focuses on high-performance logic, which largely drives the technology

$1/\tau$ and $I_{sd,leak}$ scaling for High-Performance and Low-Power Logic. Data from 2003 ITRS.



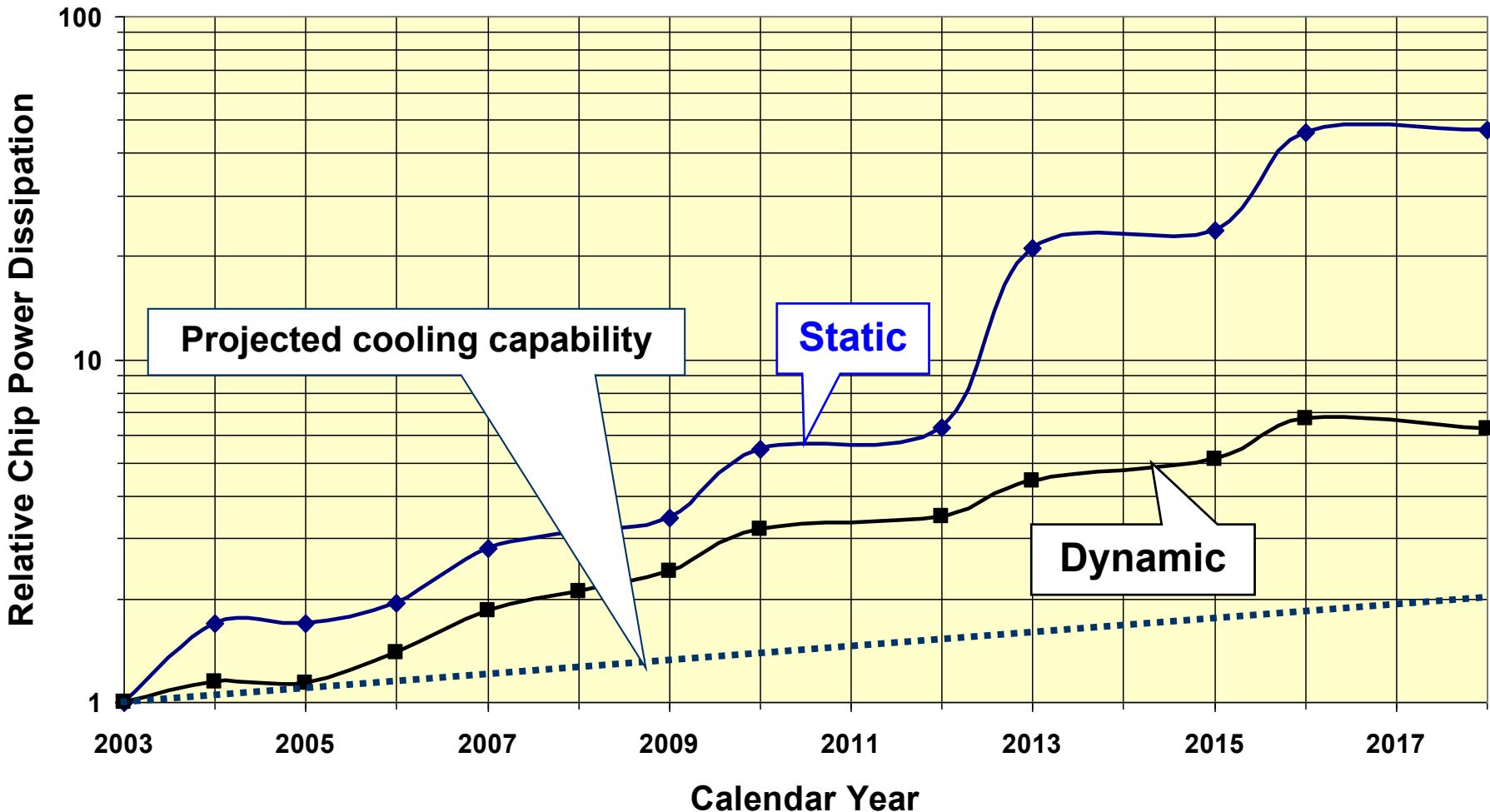
Frequency scaling: Transistor Intrinsic Speed and Chip Clock Frequency for High-Performance Logic. Data from 2003 ITRS.



Conclusion: transistor speed improvement is a critical enabler of chip clock frequency improvement

Calendar Year

Potential Problem with Chip Power Dissipation Scaling: High-Performance Logic, Data from 2003 ITRS



Unrealistic assumption, to make a point about P_{static} :
all transistors are high performance, low V_t type

Table PIDS1 Process Integration Difficult Challenges

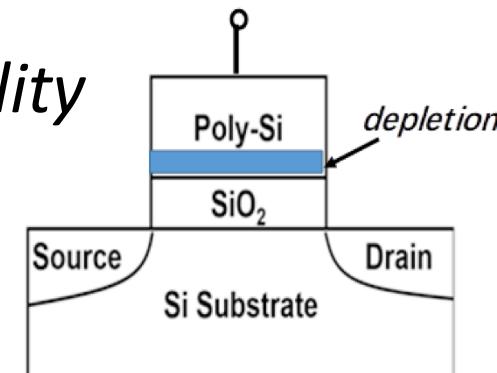
<i>Near-Term 2013–2020</i>	<i>Summary of Issues</i>
1. Scaling Si CMOS	Scaling planar bulk CMOS Implementation of fully depleted SOI and multi-gate (MG) structures Controlling source/drain series resistance within tolerable limits Further scaling of EOT with higher κ materials ($\kappa > 30$) Threshold voltage tuning and control with metal gate and high- κ stack Inducing adequate strain in new structures
2. Implementation of high-mobility CMOS channel materials	Basic issues same as Si devices listed above High- κ gate dielectrics and interface states (D_{it}) control CMOS (n - and p -channel) solution with monolithic material integration Epitaxy of lattice-mismatched materials on Si substrate Process complexity and compatibility with significant thermal budget limitations

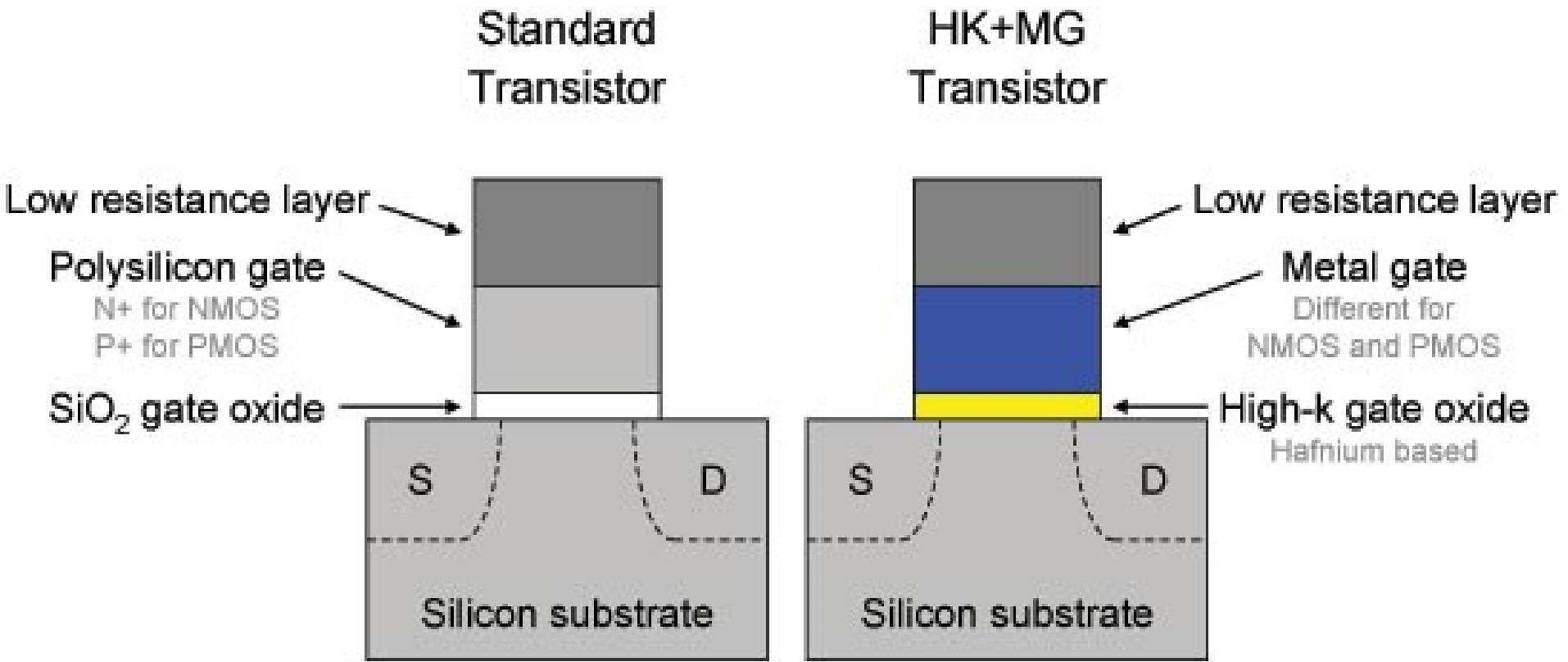
Difficult Transistor Scaling Issues

- With scaling, meeting transistor requirements requires significant technology innovations
 - *Issue: High gate leakage* → static power dissipation
 - Potential solution: high-k gate dielectric
 - *Issue: polysilicon depletion in gate electrode* → increased effective T_{ox} , reduced I_{on}
 - Potential solution: metal gate electrodes
 - *Issue: Need for enhanced channel mobility*
 - Etc.

Difficult Transistor Scaling Issues

- Assumption: highly scaled MOSFETs with the targeted characteristics can be successfully designed and fabricated
- However, with scaling, meeting transistor requirements will require significant technology innovations
 - *Issue: High gate leakage* → static power dissipation
 - Direct tunneling increases rapidly as T_{ox} is reduced
 - Potential solution: high-k gate dielectric
 - *Issue: Polysilicon depletion in gate electrode* → increased effective T_{ox} , reduced I_{on}
 - *Issue: Need for enhanced channel mobility*
 - Etc.





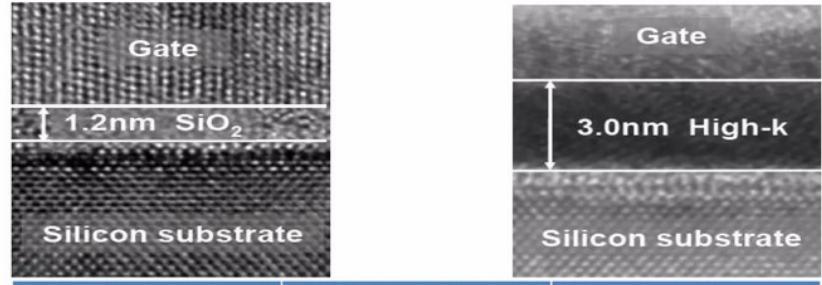
Because of the combination of a high-k dielectric and the metal gate electrode, Intel is quoting a greater than 20% improvement in switching speed compared to its 65nm transistors. At the same speed as its 65nm transistors, there's a greater than 5x reduction in source-drain leakage power and a greater than 10x reduction in gate oxide leakage power;

Need for high- κ materials

$$C = \frac{\kappa \epsilon_0 A}{t}$$

where

- A is the capacitor area
- κ is the **relative dielectric constant** of the material (3.9 for **silicon dioxide**)
- ϵ_0 is the **permittivity of free space**
- t is the thickness of the capacitor oxide insulator



	High-k vs. SiO ₂	Benefit
Capacitance	60% greater	Faster transistors
Dielectric leakage	100x reduction	Far cooler

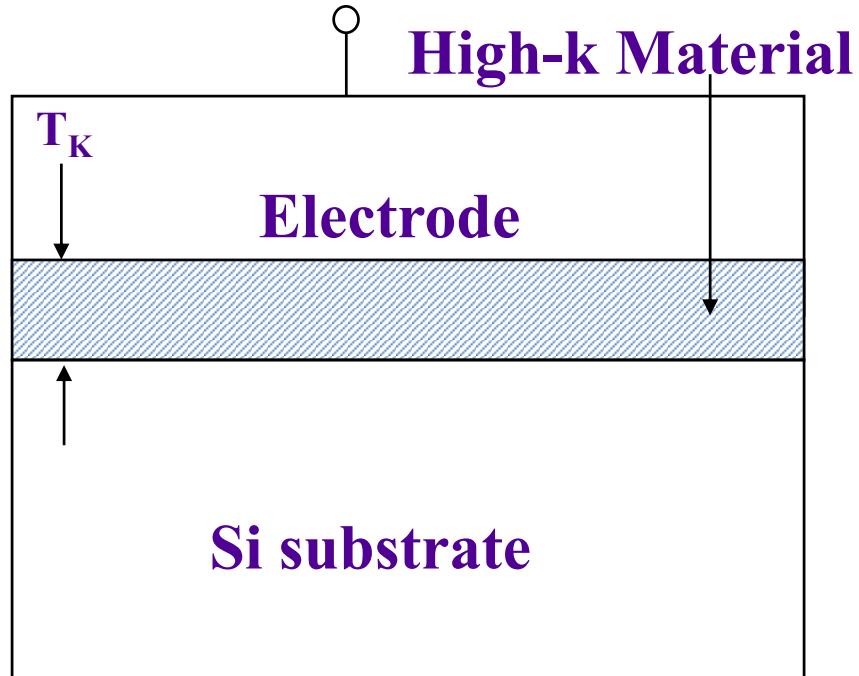
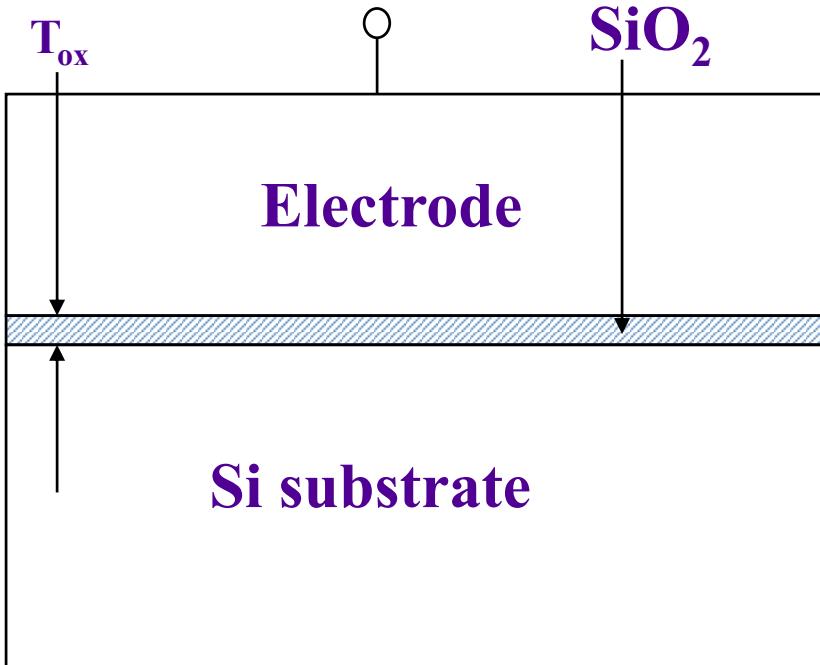
Conventional silicon dioxide gate dielectric structure compared to a potential high- κ dielectric structure where $\kappa = 16$

$$I_{D,\text{Sat}} = \frac{W}{L} \mu C_{\text{inv}} \frac{(V_G - V_{\text{th}})^2}{2}$$

where

- W is the width of the transistor channel
- L is the channel length
- μ is the channel carrier mobility (assumed constant here)
- C_{inv} is the capacitance density associated with the gate dielectric when the underlying channel is in the inverted state
- V_G is the voltage applied to the transistor gate
- V_{th} is the **threshold voltage**

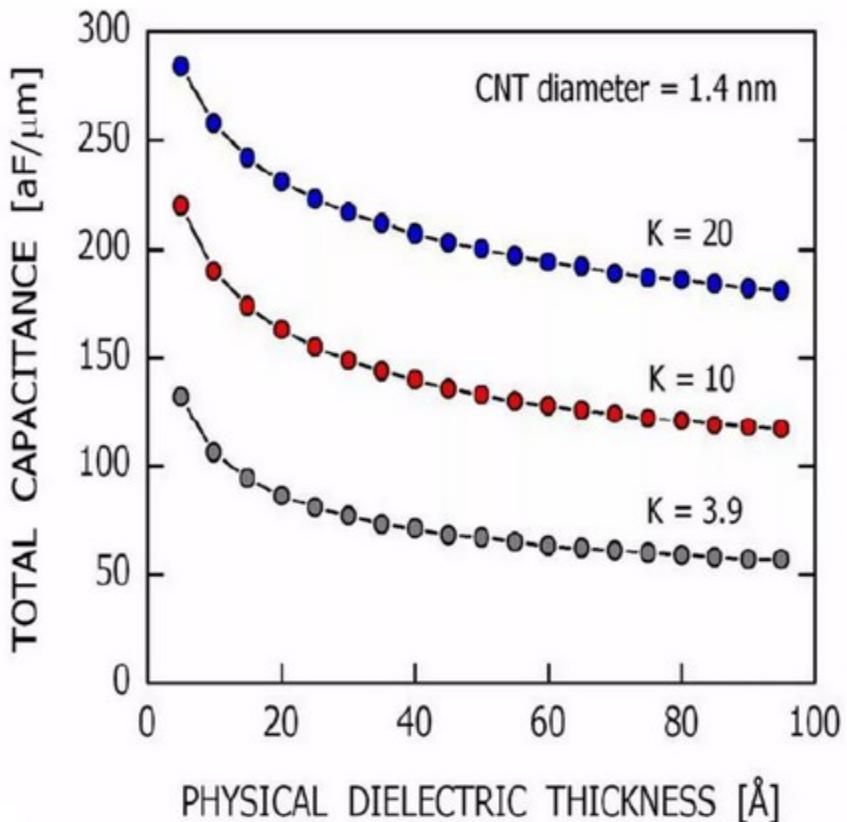
High K Gate Dielectric to Reduce Direct Tunneling



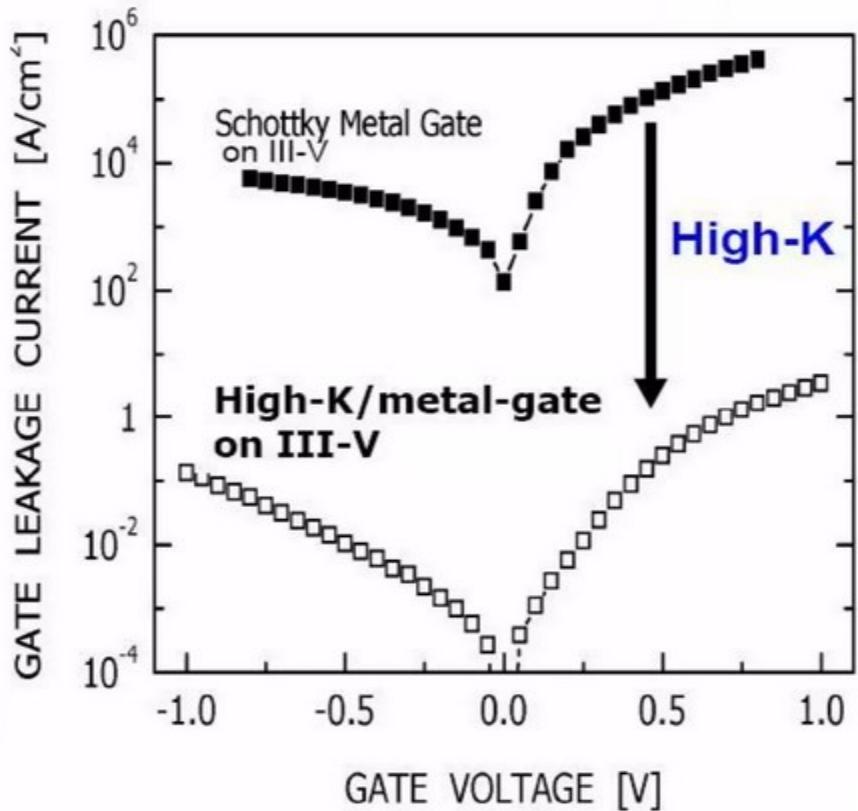
- Equivalent Oxide Thickness = EOT = $T_{ox} = T_K * (3.9/K)$, where 3.9 is relative dielectric constant of SiO₂ and K is relative dielectric constant of high K material
 - $C = C_{ox} = \epsilon_{ox}/T_{ox}$
 - To first order, MOSFET characteristics with high-k are same as for SiO₂
- Because $T_K > T_{ox}$, direct tunneling leakage much reduced with high K
 - If energy barrier is high enough
- Current leading candidate materials: HfO₂ ($K_{eff} \sim 15 - 30$); HfSiO_x ($K_{eff} \sim 12 - 16$)
 - Materials, process, integration issues to solve

6 nm of HfO₂ is replaced with 1 nm of SiO₂ for K = 25

Why High K ?

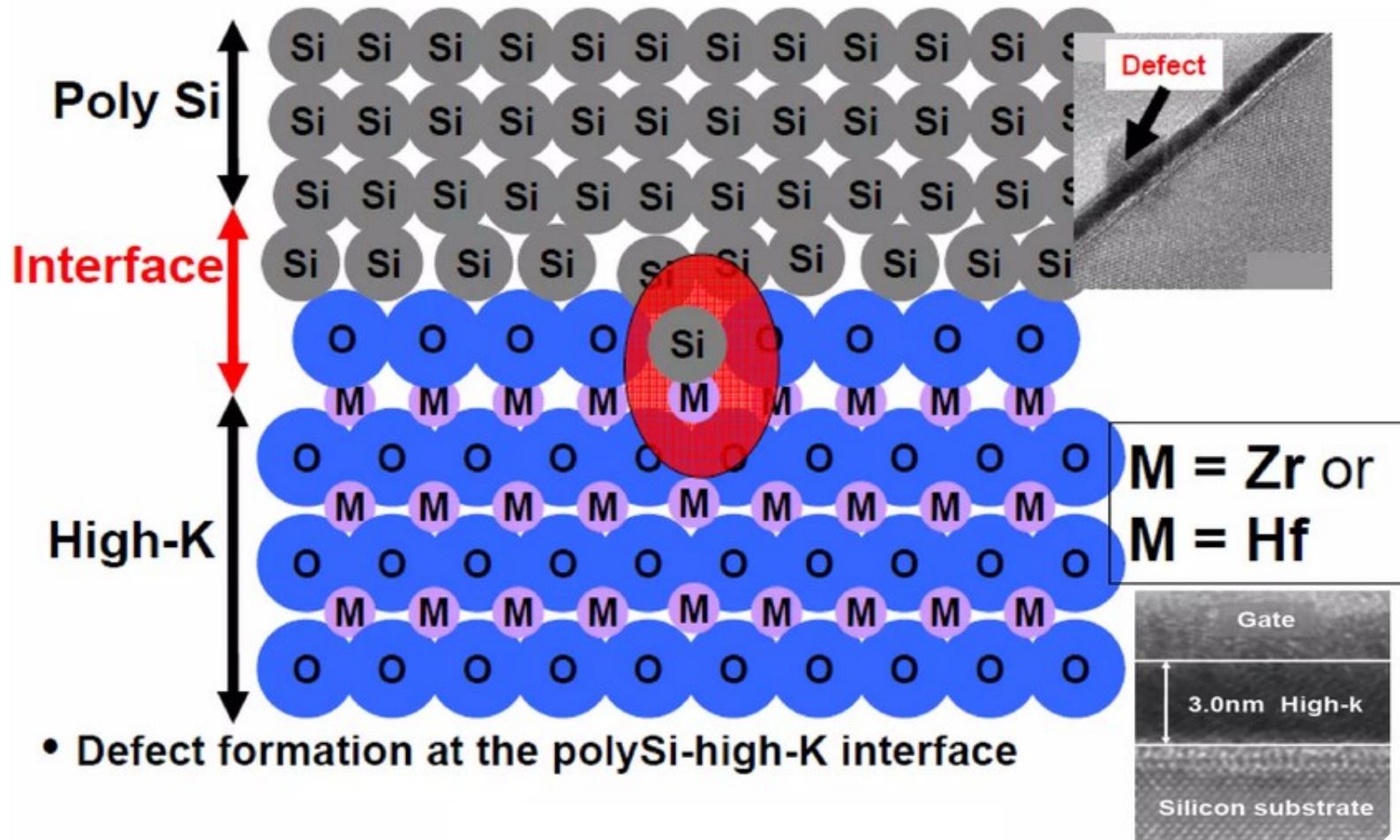


Capacitance vs. Dielectric thickness plot

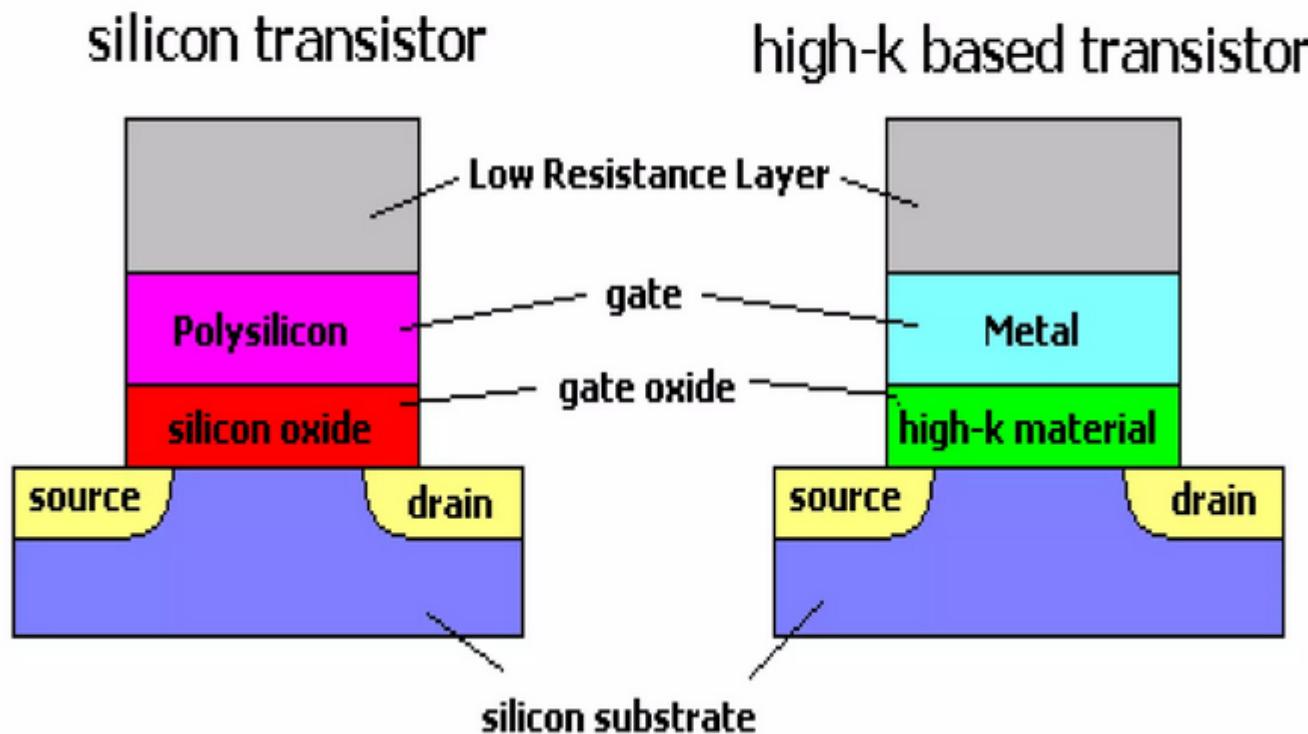


Leakage current vs. V_g plot

High K and polysilicon interface



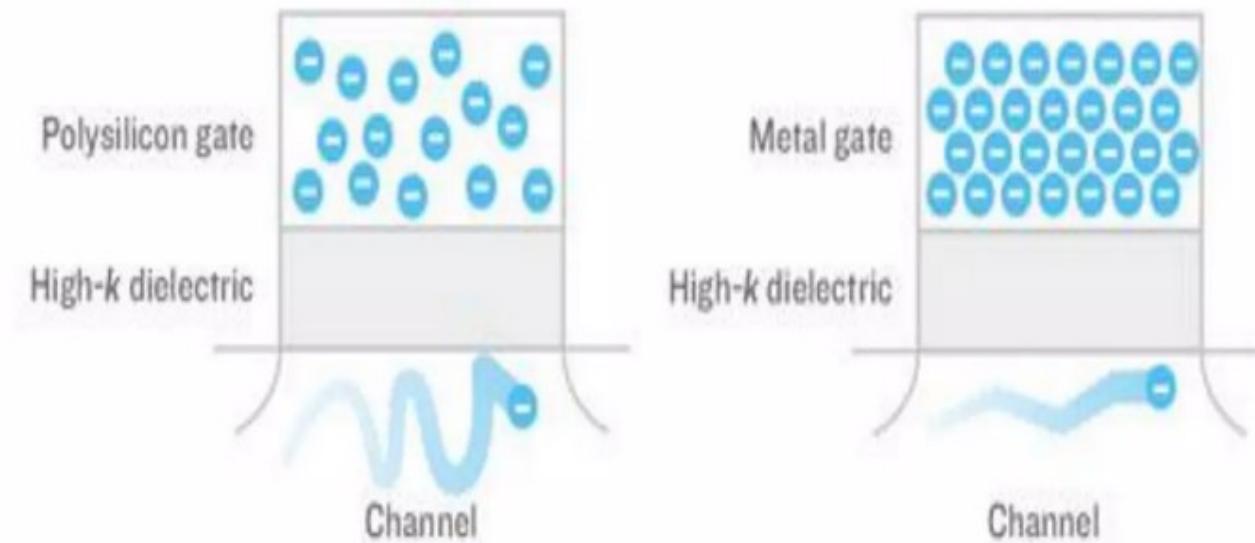
When SiO_2 is replaced with a high-k material it was found that PolySi and High-k material were not compatible so PolySi is being replaced by a Metal to make it compatible with the high-k material.



Conventional vs HK based transistor

Use of Metal Gates

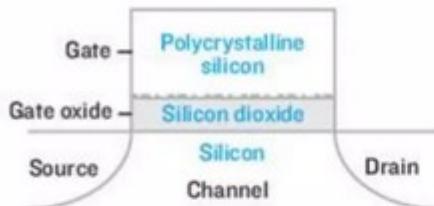
- As a conductor, metal can pack in hundreds of times more electrons than poly silicon
- Metal gate electrodes (Co, Ni, Mo, W) are able to decrease phonon scatterings and reduce the mobility degradation problem.
- The key property - Work Function of metal.



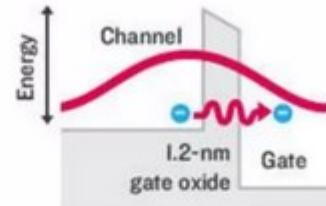
Scattering in Poly vs Metal gate

The High-k – Metal gate solution

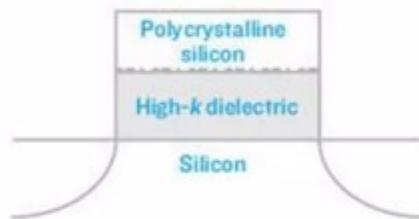
CONVENTIONAL TRANSISTORS



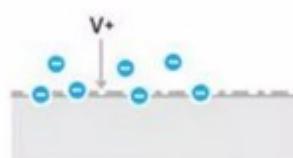
PROBLEM: Electron leakage through gate oxide



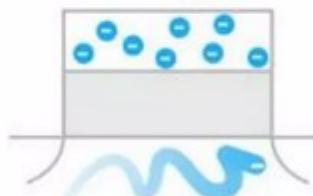
HIGH-k TRANSISTORS



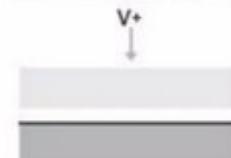
PROBLEM: Uneven dielectric surface traps charges.



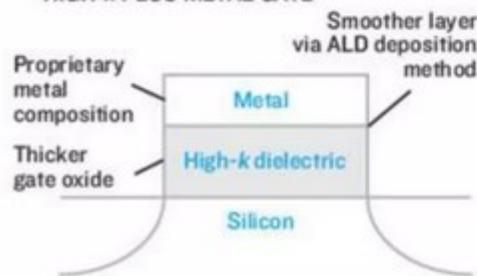
PROBLEM: Phonons scatter electrons in channel.



PROBLEM: Poor bonding between gate and dielectric makes transistor hard to turn on.

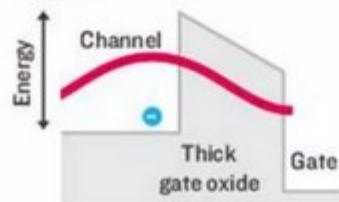


HIGH-k PLUS METAL GATE

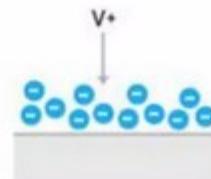


Smoother layer via ALD deposition method

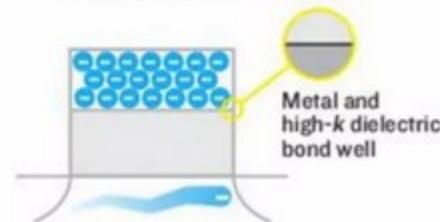
SOLUTION: Thicker, high-k gate oxide prevents electron leakage.



SOLUTION: New atomic-layer deposition creates smooth dielectric layer.



SOLUTION: Metal gate's higher electron density screens out electron-scattering phonons.



Metal Gate

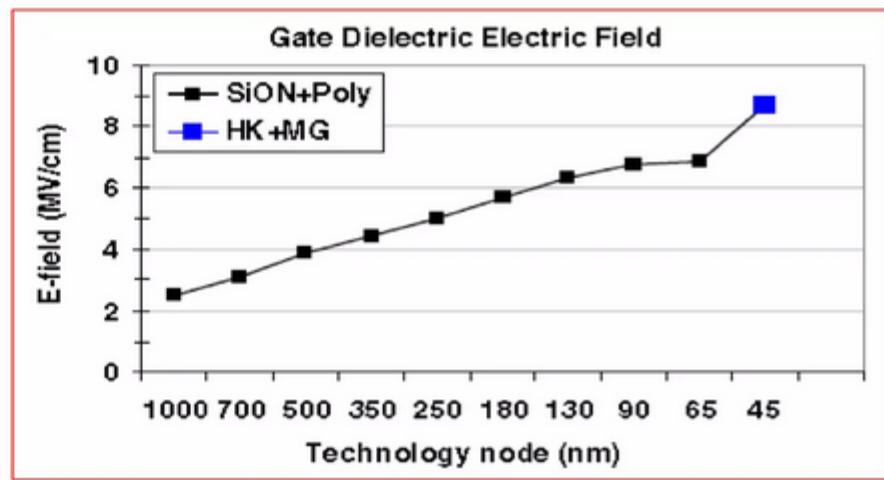
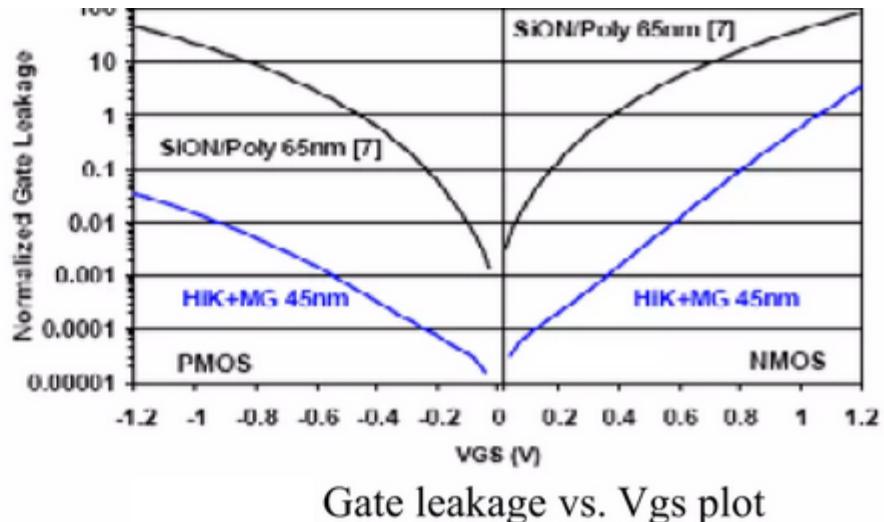
- Increases the gate field effect

High-k Dielectric

- Increases the gate field effect
- Allows use of thicker dielectric layer to reduce gate leakage

HK + MG Combined

- Drive current increased >20% (>20% higher performance)
- Or source-drain leakage reduced >5x
- Gate oxide leakage reduced >10x



E-field vs. Technology node plot

Yeah...Nobody knows for sure.....!!!

- ✓ Intel achieved 20 percent improvement in transistor switching speed by using metal Gate /high-K transistor with HfO₂ as dielectric.

Intel 45nm Transistor – performance compared to 65nm

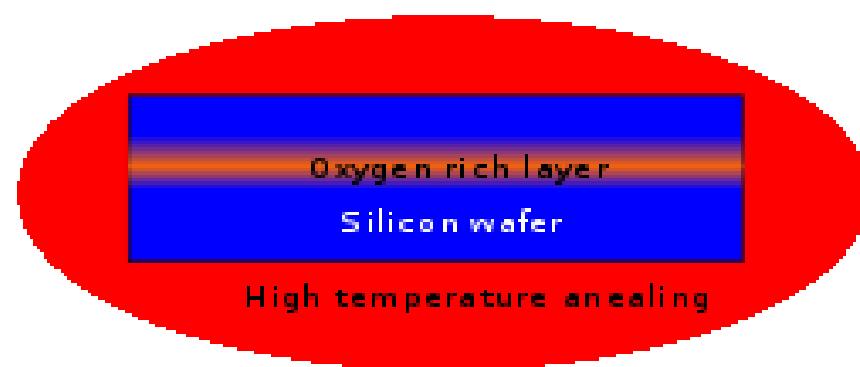
- ✓ 2x improvement in transistor density
- ✓ 30% reduction in switching power
- ✓ 20% improvement in switching speed
- ✓ 10x reduction in gate oxide leakage power

Limits of Scaling Planar, Bulk MOSFETs

- 65 nm tech. generation (2007, $L_g = 25\text{nm}$) and beyond: increased difficulty in meeting all device requirements with classical planar, bulk CMOS (even with high-k, metal electrodes, strained Si...)
 - Control of SCE
 - Impact of quantum effects and statistical variation
 - Impact of high substrate doping
 - Control of series S/D resistance ($R_{\text{series,s/d}}$)
 - Others
 - **Alternative device structures (non-classical CMOS) may be utilized**
 - Ultra thin body, fully depleted: single-gate SOI and multiple-gate transistors
- 

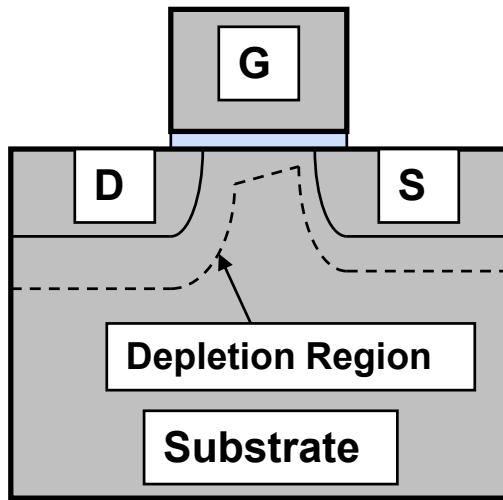
Benefits of SOI technology relative conventional silicon (bulk CMOS) processing include:

1. *Lower parasitic capacitance* due to isolation from the bulk silicon, which improves power consumption at matched performance.
2. Higher performance at equivalent VDD. C work at low VDD's.
3. Reduced temperature dependency due to doping.
4. Better yield due to high density, better wafer utilization.
5. Lower leakage currents due to isolation thus higher power efficiency.
6. Inherently radiation hardened (resistant to errors), thus reducing the need for redundancy.
7. Higher mobility

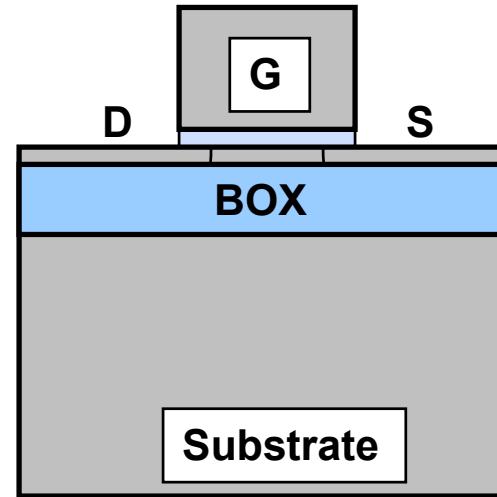


Transistor Structures: Planar Bulk & Fully Depleted SOI

Planar Bulk



Fully Depleted SOI



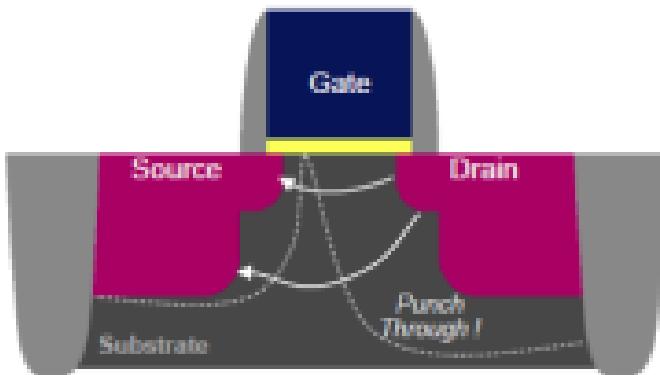
- + Wafer cost / availability
- SCE scaling difficult
- High doping effects and Statistical variation
- Parasitic junction capacitance

- + Lower junction cap
- + Light doping possible
- + V_t can be set by WF of Metal Gate Electrode
- SCE scaling difficult
- Sensitivity to Si thickness (very thin)
- Wafer cost/availability

REFERENCES

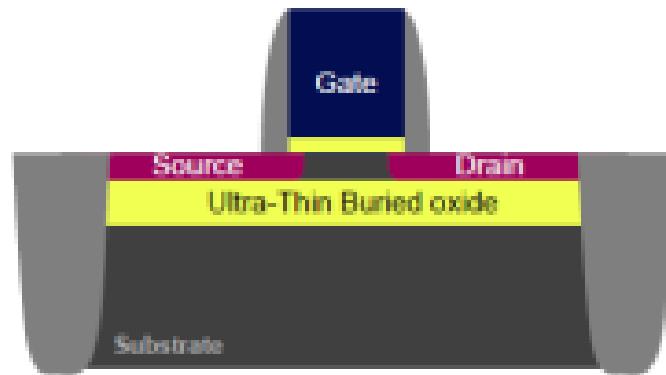
1. P.M. Zeitzoff, J.A. Hutchby and H.R. Huff, *MOSFET and Front-End Process Integration: Scaling Trends, Challenges, and Potential Solutions Through The End of The Roadmap*, International Journal of High-Speed Electronics and Systems, **12**, 267-293 (2002).
2. Mark Bohr, ECS Meeting PV 2001-2, Spring, 2001.

Bulk



Typical Transistor in today CMOS System on Chip

FD-SOI



Change of Substrate adding the thin Buried oxide

FD-SOI advantages:

- Excellent electrostatic control of the channel
- No channel doping required
- Back bias ability if BOX is also thin



- Excellent VT variability
- Low DIBL (Drain Induced Barrier Lowering) – especially at low VDD
- Limited Short Channel Effects
- Very good Sub-threshold Slope
- Minimum junction capacitance and diode leakage
- **Simpler process: no halo doping, simpler STI (End Bevel Etch)**

FD-SOI is Scalable

8

- ST has already identified an FD-SOI roadmap covering three nodes:
 - 28nm, 14nm and 10nm

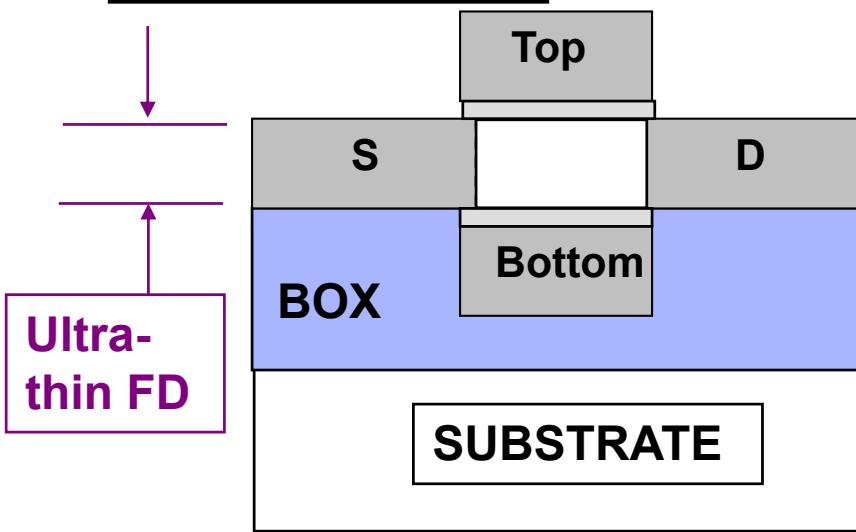


Double Gate Transistor Structure

REFERENCES

1. P.M. Zeitzoff, J.A. Hutchby and H.R. Huff, *MOSFET and Front-End Process Integration: Scaling Trends, Challenges, and Potential Solutions Through The End of The Roadmap*, *International Journal of High-Speed Electronics and Systems*, **12**, 267-293 (2002).
2. Mark Bohr, *ECS Meeting PV 2001-2, Spring, 2001*.

Double-Gate SOI:



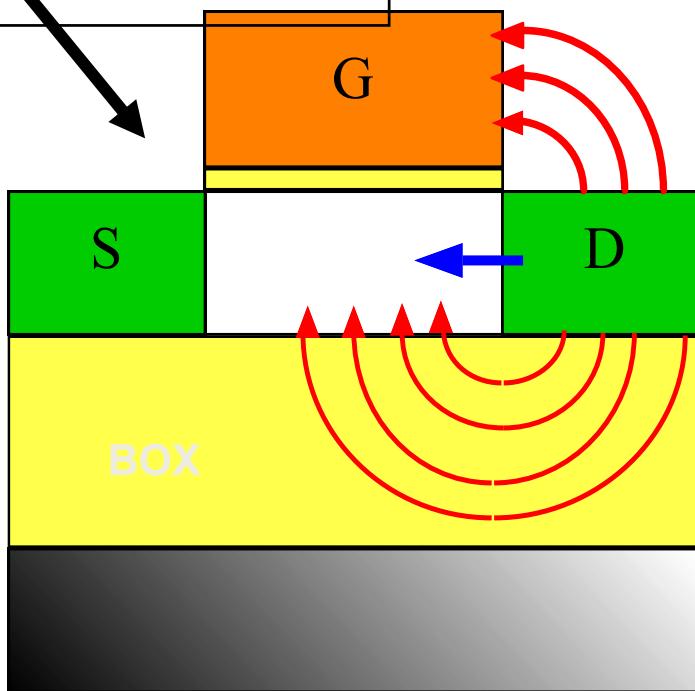
- + Enhanced scalability
- + Lower junction capacitance
- + Light doping possible
- + V_t can be set by WF of metal gate electrode
- + ~2x drive current
- ~2x gate capacitance
- High $R_{series,s/d} \rightarrow$ raised S/D
- Complex process

Summary: more advanced, optimal device structure, but difficult to fabricate, particularly in this SOI configuration

Field Lines for Single and Double-Gate MOSFETs

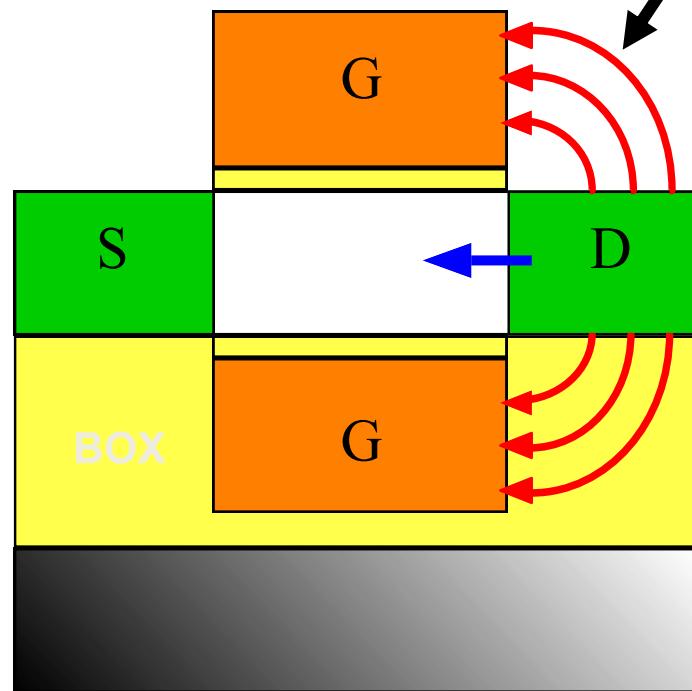
E-Field lines

To reduce SCE's,
aggressively reduce
Si layer thickness



Single-Gate SOI

Double gates
electrically shield
the channel



Double-Gate

Courtesy: Prof. J-P Colinge, UC-Davis

FinFET Device

FinFET vs. Planar Characteristics

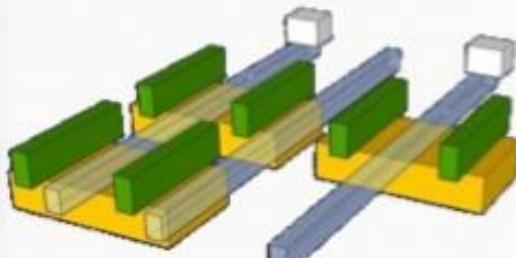
- FinFET Benefits

- Lower leakage
- Higher driving current
- Low-voltage operability
- Better mismatch
- Higher intrinsic gain

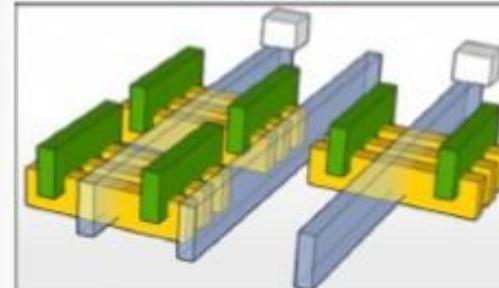
- FinFET Challenges

- Higher parasitic capacitance due to 3D profile
- Higher parasitic resistance due to local interconnect
- Quantized device widths

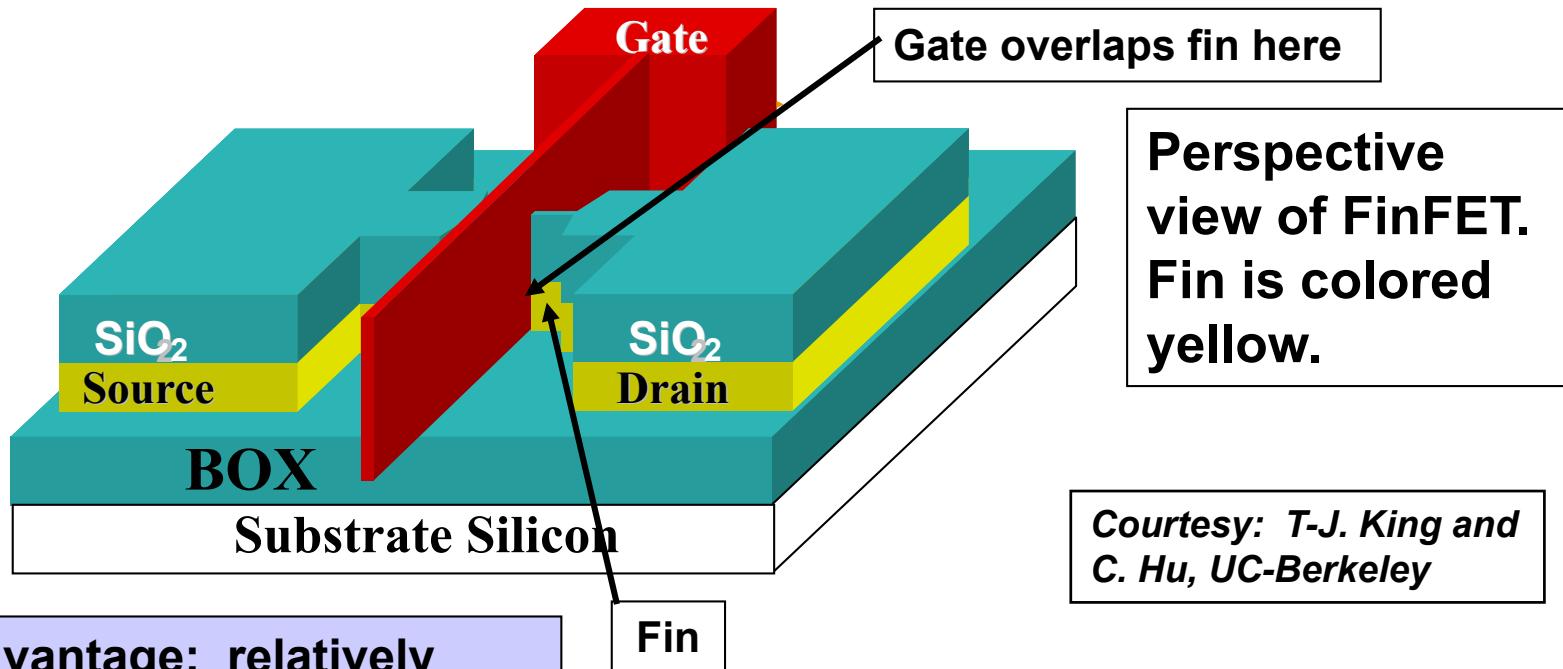
Planar Device



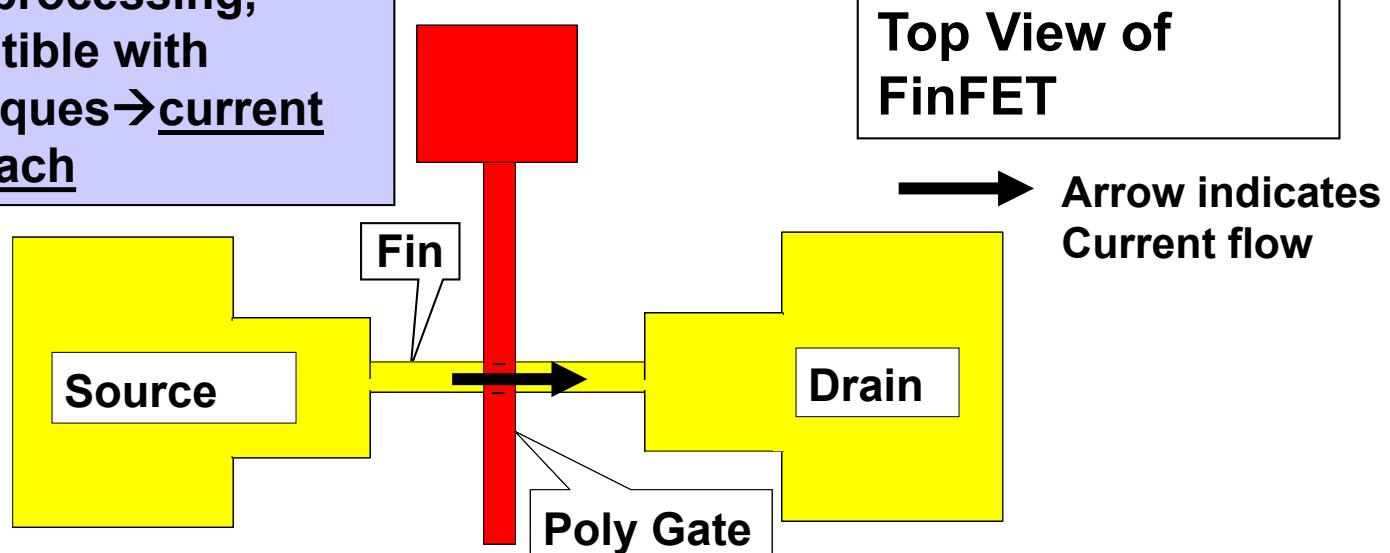
FinFET



Other Double-Gate Transistor Structures (FinFET)



Key advantage: relatively conventional processing, largely compatible with current techniques → current leading approach

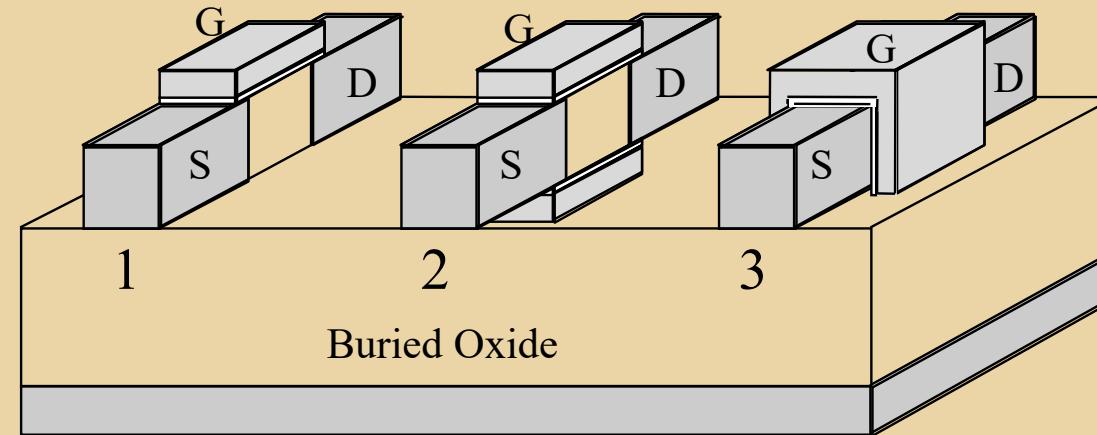


FinFET disadvantage

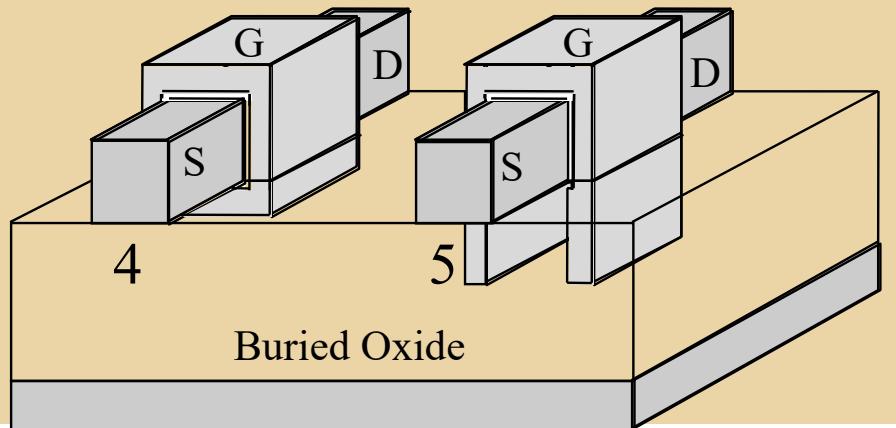
Although FinFETs are wonderful from some points of view (low leakage, high current, lower voltage) they have some disadvantages too (higher parasitic capacitance, higher parasitic resistance due to local interconnect, quantized device widths). The biggest challenge has probably been RC extraction accuracy.

Types of Multiple-Gate Devices

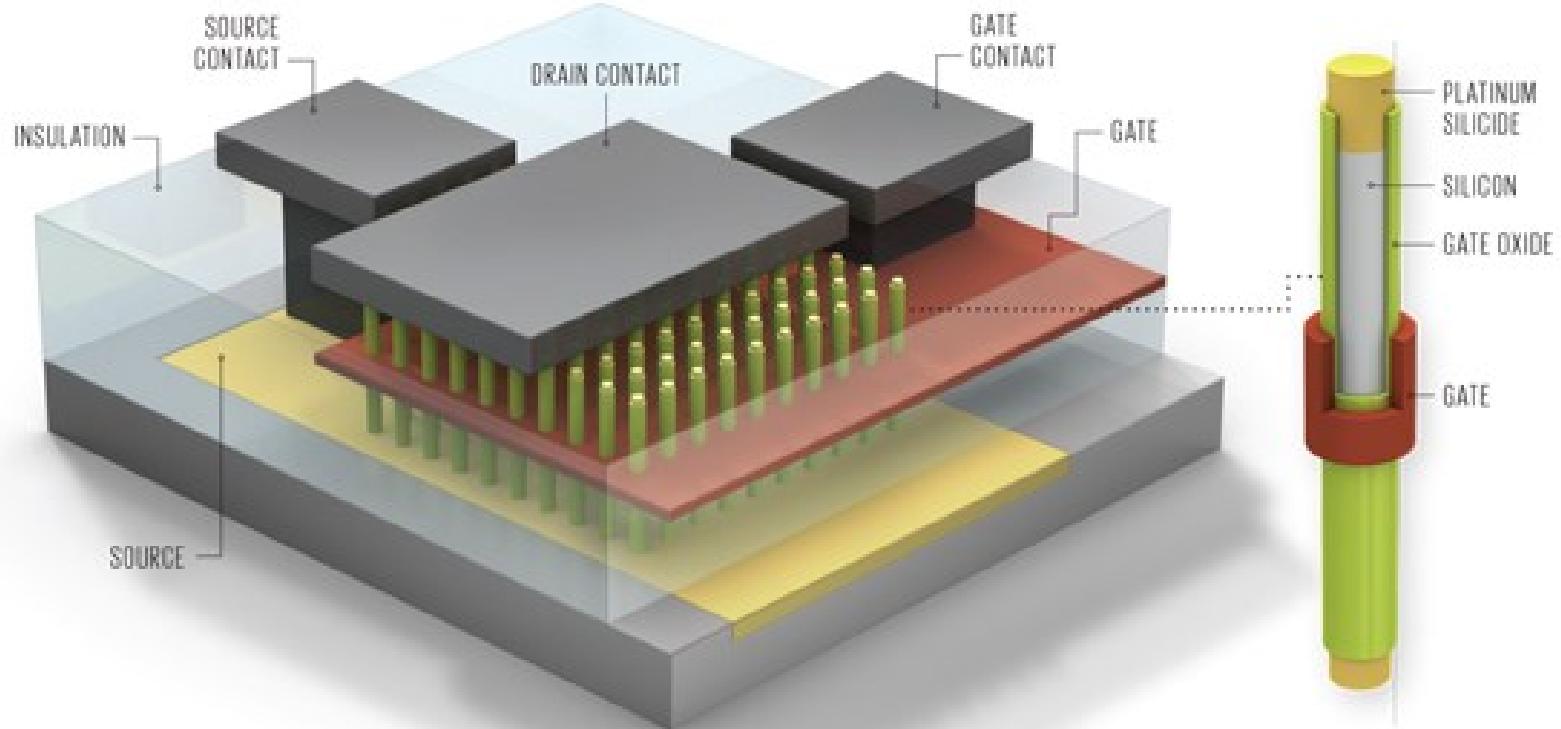
Courtesy:
Prof. J-P
Colinge,
UC-Davis



- Increasing process complexity, increasing scalability
- 1: Single gate
2: Double gate
3: Triple gate
4: Quadruple gate (GAA)
5: Π gate



Nanowire Transistors



Gate-All-Around Transistors: In a new design, the transistor channel is made up of an array of vertical nanowires. The gate surrounds all the nanowires, which improves its ability to control the flow of current. Platinum-based source and drain contacts sit at the top and bottom of the nanowires.

Timeline of Projected Key Technology Innovations

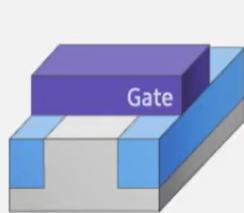
	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018
Strained Si--HP																
			Production													
High-k (Low Power)						Production										
Elevated S/D							Production									
High-k (HP)							Production									
Metal Gate (HP, dual gate)							Production									
Metal Gate (Low Power, dual gate)								Production								
Ultra-thin Body (UTB) SOI, single gate (HP)								Production								
Metal gate (near midgap for UTBSOI)									Production							
Strained Si (Low Power)									Production							
Multiple Gate (HP)										Production						
Ultra-thin Body (UTB) SOI, single gate (Low power)											Production					
Multiple Gate (Low Power)												Production				
Quasi-ballistic transport (HP)												Production				
Quasi-ballistic transport (LOP)													Production			

	Year of Production	2013	2015	2017	2019	2021
1	Logic Industry "Node Name" Label	16/14	10	7	5	3.5
2	Logic ½ Pitch (nm)	40	32	25	20	16
3	FinFET Fin Half-pitch (new) (nm)	30	24	19	15	12
4	FinFET Fin Width (new) (nm)	7.6	7.2	6.8	6.4	6.1
5	FinFET Fin Width (nm) (<i>Detailed</i>)	6.4	5.3	4.4	3.7	3.1
6	6-t SRAM Cell Size(um ²) [@60f2]	0.096	0.061	0.038	0.024	0.015
7	MPU/ASIC HighPerf 4t NAND Gate Size(um ²)	0.248	0.157	0.099	0.062	0.039
8	4-input NAND Gate Density (Kgates/mm) [@155f2]	4.03E+03	6.37E+03	1.01E+04	1.61E+04	2.55E+04
9	450mm Production High Volume Manufacturing Begins (100Kwspm)			2018		
10	Vdd (High Performance, high Vdd transistors)[**]	0.86	0.83	0.8	0.77	0.74
11	1/(CV/I) (1/psec) [**]	1.13	1.53	1.75	1.97	2.1
12	On-chip local clock MPU HP [at 4% CAGR] (GHz)	5.5	5.95	6.44	6.96	7.53
13	Maximum number wiring levels [unchanged]	13	13	14	14	15
14	MPU High-Performance (HP) Printed Gate Length (GLpr) (nm) [**]	28	22	18	14	11
15	MPU High-Performance Physical Gate Length (GLph) (nm) [**]	20	17	14	12	10
16	ASIC/Low Standby Power (LP) Physical Gate Length (nm)	23	19	16	13	11

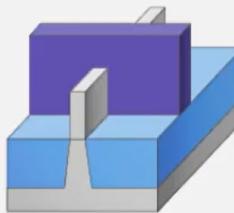


SAMSUNG

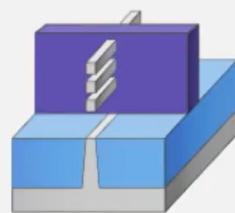
3nm GAA Technology



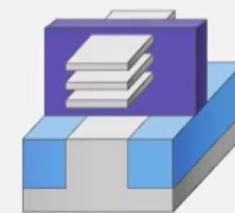
Planar FET



FinFET



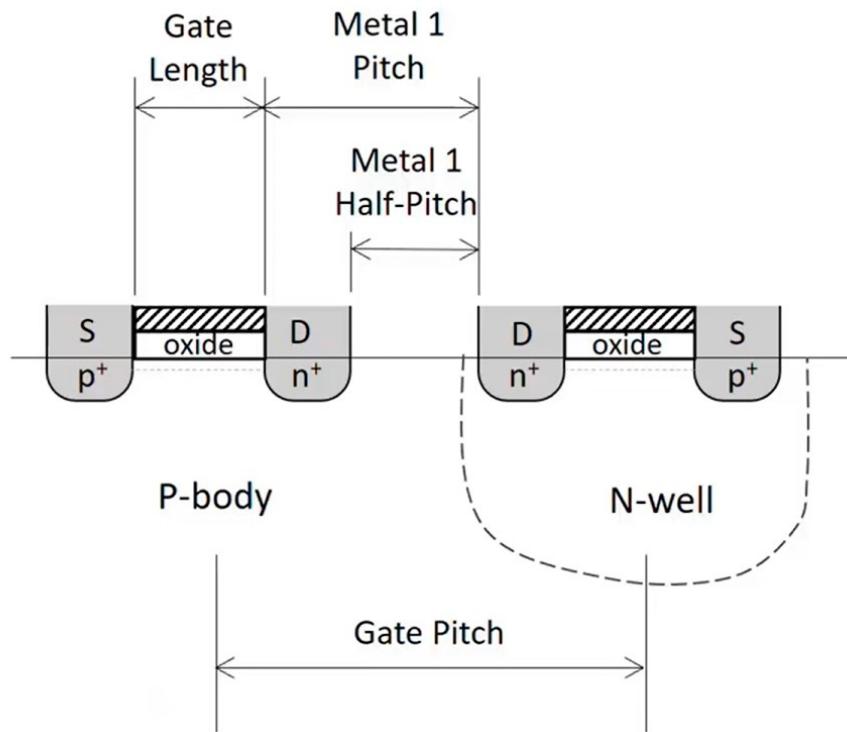
GAAFET
(Nanowire)



MBCFET™
(Nanosheet)

- MBCFET™ technology could lead to 45% less space than the latest 7nm FinFET transistors, and is expected to bring about around 50% power consumption savings and approximately 35% performance improvements.
- The width of nano sheets can be adjusted according to the chip features.
- MBCFET™ is highly compatible with conventional FinFET processes.

Technology node – refers to the gate length and the metal half-pitch, which until about 2000 were about equal.



Technology node is no longer a meaningful indication of feature size

- Metal Half-Pitch has not been shrinking as aggressively as Gate Length
- Gate length reduction is superseded by 3D FINFETs

The processor in a new smartphone was fabricated at the 7 nm technology node.
100 million transistors/mm²

7 nm node

Released in

2018 by TSMC

2019 by Samsung

2021 by Intel

Uses FINFETs

Gate length 8-10 nm (same as the 5 nm node)

Manufactured with extreme ultraviolet (EUV) lithography

Moving forward with a new technology designation

The LMC Method – a big picture approach

Logic Density, D_L

Main Memory Density, D_M

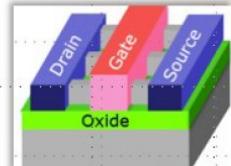
Interconnects Density, D_C

Watch for the IEEE International Roadmap for Devices and Systems (IRDS) to adopt a new strategy soon.

Device Roadmap and Technology Anchors for More Moore Scaling

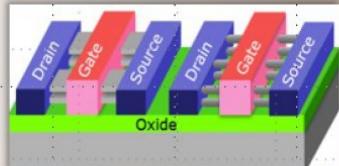
YEAR OF PRODUCTION	Edition	2023	2025	2028	2031	2034	2037
	New	2022-FF+	2025-LGAA	2028-LGAA	2031-CFET	2034-CFET	2037-CFET
	Updated	G48M24	G45M20	G42M16	G40M16	G38M16/T2	G38M14/T4
<i>Logic industry "Node Range" Labeling</i>	Updated	"3nm+"	"2nm"	"1.5nm"	"10nm eq"	"7nm eq"	"5nm eq"
<i>Fine-pitch 3D integration scheme</i>	Updated	Stacking	Stacking	Stacking	3DVLSI	3DVLSI	3DVLSI
<i>Logic device structure options</i>	Updated	finFET LGAA	LGAA	LGAA	LGAA-3D CFET	LGAA-3D CFET	LGAA-3D CFET
<i>Backside structure options</i>	New	-	Backside via	Direct contact	Decap+ESD	Active devices	Active devices
<i>Platform device for logic</i>	Updated	finFET	LGAA	LGAA	CFET	CFET	CFET
	Updated						
LOGIC TECHNOLOGY ANCHORS							
Device technology inflection	Updated	Taller fin	LGAA	LGAA	CFET Low-Temp Device	Low-Temp Device	Low-Temp Device
Patterning technology inflection for Mx interconnect		193i, EUV DP	193i, EUV DP	193i, High-NA EUV	193i, High-NA EUV	193i, High-NA EUV	193i, High-NA EUV
Specialty transistors add-ons	Updated	-	-	2D, IGZO	2D, IGZO	2D, IGZO	2D, IGZO
Local interconnect inflection	Updated	Self-Aligned Vias	Backside Via	Backside contact Substractive metal	Tier-to-tier via Active interconnect	Tier-to-tier via Active interconnect	Tier-to-tier via Active interconnect
Process technology inflection	Updated	Channel, RMG	Lateral/AtomicEtch	Low-temp contact	3DVLSI	3DVLSI	3DVLSI
Stacking generation inflection	Updated	3D-stacking, Mem-on-Logic	3D-stacking, Mem-on-Logic	3D-stacking, Mem-on-Logic	3D-stacking, CFET, 3DVLSI	3D-stacking, CFET, 3DVLSI	3D-stacking, CFET, 3DVLSI

FinFET
2011-2025



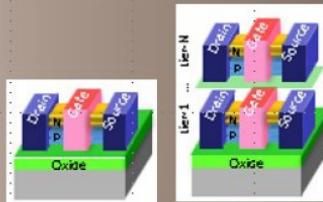
- Increasing drive by taller fin
- Better channel control for better perf-power

Lateral GAA
2025-2037



- Increasing drive by stacked devices
- Better channel control for better perf-power
- Reduced footprint stdcell

3D VLSI
2031 - 2037



- Monolithic NMOS-over-PMOS
- Sequential integration of multi-device tiers

Number of Semiconductor Manufacturers with a Cutting Edge Logic Fab											
SilTerra											
X-FAB											
Dongbu HiTek											
ADI	ADI										
Atmel	Atmel										
Rohm	Rohm										
Sanyo	Sanyo										
Mitsubishi	Mitsubishi										
ON	ON										
Hitachi	Hitachi										
Cypress	Cypress	Cypress									
SkyWater	SkyWater	SkyWater									
Sony	Sony	Sony									
Infineon	Infineon	Infineon									
Sharp	Sharp	Sharp									
Freescale	Freescale	Freescale									
Renesas (NEC)	Renesas	Renesas	Renesas	Renesas							
Toshiba	Toshiba	Toshiba	Toshiba	Toshiba							
Fujitsu	Fujitsu	Fujitsu	Fujitsu	Fujitsu							
TI	TI	TI	TI	TI							
Panasonic	Panasonic	Panasonic	Panasonic	Panasonic	Panasonic						
STMicroelectronics	STM	STM	STM	STM	STM						
HLMC	HLMC		HLMC	HLMC	HLMC						
IBM	IBM	IBM	IBM	IBM	IBM	IBM					
UMC	UMC	UMC	UMC	UMC	UMC				UMC		
SMIC	SMIC	SMIC	SMIC	SMIC	SMIC				SMIC		
AMD	AMD	AMD	GlobalFoundries	GF	GF	GF	GF				
Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung
TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC
Intel	Intel	Intel	Intel	Intel	Intel	Intel	Intel	Intel	Intel	Intel	Intel
180 nm	130 nm	90 nm	65 nm	45 nm/40 nm	32 nm/28 nm	22 nm/20 nm	16 nm/14 nm	10 nm	7 nm	5 nm	

Career Aspects

Major Industries in Electronics Using Nanotechnology in their Products

- **Samsung®**
- **AMD®**
- **a123systems**
- **Starkey, Inc.**
- **Multiple Manufacturers**
- **IBM®**
- **Apple®, Inc.**
- **Intel®**
- **Eikos® Inc.**
- **IOGEAR®, Inc.**
- **Lenovo**
- **LG® Electronics**
- **Asahi® Glass Co., Ltd.**

Career Aspects-Contd.

Various Positions in Electronics/ Electrical/ Communication Industries in the area of Nano scale fabrication, Micro/Nano electromechanical systems (in Engineering/Management domains). Some of them are given below:

- Service Engineer (Microscopy)
- Research Scientist (Materials – Photovoltaic's)
- Application and Business Support Engineer
- Research Assistant/Associate
- Solar Energy Competitive Intelligence Leader
- Development Engineer (Wafer Fabrication)
- Senior Wafer Fabrication Process Engineer (Etching)
- Senior Wafer Fabrication Process Engineer (Photolithography)
- Senior Research Engineer (Packaging Reliability)
- Senior Research Engineer (Circuit designer)
- Senior Research Engineer/Officer (Millimeter Wave and Modeling)
- Senior Research Engineer (MEMS Sensor Design)
- Market and Technology Development Manager