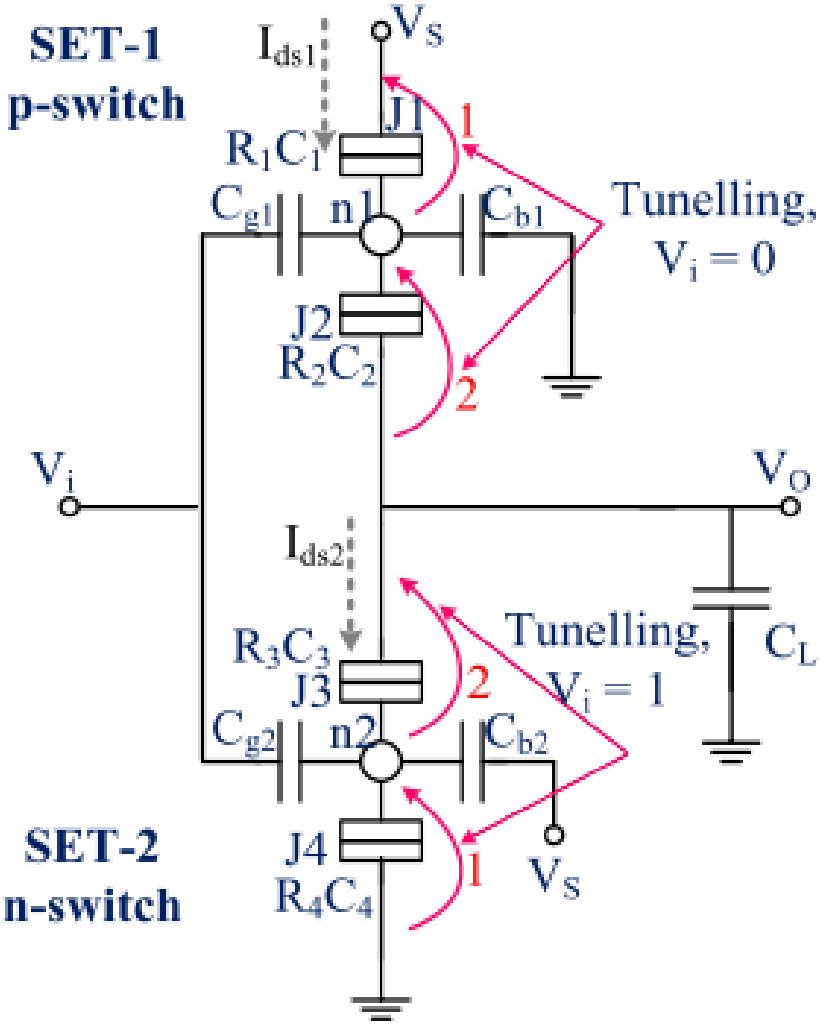
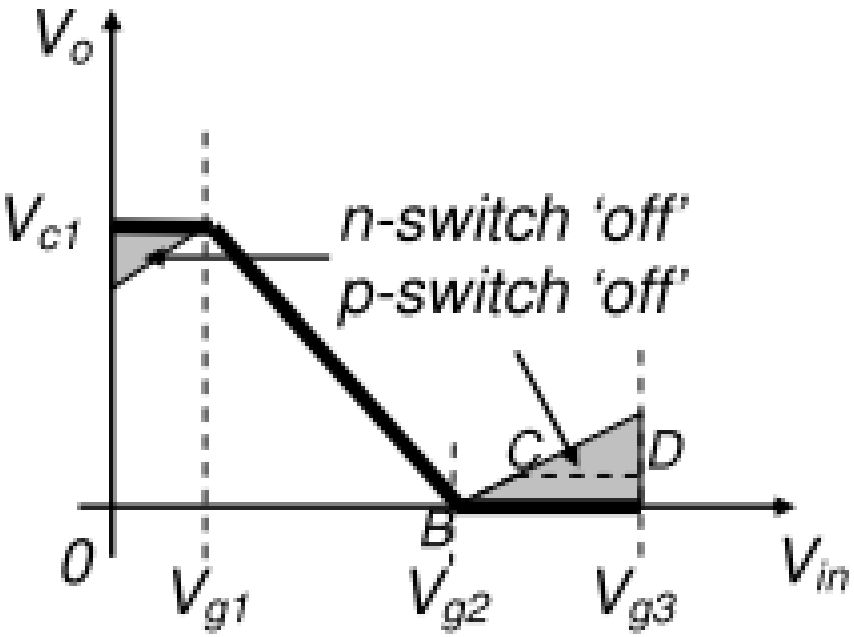
SINGLE ELECTRON TRANSISTOR CIRCUITS

SET INVERTER



SET INVERTER CIRCUIT



SET INVERTER TRANSFER CHARACTERISTICS

Complementary SET NAND and NOR gates

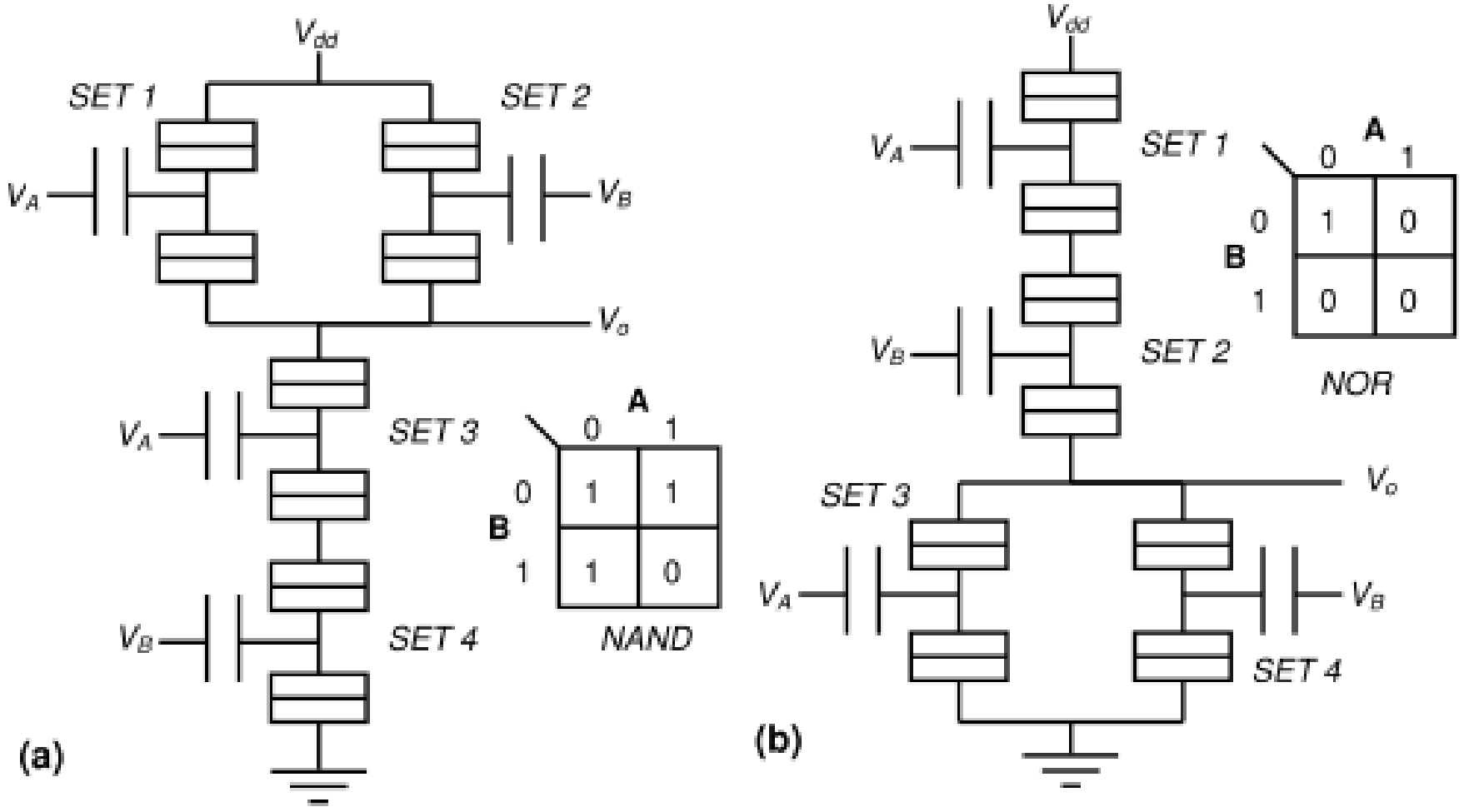
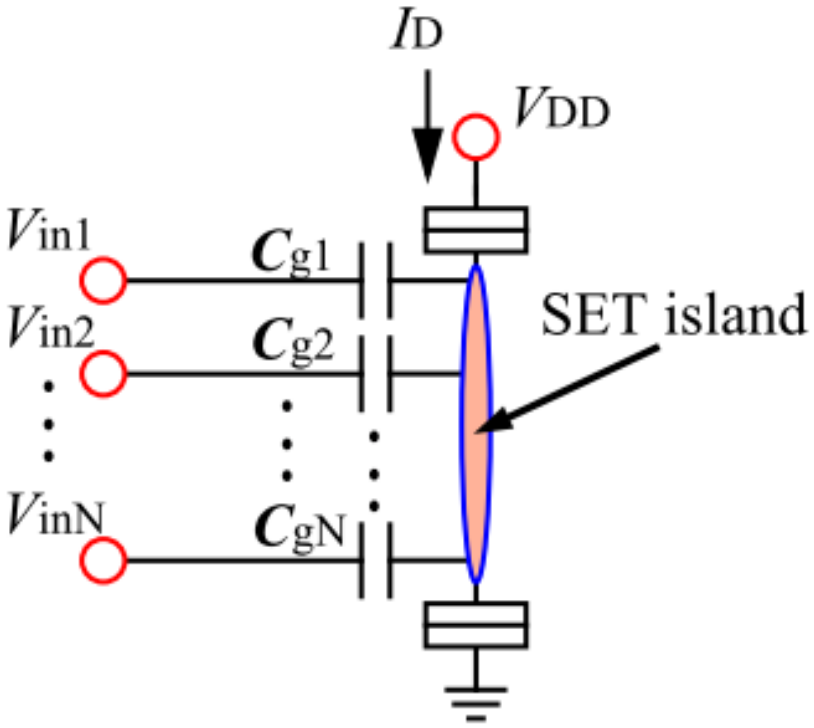
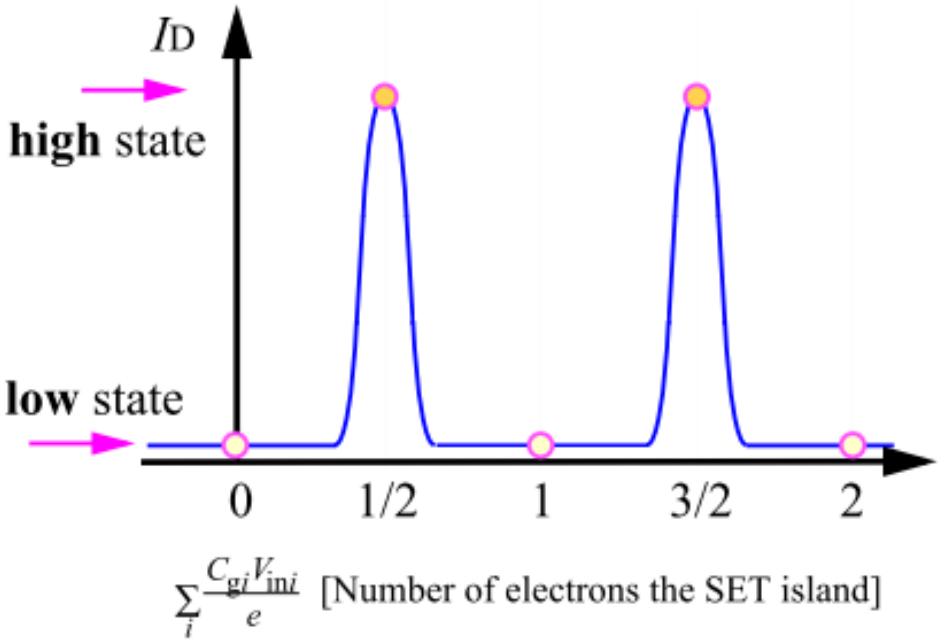


Fig. 6.6 Complementary SET gates. (a) NAND gate. (b) NOR gate.

Exclusive-OR gate



Equivalent circuit of a multigate SET

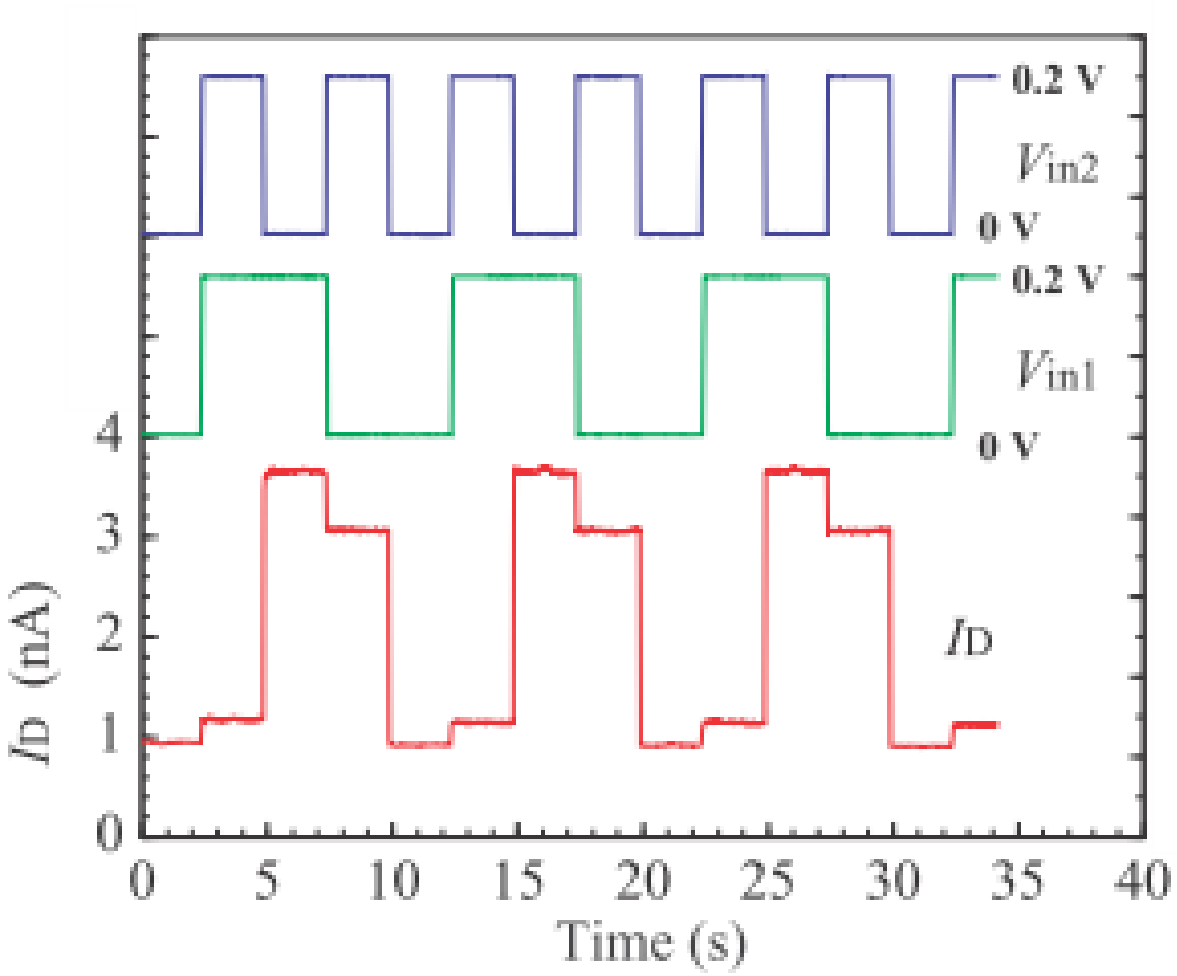


Typical current vs. input gate voltage characteristics of a multigate SET

In this device with N input gates, the drain current is determined by

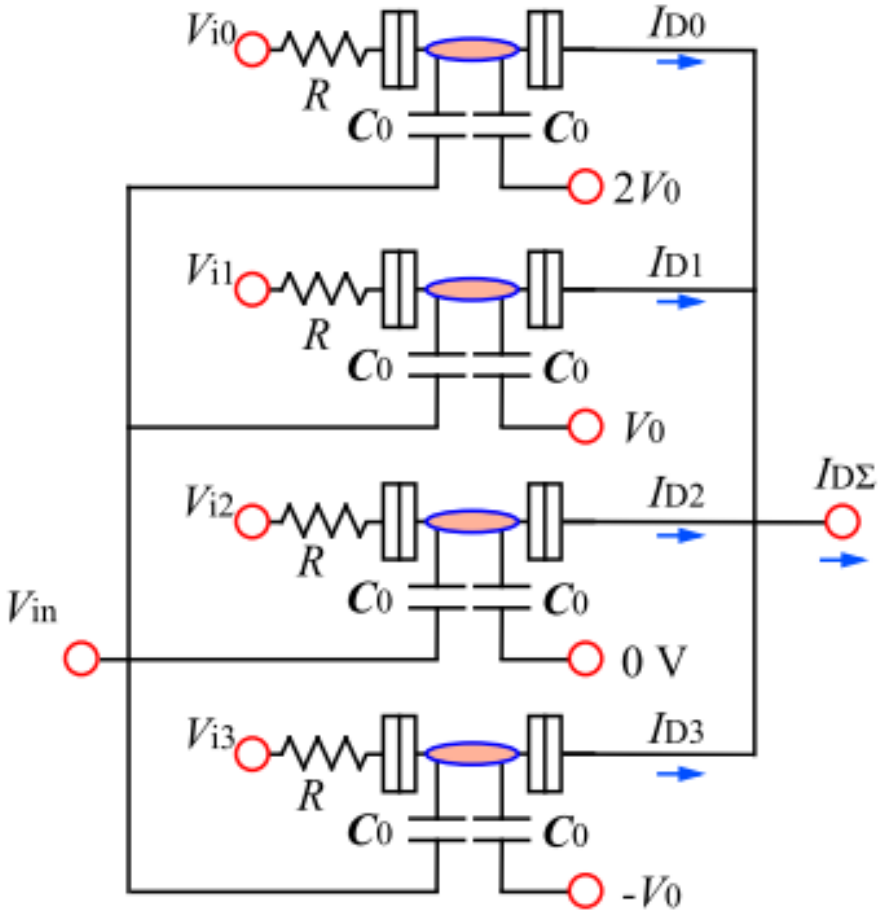
$$I_D(V_{in1}, V_{in2} \cdots V_{ini} \cdots V_{inN}) = f(\sum_i^N C_i V_{ini}/e)$$

Exclusive-OR gate



Current switching characteristics of the SET when the input-gate voltages (Vin1 and Vin2) were switched between 0 and 0.2 V

T-gate: multiple-valued multiplexer



Equivalent circuit of a T-gate for radix-4 that uses four dual-gate SETs.

$$V_{out} = V_{i0} \quad \text{when } V_{in} = 0,$$
$$V_{out} = V_{i1} \quad \text{when } V_{in} = V_0,$$
$$V_{out} = V_{i2} \quad \text{when } V_{in} = 2V_0,$$
$$V_{out} = V_{i3} \quad \text{when } V_{in} = 3V_0$$

Proposed T-gate for radix-4 which can produce any output pattern depending on the input signals in radix-4.

Adder

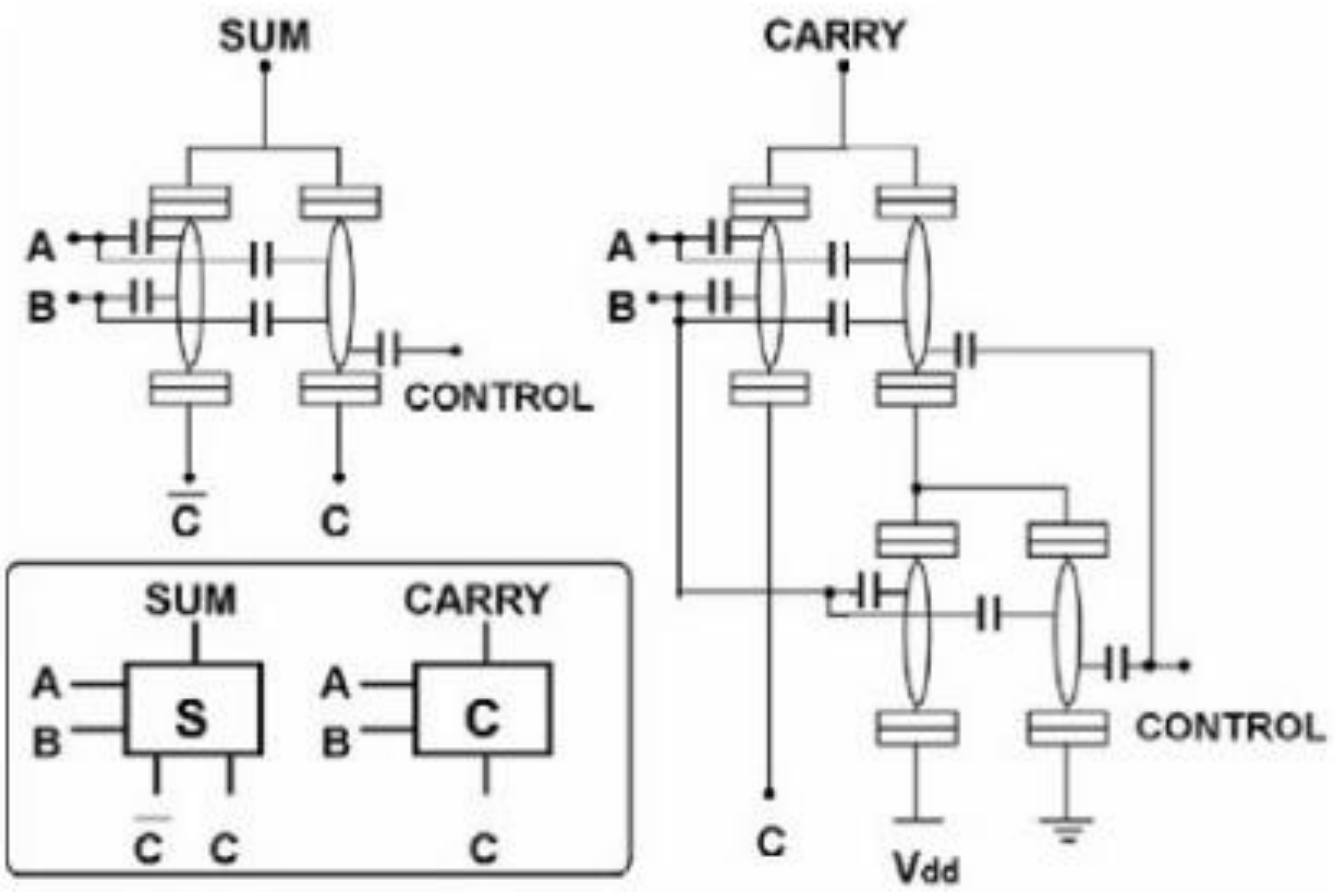


FIGURE 11.20 Equivarent circuits for sum-bit and carry-bit. The inset shows symbols for the sum and carry circuits.

Adder

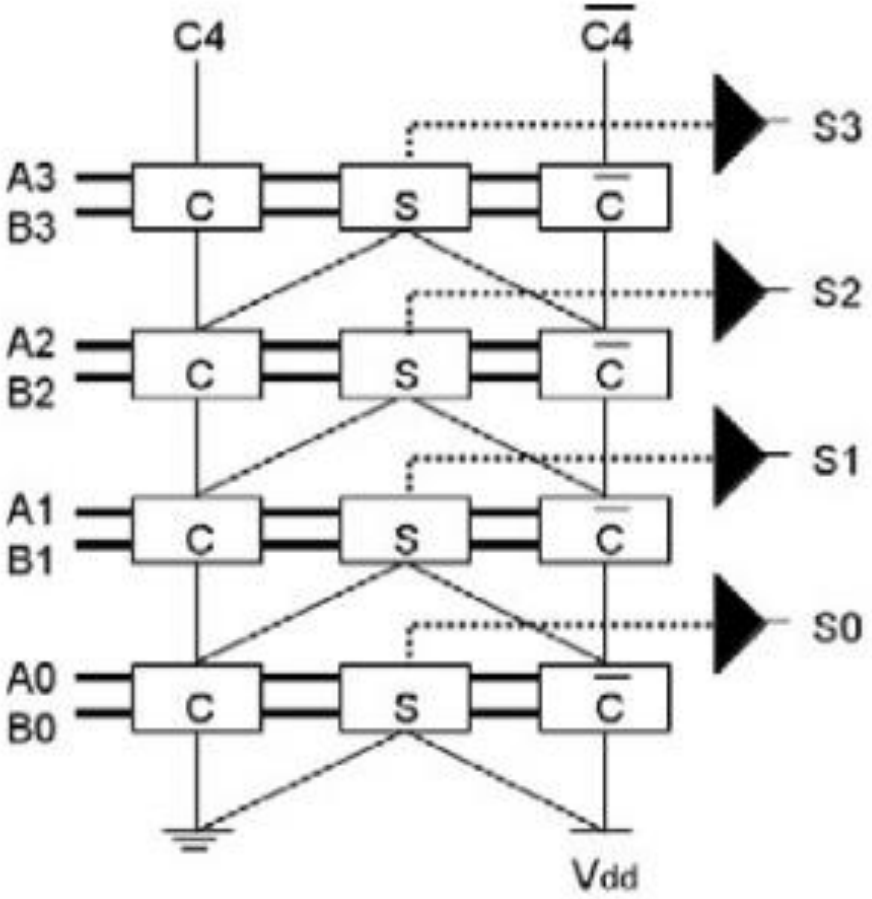


FIGURE 11.21 Structure of the 4-bit adder. The bold solid lines represent the input gates, and the fine solid lines the routes for the pass signals. The sum output nodes are shown by the dotted lines.

Multiple - Valued Operation

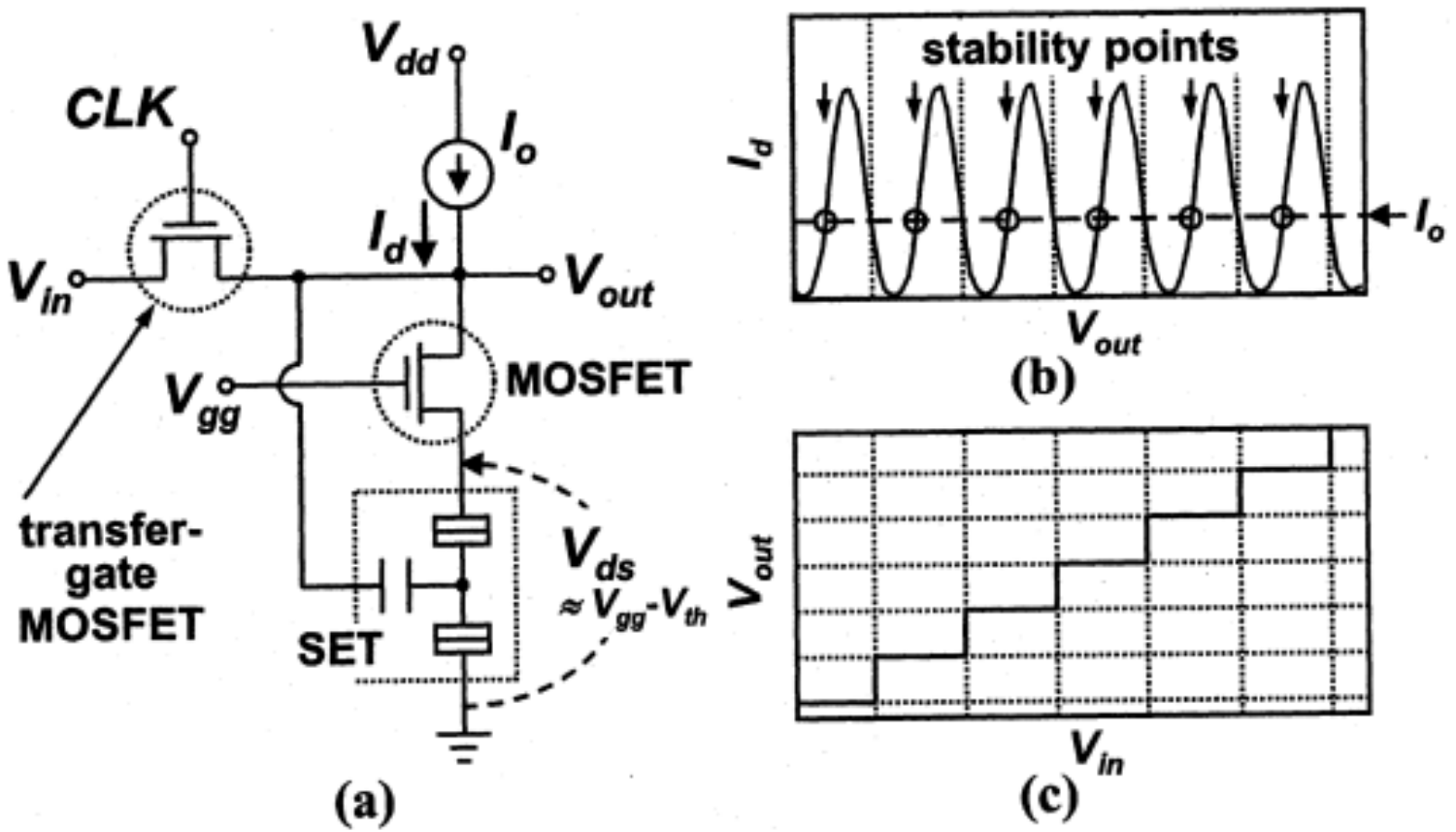


Fig. 2. (a) Schematic of the proposed quantizer (static memory). (b) Two-terminal I_d–V_{out} characteristics of the SET-MOSFET device with the SET gate shorted to the MOSFET drain. (c) Expected transfer (V_{in}–V_{out}) characteristics. V_{in} is transferred to V_{out} through the transfer gate MOSFET and is quantized to a stability point after the gate is cut off.

Digital communication transmitter system

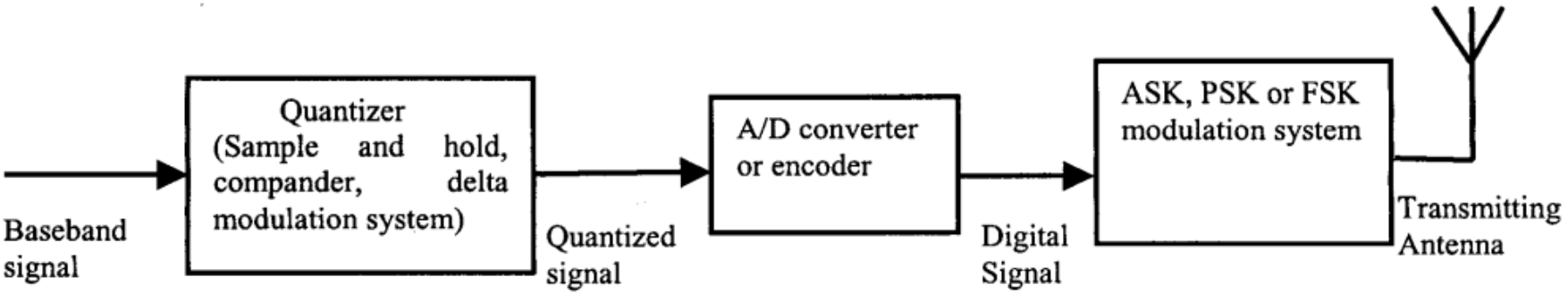
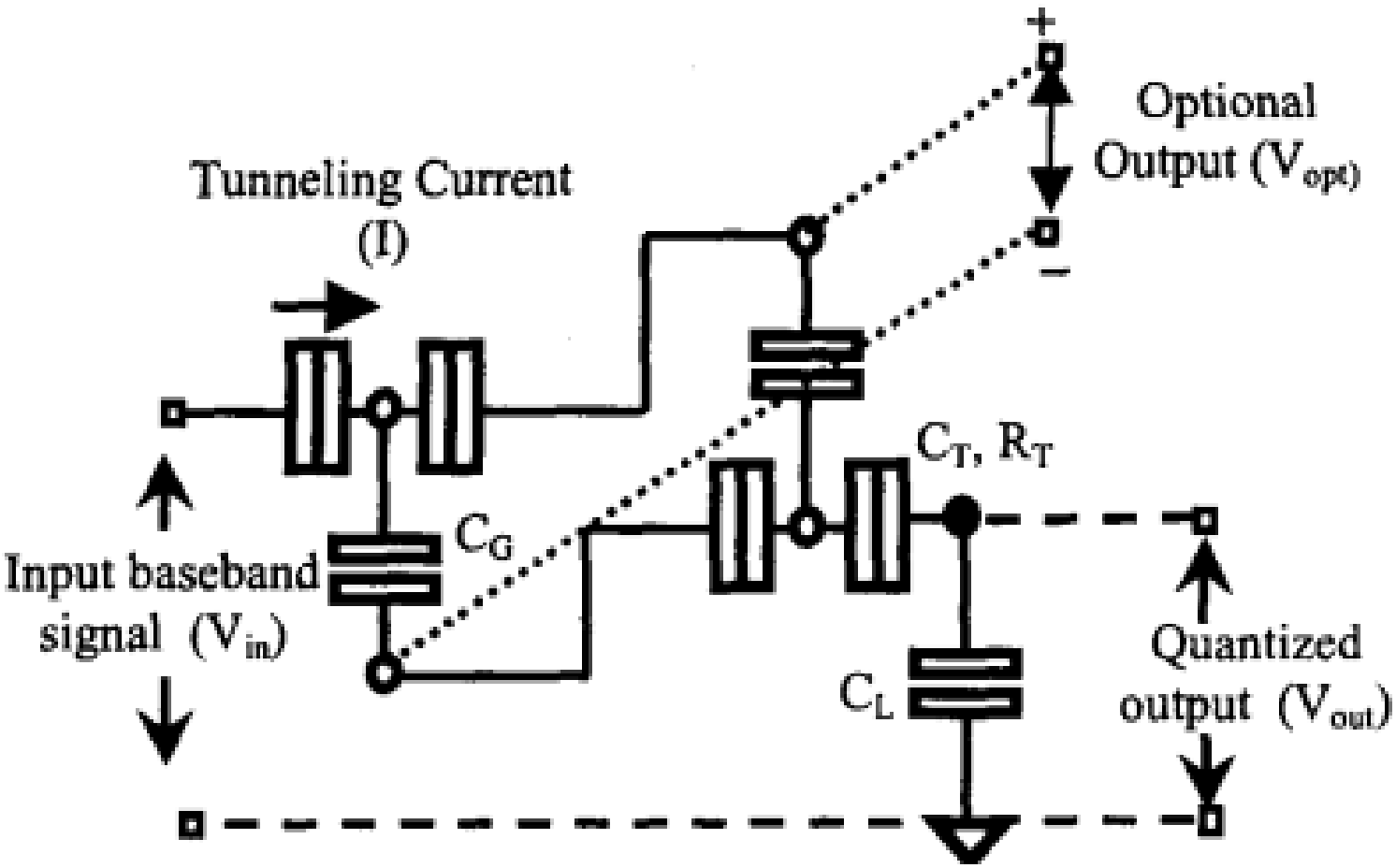


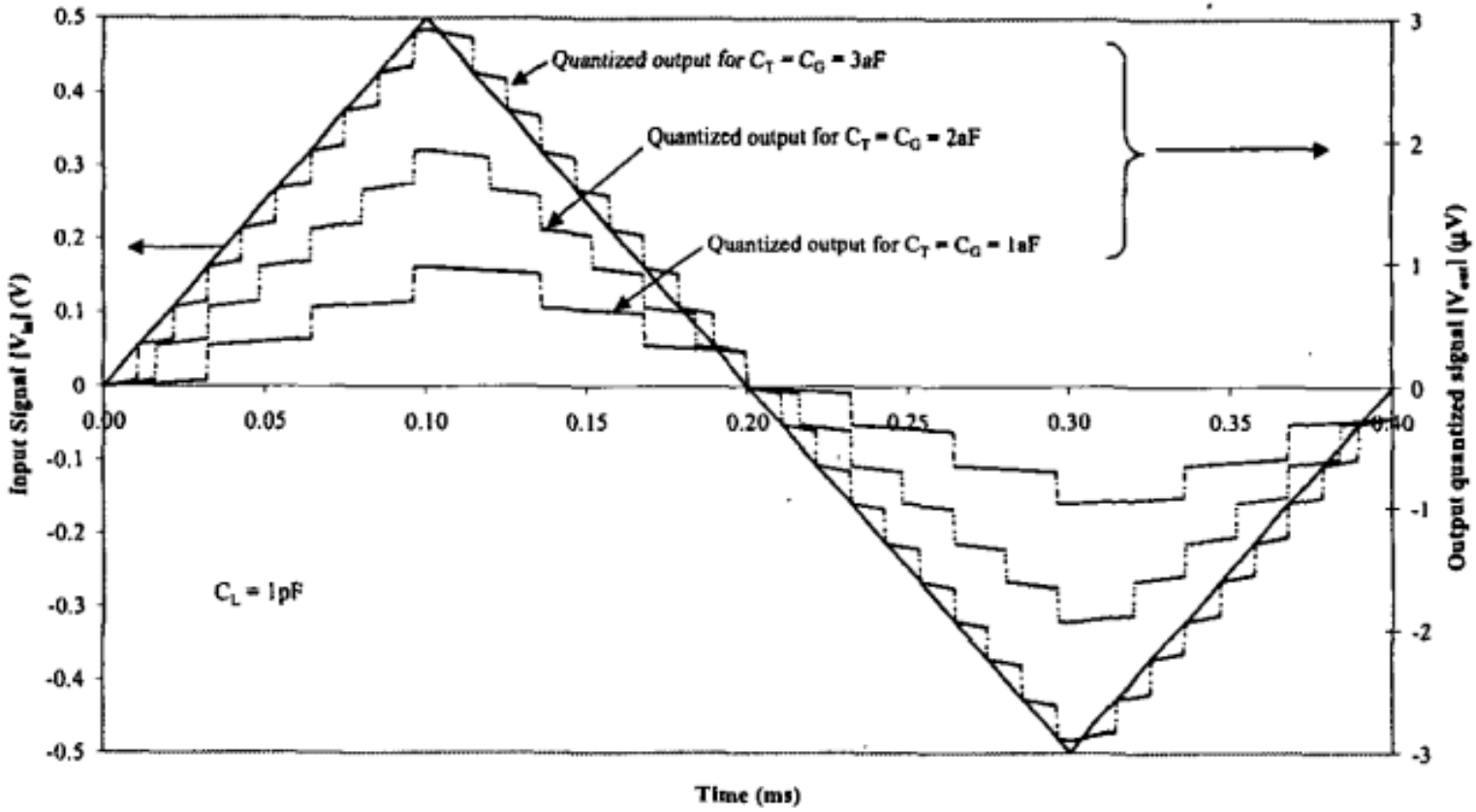
Fig. 1. Block diagram of a simple digital communication transmitter system

Quantizer

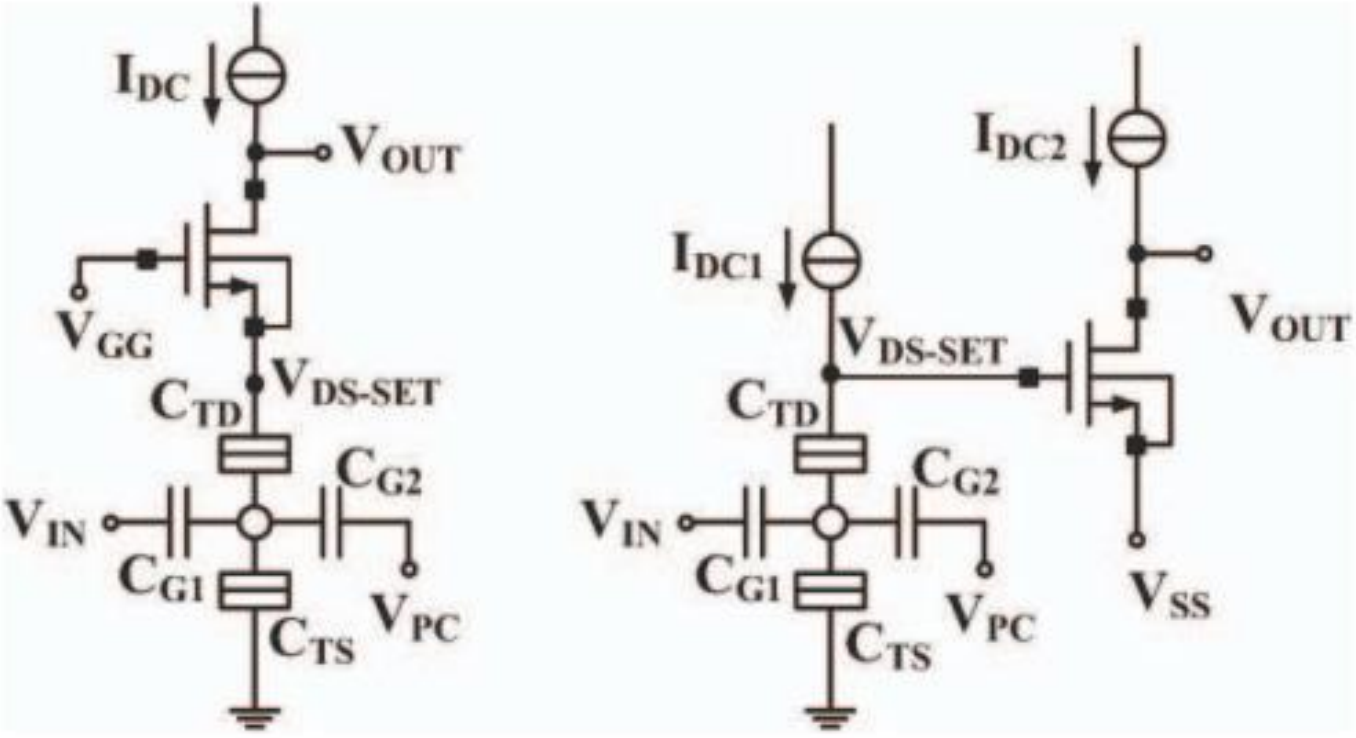


Circuit diagram of the proposed SET-based quantizer:

Quantizer operation characteristics



Hybrid CMOS-SET Parallel Architectures



(a) (b)

Figure 1. Serial SETMOS (a) and parallel SETMOS (b).

gic gates

Gate	V_{IN-A}	V_{IN-B}	V_{DS-SET}	V_{OUT}
AND	V_L-0	V_L-0	V1	V_L-0
	V_L-0	V_H-1	V5	V_L-0
	V_H-1	V_L-0	V5	V_L-0
	V_H-1	V_H-1	V0	V_H-1
NOR	V_L-0	V_L-0	V0	V_L-0
	V_L-0	V_H-1	V3	V_L-0
	V_H-1	V_L-0	V3	V_L-0
	V_H-1	V_H-1	V4	V_L-0
XOR	V_L-0	V_L-0	V5	V_L-0
	V_L-0	V_H-1	V0	V_H-1
	V_H-1	V_L-0	V0	V_H-1
	V_H-1	V_H-1	V2	V_L-0

Parallel SETMOS with three-gate SET transistor

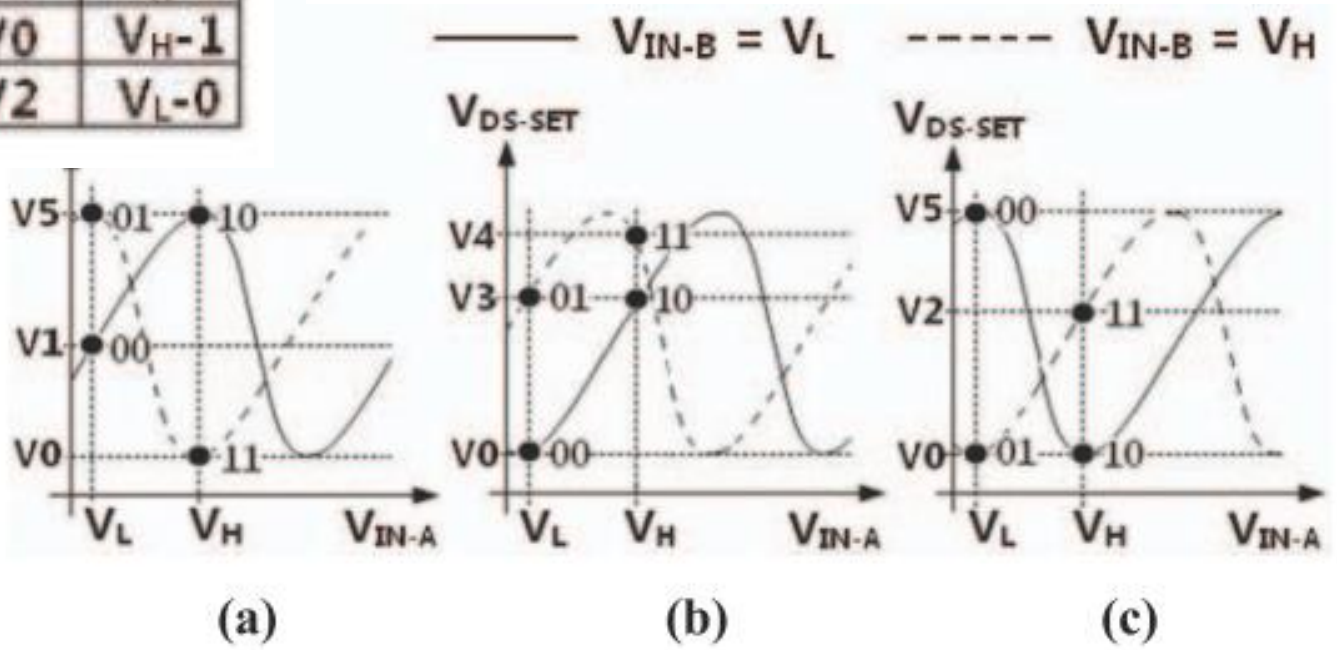


Figure 3. Imlementation of AND logic (a), NOR logic (b) and XOR logic (c).

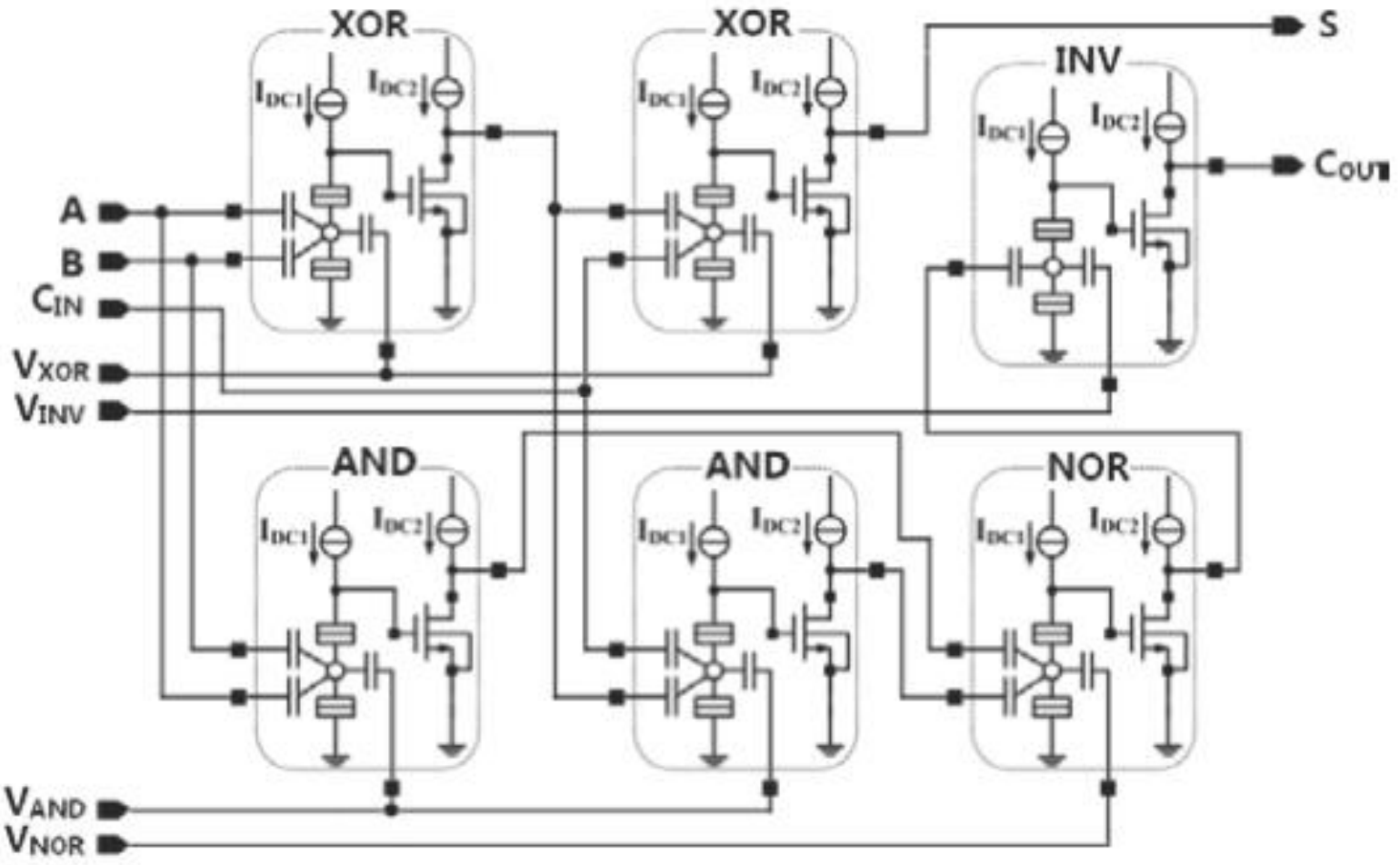


Figure 5. Boolean-logic-based hybrid CMOS-SET full adder.

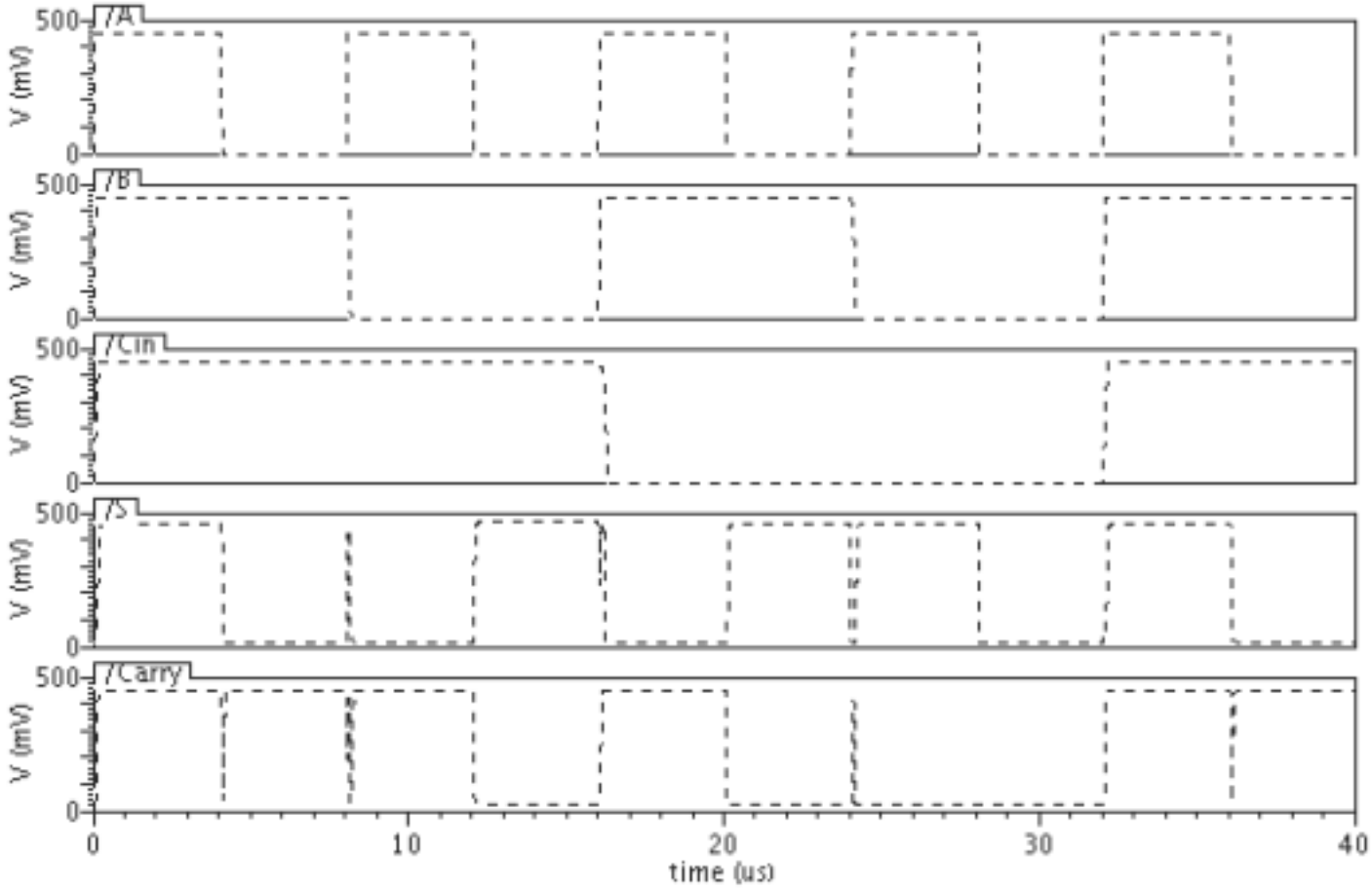


Figure 10. Simulation results of Boolean-logic-based hybrid CMOS-SET FA.

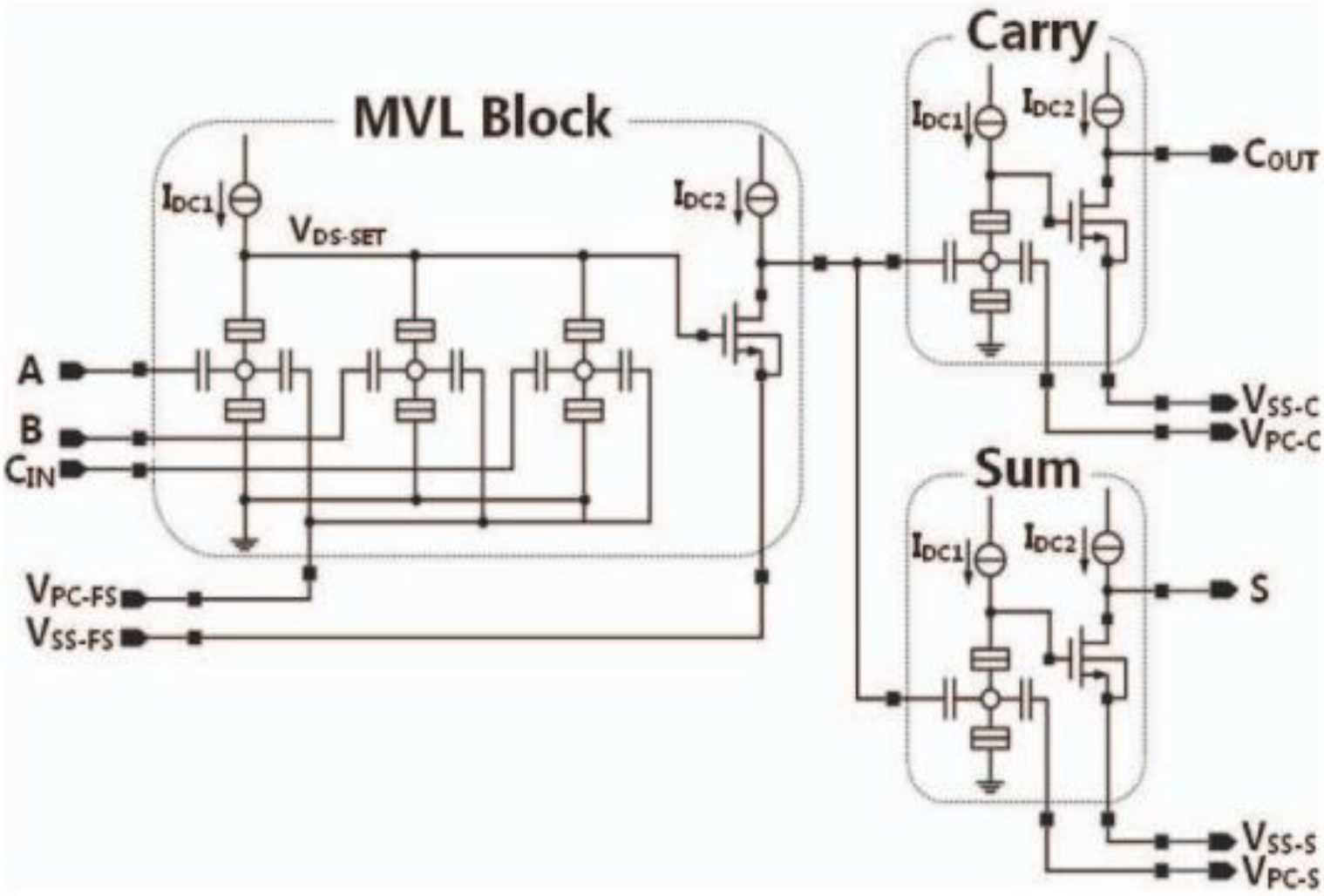


Figure 9. The MVL-based hybrid CMOS-SET full adder.

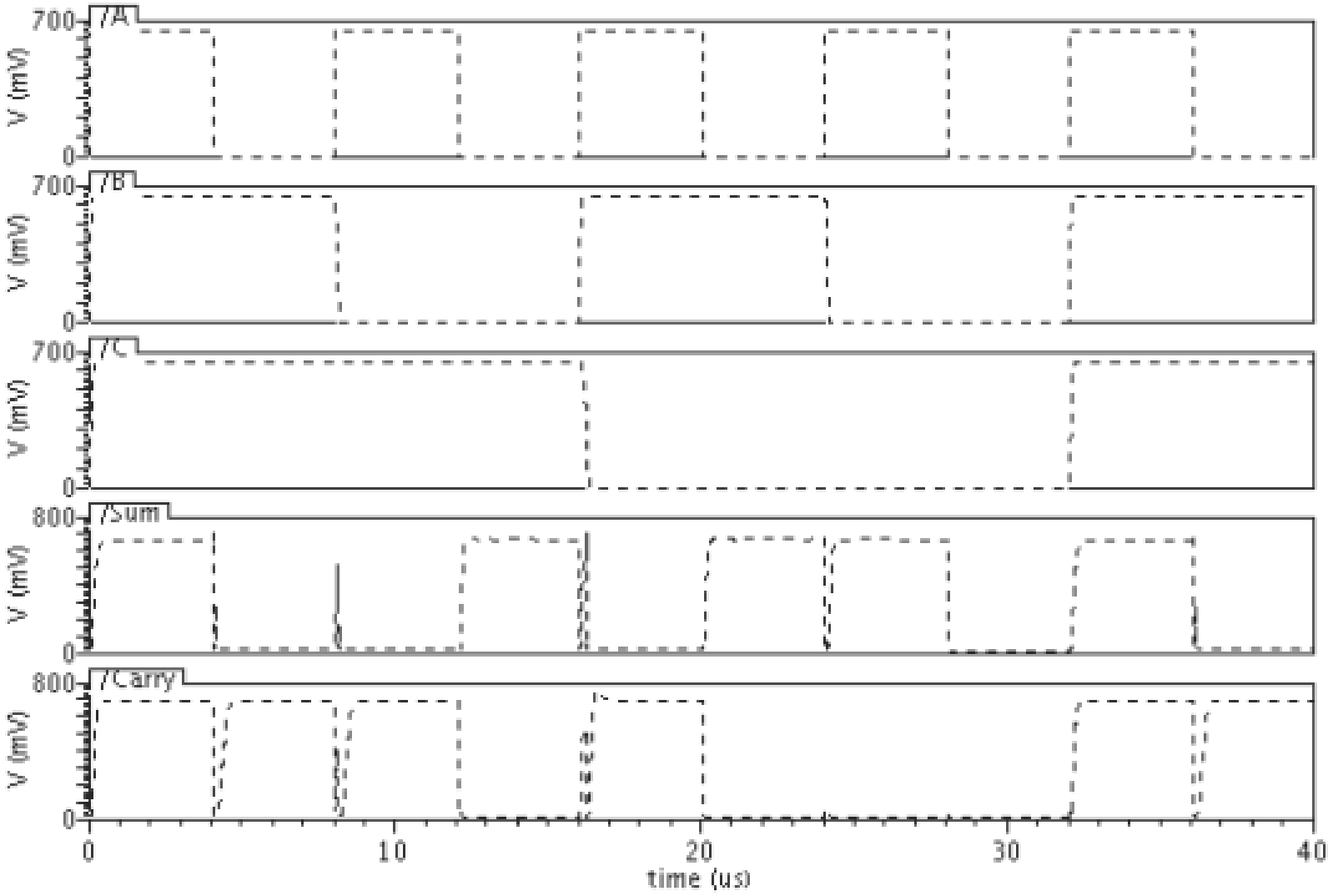


Figure 11. Simulation results of MVL-based hybrid CMOS-SET FA