EL 453 Nanoelectronics

Course Placement: Nanoelectronics is an Elective course for fourth year (7th semester) of B.Tech ICT program**,** M.Tech ICT 3rd Semester.

Course format: It is 3 hours lectures every week.

Prerequisite courses: Basic electronics ckt. (EL103)

Course content:
The course on fundamentals of nanoelectronics is to aid the student understand the origin of a number of new exciting development in this field and empower them to take advantage of the opportunities ahead of them. The term nanoelectronics encompasses developments in electronics that entail device physics and structures below the 100 nm level.

The first part of the course covers ITRS predictions about emerging research devices, the limitations of nano CMOS and various options to MOSFET optimization. The next part covers the definition of the term nanoelectronics and its relationship to the broader topic of nanotechnology. Following this, the topic begins with an introduction to the principles of quantum mechanics, the wave particle duality, wavefunctions and Schrödinger's equation, energy bands, electrical conduction and low-dimensional structures. Then, the course discusses on the emerging research devices for nanocircuits, their long-range potential, technological maturity and challenges. The objective is to pursue long term alternative solutions to technologies addressed in More-than-Moore ITRS entries.

Books and literature:

1. Book title: Nanoelectronics: Physics, Technology and Applications, by Rutu Parekh and Rasika Dhavse, IOP publisher, UK.
2. Research papers.

Course Outcomes:
Students will gain knowledge about the future trends in the technology, the physics behind the devices, its implementation and use in circuits. The objective is to give them vision about the latest in technology and future predictions. This can open many avenues for their future career.

In addition, they will work in group and conduct research in the area of emerging technology, perform simulation, analyze and discuss the results. If possible, publish a research paper.

P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12
X	X	X	X	X	X	X	x	X	X	X	X

Grading Policy:

Mid Semester Exam: 30 %
Final Semester Exam: 40 %
Report writing & Presentation based on emerging technology: 30 %

Lecture Schedule

Detailed Course Contents		
Topic Name	**Contents**	**No. of lectures**
Physical and Technological Limitations of nano CMOS Devices to the End of the Roadmap and Beyond	International Technology Roadmap of Semiconductors Acceleration and Issues Limitations and Showstoppers Coming from CMOS Scaling Technological Options to MOSFET Optimization	2
Introduction and Overview of Nanoelectronics	What is nanotechnology and nanoelectronics? Evolutionary and revolutionary developments	2
Introduction to the quantum theory of solids	Principles of quantum mechanics Schrodinger's wave equation Meaning, boundary conditions and application Allowed and forbidden energy bands Electrical conduction in solids Fermi statistics in metals and semiconductors Low-dimensional structures Superconductivity	5
Simulation and Modeling		2

Emerging research devices for Nanocircuits	Extending MOSFETs to the End of the Roadmap Carbon nanotubes and graphene for data processing Electronic properties Synthesis and fabrication Interconnects Field effect transistors Carbon nanotube circuits Nanotubes for memory application All-carbon nanoelectronics prospects Channel Replacement Devices Tunnel FET	11
	Quantum dots, wires and wells Physical Principles Single electron effect quantum confinement, tunneling effect, and Coulomb blockade Fabrication Bottom-up preparation Top-down preparation Applications	4
	Charge-Based Beyond CMOS: Non-Conventional FETs and Other Charge-Based Information Carrier Devices Single electron transistor (SET) Operation SET-CMOS hybridization Circuits and implementation NEMS Devices Atomic switch and memristor MOTT FET Spin FET and Spin MOSFET transistors	12
	Alternative Information Processing Devices Nanomagnetic and all spin logic Spin wave devices	3
Tentative topics	Emerging memory devices	3
	Emerging architecture	2