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Logic gates with a single graphene transistor

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The operation of four basic two-input logic gates fabricated with a single graphene transistor is demonstrated. Single-transistor operation is obtained in a circuit designed to exploit the charge neutrality point of graphene to perform Boolean logic. The type of logic function is selected by offset of the input digital signals. The merits and limitations of the fabricated gates are assessed by comparing their performance with that of conventional logic gates. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3079663]

The exponential decrease in the minimum feature size of integrated circuits[1] initiated a search for novel materials and devices at the nanometer scale. Nanoelectronic devices based on carbon nanostructures, such as carbon nanotubes (CNTs) and graphene, are a promising alternative to Si-based devices due to their small size and extraordinary properties.[2,3] Although CNTs are now well-established as efficient channels for field-effect transistors (FETs) (Ref. 4) they have not been successfully implemented in large-scale integration electronics mainly due to a difficulty in their precise positioning on a chip.[5] Graphene, if epitaxially grown,[6,7] transfer printed,[8] or deposited from a solution[9] on a large wafer, does not suffer from this limitation as it can be patterned by Si-compatible lithographic techniques.[10] The high mobility of carriers in graphene[11,12] could allow fabrication of transistors operational in a sub-10 nm regime in which the ultimate limits of Si technology would probably be reached.[13] However, intrinsic graphene is a semimetal,[14] implying a very small current on/off ratio of graphene transistors.[15] If graphene devices were to replace conventional Si devices, new approaches in bandgap engineering[10,16–18] or circuit design would be needed, with the most attractive possibility being to implement the same functionality with fewer transistors.[19–22] Here we demonstrate the latter approach by realizing four basic logic gates with just one graphene transistor. This was obtained by exploiting the existence of a maximum in the transfer resistance of a graphene transistor. Most of the fabricated logic gates, such as the exclusive OR (XOR) gate, require at least four conventional FETs.[23,24]

The fabricated device is shown in Fig. 1. Graphene flakes were deposited by mechanical exfoliation of highly oriented pyrolitic graphite on a highly doped Si substrate with 300 nm of thermally grown dry SiO_2 on top.[14] The flakes were exfoliated by wafer dicing tape as it leaves almost no adhesive residue on the substrate. The flake shown in Fig. 1 was identified as monolayer graphene by Raman spectroscopy.[25] The flake was contacted by four Cr(5 nm)/Au(50 nm) electrodes patterned by e-beam lithography. The electrical measurements were performed in a conventional FET configuration, with two neighboring electrodes acting as source and drain contacts, the other two electrodes not connected, and metal contact evaporated on the back of the substrate as gate.

The measured resistance R between the source and drain contacts on the monolayer graphene as a function of the applied back-gate voltage V_G is shown in Fig. 2. Monolayer graphene not subjected to further treatment generally shows p-type behavior at small gate voltages, which has been attributed to hole doping by physisorbed ambient impurities such as water[14] and oxygen.[26] In doped samples the transition between p- and n-type conduction occurs not at zero but at a positive gate voltage, as seen in Fig. 2 where the resistance peak is shifted to $V_G = 22.85$ V. Due to a small overlap between valence and conduction bands and formation of electron-hole puddles,[27] graphene undergoes ambipolar transition without carrier depletion, in contrast with semiconducting CNTs.[28] As a consequence, graphene transistors cannot be turned off and they do not exhibit the drain current saturation effect as conventional FETs do.[29] Instead, they stay in the Ohmic regime even at very large drain biases, functioning as simple voltage controlled resistors whose resistance R depends solely on the applied gate voltage V_G. In addition, the change in drain current I_D caused by the change in the gate voltage V_G is relatively small. In the investigated drain-source (two-probe) configuration, this change is further suppressed because the resistance R includes also lead and contact resistances that limit the maximum drain current at a given drain voltage V_D.[30] In the investigated sample, the total contact resistance of all four electrodes was found to be 2.2 kΩ. In order to evaluate the upper limit of performance of the suggested logic gates, samples were measured at cryogenic temperatures. At higher temperatures the principle of

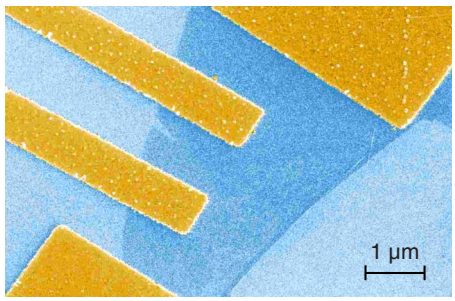

FIG. 1. (Color online) Scanning electron microscopy image of monolayer graphene contacted with four electrodes patterned by e-beam lithography. The two bottom contacts were used in the electrical measurements.

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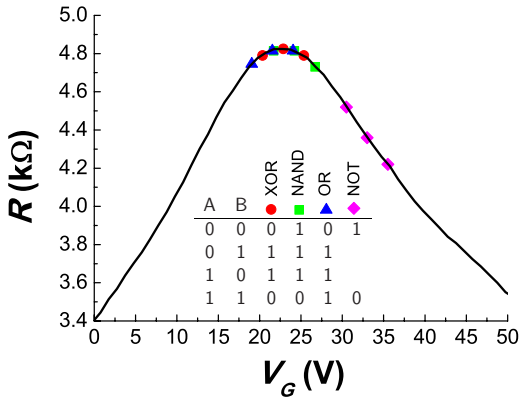

FIG. 2. (Color online) Transfer curve R vs V_G of the monolayer graphene shown in Fig. 1 at $T=1.5$ K. Three equidistant operating points (with a total gate voltage swing of 5 V), which correspond to different functions of the logic gate shown in Fig. 3, are marked by symbols. The offset V_I (V_G of the middle point) determines the type of the function. An XOR gate (circles) is obtained for $V_I=22.85$ V, a NAND gate (squares) for $V_I=24.20$ V, an OR gate (triangles) for $V_I=21.55$ V, and a NOT gate (rhombuses) for $V_I=33.00$ V. Inset: truth table of all presented gates. Logic levels A and B correspond to the digital inputs shown in Fig. 3.

operation will not be changed even though the change in resistance will be damped.

The existence of a maximum in the transfer curve R versus V_G can be exploited to design different logic gates with just one graphene transistor, as shown in Fig. 3. The input stage is designed such that the gate voltage V_G is an arithmetic mean of the two inputs, i.e., $V_G=(V_A+V_B)/2$. Since digital inputs V_A and V_B can have one of two discrete values: low V_L (Boolean 0) and high $V_H>V_L$ (Boolean 1), the gate voltage V_G can take one of three possible discrete values: V_L (both inputs 0), V_H (both inputs 1), and a value half way between $V_I=(V_L+V_H)/2$ (inputs different). If the voltage levels V_L and V_H are chosen such that the maximum of the transfer curve is at $V_G=V_I$ and R has a smaller (and identical) value at $V_G=V_L$ or V_H (these three operating points are denoted by circles in Fig. 2), then an XOR gate is obtained.[31] In this case, the resistance R is high (1) for different inputs and low (0) when both inputs are the same. Similarly,[32] a NOT-AND (NAND) gate is obtained if the voltage levels are chosen such that the resistance R is high for $V_G=V_L$ or V_I and low for $V_G=V_H$. An OR gate is obtained if the resistance R is low for $V_G=V_L$ and high for $V_G=V_I$ or V_H. Finally, a NOT gate is obtained if the resistance R is high for $V_G=V_L$ and low for $V_G=V_H$. The complete truth table of the designed logic gates is given in the inset of Fig. 2.

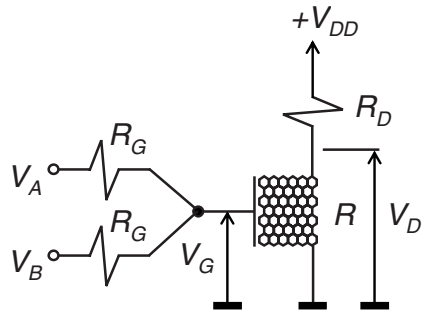

FIG. 3. A two-input (A and B) logic gate incorporating one monolayer graphene transistor. R is the output resistance of the graphene transistor, which depends on the gate voltage V_G (as shown in Fig. 2).

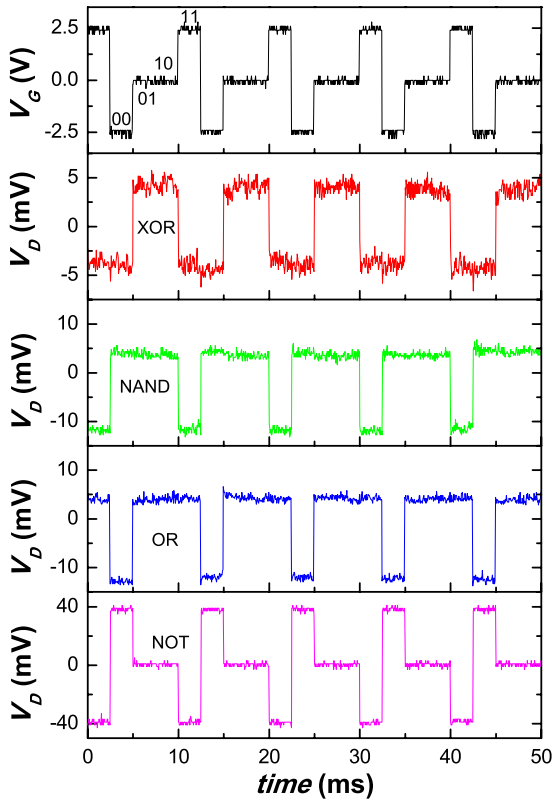

FIG. 4. (Color online) Digital waveforms measured on single-graphene-transistor logic gates with input voltage levels chosen as in Fig. 2, power supply $V_{DD}=5$ V, and pull-up resistor $R_D=4.8$ kΩ. All signals are plotted without offset values V_I (of the gate voltage V_G) and V_O (of the drain voltage V_D). The output offset in the XOR, NAND, and OR gate is $V_O\sim V_{DD}/2=2.5$ V and in the NOT gate is $V_O\sim 2.4$ V.

In order to be useful in a real digital circuit, the logic function must be presented as a change in voltage levels. For that purpose, the drain contact of the graphene transistor is connected via a pull-up resistor R_D to a supply voltage V_{DD}, which makes a simple voltage divider. The output drain voltage is then given by $V_D=V_{DD}/(1+R_D/R)$. Consequently, the output voltage V_D is low (high) if the resistance R is low (high). Figure 4 shows measured output drain voltages in logic gates in which the input voltage levels V_L and V_H and power supply V_{DD} are chosen to correspond to the voltage levels used in conventional complementary metal-oxide semiconductor (CMOS) circuits; the total gate voltage swing V_H-V_L and supply voltage V_{DD} are 5 V. The actual logic function is determined by the midvalue V_I, as shown in Fig. 2. The pull-up resistor R_D is chosen to maximize the output voltage swing. Since a change in drain voltage $\partial V_D/\partial R=R_D V_{DD}/(R+R_D)^2$ as a function of R_D has a maximum value at $R_D=R$, the value of $R_D=4.8$ kΩ, which corresponds to the resistance maximum in Fig. 2, is used in all measurements. Under these conditions, stable and separated output logic levels are obtained for all logic functions, as shown in Fig. 4. However, in all cases, the output drain voltage swing (e.g., 80 mV in case of a NOT gate) is much smaller than the input gate voltage swing (5 V) because of the very small voltage gain $A_v=\partial V_D/\partial V_G$ of the fabricated logic gates (in the whole range of the gate voltage $|A_v|<0.025$). Such a small gain is due to a very small change in the transfer resistance around the charge neutrality point

($\Delta R/R < 7\%$), i.e., due to inability to turn off the graphene transistor. Although small gain also suppresses noise, the logic gates do not have a noise margin, nor do they have a well defined threshold voltage as the gain is always less than 1. Moreover, small output voltage swing makes fabricated gates prone to noise, which can be seen from the waveforms in Fig. 4.

The main advantage of the proposed concept is the possibility of realizing different logic gates with just one graphene transistor. Although such a low transistor count seems very attractive, there are several other factors that should be considered in estimating a figure of merit. First, the present logic gates are always conducting, i.e., the output stage dissipates a static power, $V_{DD}^2/(R+R_D) \sim V_{DD}^2/(2R_D)$, in contrast with CMOS logic gates in which the output stage dissipates zero static power. The static dissipation could be reduced by using a graphene transistor with a higher resistance, but this would increase the output transient response time making this gate slower than a state-of-the-art CMOS gate,[33] whose output resistance is $\sim 736\ \Omega/(w/\mu\mathrm{m})$, where w/μm is the width of the transistor in micrometers. In the present case, the output resistance $R_O = R_D/2 = 2.4\ \mathrm{k}\Omega$ of the logic gate and the total parasitic capacitance $C_O \sim 3$ nF of the measurement equipment connected to the output limit the clock rate to $f_O = 1/(2\pi R_O C_O) \sim 22$ kHz, which was confirmed by measurements. In principle, by loading the output with a typical gate capacitance of $C_O \sim 10\ \mathrm{fF}(w/\mu\mathrm{m})$,[33] the clock rate of $f_O \sim 6.6$ GHz [for $(w/\mu\mathrm{m}) \sim 1$] could be obtained. Further increase in f_O by reduction in transistor length (to reduce R_O) will be hampered by contact resistance. As in CMOS technology, the clock rate will eventually be limited by power dissipation rather than intrinsic transistor parameters.[34] Second, if inputs are different then the logic gates dissipate additional static power $(V_H - V_L)^2/(2R_G) = V_{DD}^2/(2R_G)$ in the input stage. The input dissipation could be minimized by increasing the resistance R_G at the expense of increasing the input transient response time. Hence, there is a tradeoff between the total static dissipation and the highest possible clock rate both in the input and output stages. Third, input and output logic voltage levels are not the same, so the logic gates could not be cascaded without level shifters, which introduce additional transistors. This problem could be mitigated to some extent by decreasing the input voltage level V_I from the present value of ~ 23 V to $V_{DD}/2 \sim V_O$ by annealing the transistor.[35] Although annealing offers a simple way of tuning the position of the charge neutrality point, the resistance maximum of transistors exposed to air slowly drifts back to the original position. The permanent solution would be to use a thinner insulator with a higher dielectric constant,[36] in which the same charge is accumulated at lower gate voltages. However, resistance change cannot be increased by any of these methods so the mismatch between the input and output voltage swing would prevent direct cascading of the logic gates as long as gapless graphene is used.

In conclusion, four basic logic gates (XOR, NAND, OR, and NOT) are designed and fabricated with a single graphene transistor operated close to the charge neutrality point. The logic function is chosen by the choice of input logic voltage levels and operation of all logic gates is demonstrated. Although further improvements are required to approach the performance of conventional Si CMOS logic gates, the fabricated logic gates offer an attractive alternative to conventional gates due to their minimal transistor count.

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