EL527 ASIC Design (3-0-2-4)

Course Placement: ASIC Design is an Elective course for SEMESTER II M.Tech, ICT in VLSI and Embedded Systems program and SEMESTER VI/VIII B Tech (ICT and CS)

Course format: It is 3 hours lectures and 2 hours of laboratory every week.

Prerequisite courses: Basics of VLSI

Course Overview:

VLSI (Very Large Scale Integration) technology has emerged as a very important technology in modern electronics featuring deep sub-micron manufacturing processes, low voltage operations, exploding speeds and smart programmable devices sufficient enough to digest ambient conditions to extremes. The electronics industry worldwide is rapidly approaching another revolutionary leap in the global market scenario. Semiconductor technology has crossed the quarter-micron threshold, making tens of millions of transistors available on a single chip equipped with the powerful arm of VLSI design. This imparts the electronics industry a potential to create designs of incredible densities and lightning speeds while utilizing batteries to power them. This has had a phenomenal impact on widespread applications ranging from consumer electronics, communications, and defense to just about everything.

As part of Electronics India program by Govt. of India, most of the electronic products and semiconductor ICs are planning to make in India. This skill development program in VLSI Physical design will help to generate skilled manpower in IC design and manufacturing.

Course Content:

In this course, the individuals shall learn how to implement a design from RTL-to-GDSII. It will start by coding a design in VHDL or Verilog. Then simulate the coded design, followed by design synthesis and optimization. Further, run equivalency checks at different stages of the flow. After synthesizing the design, it will be followed by floorplan, and place-and-route the synthesized netlist while meeting timing. Gate-level simulation shall be run throughout the flow. Finally, write out a GDSII file.

Books and literature:

There is no text book for it. Students will use the material prepared by the instructor and online references.

Assessment method: Mid-semester, End semester examination, research based project and related presentations.

Course Outcomes:

Learn about the various ASIC architectures, ASIC design flow, issues in ASIC design and verification and its fix. The following are the highlights:

1. Describe architecture based on application specifications. Identify circuit topology. [P1 – P5]
2. Derive, design and define circuit parameters. [P1 – P5]

3. Write synthesizable RTL code. [P1-P3, P5]
4. Perform synthesis, process design flow, CTS, routing etc. [P1-P5, P9, P12]
5. Verifying and validating the integrated circuit at various stages of design. [P1-P5, P9, P12]
6. The final step is generating the GDSII file of the design that is sent to the foundry for fabrication. [P5]

P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12
X	X	X	X	X				X			X

Lecture Schedule

SI. No.	Description	No. of Lectures
1	Frontend design	3
2	Introduction to backend flow, Inputs and outputs of synthesis, Synthesis	5
3	Types of synthesis, Command flow of synthesis	4
4	Static timing analysis, Timing paths, Timing slack calculations	4
5	Constraint designing, Report analysis of timing paths, MMMC, OCV	4
6	Introduction to PD flow, Floor plan, Power plan	5
7	Placement, Types of Placement, Congestion	5
8	Clock tree synthesis, Clock skew, Clock tree optimization	4
9	Routing, Types of routing, Crosstalk	4
10	Physical Verification, Timing fixes	4
11	Project	Throughout the semester as lab component

Grading Policy:

Mid-Semester: 30 %
End-Semester: 40 %
Project: 30 %