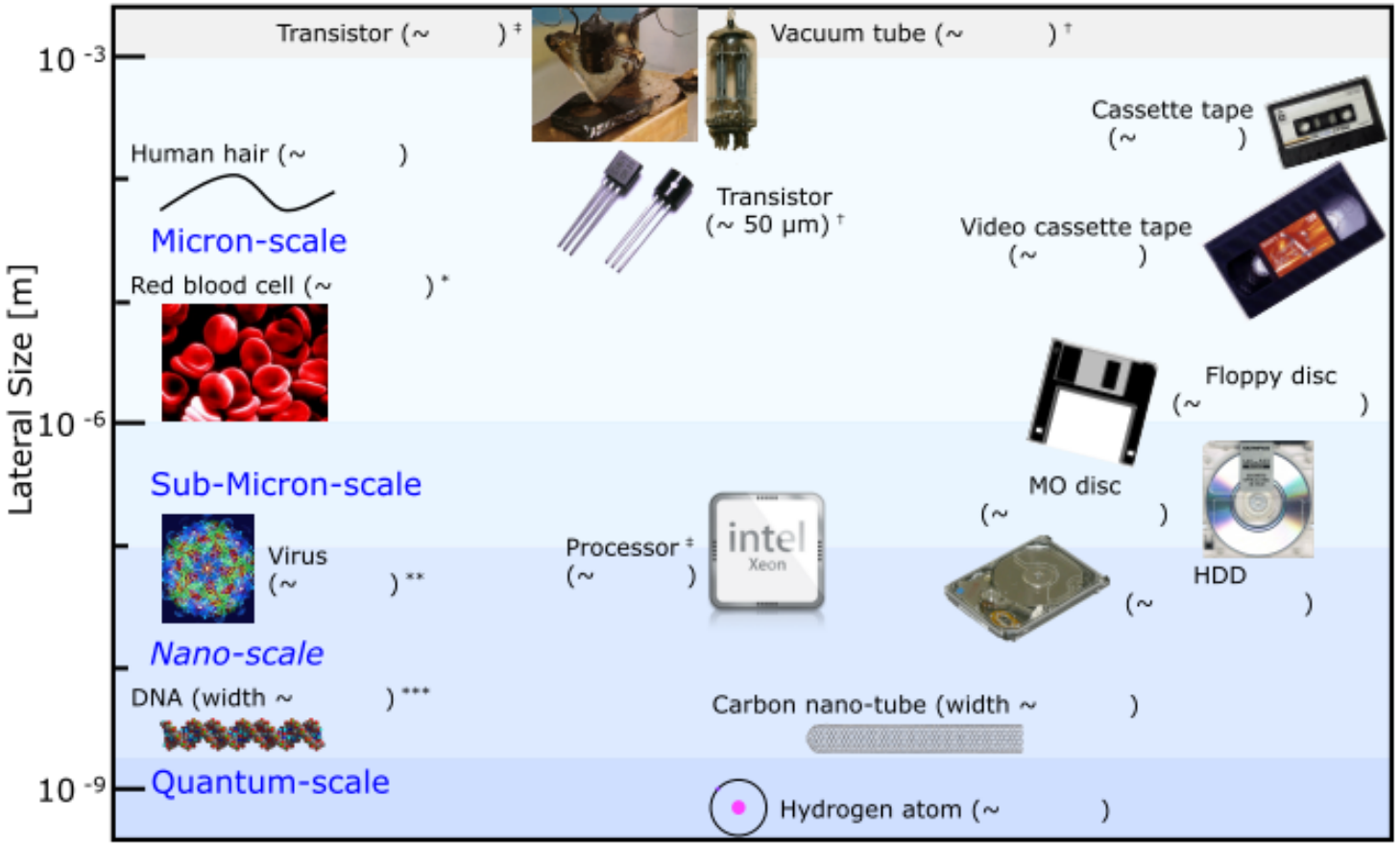
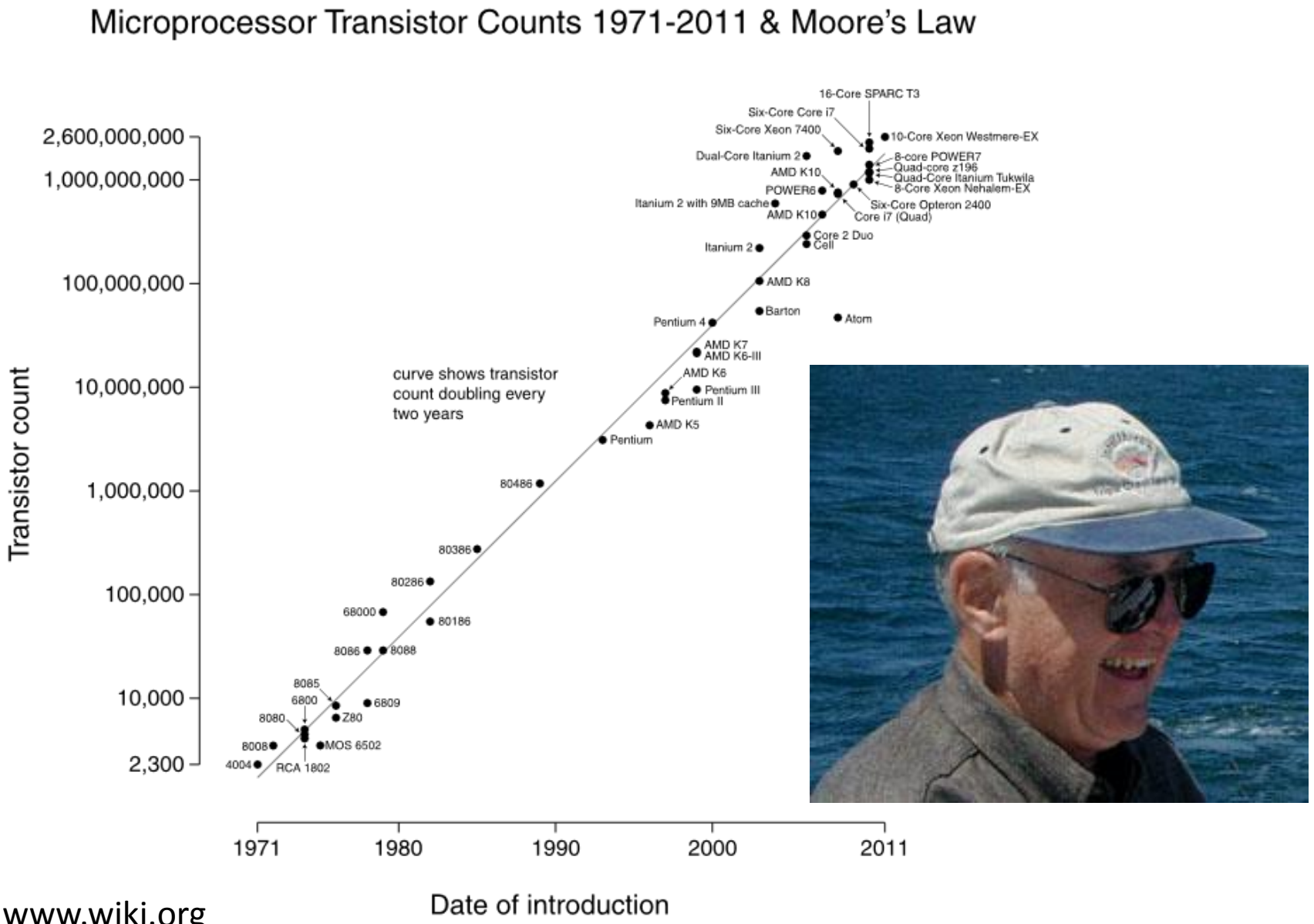
Introduction to Microelectronics

Go into Nano-Scale



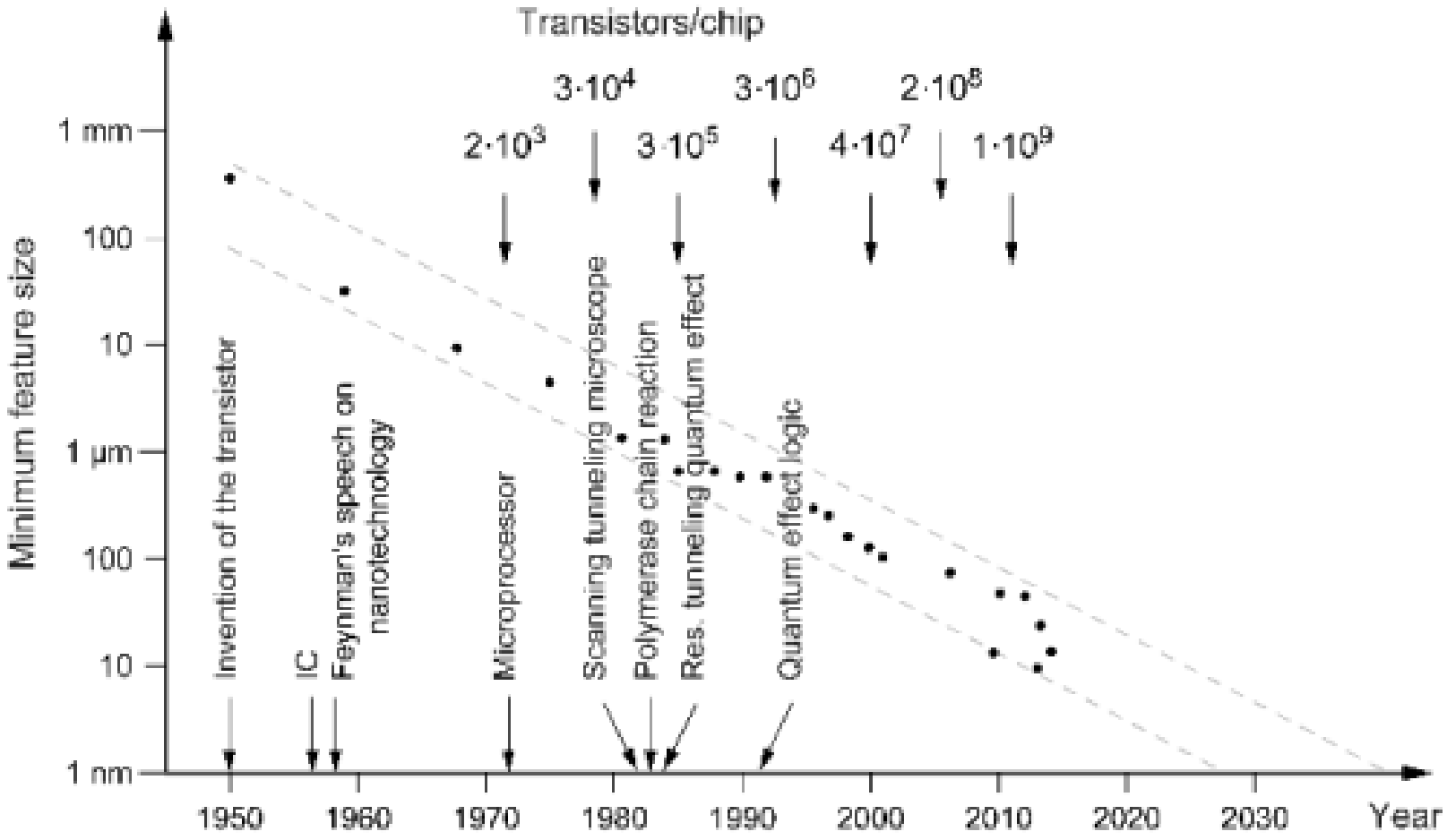
The term nanoelectronics encompasses developments in electronics that entail device physics and structures below the 100 nm level. Research in nano-electronics envisions extending CMOS and proposes new devices and technologies that perform either processor or memory functions or both in universal devices.

Miniaturization and Integration in Semiconductor Devices



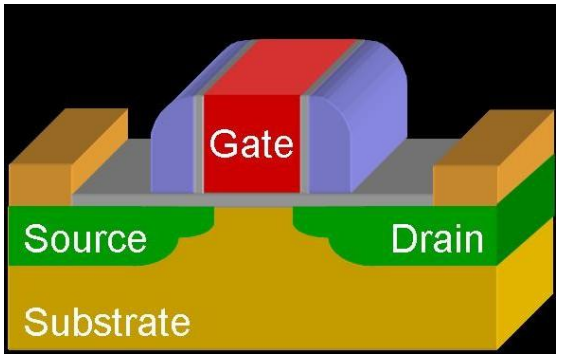
www.wiki.org

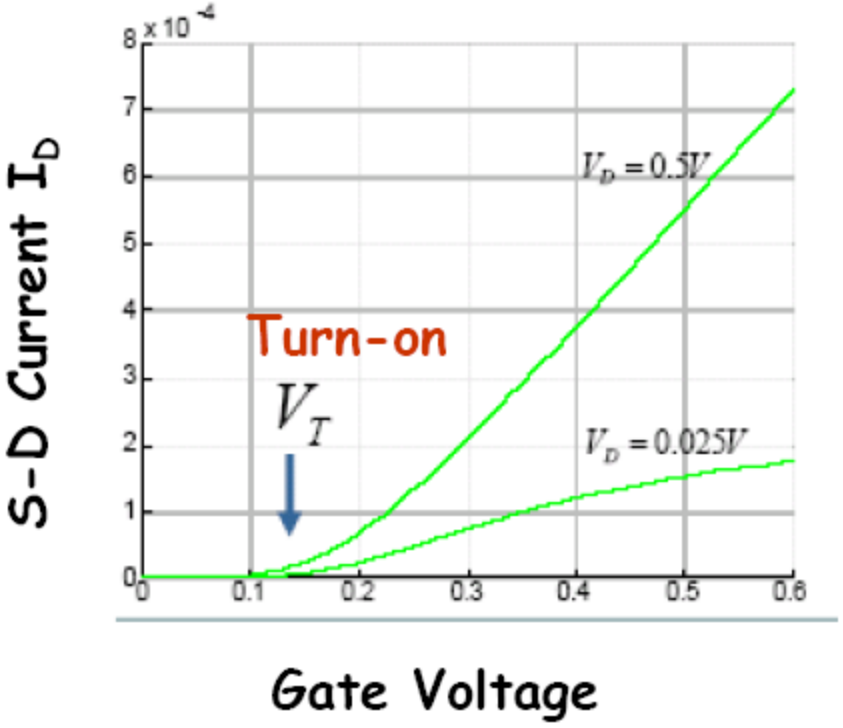
Moores Law

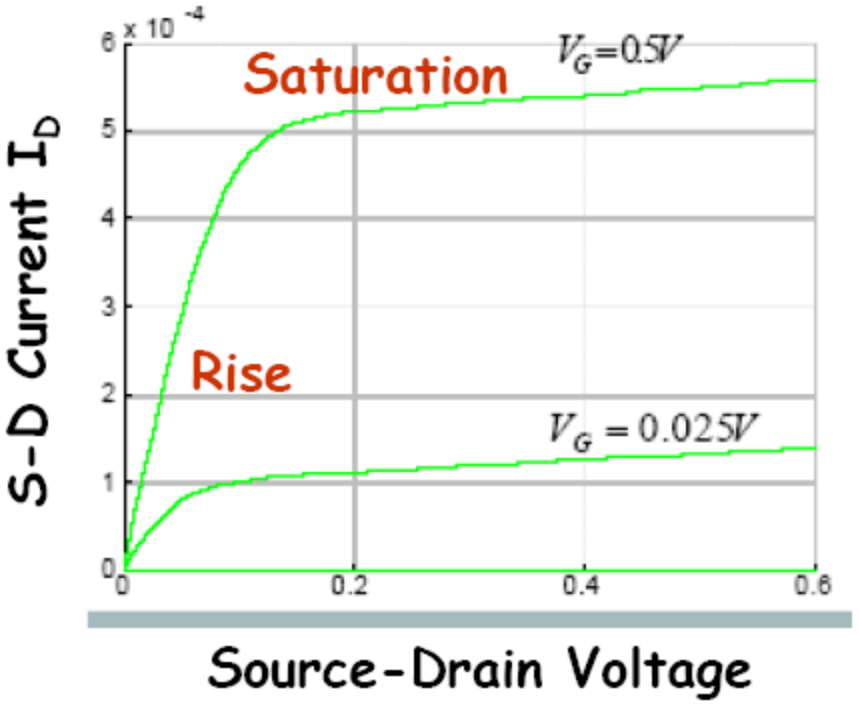


Nanotechnology and Nanoelectronics Materials, Devices, Measurement Techniques, W. R. Fahrner (Editor), Springer

MOSFET I-Vs

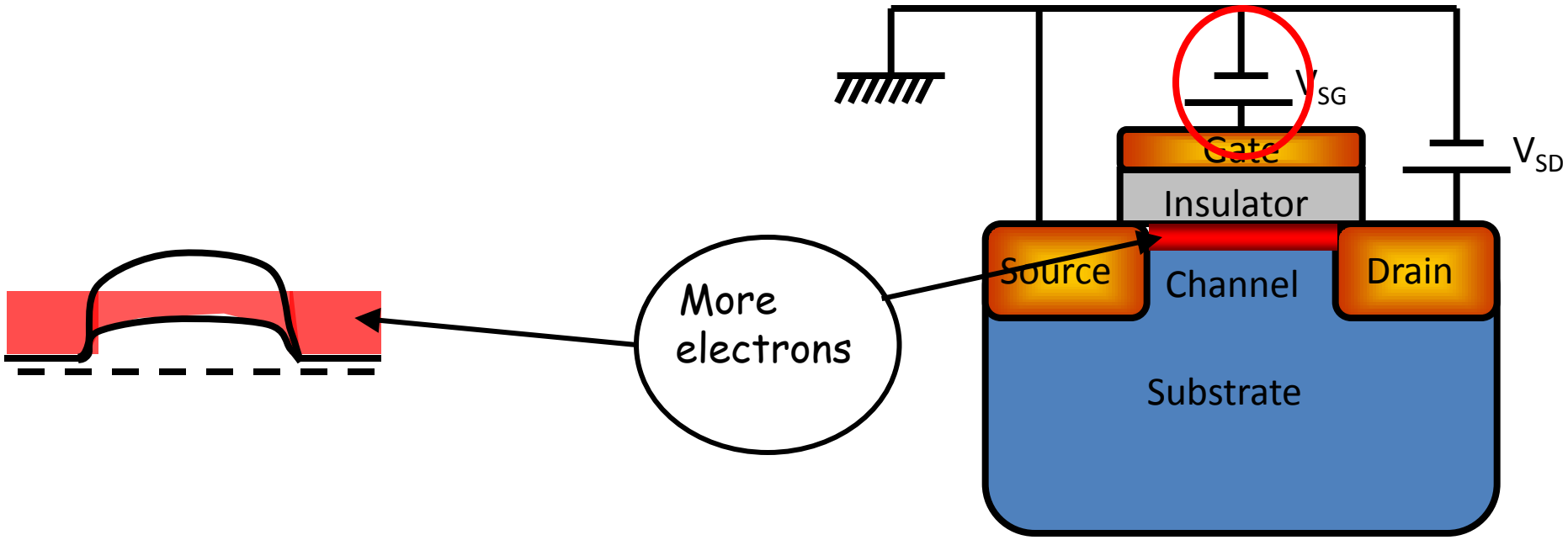

Gate
Source
Drain
Substrate


S-D Current I_D
x 10^-4
8
7
6
5
4
3
2
1
0
0
0.1
0.2
0.3
0.4
0.5
0.6
$V_D = 0.5V$
Turn-on
V_T
$V_D = 0.025V$
Gate Voltage


S-D Current I_D
x 10^-4
6
5
4
3
2
1
0
0
0.2
0.4
0.6
Saturation
$V_G = 0.5V$
Rise
$V_G = 0.025V$
Source-Drain Voltage

Operation of a transistor

$V_{SG} > 0$
n type operation

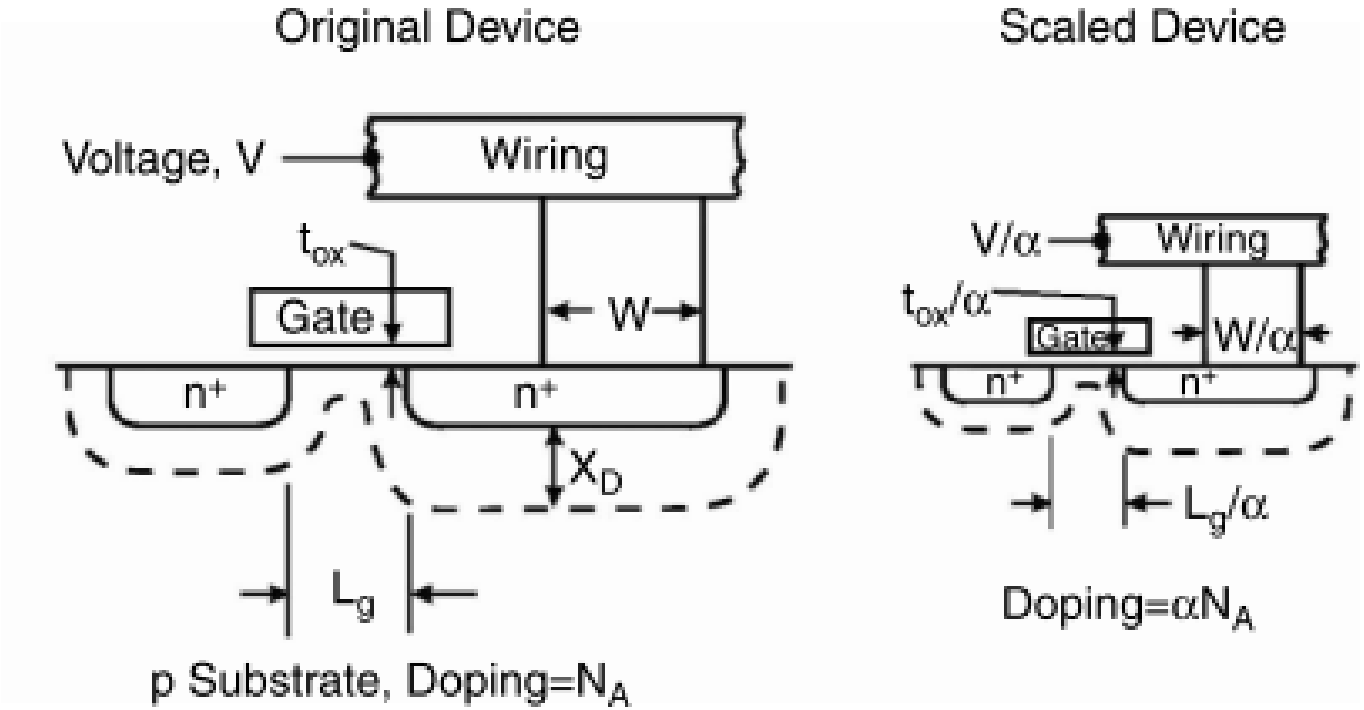


Positive gate bias attracts electrons into channel
Channel now becomes more conductive

ITRS Projections

Year of Production	2013	2016	2019	2022	2025
Technology Node (nm) (DRAM Half pitch)	28	20	14.2	10	7.1
Transistor Gate Length in Microprocessors circuits (nm)	20	15.3	11.7	8.9	6.6
Wafer diameter (inch)	12	18	18	18	18
Transistors density in Microprocessor (billion / cm2)	1.59	3.19	6.38	12.77	25.54
Number of interconnect wiring levels in the Microprocessor	12	13	14	15	16
Operating voltage (V)	0.85	0.77	0.71	0.64	0.59

Schematic illustration of the scaling of Si technology by a factor alpha



Oda, S. et Ferry, D. (2006), Silicon Nanoelectronics.

Technology Scaling Rules for Three Types of Scaling

Physical Parameter	Constant-Electric Field Scaling Factor	Generalized Scaling Factor	Generalized Selective Scaling Factor
Channel length, insulator thickness	$1/\alpha$	$1/\alpha$	$1/\alpha_d$
Wiring width, channel width	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
Electric field in device	1	ε	ε
Voltage	$1/\alpha$	ε/α	ε/α_d
On-current per device	$1/\alpha$	ε/α	ε/α_w
Doping	α	$\varepsilon\alpha$	$\varepsilon\alpha_d$
Area	$1/\alpha^2$	$1/\alpha^2$	$1/\alpha_w^2$
Capacitance	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
Gate delay	$1/\alpha$	$1/\alpha$	$1/\alpha_d$
Power dissipation	$1/\alpha^2$	ε^2/α^2	$\varepsilon^2/\alpha_w\alpha_d$
Power density	1	ε^2	$\varepsilon^2\alpha_w/\alpha_d$

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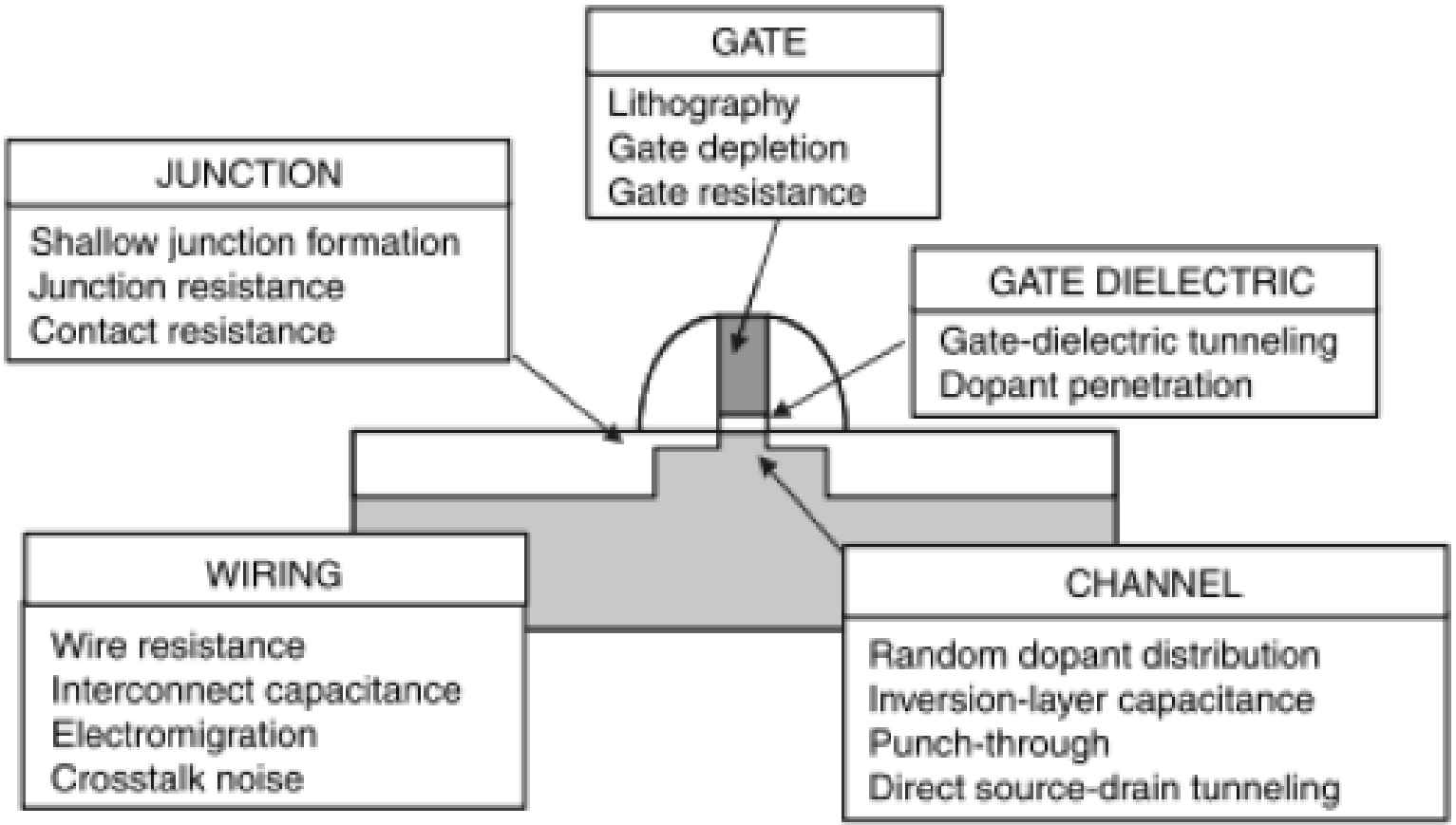
Problems in the Scaling of MOSFETs



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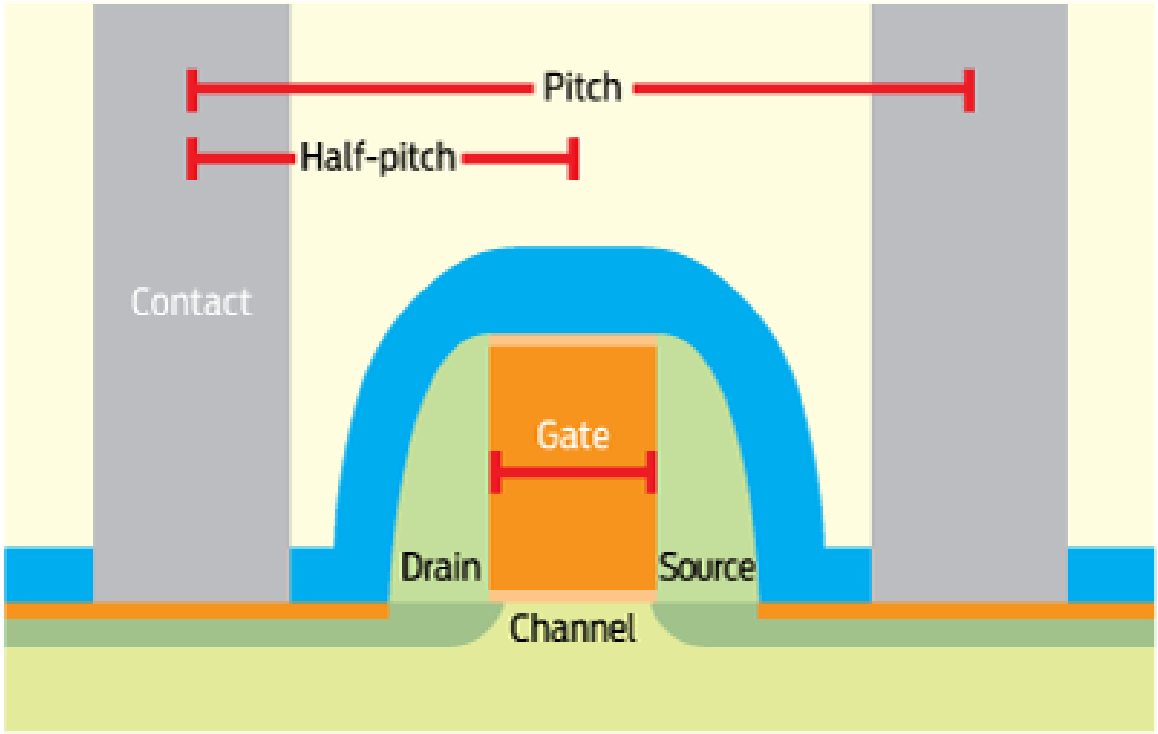
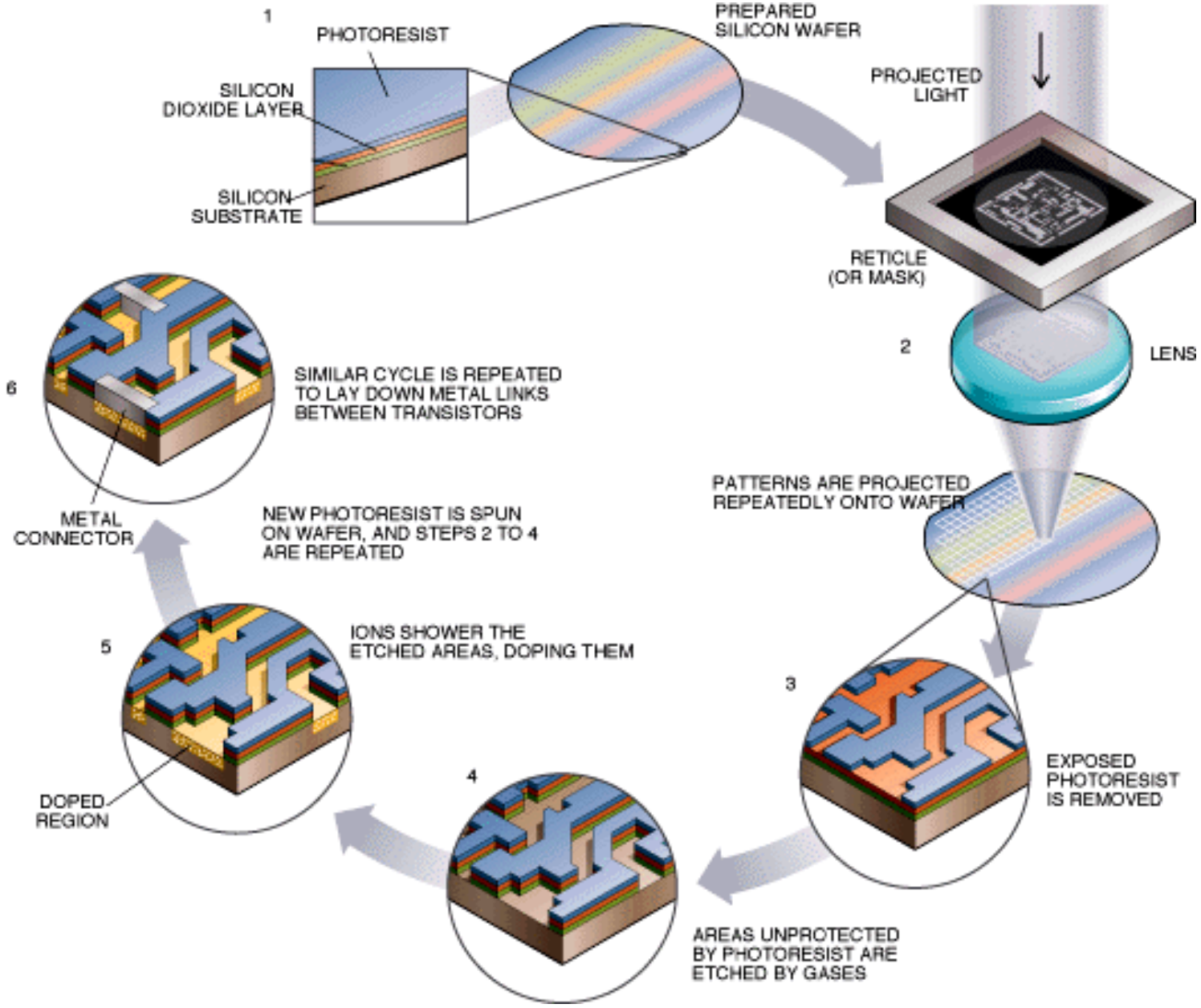


The half-pitch of the first wiring layer is the defining feature for memory chips, while the gate length is the gauge for logic manufacturers.

IC fabrication process



Home-work

1. Describe micro fabrication process with proper diagrams.
2. Describe short channel effects in MOSFETs

Good Luck !