Layout Design Examples

The initial phase of layout design can be simplified significantly by the use of stick diagrams as shown in Fig.2.8. A stick diagram is a simplified layout form, which contains information related to each of the process steps, but does not contain the actual size of the individual features.

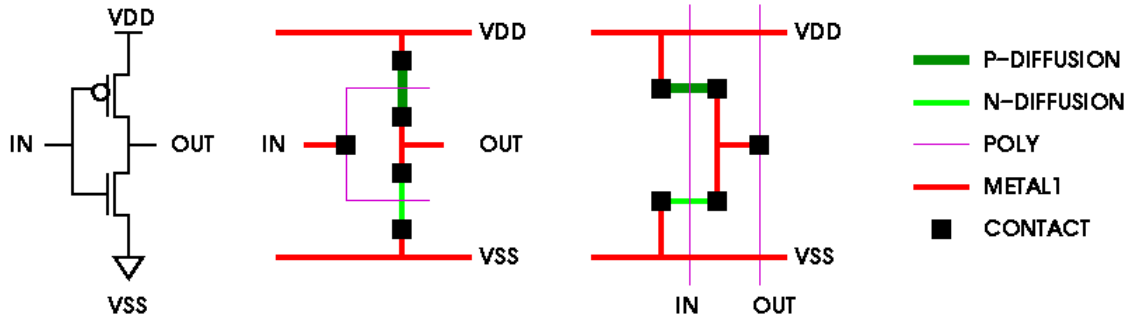


Fig.2.8 Examples of stick diagram for inverter

The purpose of the stick diagram is to provide the designer a good understanding of the topological constraints, and to quickly test several possibilities for the optimum layout without actually drawing a complete mask diagram. The stick diagram can easily be drawn by hand and is a handy intermediate form between the circuit diagram and the physical layout since it can easily be modified and corrected. It can therefore be used to anticipate and avoid possible problems when laying out the circuit.

CMOS INVERTER

In Fig.2.9, the mask layout design of a CMOS inverter will be examined step-by-step. Although the circuit consists of one NMOS and one PMOS transistor, there exists a number of different design possibilities even for this very simple circuit. Fig.2.8 shows two such possibilities.

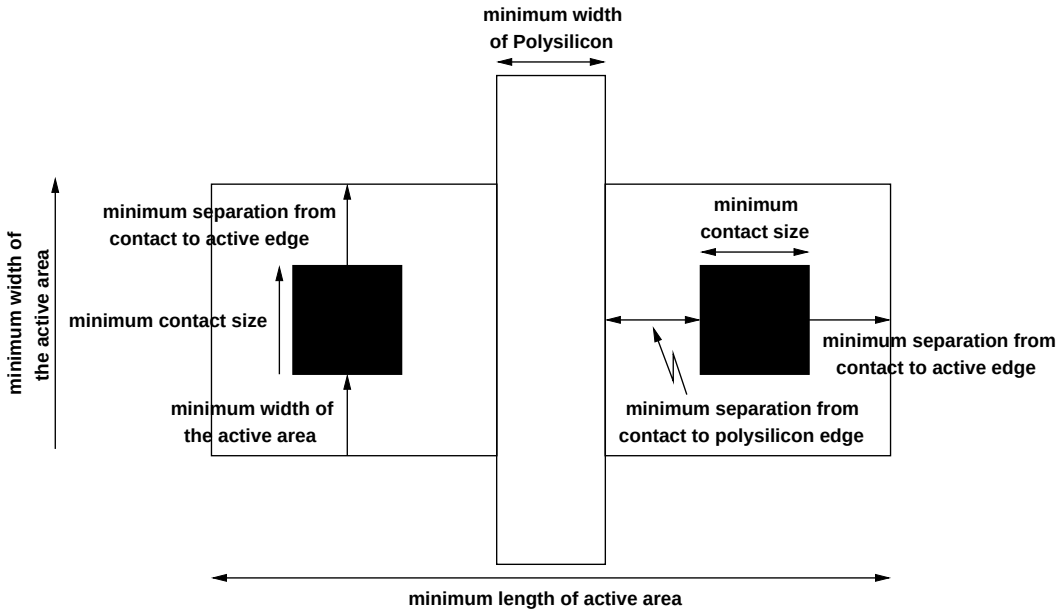
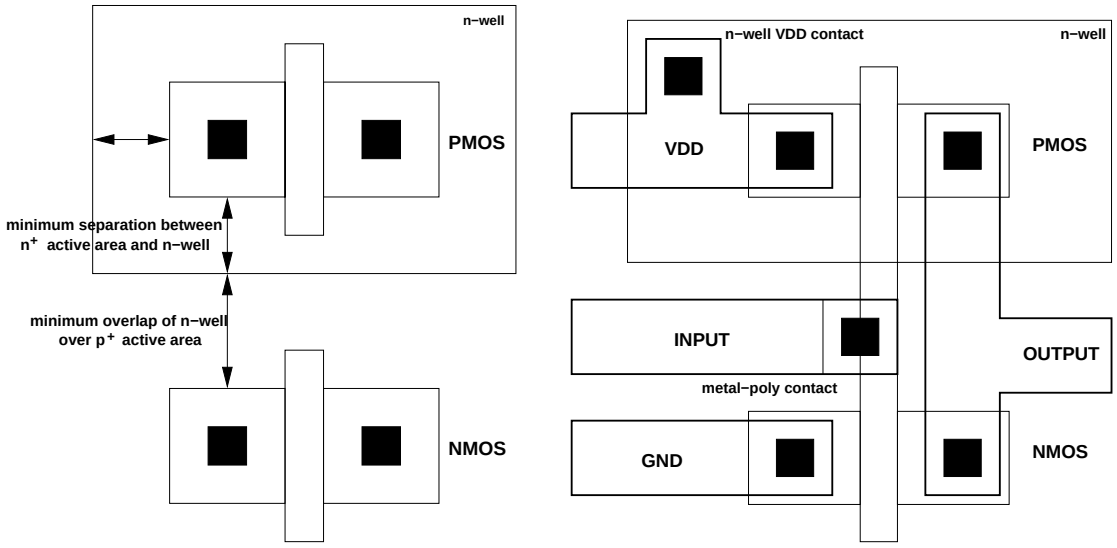


Fig.2.9 Design rule constraints which determine the dimensions of a minimum-size transistor [KAL].

First, it is necessary to create the individual transistors according to the design rules (Fig.2.9). Assume that the design goal is to design an inverter with minimum-size transistors. The width of the active area is then determined by the minimum diffusion contact size (which is necessary for source and drain connections) and the minimum separation from diffusion contact to both active area edges. The width of the polysilicon line over the active area (which is the gate of the transistor) is typically taken as the minimum poly width.

Then, the overall length of the active area is simply determined by the following sum: (minimum poly width) + 2 x (minimum poly-to - contact spacing) + 2 x (minimum spacing from contact to active area edge). The PMOS transistor must be placed in an n-well region, and the minimum size of the n-well is dictated by the PMOS active area and the minimum n-well overlap over n^+. The distance between the NMOS and the PMOS transistor is determined by the minimum separation between the n^+ active area and the n-well (Fig.2.10 (a)). The polysilicon gates of the NMOS and the PMOS transistors are usually aligned.



(a) (b)

Fig.2.10 (a) Placement of one NMOS and one PMOS transistor, and (b) Complete mask layout of the CMOS inverter [KAL].

The final step in the mask layout is the local interconnections in metal, for the output node and for the V_{DD} and GND contacts (Fig.2.10 (b)). Notice that in order to be biased properly, the n-well region must also have a V_{DD} contact.

NAND2 and NOR2

Fig.2.11 shows the sample layouts of a two- input NAND gate and a two-input NOR gate, using single-layer polysilicon and single-layer metal. Here, the p-type diffusion area for the PMOS transistors and the n-type diffusion area for the NMOS transistors are aligned in parallel to allow simple routing of the gate signals with two parallel polysilicon lines running vertically. Also notice that the two mask layouts show a very strong symmetry, due to the fact that the NAND and the NOR gate have a symmetrical circuit topology.

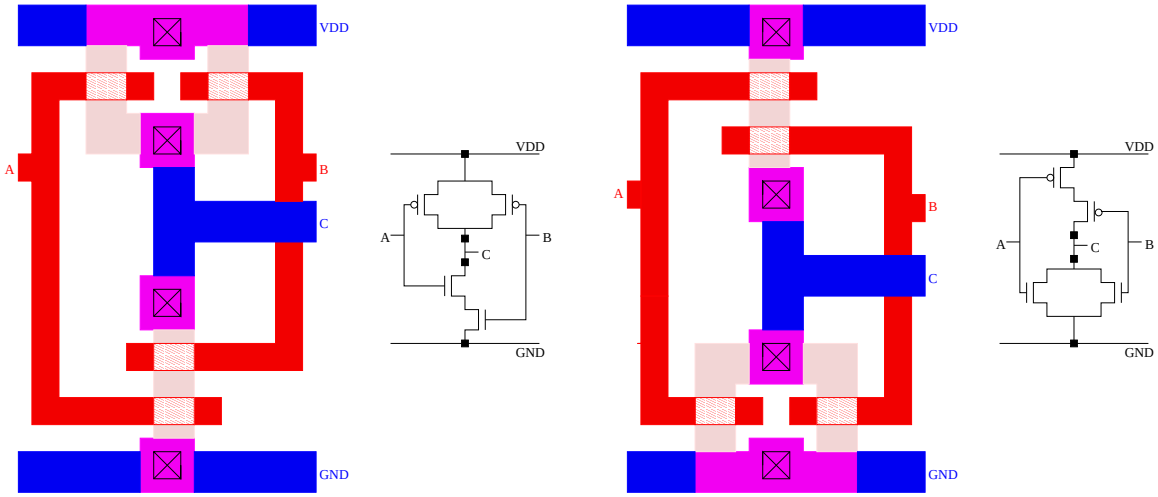


Fig.2.11 Sample layouts of a CMOS NAND2 gate and a CMOS NOR2 gate [WAE]

Complex CMOS Logic Gate Design

The design steps for a more complex CMOS logic, for example AOI22, are the following:

First, construct a logic graph of the schematic (Fig.2.12 (a)) using the following steps:

a. Identify each transistor with a unique name (A, B, C, and D as in the example).

b. Identify each connection to the transistor with a unique name (n1, n2, n3 in the example).

Next, construct one Euler path for both the Pull up and Pull down network (Fig.2.12 (b)).

a. Euler paths are defined by a path, such that each edge is visited only once.
b. A path is defined by the order of each transistor name. If the path traverses transistor A, B, and C, then the path name is {A, B, C}.
c. The Euler path of the Pull-up network must be the same as the path of the Pull-down network.
d. Euler paths are not necessarily unique.

Finally, once the Euler path is found, it is time to draw the stick-diagram (See Fig.2.12(c)). The final step is to draw the layout.

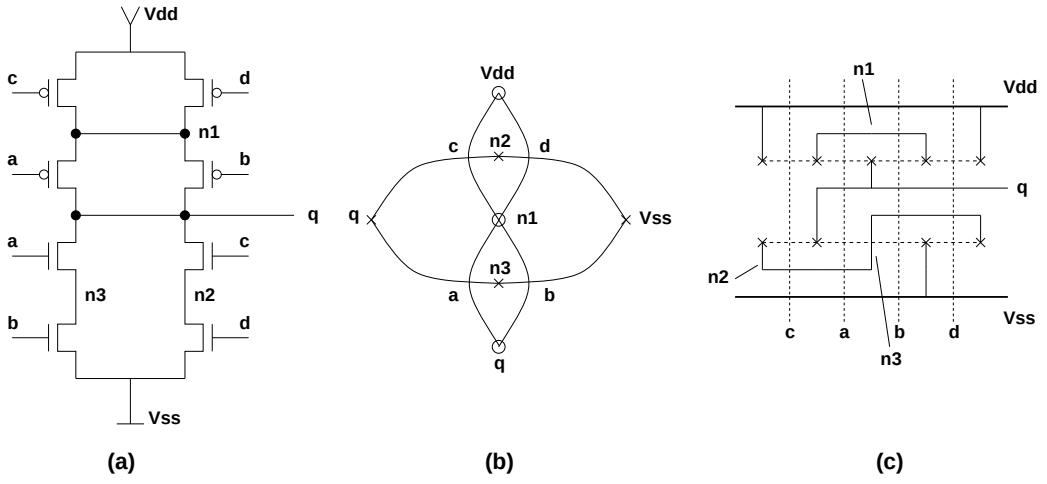


Fig.2.12 An example of (a) Schematic, (b) Euler Path, and (c) Stick Diagram.

2.5 Layout Considerations

Device Sizing

Fig.2.13 shows a basic transistor which is built from a polysilicon gate, placed over a region of thin silicon dioxide. In the figure, the rectangle represents the edges of the gate material and the other rectangle depicts the edges of the thin oxide area. The oxide layer is referred to as the active layer. The active is where atoms will be implanted to create a transistor. The overlap of the gate and active layers determine the size of the device.

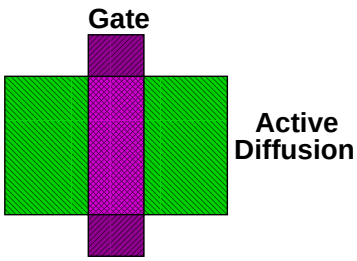


Fig.2.13 Top layout view of an MOS transistor showing gate area and active diffusion area.

Before deciding the size, a designer needs to know at which frequency the circuit must operate. For example, a circuit designer might be given a list of requirements that says “The target multiplier must be running at 50MHz and take 0.1mA from a 3.3V supply.” This is the starting point where the numbers are called the circuit specifications, or specs. With detailed information about a particular process, the specs can determine the necessary device sizes. Many different circuit techniques can be used to design a component such as a multiplier. A designer chooses a circuit topology among them that will give the required performance. Then, the designer calculates the basic capabilities of the circuit and verifies that the circuit meets the specs.

The way to verify IC design assumptions is to build the circuit and run it. The designer runs the design through a computer program called a simulator. The simulation program indicates what the circuit does, how much current it consumes, the frequency response, etc. These circuit simulation programs are commonly called Simulation Program for Integrated Circuits Emphasis

(SPICE). The original SPICE was developed by the University of California at Berkeley in the 1970's. Running a simulation is cheaper and faster than building a chip.

In order for SPICE to accurately predict the complex behaviors of a circuit, a mathematical representation of the circuit elements is needed. This is called a model. The model accurately reflects the physics of the device and its electrical and physical characters. The SPICE simulation results show how the circuit performs with the given device sizes and values. Since the input values in the simulation deck can be adjusted easily, the simulator allows designers to sweep the input data, and they can tune the device sizes and values to optimize the design. Some layout tips are found in the following subsections [SNT, BTT, CLN].

Long and Thin Transistors

Many processes have a design rule specifying the maximum width of a transistor to ensure effective current conduction at the end opposite the driving signal. When larger transistors are required (e.g. in buffers to drive cross-chip or off-chip signals), many smaller transistors can be connected in parallel to achieve the same effect.

In reality, the resistance and capacitance are evenly distributed along the width of the gate. The gate voltage will rise and fall according to the RC time constant. These parasitic elements prevent the device from operating optimally. Since the transistor gate width defines the speed at which the transistor switches, the gate width cannot be changed. Thus, the effective gate width should be maintained.

A long transistor can be split into several smaller transistors that are hooked up in parallel. This is the same size transistor with the same effective gate width, but with less parasitic resistance. In Fig.2.14, each individual transistor has a Gate finger that is one fourth of the width of the original device. This means that the gate finger has a resistance that is one fourth of the resistance of the original device. In addition, the gate fingers are wired in parallel. Four equal resistors in parallel yield an overall resistance of one fourth of the individual resistance value.

The overall effect of this splitting technique gives a parasitic resistance that is one sixteenth of the original.

Next, leg transistors can optimize routing and achieve diffusion sharing. Legging refers to the process of splitting a very wide transistor into a number of narrower parallel transistors with the equivalent overall drive strength. For example if a 32µm transistor is split into four parallel 8µm transistors, the entire structure is referred to as a four-leg transistor. Fig.2.14 shows an example of a four-legged transistor. Besides being necessary for wide transistors, legging can also aid routing and layout density. By choosing to leg a transistor, its aspect ratio may be better suited to the available space. Also, with the choice of an even or odd number of legs and which nodes are source and drain, additional opportunities for diffusion sharing may be exposed. For example, imagine a transistor connecting to V_{DD} and some signal out. If no other transistor has a diffusion connection to out, then this transistor may only share diffusion on the V_{DD} side. However, if the transistor were legged by a factor of two with out in the center and V_{DD} on either side, any transistor connecting to V_{DD} could share with either side of the legged transistor.

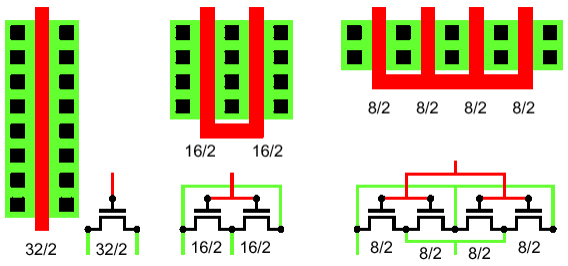


Fig.2.14 Legged transistor

Routing Layer usage

One of the earliest and most important decisions is the metal layer usage. There are a finite number of layers available for routing, and they have unique characteristics. Polysilicon has a high resistance, but it can be useful for short interconnections, especially if it turns into a gate at some point. Metal-1 (M1) is moderately narrow, fairly low in resistance, and easily accessible, making it ideal for local interconnect. Metal-2 (M2) often has a lower resistance, usually because

it is thicker or wider, but has larger space requirements and is harder to access. An M2 connection to a transistor gate, for example, requires a sizable space for a contact, a via, and the required poly, M1, and M2 landing pads (the wider metal areas surrounding vias). Therefore, in a two metal process, M2 is used for global routing. Higher metal layers are often reserved for long distance routing and global signals that require low resistance paths such as clocks and power.

Fig.2.15 shows the wiring completed. All the A terminals have been connected in metal deposited in strips above the device. Note that the fingers of metal reaching down each terminal are all connected together at the top of the diagram. The same technique can be used to join the two B terminals. Metal fingers reach up into each B terminal, joining together at the bottom of the diagram. The gate connections are slightly different in that polysilicon is used. Using polysilicon as a wire is only recommended for very short distances because polysilicon is much more resistive than metal.

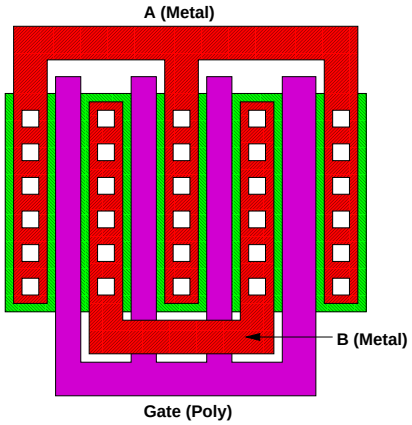


Fig.2.15 All sources, drains and Gates connected. This has the same effective Gate width as one long and thin transistor.

Another tip is to never terminate a long route (greater than ~100μm) with a diffusion region (transistor source-drain; e.g. a pass gate). Electromagnetic (transmission line) effects can cause signals to exceed V_{DD} or drop below ground momentarily, potentially forward biasing the source/drain-substrate/well diode. Long distance signals should always end at the gate of a transistor instead. This can be accomplished by placing one or two inverters between the long wire and the pass gate (usually a MUX). Obviously, if only one inverter is inserted, the logic before or after the gate will have to be adjusted.

Note that it is needed to minimize the number of times a signal switches between routing layers. Contacts and vias have resistance that can be equal to fairly long metal lines. For this reason, poly may be a better choice than M1 for very short routes between gates.

It is necessary to avoid driving one transistor through another. In other words, do not chain transistors together via their gates as shown in Fig.2.16. The combination of high poly sheet resistance and gate capacitance can cause such signals to switch very slowly. However, it is common to use the same poly line to drive complementary transistors (such as in an inverter). In this case, connect the driving signal to the poly (that forms the two gates) between the two transistors. Obviously, the impact of driving one transistor through another is more pronounced with wider transistors. Therefore, if routing is significantly simplified by going against this recommendation in a specific case, consideration should be given to the widths of the transistors involved.

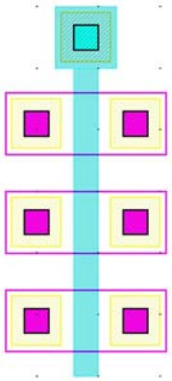


Fig.2.16 Transistor Chain [BTT].

Compact Layout

Most ICs are designed using very small circuits, which are easier to handle, and to understand the designs. These little circuits are then wired together to create a larger, more complex circuit. This approach to circuit design makes layout much easier. Instead of trying to determine how to wire twelve million transistors in one go, it is better to start with a circuit that has twelve and creep up on the larger problem. The goal is to compact layouts. A rectangular circuit layout is much easier to use in conjunction with one million other rectangular circuit blocks than irregularly shaped lumpy circuit layouts.

Next, sharing diffusion regions of interconnected transistors minimizes both area and load capacitance, which it thus improves switching speed. There are a number of techniques that optimize diffusion sharing. If the particular junction being shared is connected to V_{DD} or ground, it is acceptable to widen the diffusion region (increase the intra-gate distance) to allow one additional metal line to cross the diffusion beside the connection to the supply as shown in Fig.2.17. The extra diffusion capacitance is acceptable since the supply node is always at the same potential Since one of the transistors will see an increased resistance to the supply rail, however, the widening should be limited to accommodate a single extra line.

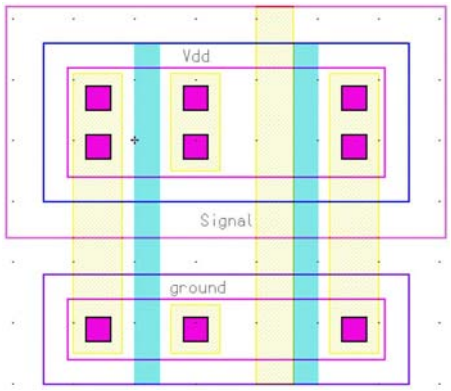
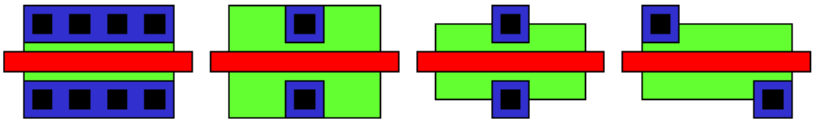


Fig.2.17 Routing over diffusion [BTT].

One of the largest design rules in many processes is the well separation distance. In addition, each well needs at least one well tap to ensure that the well is at the proper electrical potential. To minimize the area consumption by meeting these requirements, wells in subcells are often extended to the cell boundary if an adjacent cell contains a similarly placed well (sharing wells across cell boundaries). Well taps are then added at the top level for the shared well. All real-world processes have a design rule for the area of the well or substrate that can be covered by a given tap. As the distance to the tap increases, the substrate/well resistance causes the bulk voltage to deviate farther from the ideal value. In an extreme case, the result can be the forward biasing of the diode that exists between the source and the substrate/well resulting in latch-up or other undesired effects.

It is necessary to strap transistor source and drain junctions with as many contacts as possible. Place one contact as close as design rules allow to each end of the source and drain and spread as many additional contacts as possible between the ones on either end (Fig.2.17 (a)). This ensures that the entire width of the device is useful in drain current conduction.



(a) (b) (c) (d)

Fig.2.17 Contact layers: (a) Good, (b) bad, (c) bad, and (d) bad

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