# LOW POWER DESIGN

*Energy harvesting: Turning waste heat and stray signals into free power for the future.*

Low power design is a collection of techniques and methodologies that aim to reduce the circuit's power. With the increasing demand for portable electronic devices, IoT sensors, and energy-efficient computing, low-power design has become a critical aspect of modern electronics.

Several factors, including environmental concerns, economic benefits, and technological advancements, drive the shift toward energy-efficient systems. The growing complexity of modern semiconductor devices, coupled with the need for high performance, has made power efficiency a key design constraint.

## Importance

- **Battery life**: Mobile devices, wearables, and IoT sensors rely on efficient power usage.
- **Thermal management**: High power leads to excessive heat, affecting performance and reliability.
- **Energy efficiency**: Reducing power saves electricity, essential for data centres and embedded systems.
- **Cost reduction**: Lower power consumption reduces cooling costs and allows cheaper packaging solutions.



## DYNAMIC POWER

### SWITCHING POWER

This occurs when transistors switch between logic levels (0 and 1).

$$P_{dynamic}=\alpha C V^2 f$$

Key Observations:

- Reducing voltage V has the highest impact since power is proportional to V2.
- Lowering the clock frequency f helps but also affects performance.
- Reducing switching activity α through better design techniques saves power.

### Short-Circuit Power

Due to the ramp input, during the transition region, both NMOS and PMOS are ON, forming a short-circuit path between VDD and GND, hence, current flows and consumes power.

$$P_{short-circuit}=I_{sc} V_{dd} t_{sc} f$$

Mitigation:

- Reducing supply voltage
- Optimizing transistor sizing

## STATIC POWER

### Leakage Power

Even when a transistor is OFF, leakage currents flow, leading to power loss. Major components of leakage current:

$$P_{leakage}=I_{leak} V_{dd}$$

**Subthreshold leakage**: Current between drain and source when the transistor is OFF.

**Gate leakage**: Due to tunneling effects in thin gate oxides.

**Junction leakage**: Reverse-biased diode leakage in transistors.

**Mitigation:** High threshold voltage (HVT) transistors, power gating, adaptive body biasing.

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# Low Power Design Techniques:

## Architectural Level Techniques

1. **Clock Gating**: Disables the clock for idle portions of a circuit to save dynamic power.
2. **Power Gating**: Completely shuts down power to unused blocks to reduce leakage.
3. **Dynamic Voltage and Frequency Scaling (DVFS)**: Adjusts voltage and frequency dynamically based on workload.
4. **Power-Aware Clock Tree Design**: Balances power and timing by optimizing clock tree buffers and routing.

## Circuit Level Techniques

1. **Multi-Threshold CMOS (MTCMOS)**: Uses high-threshold voltage transistors to reduce leakage in idle blocks.
2. **Reverse Body Biasing (RBB)**: Increases the threshold voltage dynamically to reduce leakage.
3. **Adaptive Body Biasing (ABB)**: Adjusts body bias voltage to optimize leakage and performance dynamically.
4. **Dual-Vt Design**: Uses both high and low threshold voltage transistors for an optimal balance between speed and power.
5. **Subthreshold Logic**: Operates transistors below threshold voltage to minimize energy consumption, useful in ultra-low-power applications.

## Physical Design Level Techniques

1. **Low Power Floorplanning**: Groups blocks with similar power domains together to optimize power distribution.
2. **Power Grid Optimization**: Ensures stable power delivery while minimizing IR drop and power noise.
3. **Multi-Mode Power Management**: Designs for different power modes (sleep, idle, active).
4. **Reducing Wire Capacitance**: Minimizing interconnect lengths reduces switching power.

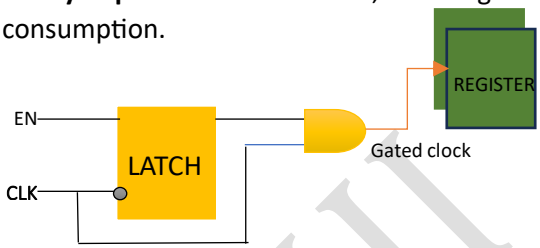
## Industry Trends in Low Power Design

- **FinFET Technology**: Replacing traditional planar MOSFETs to reduce leakage.
- **Near-Threshold Computing**: Operating circuits near the threshold voltage for ultra-low power.
- **Machine Learning-Based Power Optimization**: AI-driven tools for predicting and reducing power consumption.

# CLOCK GATING

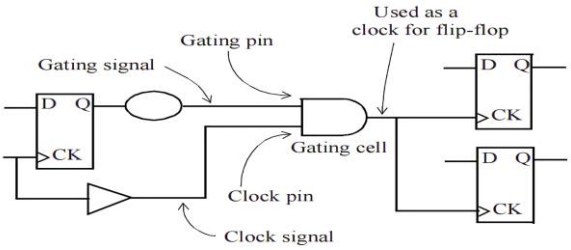
Power-saving techniques are used to reduce **dynamic power consumption** by disabling the clock signal to idle or inactive circuit blocks.

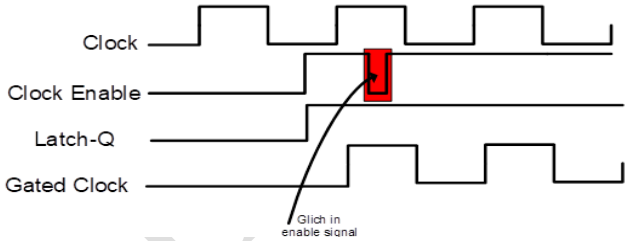
As dynamic power is directly proportional to switching activity (α), which is **directly dependent on the clock**, disabling the clock to unused parts reduces unnecessary toggling, thereby lowering power consumption.




**Types of Clock Gating Techniques:**

1. **Synchronous Clock Gating:**
   - Clock gating control is **aligned with the clock edge** to avoid glitches.
   - Implemented using enable signals with latches or AND gates.
2. **Asynchronous Clock Gating:**
   - The clock is stopped without direct synchronization, requiring careful design to avoid glitches.




*Advantages :*

- ✅ Reduces **switching activity**, saving dynamic power.
- ✅ Decreases **heat dissipation**, improving reliability.
- ✅ Saves power **without affecting functional behavior**.

*Disadvantages:*

- ⚠ Adds **timing complexity** (extra delay in the clock path).
- ⚠ Requires **extra hardware** (gating logic).
- ⚠ Poor implementation can cause **clock glitches** or **skew issues**.

# DVFS (Dynamic Voltage Frequency Supply)

**Dynamic Voltage and Frequency Scaling (DVFS)** is a power management technique that adjusts the supply voltage Vdd and clock frequency (f) dynamically based on workload requirements. By scaling down voltage and frequency when performance demand is low, DVFS helps in reducing both dynamic and static power consumption, making it a key technique in low-power design.

During idle or low workload conditions, the system reduces these parameters to save power.

$$P_{dynamic}=\alpha C V^2 f \qquad P_{leakage}=I_{leak} V_{dd}$$

Since reducing VDD has a quadratic effect on power savings and f has a linear effect, it is the most effective method of reducing power.

*Advantages of DVFS*

- Energy savings and prolonged battery life
- Thermal management and reduced heat dissipation
- Enhanced system reliability and longevity

*Challenges and Limitations*

- ⚠ Performance overhead and latency issues
- ⚠ Complexity in implementation and design
- ⚠ Stability concerns due to frequent voltage and frequency adjustments

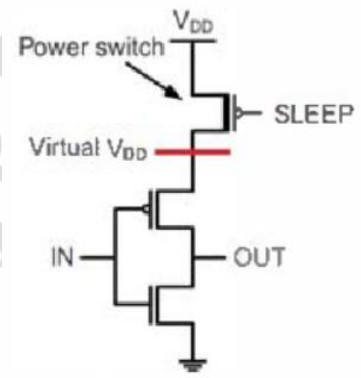
***Lowering voltage saves power exponentially, but go too low, and your circuit naps forever!***

# POWER GATING

Power gating is a low-power design technique that completely **turns power off to idle circuit blocks**, reducing dynamic and static power.

- Power gating uses **power switches (transistors)** to disconnect power from a circuit when it is not in use.
- A sleep signal controls these switches:
  - **Sleep = 1** → Power OFF (disconnects block from supply).
  - **Sleep = 0** → Power ON (normassssl operation).
- Common implementations use **high-threshold voltage (HVT) transistors** as power switches to minimize leakage current.

***Advantages of Power Gating***




✅ **Saves leakage power**, which is critical at lower technology nodes.
✅ **Improves battery life** in mobile and IoT devices.
✅ **Reduces heat dissipation**, improving device reliability.

***Disadvantages of Power Gating***

⚠ **Long wake-up time** – Power needs to stabilize before reuse.
⚠ **Complex implementation** – Requires retention flip-flops to save data before power-off.
⚠ **Power spikes** when turning back on can cause voltage noise (IR drop).

***A sleeping circuit saves more power than an idle one—power gating is the real game-changer!***

# Multi-Threshold CMOS (MTCMOS)

MTCMOS technology uses transistors with different threshold voltages to reduce leakage power:

- **High-threshold voltage (High-Vth) transistors**: These transistors exhibit lower leakage currents, making them suitable for reducing power consumption during idle or standby states. By incorporating High-Vth transistors as sleep transistors, MTCMOS effectively cuts off leakage paths when the circuit is not active.
- **Low-threshold voltage (Low-Vth) transistors**: These transistors switch faster due to their lower threshold voltage, enabling high-speed operations. However, they have higher leakage currents compared to High-Vth transistors. In MTCMOS designs, Low-Vth transistors are used in the main logic paths where speed is critical.

***Leakage power is like a slow battery drain—silent but deadly in deep submicron nodes.***

# Power-Aware Clock Tree Design

Power-aware clock tree design focuses on minimizing the power consumption associated with the distribution of clock signals in synchronous digital circuits. The clock network is a significant contributor to dynamic power consumption, often accounting for a substantial portion of the total power usage in integrated circuits. By implementing power-aware techniques, designers can achieve more energy-efficient systems without compromising performance.