Computer Organization Laboratory

Laboratory Test 3 (October 29, 2024)

SET 1

Write a Verilog module to carry out division (N/D) using repeated subtraction for two given integers N and D, and generate the quotient Q and the remainder R. You may use the following pseudo-code:

```
(int, int) divide (int N, int D)
R = N;
Q = 0;
while (R >= D) do
  R = R - D;
  Q = Q + 1;
end
return (Q, R);
```

Assume that all data items (N, D, Q, R) are unsigned 8-bit integers.

Draw the datapath diagram for the design showing the relevant control signals. Write the Verilog module for the divider using comments and indentation as required. Download the code on FPGA and demonstrate the correct working using on-board switches and LEDs. Make relevant assumptions where necessary, clearly stating them.

Include your group number, roll number and name as comment lines in the beginning of the Verilog code.

Breakup of marks:

a)	Data path diagram (to be uploaded on Moodle)	10 marks
b)	Complete Verilog code (to be uploaded on Moodle)	20 marks
c)	Demonstration on FPGA board	20 marks