A REPORT ON

VOICE DIGITIZER

PREPARED FOR

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By

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User Requirements and Technical Specifications

User Requirements

The microprocessor is responsible for digitizing and modifying the voice signal, which will be stored in memory. The system allows the user to input a numerical value (ranging from 0 to 9) that determines the amount of delay to be applied. Upon pressing the 'Sound Replay' button, the modified sound will be played back with the user-specified delay.

Technical Specifications

- The keypad has digits 0-9, backspace and enter.
- The delay value entered by the user has to be displayed on a 7-segment display.
- The audio is sampled at 1000 samples per second.
- The digitized signal is to be reproduced when the user closes a switch labelled sound replay between the amplitude of 0V and 5V and with a delay as inputted by the user in milliseconds
- The signal for a period of 6 seconds has to be digitized and stored in RAM.

Assumptions

1. The microphone's output has undergone preprocessing within the microphone itself to generate a signal that fluctuates in amplitude within the range of 0 to 5 volts.
2. The next input is awaited by the system until the user initiates it.
3. The input is obtained without any distortion caused by external noise.
4. The system initiates as soon as it receives power.

Address Mapping

Memory Mapping

ROM 1	00000H – 00FFFH
ROM 2	FF000H - FFFFFH
RAM 1	02000H - 02FFFH
RAM 2	03000H - 03FFFH

A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00	Address	Memory
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00000_h	ROM_1
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	$00FFF_h$	
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	02000_h	RAM_1
0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	$02FFF_h$	
0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	03000_h	RAM_2
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	$03FFF_h$	
1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	$FF000_h$	ROM_2
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	$FFFFF_h$	

I/O Mapping

8255(1) [For ADC and DAC]	70H - 76H
8255(2) [For 7seg, keyboard and LEDs]	80H - 86H
8253(1)	88H – 8EH
8259(1)	90H - 92H

A07	A06	A05	A04	A03	A02	A01	A00	Address	I/O Devices
0	1	1	1	0	0	0	0	70_h	8255_1
0	1	1	1	0	1	1	0	76_h	
1	0	0	0	0	0	0	0	80_h	8255_2
1	0	0	0	0	1	1	0	86_h	
1	0	0	0	1	0	0	0	88_h	8253_1
1	0	0	0	1	1	1	1	$8E_h$	
1	0	0	1	0	0	0	0	90_h	8259_1
1	0	0	1	0	0	1	0	92_h	

Components used and Justification

System Hardware

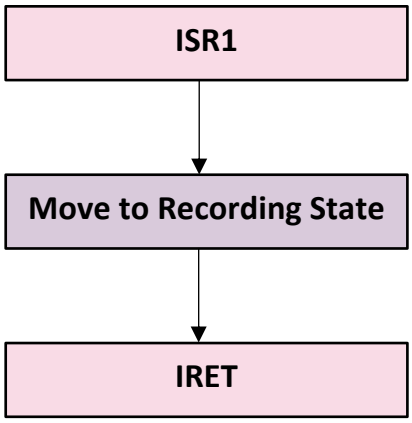
Item Name	Description	Quantity
ADC0804	Used for taking input from mic and converting it into digital 8-bit output every ms.	1
DAC08008	Takes in digital input and outputs analog value in terms of current.	1
LF3511	An op-amp, used to convert outputted current from DAC0808into a voltage value of required range (in this case 0-5V).	1
Mic	To record audio and convert into analog voltage (between 0 and 5V)	1
Resistors	To control current and voltage values, and to make RC circuits to control timings	7
Capacitors	To make RC circuits	2
LEDS	To show status of system	5
Buttons	To allow for system inputs	2
7-SEG-CA	To display number entered by user	1
Numpad	To allow user to input number	1

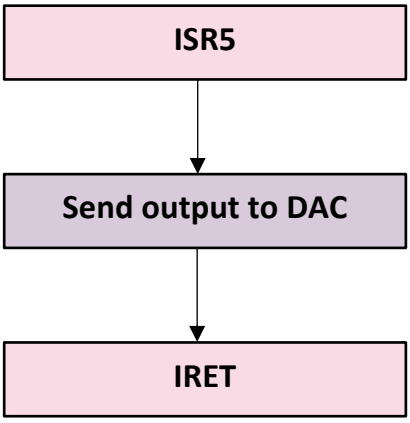
Design Hardware

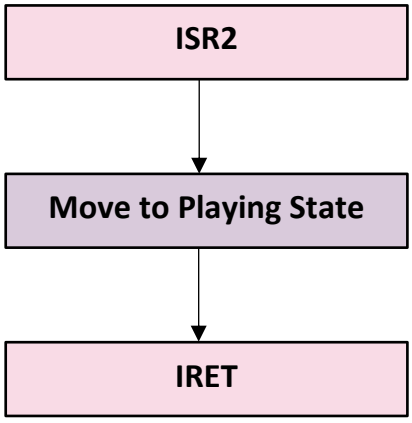
Component Number	Description and Specification	Quantity
8086	16-bit microprocessor chip	1
8284	Clock oscillator chip developed primarily for supplying clock signals for the Intel-8086/8087/8088/8089 series of processors.	1
8253A	The 8253 chip has the task of producing a pair of clock signals: • A 1ms pulse, which is utilized to generate interrupts every millisecond, and thus collect 1000 samples per second from the ADC. • An "n" millisecond pulse, where "n" is a value that is input by the user and denotes the time interval between samples.	1
8255A	To interface the microprocessor with various input/output (I/O) devices, a pair of 8255A chips has been employed. • SPEAKER_I/O, is responsible for connecting the digital-to-analog converter (DAC) and analog-to-digital converter (ADC) (specifically, the 0808 and 0804 models, respectively) to the microprocessor. • DISPLAY_IO, facilitates communication between the microprocessor and other devices such as LEDs, a 7-segment display, and a keypad.	2
8259	The system produces and oversees the order of importance for five interrupt signals, which are REC_BUTTON (activates recording), REP_BUTTON (toggles replay on/off), RDY (connected to the End-of-Conversion signal of the ADC), 1ms (triggers interrupts every 1 millisecond to collect samples from the ADC), and n ms (where "n" denotes the time delay between consecutive samples).	1

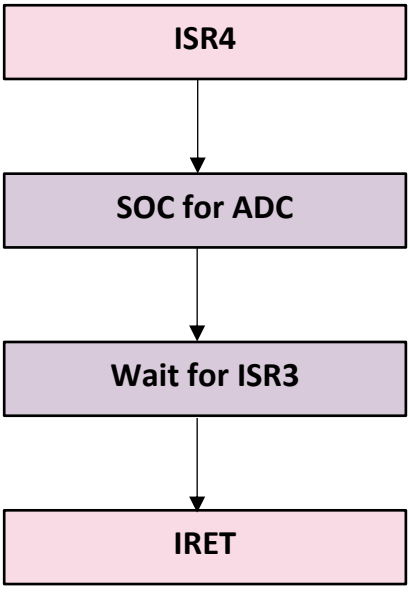
2716	2KB programmable memory EPROM chip	4
6116	2KB programmable memory SRAM chip	4
7432	OR Gate	8
7404	NOT Gate	2
74LS138	3-to-8 Decoder Chip	2
74LS373	Octal Latch with 3-state outputs	3
74LS245	Octal Bus Transmitter/Receiver designed for 8-line asynchronous 2-waydata communication between data buses	2

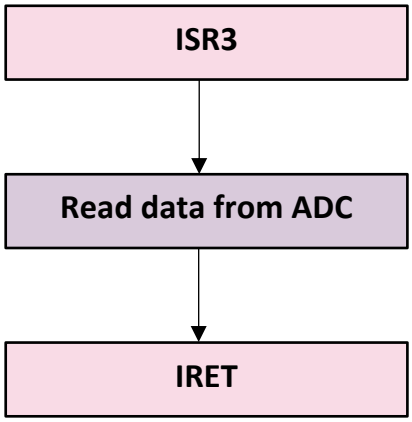
ISR Flowcharts











Main Flowchart