Indian Institute of Technology Ropar

Department of Electrical Engineering

EE204 : Digital Circuits Laboratory

Classroom - Analog and Digital Circuits Lab

Introduction:

This manual explains how to build adder circuits. An **adder** or a **summer** is a digital circuit that performs addition of binary numbers. Adders are used not only in the arithmetic logic units, but also in other parts of the processor, to calculate addresses, table indices, etc. Adder is a simple circuit, but a fundamental one.

Aim:

The objective of this lab exercise is to perform addition of binary digits using combinational circuits. In this lab exercise, we will design and implement the following arithmetic operation.

Theory:

HALF ADDER:

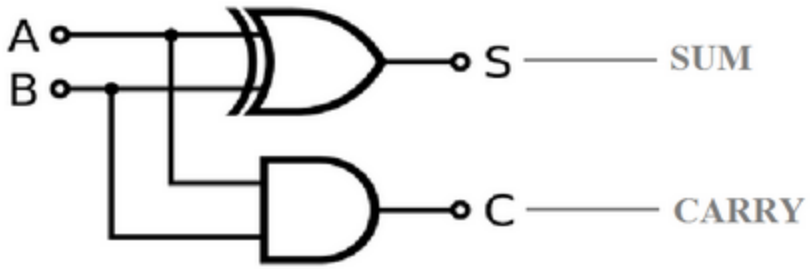
A half adder is a combinational circuit with two binary inputs (augend and addend bits) and two binary outputs (sum and carry bits). It adds two inputs (A and B) and produces the sum (S) and the carry (C) bits. It is an arithmetic circuit used to perform the arithmetic operation of addition of two single bit words.

The characteristic equation of a Half Adder is expressed as:

$$\text{Sum} = A.\bar{B} + \bar{A}.B = A \oplus B$$

$$\text{Cout} = A.B$$

When any of the inputs A and B is equal to 1, the Sum is 1. Otherwise, it is 0. Carry Cout is 1 only when both the inputs are 1. Figure given below is the schematic diagram of half adder.



FULL ADDER:

The combinational circuit that performs addition of three bits (Two significant bits and a previous carry) is called Full adder.

The characteristic equation of a Full Adder is expressed as:

$$\text{Sum} = \bar{A}\bar{B}Cin+\bar{A}BCin+A\bar{B}\bar{C}in+ABCin$$

$$= (A\bar{B}+\bar{A}B)\bar{C}in+(AB+\bar{A}\bar{B})Cin$$

$$= (A\oplus B)\bar{C}in+(\bar{}(A\oplus B))Cin$$

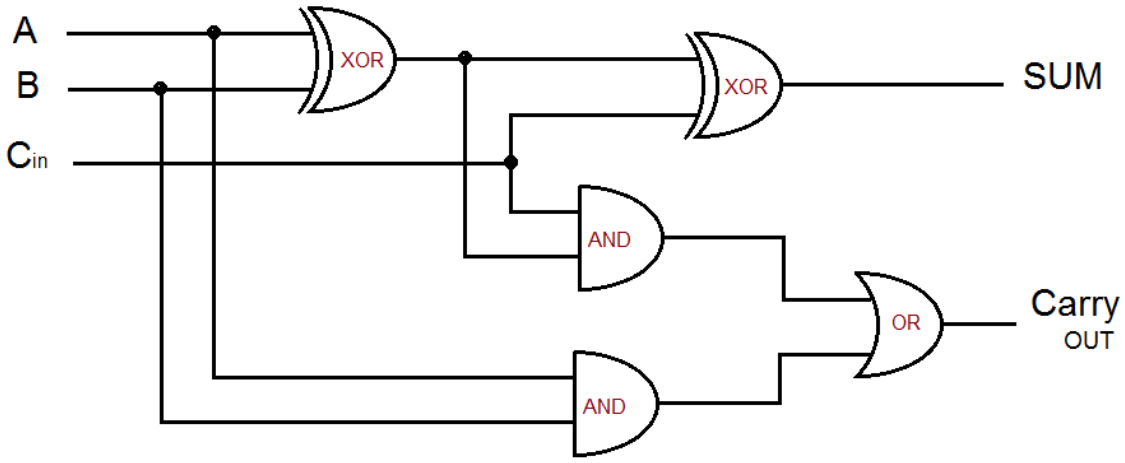
$$= A\oplus B\oplus Cin$$

$$\text{Cout} = \bar{A}.B.Cin+A.\bar{B}.Cin+A.B.\bar{C}in+A.B.Cin$$

$$= A.B+(A\oplus B).Cin$$

$$= A.B+A.Cin+B.Cin$$

The Sum is High i.e. 1 only when an odd number of the inputs are High. Carry Cout is High i.e. 1 only when more than one input is High. Figure given below is the schematic diagram of Full adder.



Pre-Lab quiz:

1. Read the experiment hand-out in full.
2. Evaluate the truth table and gate-level circuit for a half-adder. Attach the worksheet with this manual.
3. Evaluate the truth table and gate-level circuit for a full-adder. Attach the worksheet with this manual.
4. Match the following:

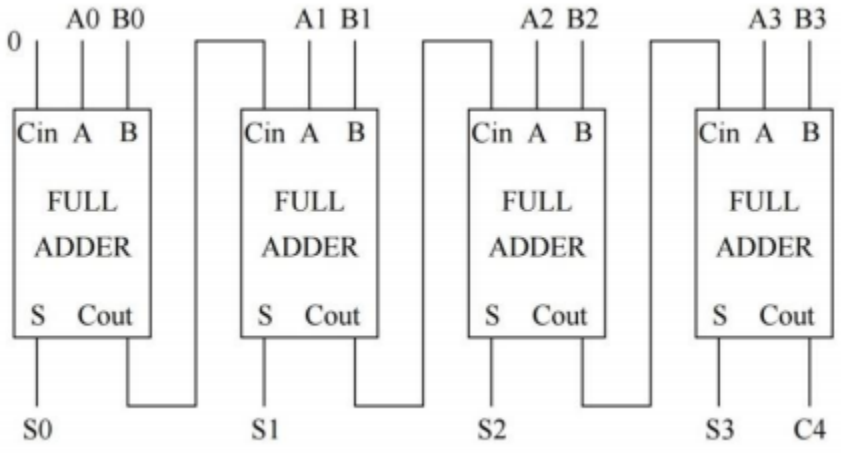
a) Comparator	(i) NAND
b) Half adder	(ii) NOR
c) Anyone input is 1, output is 0	(iii) XOR
d) Anyone input is 0, output is 1	(iv) XNOR

Procedure:

- A half-adder has two inputs- A and B and two outputs – the sum (S) and the carry (c). The S = XOR(A, B) and C = AB. Design a half-adder circuit and verify that the half-adder is functioning properly.
- A full-adder has three inputs, A, B and the carry-in, Cin. There are two outputs - the sum, S, and the carry-out, Cout. S = XOR(XOR(A,B), C). Cout = A.B + B.Cin + A.Cin. Implement a

full adder circuit and verify that the full-adder is fully functional.

- Four full-adders as shown in the figure below. This is a binary 4-bit adder. Implement the 4- bit adder and verify that the 4-bit adder is working. Set the two 4-bit inputs of the adder to 0111 and 1011 respectively. Explain the observed output.



Post-Lab quiz:

1. Can we further extend this lab exercise to subtractors?
2. Write a program in Verilog to verify the truth tables of these adders and subtractors?
3. Can we implement addition operations using Multiplexers and Decoders?

Suggested Readings: M. Morris Mano, “Digital Logic and Computer Design”, Pearson Prentice Hall, 2008