Indian Institute of Technology Ropar

Department of Electrical Engineering

EE204 : Digital Circuits Laboratory

Classroom - Analog and Digital Circuits Lab

Introduction:

This manual explains how to build adder and subtractor circuits using a 4X1 MUX. An adder (or summer) is a digital circuit that performs addition of binary numbers. Adders are used not only in the arithmetic logic units, but also in other parts of the processor, to calculate addresses, table indices, etc. Adder is a simple circuit, but a fundamental one. Vice versa for the case of a Subtractor.

Aim:

Realization of adder and subtractor using 4 ×1 Multiplexer

Theory:

Multiplexers are very useful components in digital systems. They transfer a large number of information units over a smaller number of channels, (usually one channel) under the control of selection signals. Multiplexer means many to one. A multiplexer is a circuit with many inputs but only one output. By using control signals (select lines) we can select any input to the output. Multiplexer is also called a data selector because the output bit depends on the input data bit that is selected. The general multiplexer circuit has 2n input signals, n control/select signals and 1 output signal. De-multiplexers perform the opposite function of multiplexers. They transfer a small number of information units (usually one unit) over a larger number of channels under the control of selection signals. The general de-multiplexer circuit has 1 input signal, “n” control/select signals and “2n” output signals. De-multiplexer circuit can also be realized using a decoder circuit with enable.

Pre-Lab quiz:

Q. How do you evaluate the truth table and gate-level circuit for the 4×1 Multiplexer?

Q. Evaluate the truth table, Boolean function and gate-level combination circuit for the full-adder and full-subtractor using the 4×1 Multiplexer.

Components:

TTL ICs 74LS153, basic logic gates, LEDs, power supply, function generator and standard experimental setup.

Procedure:

1. Realize the function F (shown in Fig.1) using two 4 ×1 multiplexers (74153), and minimum additional gates.

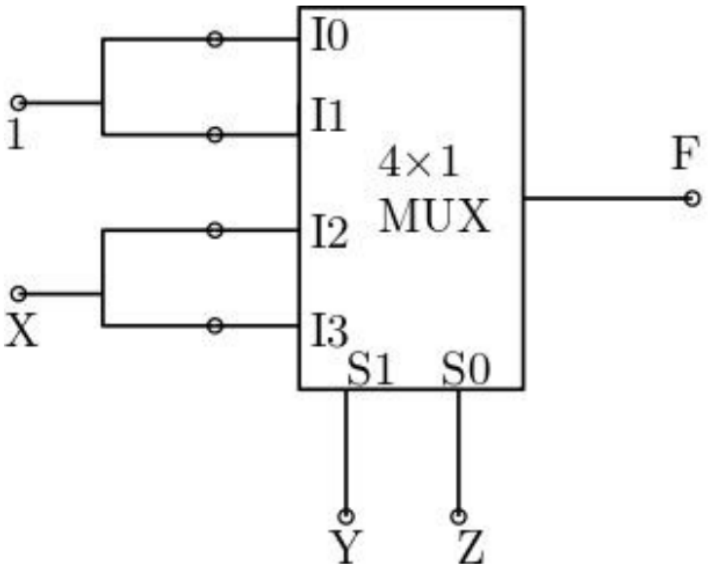

Fig.1

2. Implement a full-adder circuit using 4 ×1 multiplexers (74153) and verify that the full-adder is fully functional.

3. Implement a full-subtractor circuit using 4 ×1 multiplexers (74153) and verify that the full-subtractor is fully functional.

Post-Lab quiz:

Q. Can you design a 16×1 multiplexer using 8×1 multiplexer and additional logic gates?

Q. Can you implement the logic function, F = 0, 1, 2, 5, 6, 8, 9, 11, 13, 14, 15 using a 4×1 multiplexer?

Suggested Readings: M. Morris Mano, "Digital Logic and Computer Design", Pearson Prentice Hall, 2008.