# Indian Institute of Technology Ropar

## Department of Electrical Engineering


---

EE204 : Digital Circuits Laboratory

Classroom - Analog and Digital Circuits Lab

---

## Introduction:

A sequence detector is a sequential state machine that takes an input string of bits and generates an output 1 whenever the target sequence has been detected

## Aim:

Design and run a Sequence Detector

## Pre-Lab quiz:

Q. What is the counter? How are the Synchronous and Asynchronous Counters different?

Q. Evaluate the truth table, Boolean function, and gate-level circuit for the objective II.

## Components:

Use 74LS74 D-flip-flops, and only 74LS00 NAND gates to wire up your circuitry, and clock generator kit.

## Procedure:

Design and Implementation of sequence detector that detect the following sequence: {1, 1, 1}. The circuit has one input, X, and one serial output, Y. If the X is 0, the circuit stays in S0, but if the input is 1, it goes to state S1 to indicate that a 1 was detected. If the next X is 1, the change is to state S2 to indicate the arrival of two consecutive 1's, but if the X is 0, the state goes back to S0. The third consecutive 1 sends the circuit to state S3. If more 1's are detected, the circuit stays in S3. Any 0 input sends the circuit back to S0. In this way, the circuit stays in S3 as long as there are three or more consecutive 1's

received. This is a Moore model sequential circuit, since the output is 1 when the circuit is in state S3 and is 0 otherwise.

Design a sequence detector in the following manner.

1. Construct a state diagram for the finite state machine.
2. Calculate the number of flip-flops you need.
3. Assign values to each state in the state diagram.
4. Construct the state table from the state diagram. Use D-flip flops.
5. Use Karnaugh maps to generate each of the inputs to each of the flip flops.
6. Make the circuit using flip-flops, and logic gates.

Post-Lab quiz:

Q. What is the difference between Mealy and Moore state Machine?

Q. Develop the Verilog code sequence detector that detects a sequence of three or more consecutive 1's in a string of bits coming through an input line.

Suggested Readings: M. Morris Mano, "Digital Logic and Computer Design", Pearson Prentice Hall, 2008.