Indian Institute of Technology Ropar

Department of Electrical Engineering

EE204 : Digital Circuits Laboratory

Classroom - Analog and Digital Circuits Lab

Introduction:

The **combinational circuit** does not use any memory. Hence the previous state of input does not have any effect on the present state of the circuit. But a **sequential circuit** has memory so output can vary based on input. This type of circuit uses previous input, output, clock and a memory element. **Flip flop** is a sequential circuit which generally samples its inputs and changes its outputs only at particular instants of time and not continuously. Flip flop is said to be edge sensitive or edge triggered rather than being level triggered like latches.

Aim:

The objective of this lab exercise is to realise the sequential circuits. In this lab exercise, we will design and implement the following arithmetic operation

Components and ICs required: TTL ICs 74LS00, 74LS10, 74LS14, and clock generator kit.

Theory:

J-K flip flop:

The JK Flip Flop is a gated SR flip-flop having the addition of a clock input circuitry. The invalid or illegal output condition occurs when both of the inputs are set to 1 and are prevented by the addition of a clock input circuit. So, the JK flip-flop has four possible input combinations, i.e., 1, 0, "no change" and "toggle". The symbol of JK flip flop is the same as **SR Bistable Latch** except for the addition of a clock input.

J	K	CLK	Q
0	0	Edge rise	No change
1	0	Edge rise	1
0	1	Edge rise	0
1	1	Edge rise	Toggles

Master Slave flip flop:

Master slave JK FF is a cascade of two S-R FF with feedback from the output of second to input of first. Master is a positive level triggered. But due to the presence of the inverter in the clock line, the slave will respond to the negative level. Hence when the clock = 1 (positive level) the master is active and the slave is inactive. Whereas when clock = 0 (low level) the slave is active and master is inactive.

J	K	CLK	Q
0	0	Edge rise	No change
1	0	Edge rise	1
0	1	Edge rise	0
1	1	Edge rise	Toggles

Pre-Lab quiz:

1. Read the experiment hand-out in full.
2. What are the differences between J-K latch, J-K master-slave latch, and J-K flip-Flops? Attach the worksheet with this manual.
3. Evaluate the truth table, Boolean function, and gate-level circuit for the J-K flip-flops using NAND gates only. Find the Figure 1 , Figure 2 and Fig. 3 circuits outputs (Q and Q) for inputs (J-K) 00, 01, 10, 11, 11, 10, 01, 00 sequence over time. Attach the worksheet with this manual.

Procedure:

- Implement J-K flip-flop with the two inputs (J and K), as shown in Fig.1. Find the circuit output for 00, 01, 10, 11, 11, 10, 01, 00 sequences over time. This circuit is known as a level sensitive J-K flip-flop.

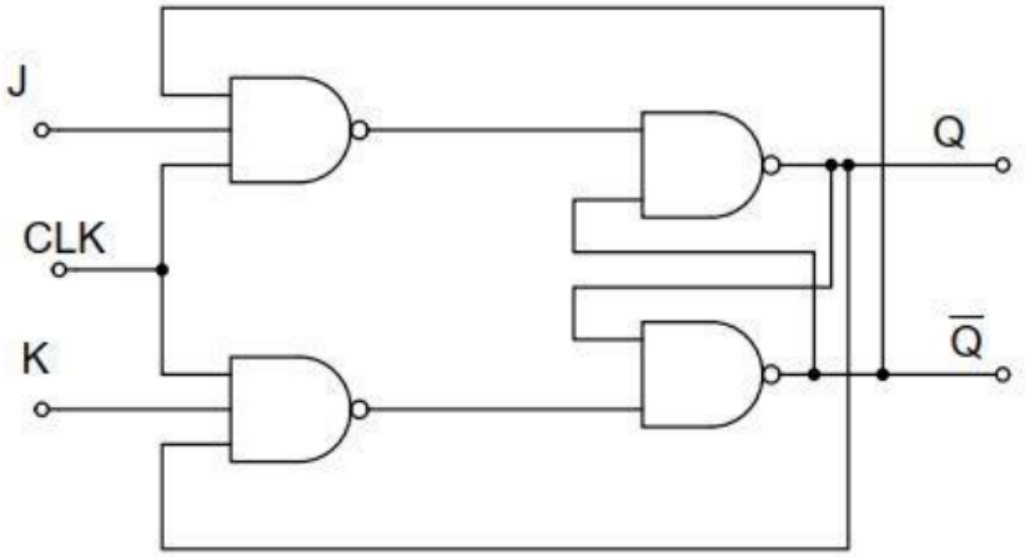

Figure1. Level sensitive J-K flip-flop

- Connect two level-sensitive J-K latch one after the other, with the CLK as shown in Fig. 2. Explore its performance and

identify its output for 00, 01, 10, 11, 11, 10, 01, 00 sequences over time. The first flip-flop is called a master, the second is called a slave, and the combination is known as a master-slave J-K latch

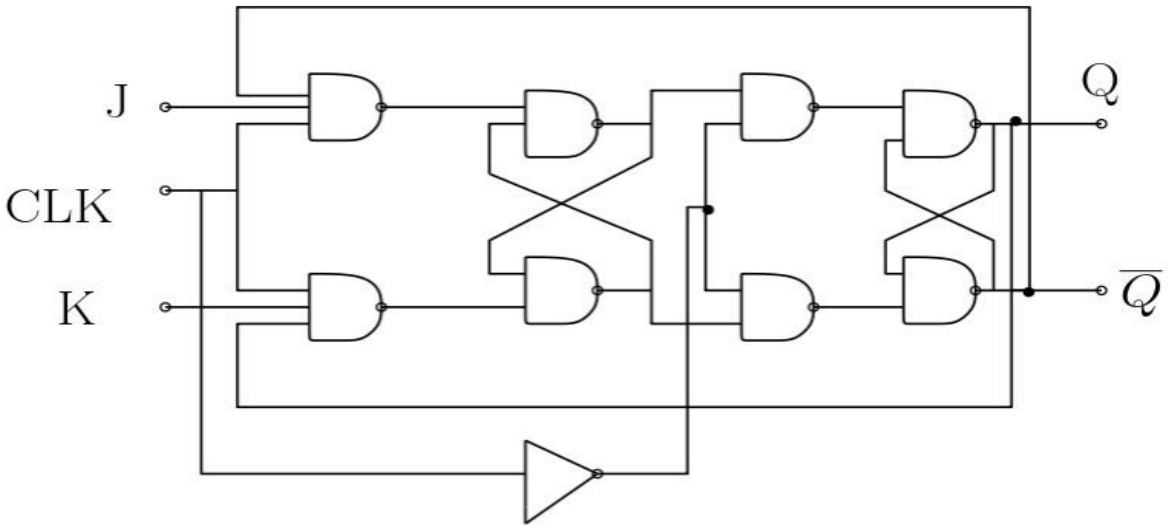

Figure2. Master-Slave J-K flip-flop

- Figure 3 shows the negative edge-triggered J-K flip-flop, where the CLK signal is activated only for a brief period of time. This approach is known as an edge-triggered J-K flip-flop. Evaluate its performance for inputs (J-K) 00, 01, 10, 11, 11, 10, 01, 00 sequences over time. Is there any difference in the truth table, from that of the master-slave J-K flip-flop? .

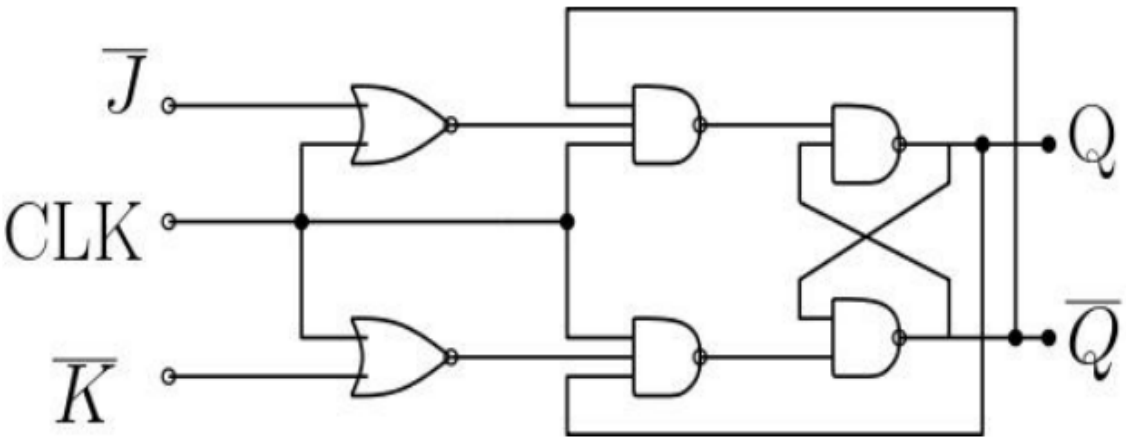

Figure3. Negative Edge trigged J-K flip-flop

Post-Lab quiz:

1 What are the differences between combinational and sequential circuits? Where can we use the sequential circuit?

2. Draw gate level circuit for positive edge triggered J-K flip-flop.

3. Unlike combinational circuits, sequential circuits have two outputs. Why?

Suggested Readings: M. Morris Mano, "Digital Logic and Computer Design", Pearson Prentice Hall, 2008