Indian Institute of Technology Ropar
Department of Electrical Engineering

EE204 : Digital Circuits Laboratory
Classroom - Analog and Digital Circuits Lab

Introduction:

This manual explains how to build registers which are the units of memory storage in computers. In computer architecture, a processor register is a small amount of storage available as part of a CPU or other digital processor. Such registers are (typically) addressed by other mechanisms than main memory and can be accessed more quickly. Almost all computers, load-store architecture or not, load data from a larger memory into registers where it is used for arithmetic, manipulated, or tested, by some machine instruction. Manipulated data is then often stored back in main memory, either by the same instruction or a subsequent one.

Aim:

The objective of this lab exercise is to implement PISO Shift Register using D flip flop and NAND gates.

Components and ICs required: TTL ICs 74LS00, 7474, LEDs, power supply and standard experimental setup.

Theory:

Shift registers are basically of 4 types. These are:

- Serial In Serial Out shift register
  The shift register, which allows serial input and produces serial output is known as Serial In-Serial Out *SISO* shift register. The **block diagram** of the 3-bit SISO shift register is shown in the following figure.
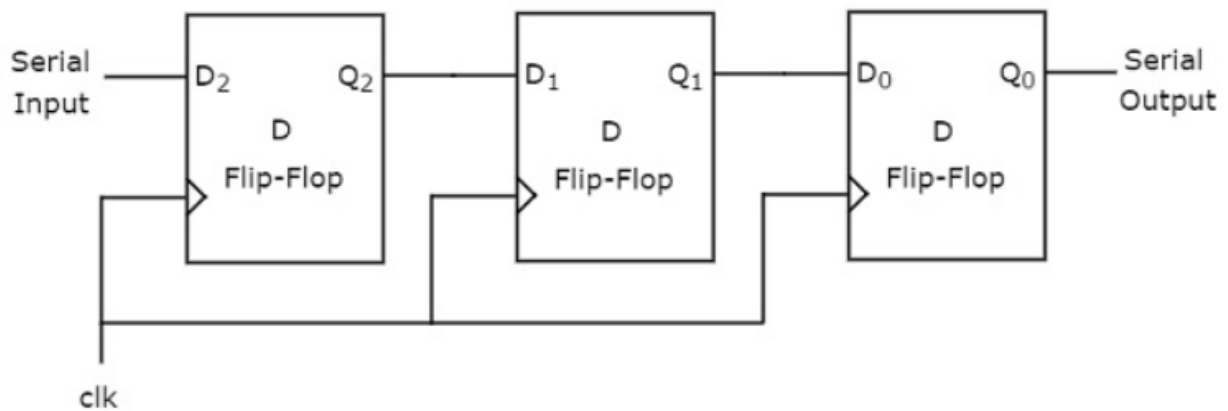
- Serial In parallel Out shift register
  The shift register, which allows serial input and produces parallel output is known as Serial In-Parallel Out *SIPO* shift register. The **block diagram** of the 3-bit SIPO shift register is shown in the following figure.
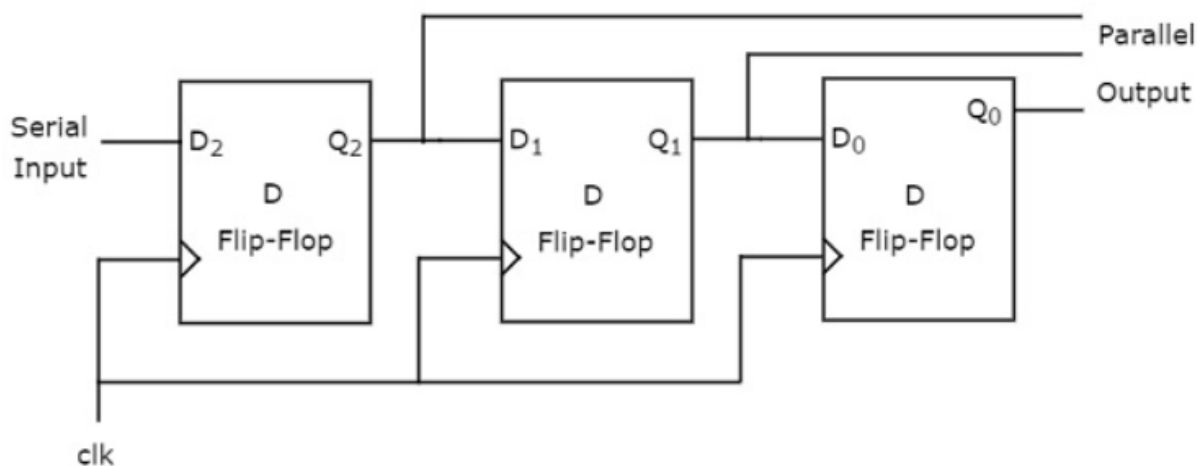
- Parallel In Serial Out shift register
- Parallel In parallel Out shift register

Pre-Lab quiz:
1. Read the experiment hand-out in full.
2. Design a 4-bit binary counter using TFFs?

3. Design a BCD counter which counts from 0 to 9999, using the BCD decade counter as black box?

Procedure:
- Check all the components for their working.
- Insert the appropriate IC into the IC base.
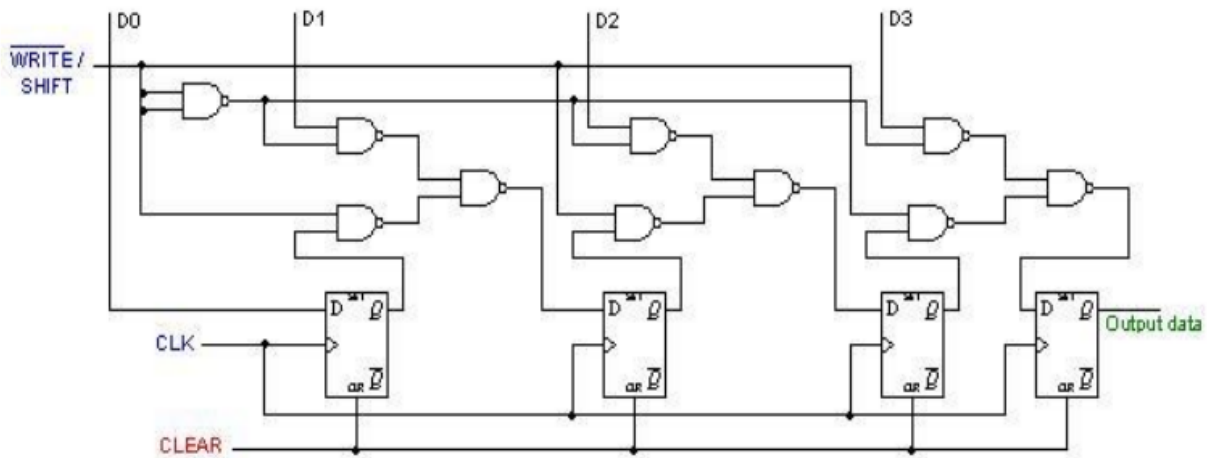- Make connections as shown in the circuit diagram.

Fig. 1: PISO (Parallel in Serial out) Shift Register

- D0, D1, D2, and D3 are the parallel inputs, where D0 is the most significant bit and D3 is the least significant bit. To write data in, the mode control line is taken to LOW and the data is clocked in. The data can be shifted when the mode control line is HIGH as SHIFT is active high. The register performs right shift operation on the application of a clock pulse, as Shown in the table below:

	Q0	Q1	Q2	Q3
CLEAR	0	0	0	0
WRITE	1	0	0	1
SHIFT	1	0	0	1
	1	1	0	0
	1	1	1	0
	1	1	1	1
	1	1	1	1

- Verify the Truth Table and observe the outputs.

Result: At the end of this lab exercise, one should be able to implement a PISO Shift Register using D flip-flop and NAND gates and verify its table.

Post-Lab quiz:
1. Design a SIPO (Serial in Parallel out) shift register using D flip-flop.
2. Design a 3-bit shift register using 2:1 Mux and D Flip Flops which shifts right if the control input, $C = 0$ and shifts left if $C = 1$?
3. What are the unused states in a 3-bit Johnson counter?

Suggested Readings: M. Morris Mano, "Digital Logic and Computer Design", Pearson Prentice Hall, 2008