

### Ans 4) Starvation in Reader - Writer Problem

→ Starvation : Occurs when a writer is continually blocked by a constant stream of newly arriving readers in a Reader - Writer scheme. The writers are guaranteed access as soon as possible.

→ Prevention : Implement a writer - priority scheme when a writer arrives, no new readers are allowed to start. The writers are guaranteed access as soon as the currently active reader & finish, preventing indefinite delay.

### Ans 5) Drawback of Eliminating "Hold and Wait"

→ Elimination Method : force a process to request utilization. Resources are tied up for the entire duration of a process even if only needed briefly. This restricts other processes and reduces overall system throughput.

### Ans 6) Banker's Algorithm Simulation

→ Total Instant :  $A = 10, B = 5, C = 7$   
 → Allocation :  $A = 7, B = 2, C = 5$   
 → Initial Available :  $(10-7, 5-2, 7-5) = (3, 3, 2)$   
 9) Calculate the Need Matrix.

Need ( $A, B, C$ )

$P_0$	7, 4, 3
$P_1$	1, 2, 2
$P_2$	6, 0, 0
$P_3$	0, 0, 0
$P_4$	5, 3, 1

b) Depthwise the system is in a safe state.

~~renders~~ → Safe Sequence (one possibility): safe state.

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when  
to  
as  
rule  
the  $\beta_1$  moment,  
 $(3,3,2) \rightarrow \beta_3(0,0,0) \rightarrow (5,4,3) \rightarrow \beta_2(1,2,2) \rightarrow$   
 $\beta_0(7,4,3) \rightarrow (10,5,7) \rightarrow$

to the  $\mu_1$  request (1,0,2), check whether it can be granted immediately.

1. Check Request  $\leq$  Need :  $(1,0,2) \leq (1,2,2)$  — True.
2. Check Request  $\leq$  Available :  $(1,0,2) \leq (3,3,2)$  — True.  
 $(1,0,2) - (3,3,2) = (2,3,0)$
3. Simulate Grant : New Available  $\Rightarrow (3-1, 3-0, 2-2) = (2,3,0)$
4. Safety Check with New State : A safe sequence can still be found (eg  $\langle P_3, P_1 \text{ new}, P_4, P_2, P_0 \rangle$ )
- ∴ The request  $(1,0,2)$  can be granted immediately because the resulting state is remain safe.

$P_1, P_2, \dots$ ) waits for  $P_0$ ) deadlocks. Circular wait: Impose  $\rightarrow$  Deadlock avoidance. Hodjicahao (Break circular wait): Impose ordering for one philosopher.

Deadline ordering for one Right Chopstick  
on asymmetric, then Right Chopstick  
 $\rightarrow \beta_0 \rightarrow \beta_3$ : Acquire left Chopstick,

## Operating System

### Assignment - 3

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Ans 1

#### Ans 1) Race Condition & Mutual Exclusion

- Race Condition Example (Bank): Two people simultaneously withdrawing the last \$100 from a \$100 account. Both read \$100 deduct, and write \$0, resulting in an incorrect overdrawn balance.

- Mutual Exclusion: Ensures only one person/process can update the shared balance at a time. The first process looks the balance until the transaction is complete, preventing the second process from reading the initial \$100 value.

#### Ans 2) Peterson's Solution vs Semaphores

##### feature

- Implementation Complexity

##### Peterson's Solution

- low. Simple logic with standard variables (flag, turn).

##### Semaphores

- Moderate to high. Requires kernel support for system calls (wait/signal) and process queue management.

##### Hardware Dependency

- Moderate. Requires atomic read/write guarantees (of memory barriers)

- low. Implemented as OS kernel primitives; less dependent on specific CPU architecture.

#### Ans 3) Monitors

- Monitors provide a higher level abstraction that automatically handles locking and signalling often allows for finer-grained multi core systems, resulting in better performance and less contention compared to the typically coarse-grained locking associated with basic semaphore implementations.

### Ans 8) VLSI system analysis

- a) Calculate CPU time spent handling interrupts per second.
- Intupts per second ( $N$ ):
- $$N = \frac{\text{Data Rate}}{\text{Block Size}} = \frac{\text{5.12000 B/s}}{100 \text{ byte}} = \frac{5.12000}{100} = 51.20 \text{ interrupt/s}$$
- Total CPU Time ( $T_{CPU}$ ):
- $$T_{CPU} : N \times T_{int} = 51.20 \times 5 \mu\text{s} = 25600 \mu\text{s} = 0.0256 \text{ sec}$$
- b) Suggest one improvement to reduce CPU context switch overhead.
- Improvement: Use direct Memory Access (DMA).
  - Reason: DMA allows data transfer directly between the device and memory, bypassing the CPU. The CPU is interrupted only once per transfer buffer (not every 100 bytes), drastically reducing overhead.

### Ans 9) Air traffic control system

- a) Critical Sections and IPC Mechanism
- Critical Section:
  - Shared flight database update: ~~Requires mutual exclusion for data integrity.~~
  - Radio Transmitter / Receiver Access: Require exclusive access.
  - Deadlock Detection and Recovery Strategy
  - Detection: Use a Resource - Allocation Graph Algorithm to check for cycles involving RDA and FPC processes.
  - Recovery
    - Selected Victim
    - Promotion
    - Roll back.