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Assignment no: 2

AIM : To design & implement of single digit BCD using IC7483.

OBJECTIVE: 1. To study the BCD arithmetic rules.

2. Comparison between binary and BCD codes.

IC's USED:

IC 7483 (4 bit Binary adder), IC 7404(Hex INV), 7432 (OR-gate), 7408 (AND-gate), 7486 (EX-OR gate)

THEORY:

BCD Adder:
BCD adder is a circuit that adds two BCD digits & produces a sum of digits also in BCD.
Rules for BCD addition:

1. Add two numbers using rules of Binary addition.
2. If the 4 bit sum is greater than 9 or if carry is generated then the sum is invalid. To correct the sum add 0110 i. e. (6)10 to sum. If carry is generated from this addition add it to next higher order BCD digit.
3. If the 4 bit sum is less than 9 or equal to 9 then sum is in proper form. **CASE I : Sum <= 9 & carry = 0.**

Add BCD digits 3 & 4

1. 0 0 1 1
+ 0 1 0 0

.....
0 1 1 1

Answer is valid BCD number = **(7)BCD** & so 0110 is not added.

CASE II : Sum > 9 & carry = 0.

Add BCD digits 6 & 5

1. 0 1 1 0
   + 0 1 0 1

   .....
   10 1 1

Invalid BCD (since sum > 9) so 0110 is to be added

2. 1 0 1 1

   + 0 1 1 0

   .....
   1 0 0 0 1

   | |

   ———

   (1 1)BCD

   |

Valid BCD result = **(11) BCD**

CASE III : Sum < = 9 & carry = 1.

Add BCD digits 9 & 9

1. 1 0 0 1

   + 1 0 0 1

   .....
   1 0 0 1 0

Invalid BCD (since Carry = 1) so 0110 is to be added

2. 1 0 0 1 0
   + 0 1 1 0

.....
1 1 0 0 0

(1 8)BCD

Valid BCD result = **(18) BCD**

Design of BCD adder :

1. To execute first step i. e. binary addition of two 4 bit numbers we will use IC 7483 (with Cin = 0), which is 4 bit binary adder.
2. We need to design a digital circuit which will sense sum & carry of IC 7483 & if sum exceeds 9 or carry = 1, this digital circuit will produce high output otherwise its output will be zero.

Circuit to check invalid BCD :

First we will design circuit to check sum & then we will logically OR output of this circuit to carry output of IC 7483

For digital circuit which we are going to design we will have 4 inputs (S3, S2, S1, S0) & only 1 output Y.

a) Y output of this circuit. Will be ORed with carry output of first adder IC 7483.

b) If BCD result is invalid i. e. sum output of first 7483 we have to add (6)10 i.e. (0110)2 that means we need one more binary adder IC 7483.

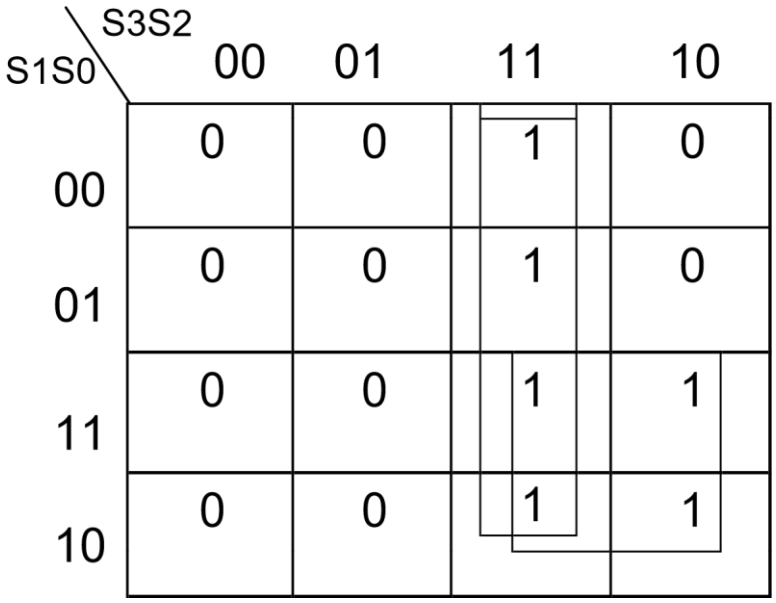
c) If BCD result is valid (i.e. final output of the circuit to check validity is 0) we will make an arrangement that second adder IC 7483 adds (0)10 i. e. (0000)2 to the sum of the first adder IC 7483. The output of the combinational circuit is used as final output carry & carry output of second adder IC is ignored.

i) Truth Table for design of combinational circuit for BCD adder to check invalid BCD :

INPUT				**OUTPUT**
S3	**S2**	**S1**	**S0**	**Y**
0	**0**	**0**	**0**	**0**
0	**0**	**0**	**1**	**0**
0	**0**	**1**	**0**	**0**
0	**0**	**1**	**1**	**0**

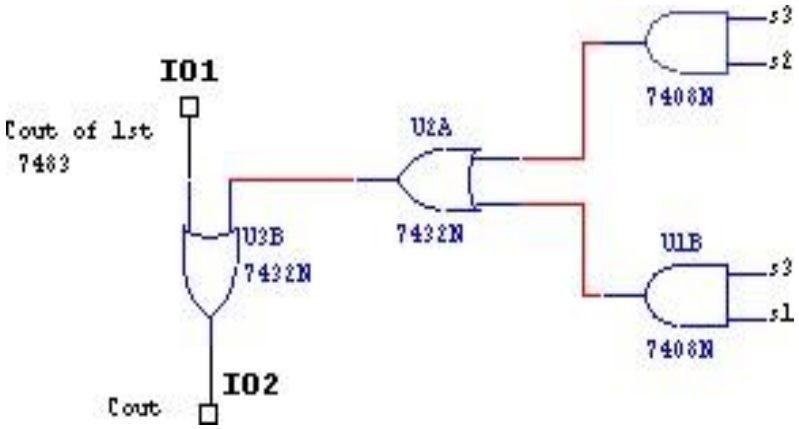
0	**1**	**0**	**0**	**0**
0	**1**	**0**	**1**	**0**
0	**1**	**1**	**0**	**0**
0	**1**	**1**	**1**	**0**
1	**0**	**0**	**0**	**0**
1	**0**	**0**	**1**	**0**
1	**0**	**1**	**0**	**1**
1	**0**	**1**	**1**	**1**
1	**1**	**0**	**0**	**1**
1	**1**	**0**	**1**	**1**
1	**1**	**1**	**0**	**1**
1	**1**	**1**	**1**	**1**

ii) <u>K-map for reduced Boolean expressions of output :</u>

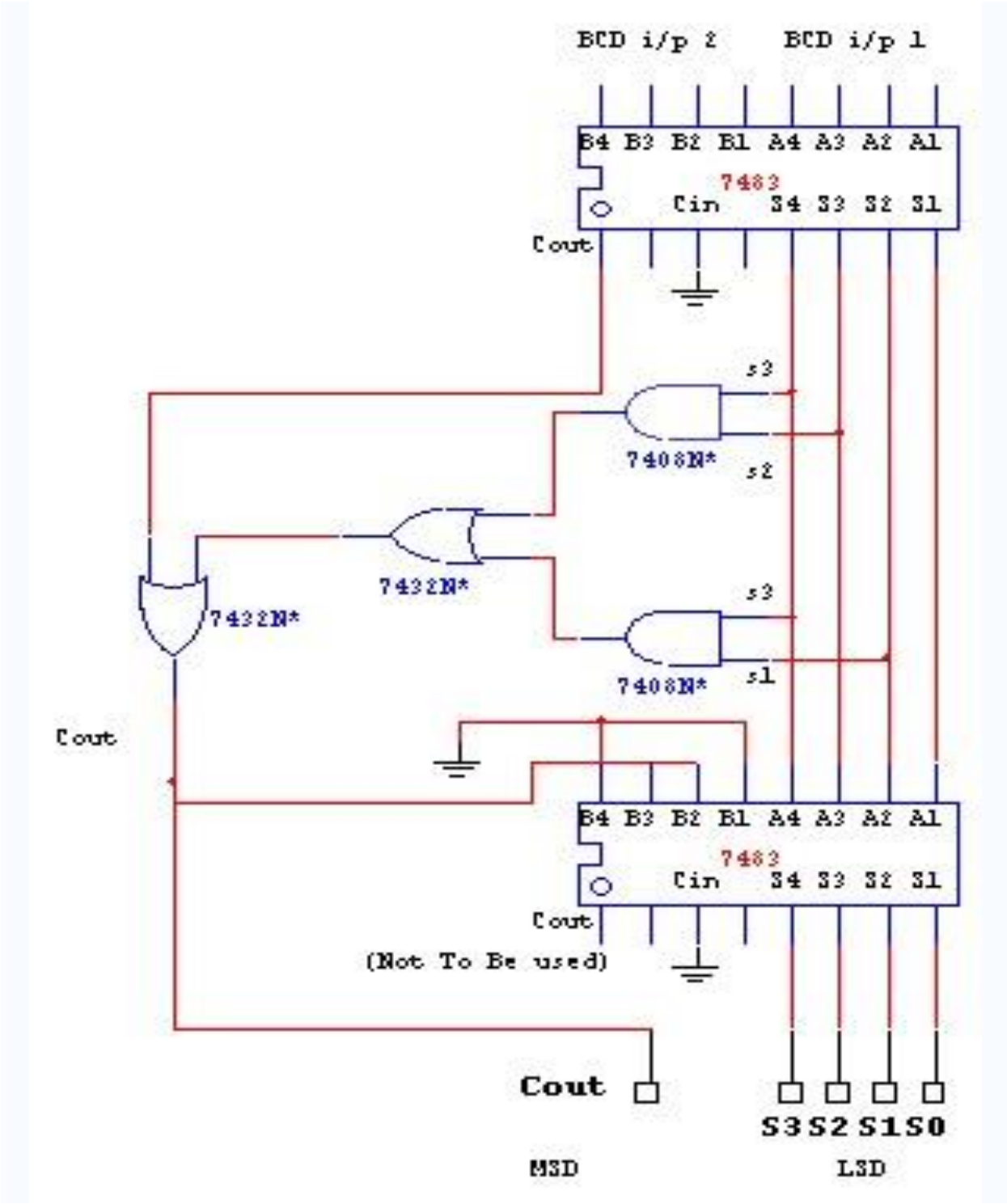


Y = S3S2 + S3S1

iii) <u>Circuit diagram:</u>



iv) <u>Circuit diagram for BCD adder :</u>



v) Hardware Requirements :

GATE	Quantity	IC	Quantity
Binary adder	2	7483	2
AND	2	7408	1
OR	2	7432	1

OBSERVATION :

BCD adder :

INPUT								OUTPUT				
1st Operand				2nd Operand				MSD	LSD			
A3 (MSB)	A2	A1	A0 (LSB)	B3 (MSB)	B2	B1	B0 (LSB)	Cout	S3 (MSB)	S2	S1	S0 (LSB)

2. BCD & Excess 3 Adder

CONCLUSION :

BCD adder is designed using IC 7483 & tested for all possible combinations**.**

OUTPUT: