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Assignment no: 3

AIM: Part A – MUX IC 74153

1) Verification of IC.
2) Implementation of 8:1 Mux by cascading 2, 4:1 mux in IC 74153
3) Boolean function implementation
4) Full adder implementation using hardware reduction table.

OBJECTIVE:

1. To study the multiplexer, Types of Multiplexer.
2. To study the applications of multiplexer.

IC's USED :

IC 74153, 7404.

THEORY :

Multiplexer:

Multiplexer are combinational digital circuits equating as controlled switches with several data inputs (I_0, I_1, I_2 …) & one single data output ("out").At any time one of the I/p is transmitted to output. According to binary signals applied on control pairs to circuit. Usually the number of data inputs is a power of two. Multiplexing is the process of transmitting a large no. of information units over a small no. of channel / digital multiplexer is a combinational large circuit which performs the operation of multiplexing. It selects the operation of multiplexing. It selects the operation of binary information from one of the many input lines & transfer to a single o/p line. Multiplexer is called a data selector or multiposition switch because it selects one of the many input. Selection of a particular line is controlled by a set of a selection lines or selects inputs. The number of select lines depends upon no. of input lines. Generally, there is 'n' selects line for 'm' input lines. By applying a particular code on select lines is transmitted on the output lines.

Block diagram of MUX is shown. at contains '2^m' input lines 'm' select & one unable input which is used to activate.

Study of Multiplexer

Dedicate MUX . Depending upon the no. of I/P & O/P lines various types of multiplexers are available. We have 2:1, 4:1, 8:1, 16:1 MUX. Here the first no. indicates the no. of input lines & second no. indicates the no. of output lines.

Uses of Mux. :

1) Use for Boolean function implementation.
2) Construct a common bus system.
3) To select between multiple sources & signal destination.
4) Inter register transfer.

Advantages :

1) Simplification of logic expression not required.
2) Logic design is simplified.

Disadvantage :

Only one function can be implemented using one MUX. Hence they can't be used in combinational logic circuit which contains many function.

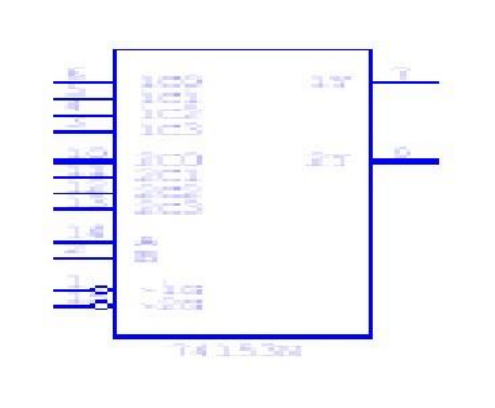
***Part-A (IC 74153*)**

1. **VERIFICATION OF IC 74153 :**

IC 74153 is a dual layer 4:1 MUX. It has four input lines for (I_0D-I_3D) for second MUX & active high output. 'Y_a', 'Y_b' (1Y or 2Y). It has select lines S_1S_0 common to both MUX. The Enable inputs are active low, E_a & E_b (1G and 2G). The MUX is activated when they are at logic o.

			Inputs (I or II)				Output
S_1	S_0	E (I or II)	D_0	D_1	D_2	D_3	Y
X	X	1	X	X	X	X	0
0	0	0	0	X	X	X	0
0	0	0	1	X	X	X	1
0	1	0	X	0	X	X	0
0	1	0	X	1	X	X	1
1	0	0	X	X	0	X	0
1	0	0	X	X	1	X	1
1	1	0	X	X	X	0	0
1	1	0	X	X	X	1	1

Pin out of IC 74153:

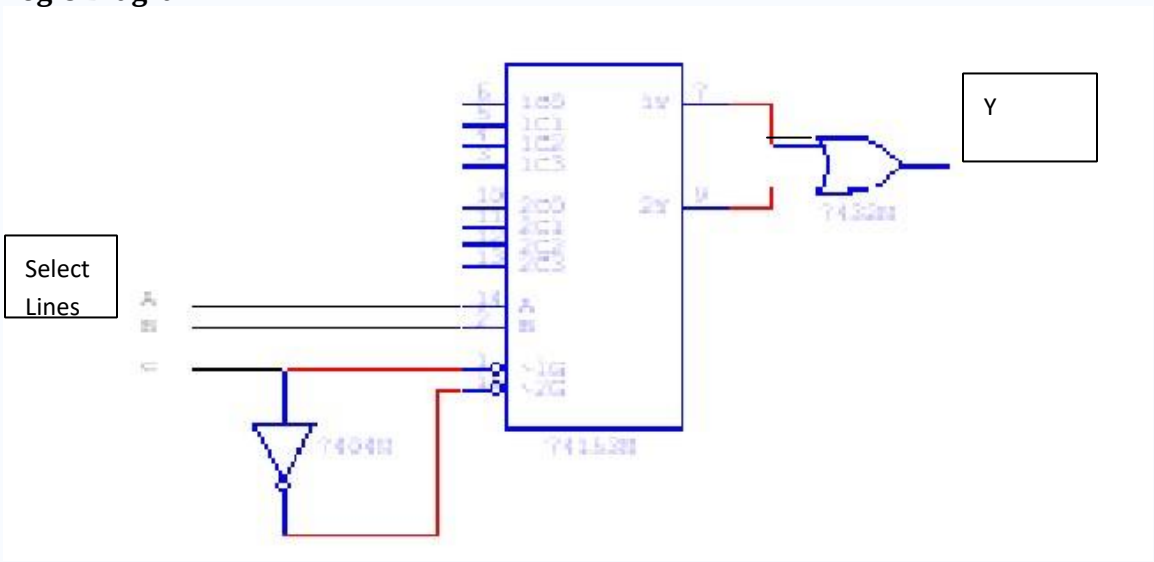


Function table of IC 74153: (X= Don't Care Condition)

2. CASCADING OF IC 74153:

Cascading is done to expand two or more MUX IC's to a digital multiplexer with larger no. of inputs i.e. multiplexer stocks or tress is designed. The enable input is used for cascading. In case of IC 74153 we have only two select lines. But for certain application 3 select lines are required then it can be obtained by cascading using enable. Now with 3 select lines we have 8 combinations. Out of this combination the MSB is O. MSB is 1 for last four combination so we can use these MSB to select any 1 MUX out of two by connecting it to E pin of first 4:1 MUX .

Logic Diagram



Function table of IC 74153 as 8: 1 Mux by cascading 2 4:1 Mux :

Select Input			***Output***
C (1G / 2G)	***B (S_1)***	***A (S_0)***	***Y***
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3
1	0	0	D_4
1	0	1	D_5
1	1	0	D_6
1	1	1	D_7

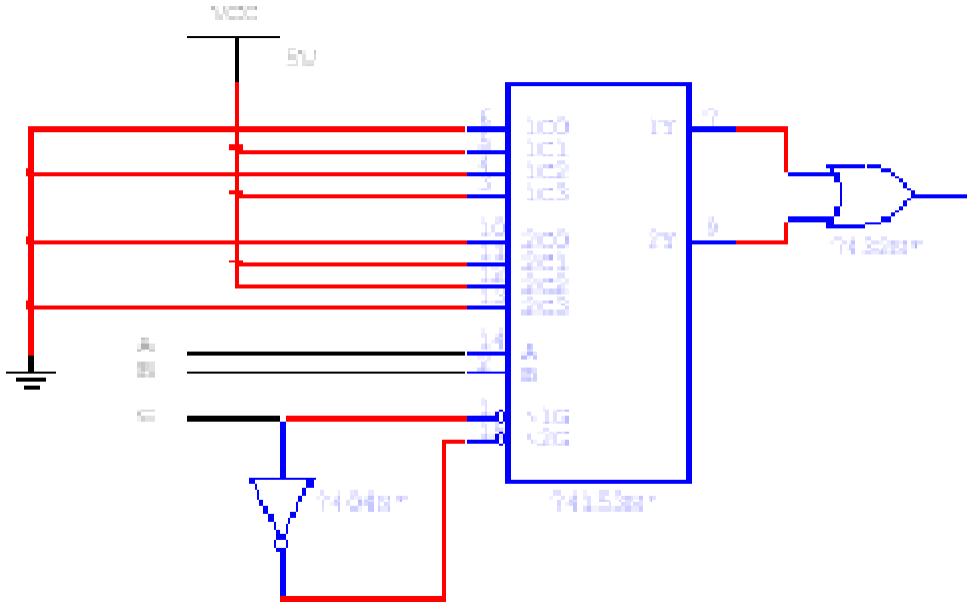
3. Function Implementation

Y= ∑ m (1, 3, 5, 6)

This expression is in Standard SOP form and it is three variable function. So, we need to use mux with three select inputs i.e. 8:1 Mux. Already we have implemented 8:1 Mux using IC 74153. For Boolean function in Standard SOP form we connect data inputs corresponding to the minterms present in the given function to Vcc and remaining data inputs to ground.

Truth table :

Inputs			***Output***
C	***B***	***A***	***Y***
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0



LOGIC DIAGRAM :

Inputs

Hardware Requirements :

GATE	Quantity	IC	Quantity
Mux.	1	74153	1
NOT	1	7404	1
OR	1	7432	1

4. IMPLEMENTATION OF FULL ADDER USING IC 74153:

A full adder is a combinational circuit that forms the arithmetic sum of three input bits. It consists of three inputs and two outputs. Two of these variables denoted by A and B represent the two

significant bits to be added. The third input represents the carry from previous lower significant position.

Truth Table for Design of full adder:

Input			***Output***	
A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Sum= $\sum$m (1, 2, 4, 7), Carry=$\sum$m (3, 5, 6, 7)

Hardware reduction table for Sum:

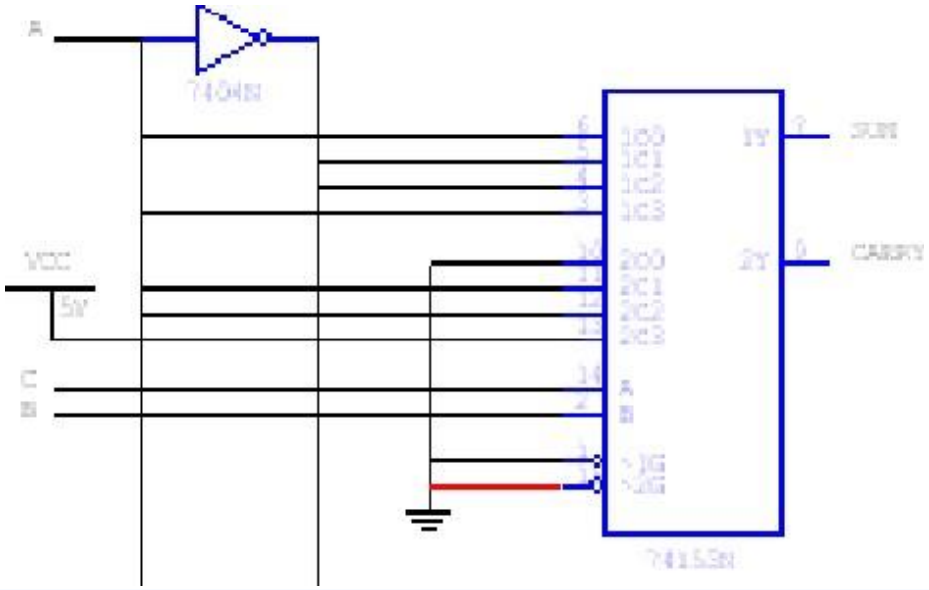
	D_0	**D_1**	**D_2**	**D_3**
A	0	1	2	3
A	4	5	6	7
i/p to MUX	A	A	A	A

Hardware reduction table for Carry:

	D_0	**D_1**	**D_2**	**D_3**

A	0	1	2	3
A	4	5	6	7
i/p to MUX	0	A	A	1

Logic Diagram of Full Adder using IC 74153:

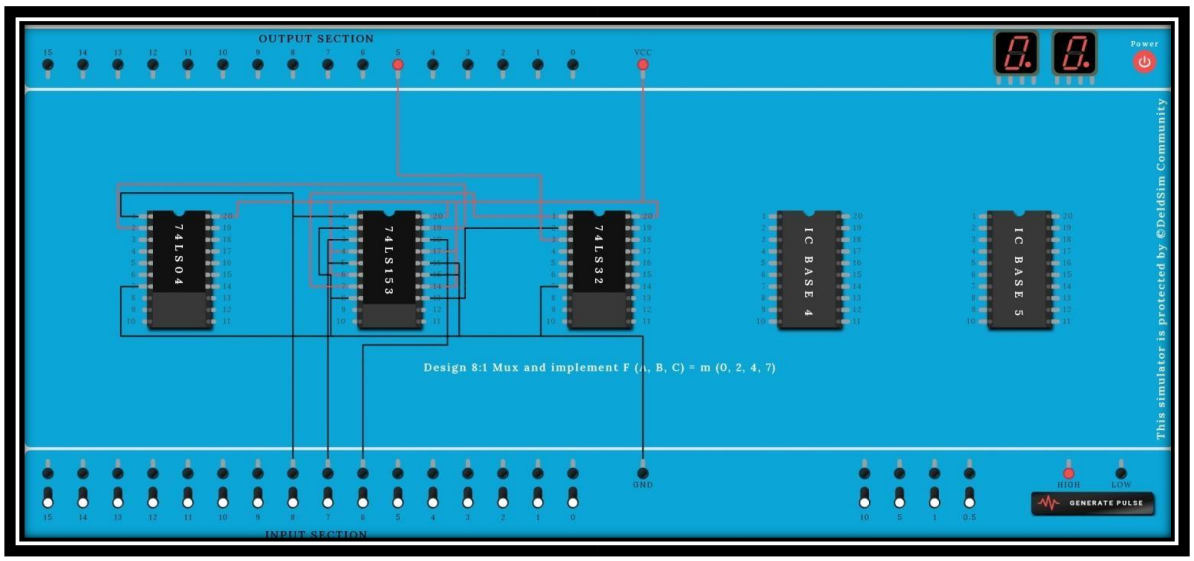


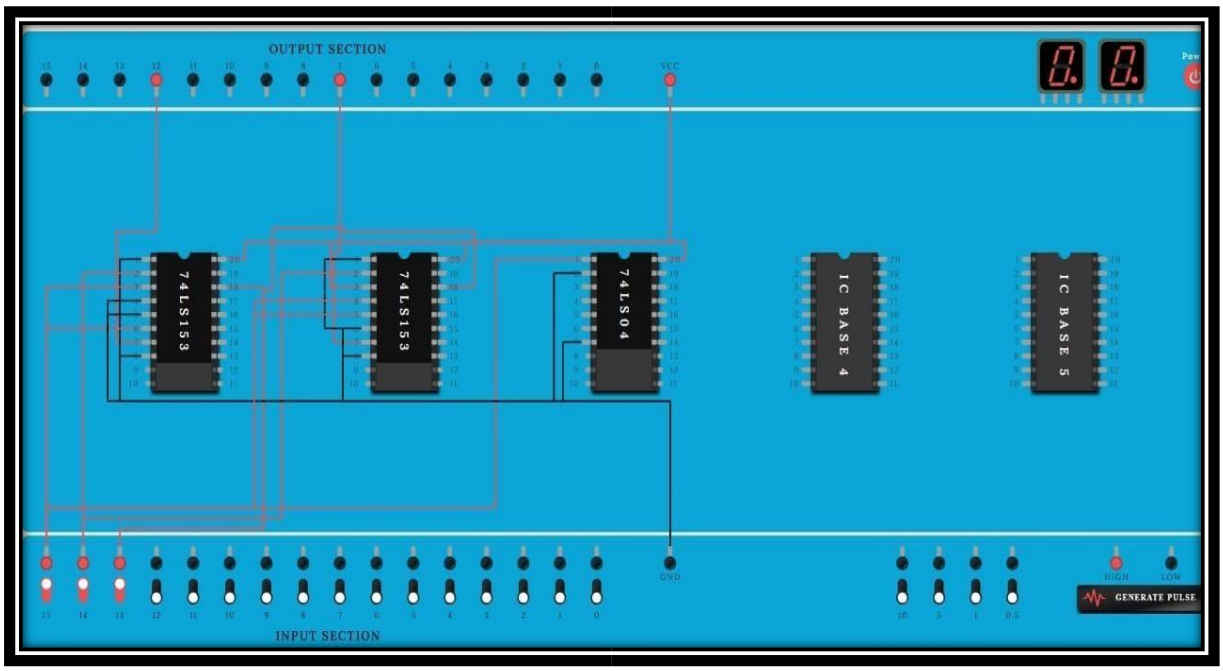
Hardware Requirements :

GATE	Quantity	IC	Quantity
Mux.	1	74153	1
NOT	1	7404	1

Conclusion : In this way multiplexer function and full adder is Designed, implemented & tested. & its applications are studied, implemented & tested.

OUTPUT :


OUTPUT SECTION
VCC
Power
74LS04
74LS153
74LS32
IC BASE 4
IC BASE 5
Design 8:1 Mux and implement F (A, B, C) = m (0, 2, 4, 7)
This simulator is protected by ©DeldSim Community
GND
HIGH
LOW
GENERATE PULSE
INPUT SECTION


OUTPUT SECTION
VCC
74LS153
74LS153
74LS04
IC BASE 4
IC BASE 5
GND
HIGH
LOW
GENERATE PULSE
INPUT SECTION