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Div-IT A

ASSIGNMENT-7
Modulus And Counter

AIM: To design and implement mod- 10, mod – 7, Mod-100 asynchronous BCD counter using IC 7490.

OBJECTIVE: To know Modules counter as well as binary &BCD Counter

IC's USED: IC 7490.

THEORY: **Part A – IC 7490**

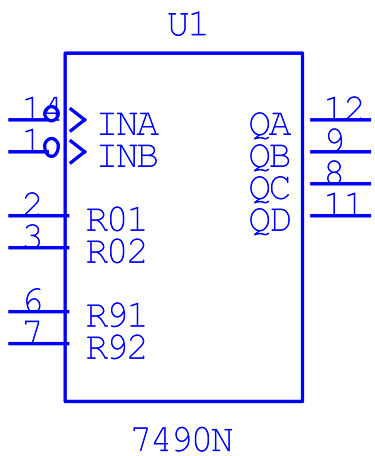
IC 7490 is a TTL MSI (medium scale integration) decade counter. It contains 4 master slave flip flops internally connected to provide MOD-2 i.e. divide by 2 and MOD-5 i.e. divide by 5 counters. MOD-2 and Mod-5 counters can be used independently or in cascading.

It is a 4-bit ripple type decade counter. The device consists of 4-master slave flip flops internally connected to provide a divide by two and divide by 5 sections. Each section has a separate clock i/p to initiate state changes of the counter on the high to low clock transition.

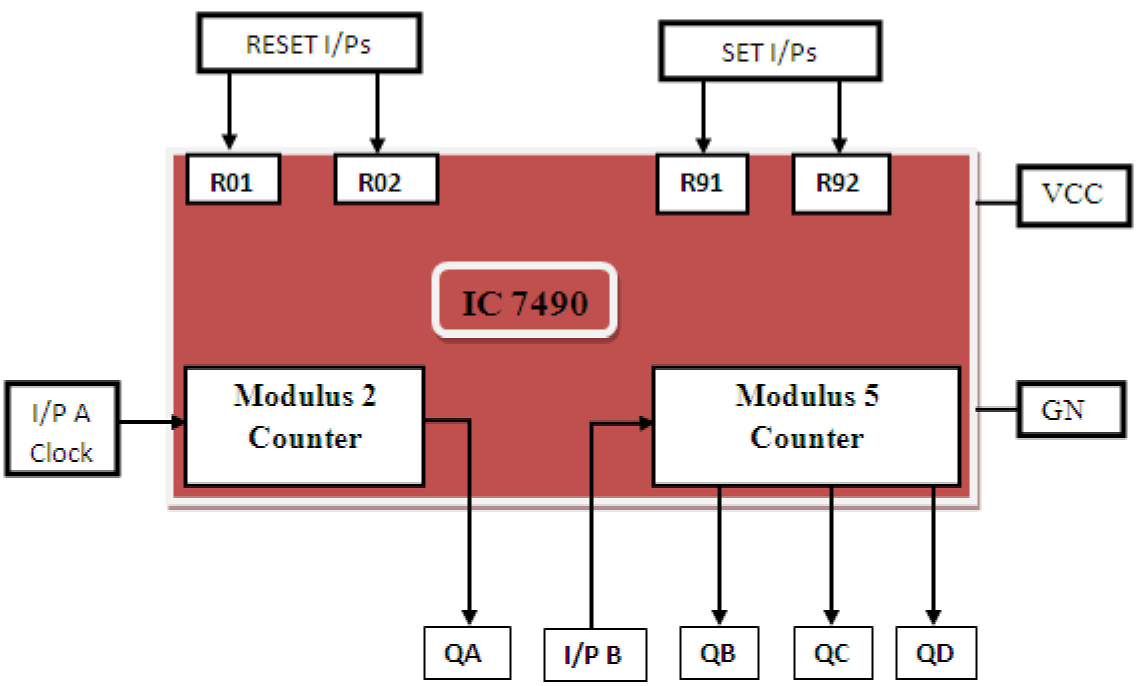
Since the o/p from the divide by 2 section is not internally connected to the succeeding stages. The device may be operated in various counting modes. In a BCD counter the CP_1 input must be externally connected to Q_A o/p. The CP_0 i/p receives the incoming count producing a BCD count sequence. It is also provided with additional gating to provide a divide by 2 counter and binary counter for which the count cycle length is divide by 5. The device may be operated in various counting modes.

There are 2 reset inputs $R_0(1)$ and $R_0(2)$ both of which need to be connected to the 'logic 1' for clearing all flip flops. Two set inputs $R_g(1)$ and $R_g(2)$ when connected to logic 1 are used for setting counter to 1001 (BCD 9).

Pin out of IC 7490:



Basic internal Structure of IC 7490:



Function Table of MOD-2 counter:

Input A clock	Output	Count
↓	0	0
↓	1	1

Function Table of MOD-5 counter:

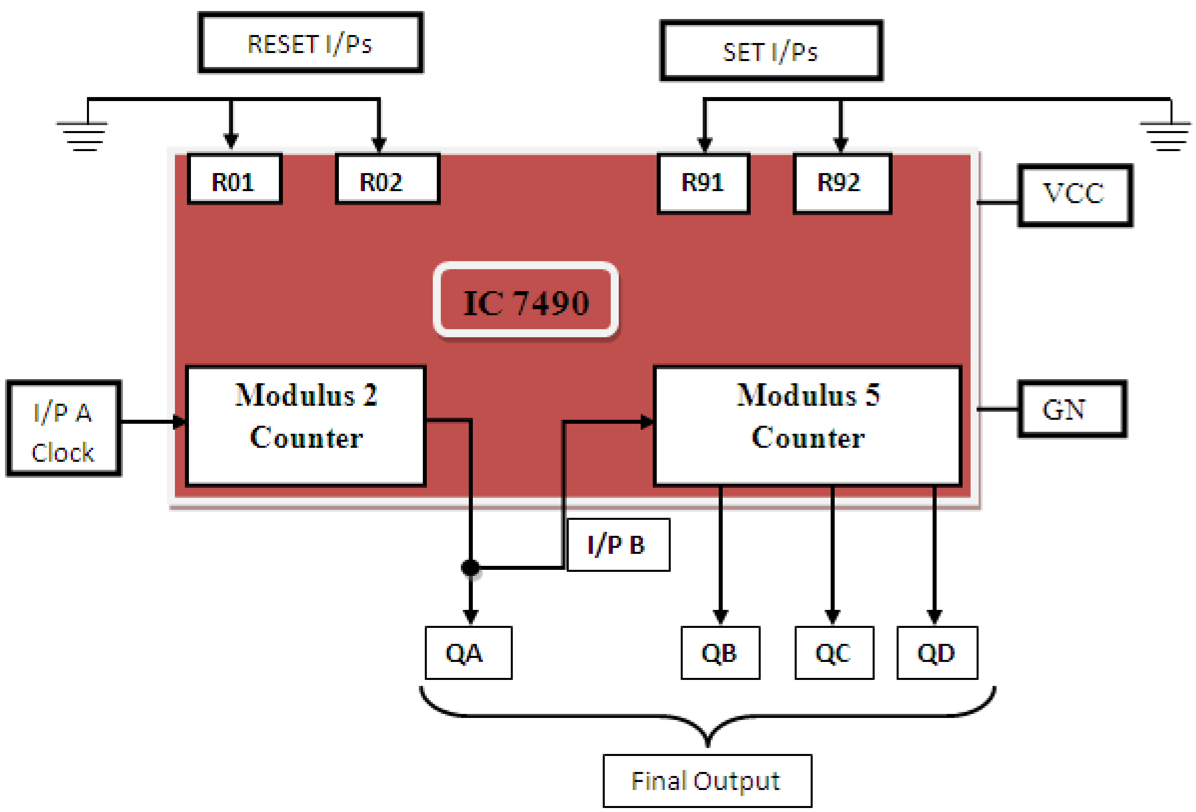
InputB clock	Output			Count
	QD	**QC**	**QB**	
↓	**0**	**0**	**0**	**0**
↓	**0**	**0**	**1**	**1**
↓	**0**	**1**	**0**	**2**
↓	**0**	**1**	**1**	**3**
↓	**1**	**0**	**0**	**4**

Design of MOD-10 counter using IC 7490:

The QA o/p the first flip flop is connected to the input B which is clock i/p of internal MOD-5 ripple counter. Due to cascading of Mod-2 and Mod-5 counters, the overall configuration the decade counters count from 0000 to 1001. After 1001 mod-5 resets to 0000 and next count after 1001 is 0000.

When QA o/p is connected to B i/p, we have the Mod-2 counter followed by Mod-5 counter. The count sequence obtained is shown in the table. It may be noted that QA changes from 0 to 1 the state of Mod-5 counter doesn't change, whereas when QA changes from 1 to 0 the Mod-5 counter goes to the next state.

Logic DiagramMOD-10 counter using IC 7490:

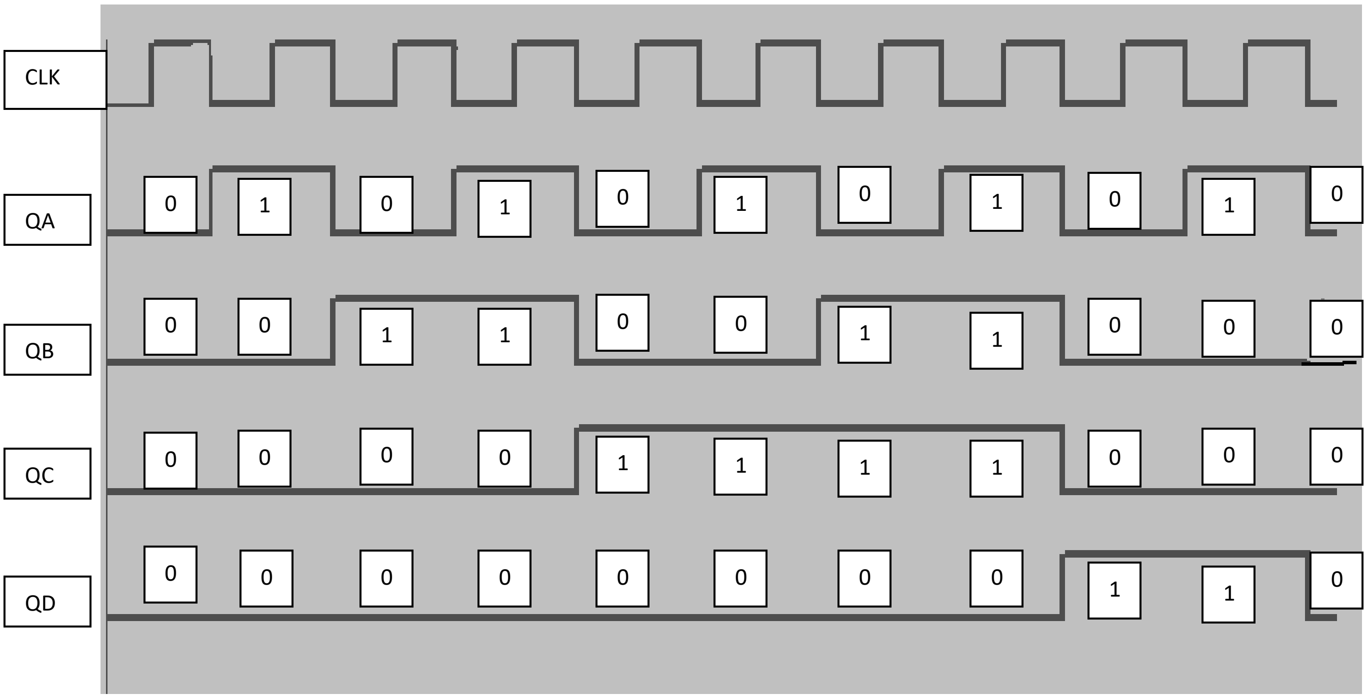


5. Modulus n Counter

Function table:

I/p clock	Output				Count
	QD	**QC**	**QB**	**QA**	
$\downarrow$	**0**	**0**	**0**	**0**	**0**
$\downarrow$	**0**	**0**	**0**	**1**	**1**
$\downarrow$	**0**	**0**	**1**	**0**	**2**
$\downarrow$	**0**	**0**	**1**	**1**	**3**
$\downarrow$	**0**	**1**	**0**	**0**	**4**
$\downarrow$	**0**	**1**	**0**	**1**	**5**
$\downarrow$	**0**	**1**	**1**	**0**	**6**
$\downarrow$	**0**	**1**	**1**	**1**	**7**
$\downarrow$	**1**	**0**	**0**	**0**	**8**
$\downarrow$	**1**	**0**	**0**	**1**	**9**

Timing diagram of mod10:



Design of Mod-7 Counter using IC 7490:

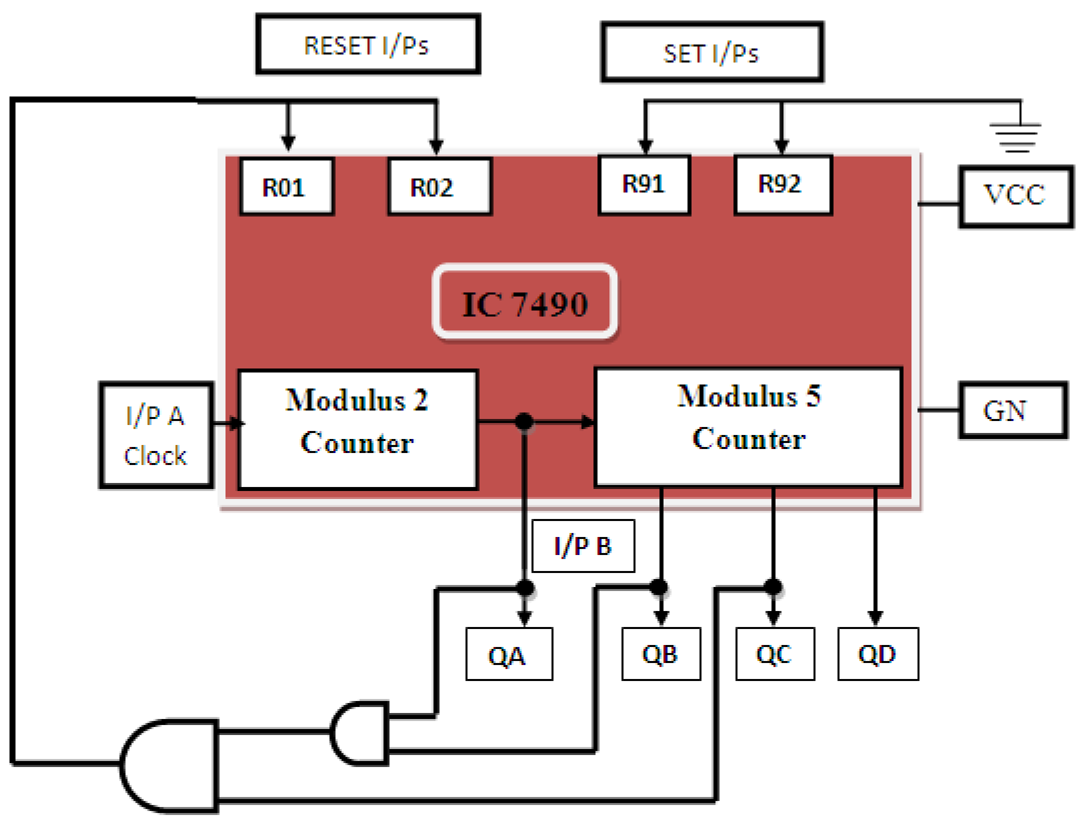
Mod-7 counter counts through seven states from 0 to 6 counters and it should reset as soon as the count becomes 7. The o/p of reset logic should be 1 corresponding to invalid states. The reset logic o/p should be applied to pin 2 and 3.

Truth Table of Reset Logic:

QD	QC	QB	QA	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0

0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1

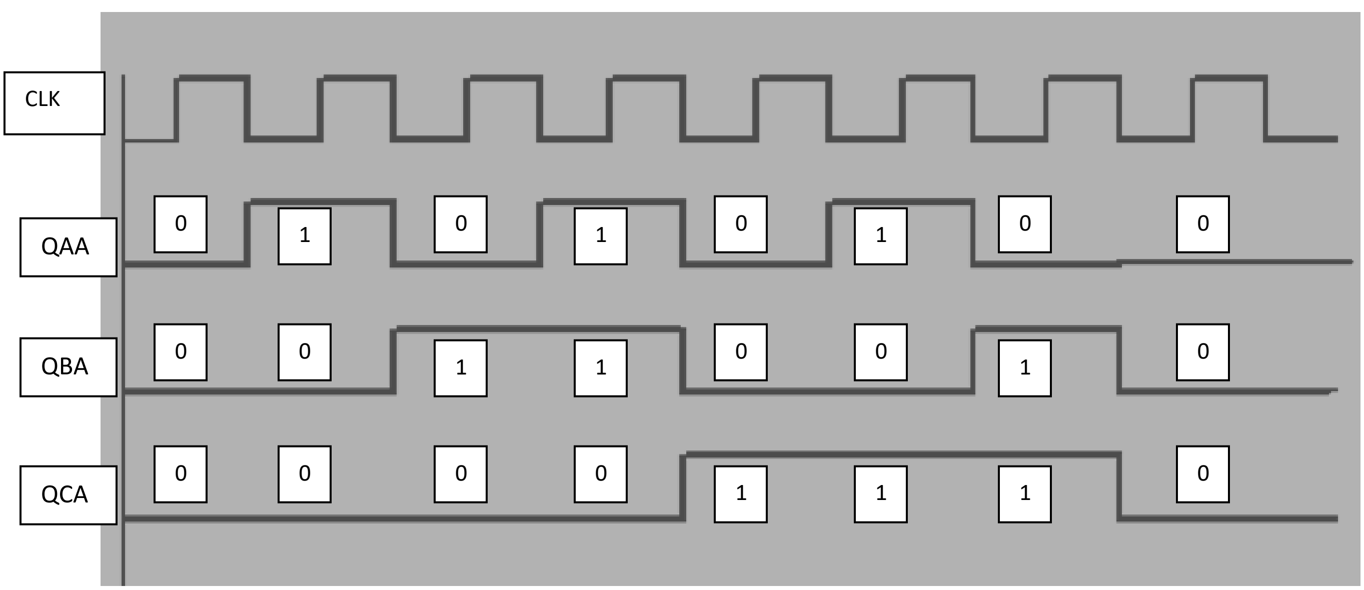
Logic Diagram Mod 7 Counter using IC 7490:



Function table:

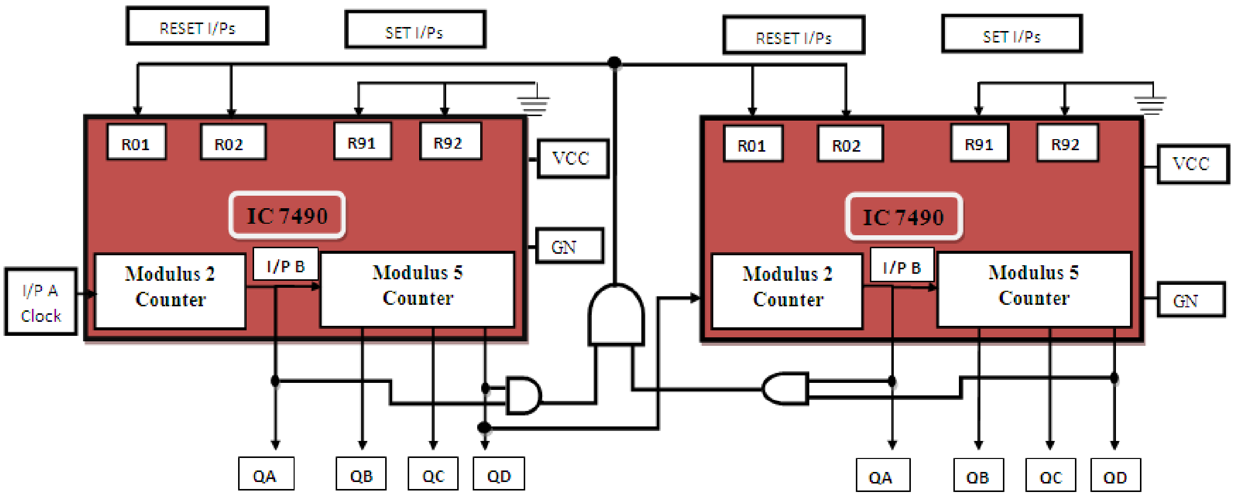
I/p clock	Output				Count
	QD	**QC**	**QB**	**QA**	
↓	**0**	**0**	**0**	**0**	**0**
↓	**0**	**0**	**0**	**1**	**1**
↓	**0**	**0**	**1**	**0**	**2**
↓	**0**	**0**	**1**	**1**	**3**
↓	**0**	**1**	**0**	**0**	**4**
↓	**0**	**1**	**0**	**1**	**5**
↓	**0**	**1**	**1**	**0**	**6**

Timing diagram of mod7:



Design of Mod-99 using IC 7490:

For Mod-99 two IC 7490’s will be required. Hence to implement a divide by 99 counter we have to use two decade counters IC’s. A divide by 99 counter counts 99 states from 0 to 98 and the counter should reset as soon as the count becomes 99. So in order to reset the counter of 99 connect the Q o/p which are equal to 1 in the count of 99 to an ‘And’ gate & then connect and o/p to the reset i/p of both IC’s.



Conclusion:Thus we have Designed MOD -100 using IC 7490

FAQs:

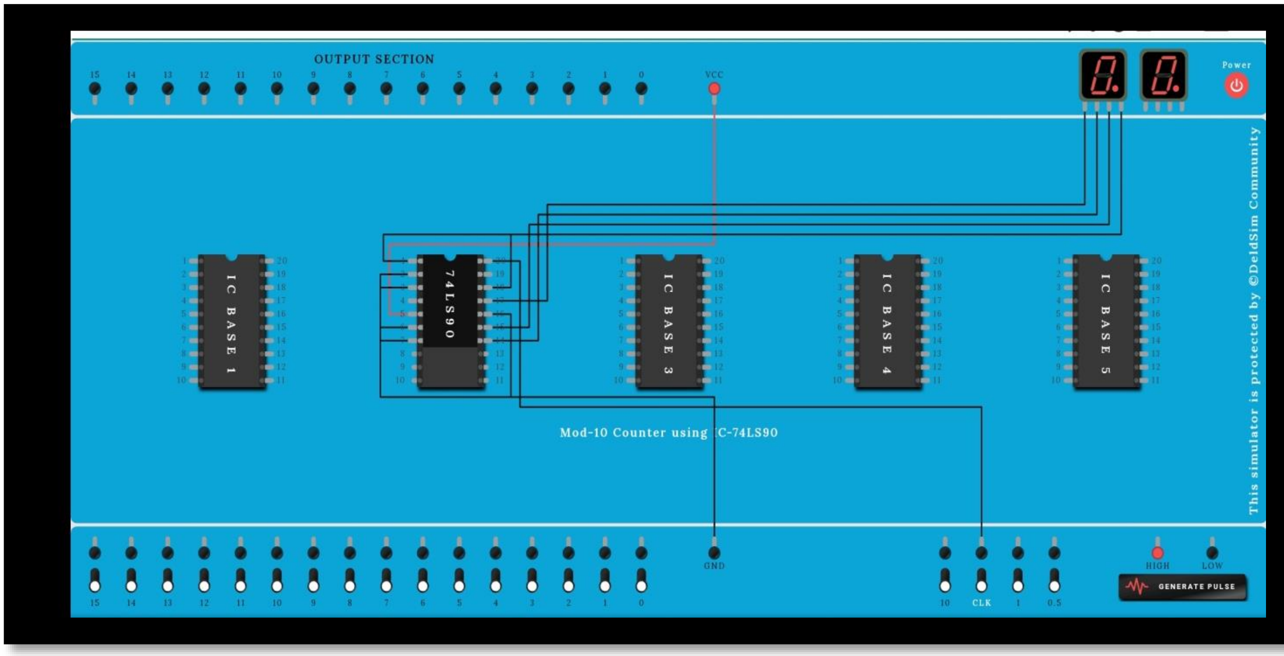
1. What do you mean modulus counter?

It represents the number of possible states of counter.

2. How will you use the 7490 IC to design symmetrical divide by 10 frequency counter?

The divide by 5 circuit followed by divide by 2 circuit will give symmetrical output.

1. Where counters are used? Give real life example of counter.


OUTPUT SECTION
Mod-10 Counter using IC-74LS90
74LS90
IC BASE 1
IC BASE 3
IC BASE 4
IC BASE 5
GENERATE PULSE
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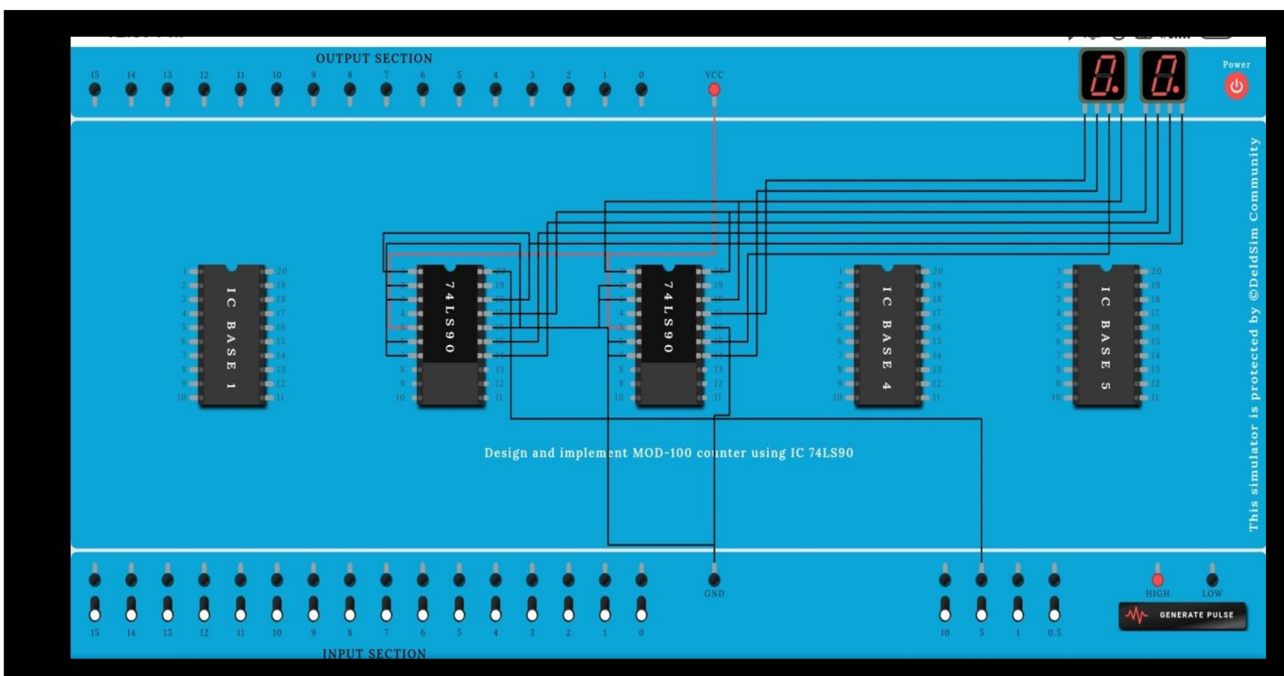
OUTPUT SECTION
Design and implement MOD-100 counter using IC 74LS90
74LS90
74LS90
IC BASE 1
IC BASE 4
IC BASE 5
GENERATE PULSE
INPUT SECTION
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