Design of 4x4 bit Content Addressable Memory

Team E : CSE 593

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Abstract

We have designed a 4x4 Content addressable memory (CAM). CAM is used as a look up table for destination addresses in router. Here, we have devised a4x4 bit CAM, where a 4 bit input word was compared with 4x4 data stored in the memory cells. This comparison was done by parallelly matching the MSB bits of all stored data line , followed by the next matched bits. The additional feature of these memory cells which makes it differ from traditional SRAM cells is the mask bit logic and the evaluation circuitry added to every bit. The word line which matches with the searched data gets charged and whereas the unmatched data lines show a logic low signal. The power consumption of CAM was also observed. The experiment was carried out on Cadence Virtuoso tool.

Introduction

In general a CAM contains a search data register connected to a series of memory blocks via search lines, and an encoder to output the memory location of the search term. Similarly, a TCAM uses the same structure, but extends the number of inputs to enable don't care conditions. This conceptual view is depicted in the diagram below:

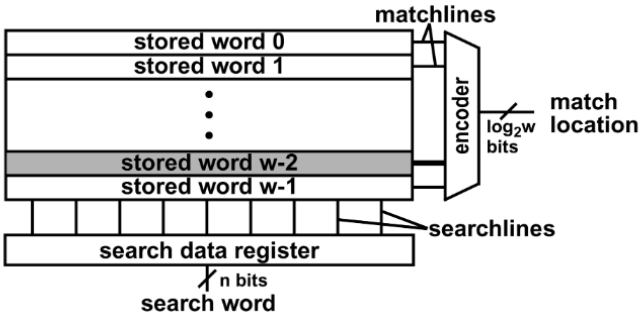

Fig 1: CAM cells

The efficient lookup time of CAM comes from the fact that the search data register is connected in parallel to all of the memory locations. Thus, allowing for the memory to be searched in a single clock cycle. This is depicted in the schematic below:

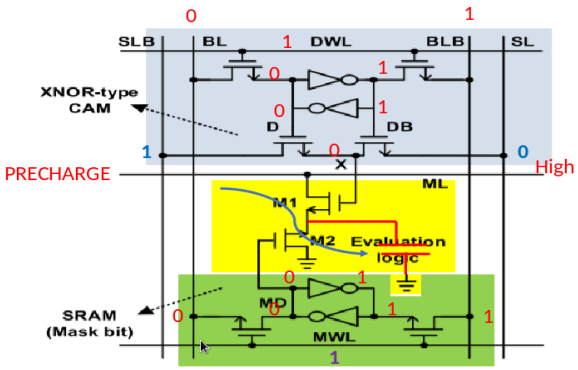

Fig 2: Architecture of a TCAM cell

Each of the memory blocks in the TCAM is similar to that of a CAM cell. It utilizes the circuitry of SRAM that uses 8 transistors including 2 inverters and 4 NMOSs and has an extract match line. However, a standard TCAM circuit uses two SRAMs to allow for ternary data storage. The single bit stored in a single CAM cell is fed through the
Furthermore, in order to implement the *don't care* condition or *ternary bit*, a 1 bit SRAM cell that stores the mask bit is implemented. Lastly, the third block is the evaluation logic block that controls the state of matchline - which is we get the information about the output of this cell.

In addition to this fundamental TCAM architecture. The power consumption of the system is known to be reduced by using techniques such as precharging certain sections of CAM memory. This can be achieved by PMOS transistors to precharge the matchline (which will be explained further in the document).

The TCAM cell has 5 major signals. The (i) differential data/bit lines, (ii) differential search lines, (iii) a match word line input, (iv) a matchline output, and (v) a precharge input.

Initially, the matchline is connected to the PMOS precharge circuitry. This precharge block is responsible for driving the matchline to VDD as soon as the circuit is started. The data/bit to be stored in a TCAM cell is fed through the differential bit lines. The data to be searched or compared is fed through the differential search lines. If the data in search lines and the data lines match, then the matchline output is kept at VDD indicating that the search *matched*. If the data in search lines and the data lines does not match, then the evaluation logic block containing the 2 NMOSs turns on and the matchline is pulled down to logic 0 indicating that the search *mismatched*. However, if the mask bit is enabled then the don't care condition will be asserted and hence the data will *match* regardless of what result is returned by the search lines in the cell. This is how data is stored, searched and matched inside a single TCAM cell. Arrays of TCAMs are created and the same process is done to search *n*-bit data in the *n*x*m* TCAM array. The fact

that the search operation on an array of large dimensions is executed in a single clock cycle should be kept in mind.

DESIGN SPECIFICATIONS

INPUTS		
1	WL	Write Line, enables data write when high and enables data read when low
2	data	used to store data bits in the latch
3	SL	Search Line, data to be searched
4	PRE	To Precharge the circuit to vdd
5	MWL	Mask bit Write Line , kept low when we need a don't care condition

DATA STORED IN CAM CELLS AT DESIGN LEVEL		
1	FIRST WORD LINE	1110
2	SECOND WORD LINE	1100
3	THIRD WORD LINE	1101
4	FOURTH WORD LINE	1010

OUTPUTS			
1	ML_1	Match line for first word line	Low
2	ML_2	Match line for second word line	High
3	ML_3	Match line for third word line	Low
4	ML_4	Match line for fourth word line	Low

CIRCUIT DESIGN:

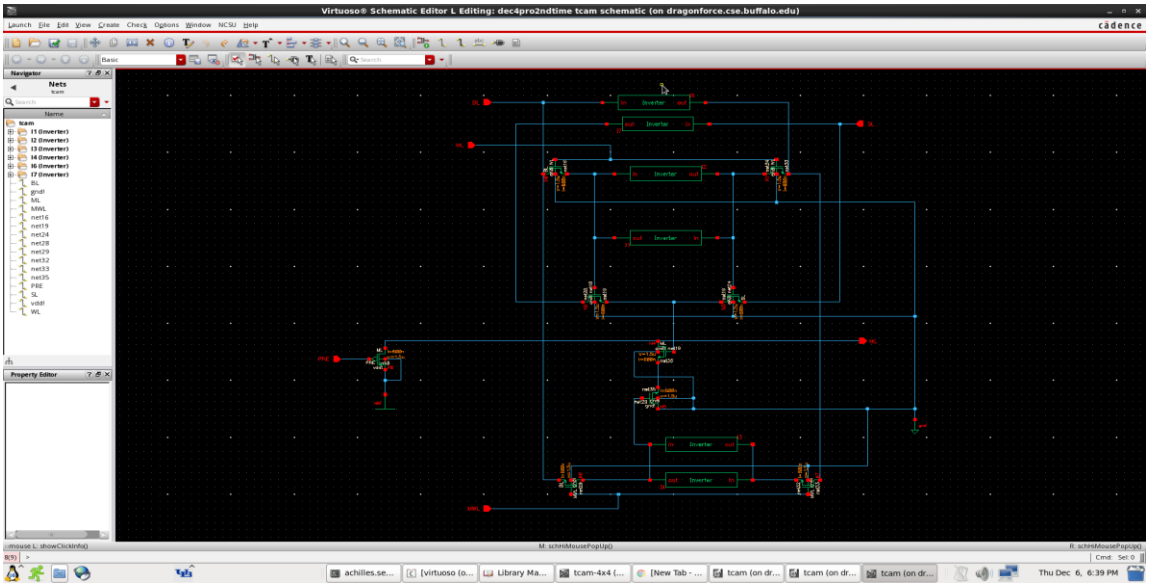

Fig3: Schematic view for a single TCAM cell

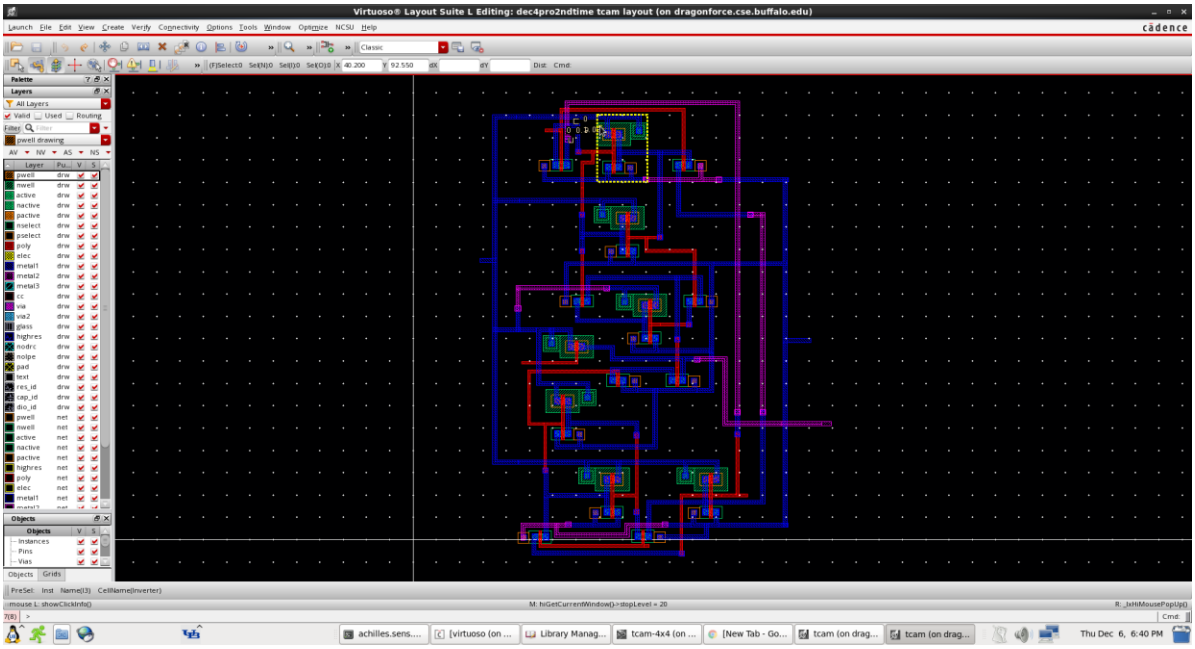

Fig 4: *Layout for a single TCAM cell*

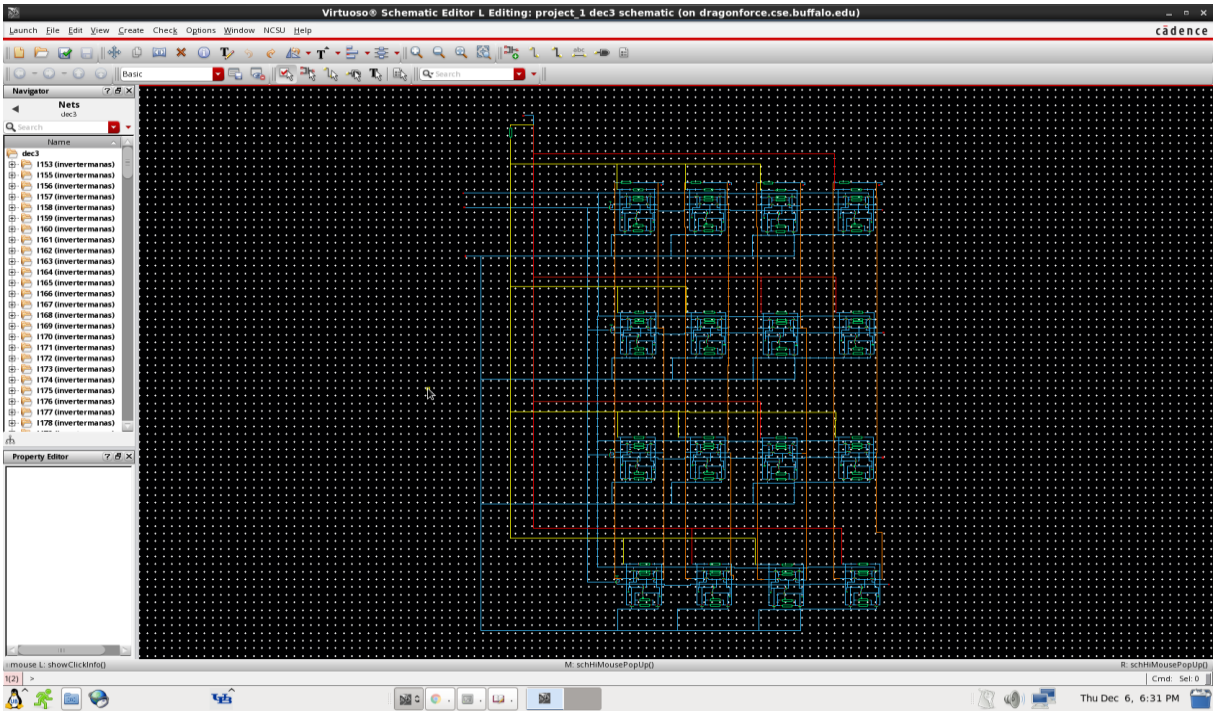

Fig 5: *Schematic for 4x4 TCAM array*

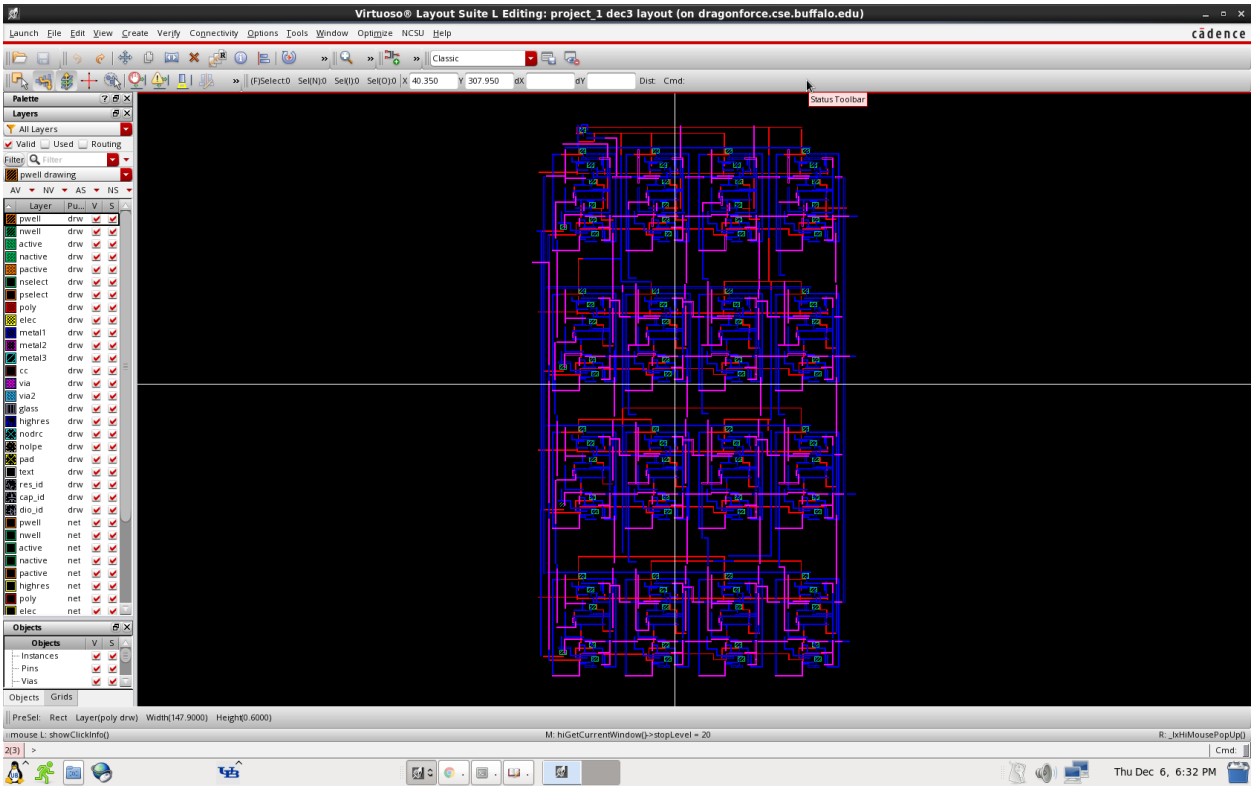

Fig 6: *Layout for 4x4 TCAM array*

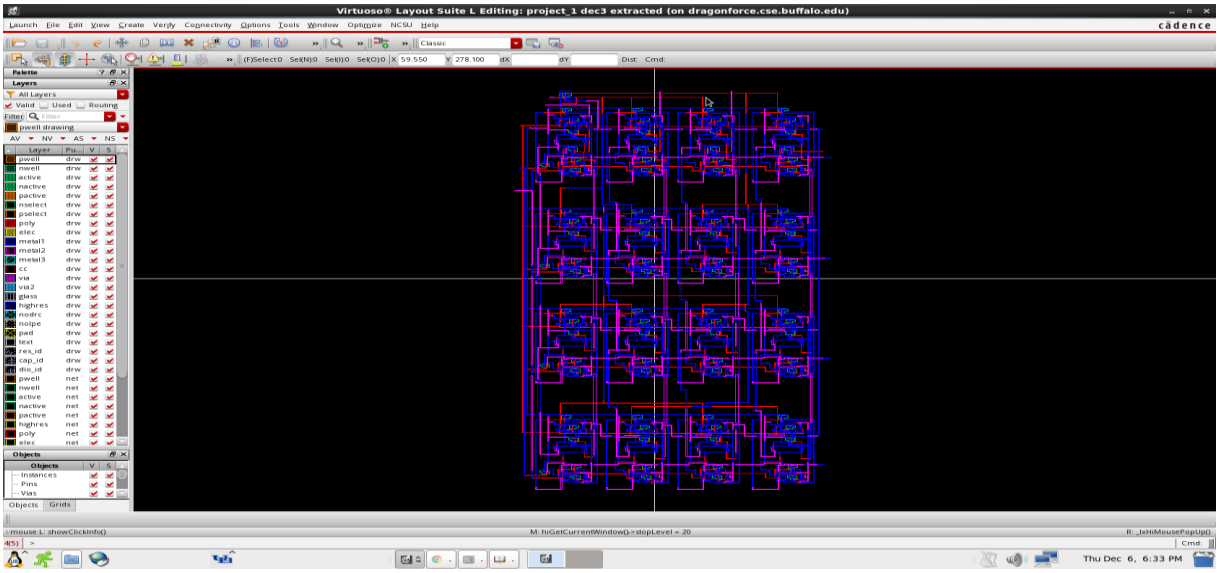

Fig 7: *Extracted for 4x4 TCAM array*

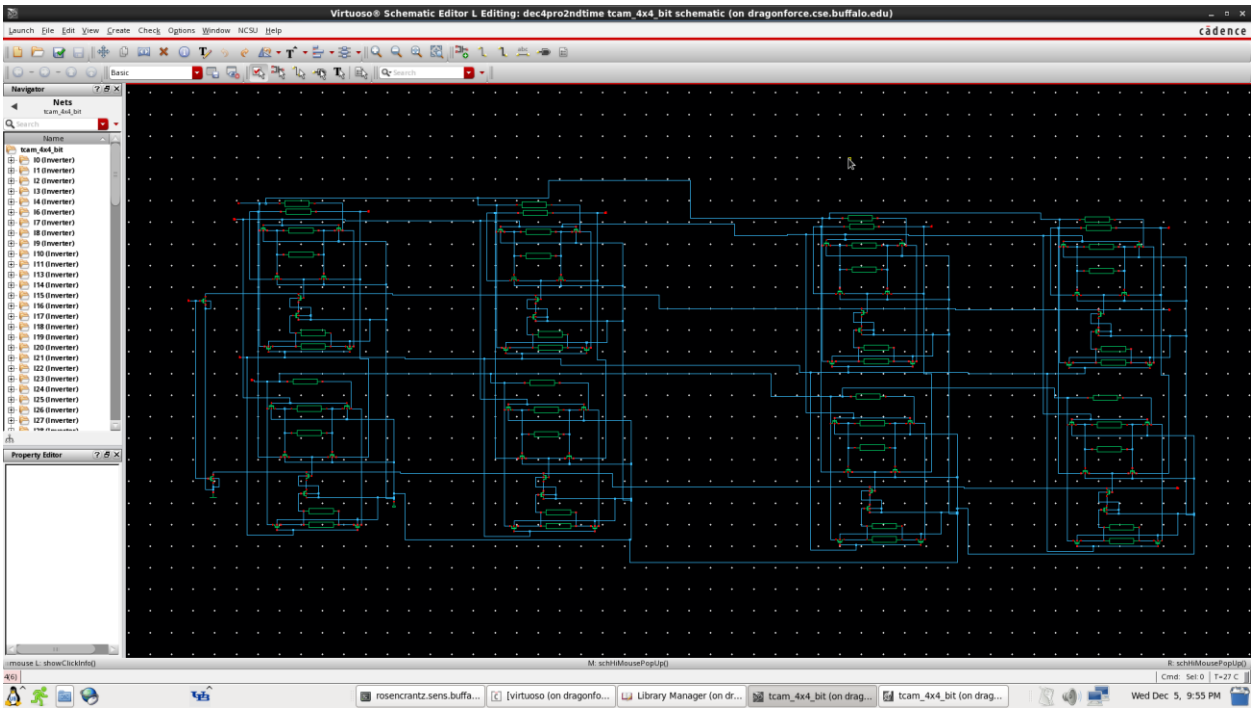

Fig 8: Schematic *for 2x4 TCAM array*

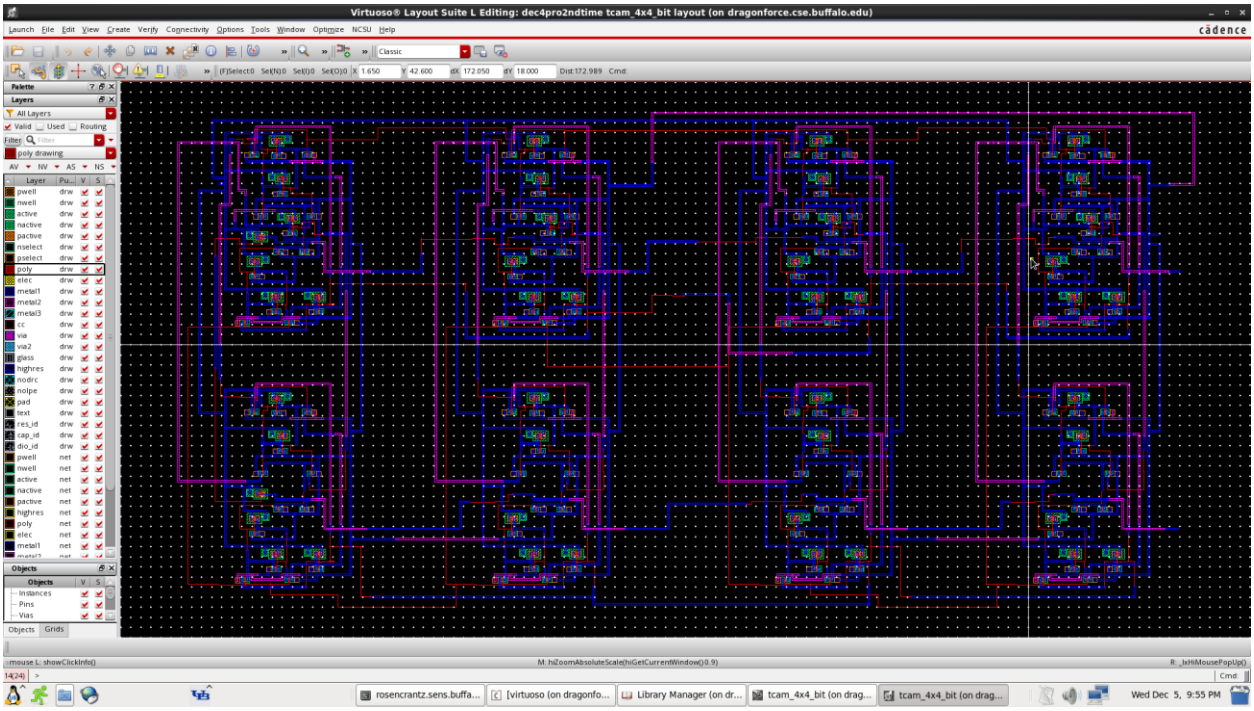

Fig 8: *Layout for 2x4 TCAM array*

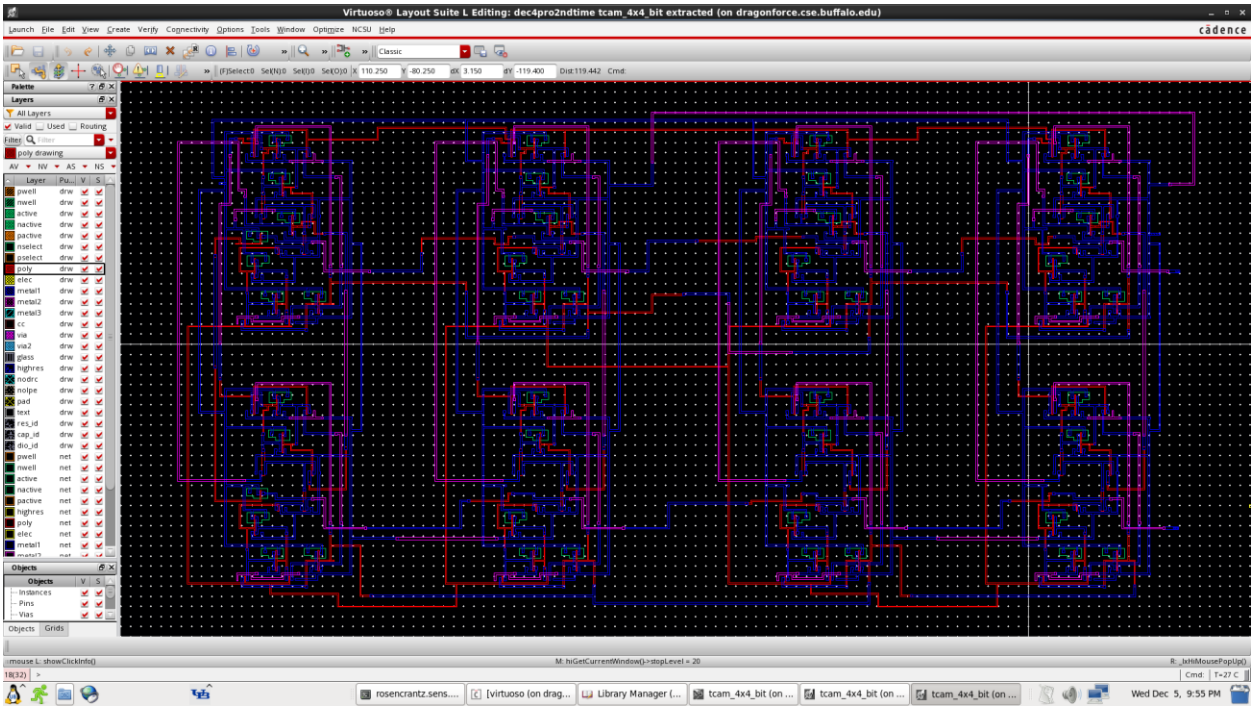

Fig 9: *Extracted view for 2x4 TCAM array*

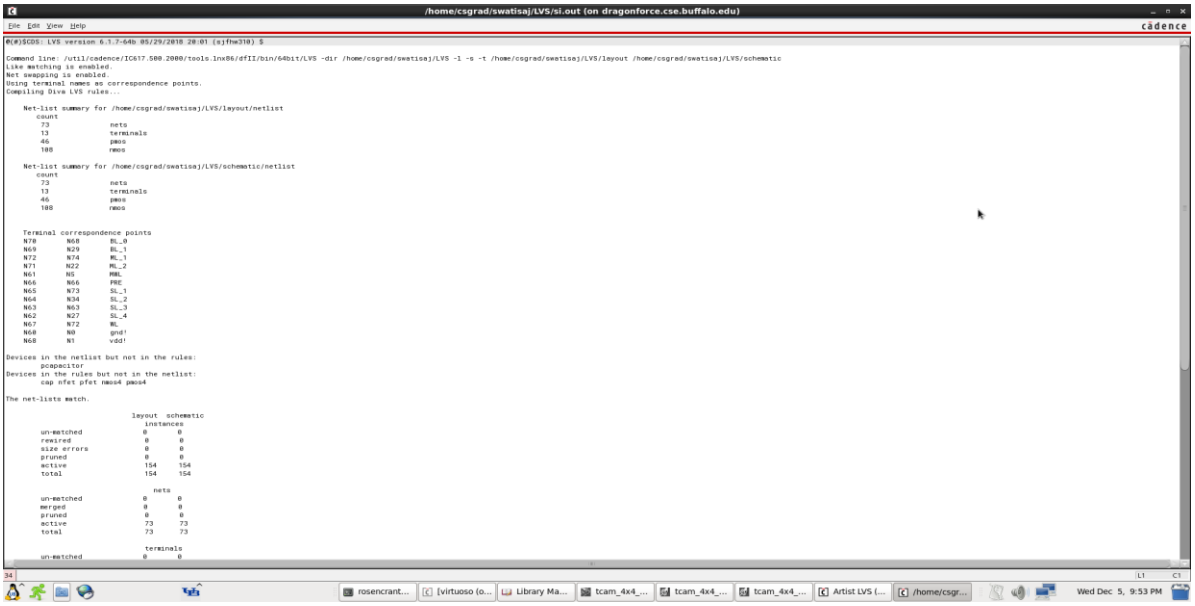

Fig 10: LVS Match

SIMULATION RESULTS

Fig 10: Simulation results for schematic when mask bit =1

When we give mask bit as 1, and when the search data is 1100, the second match line is high. Rest all are low except during the precharge time.

Fig 11: Simulation results for schematic when mask bit =0 for word line 2 and 3

Since we have masked the data bits in ML_3 and ML_2 as 11xx and 110x respectively, and since we are searching for data 1100 both ML_2 and ML_3 are high.

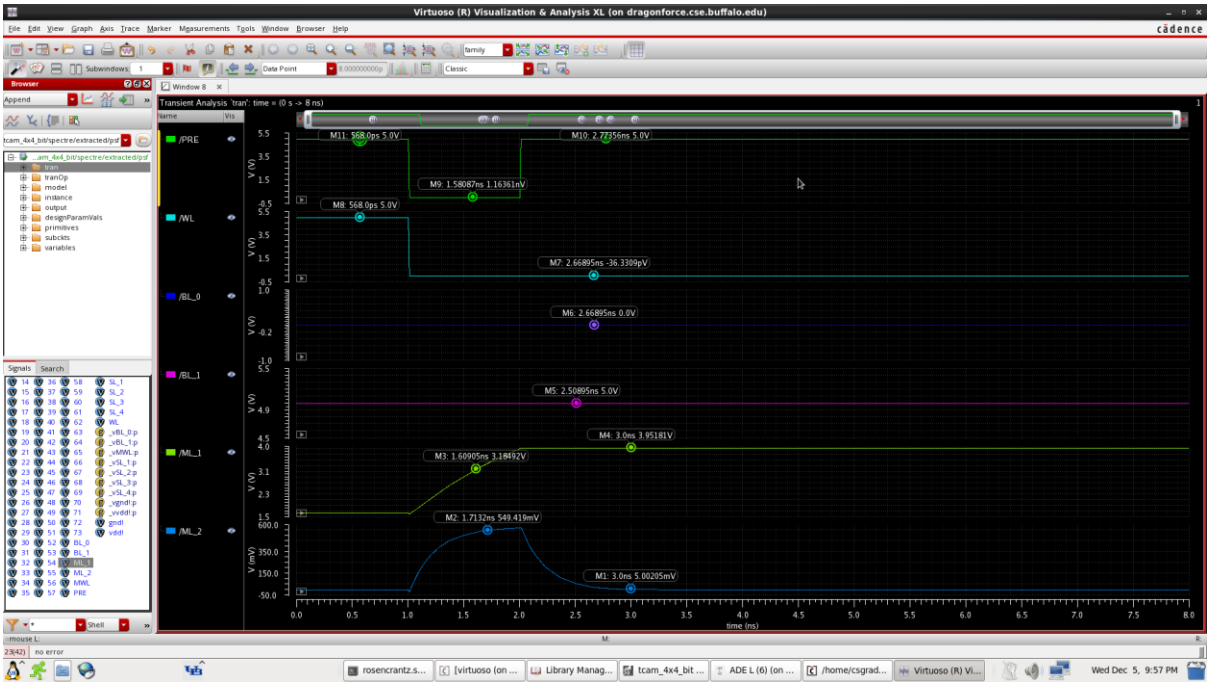

Fig 12: Simulation results for extracted view of 2x4 bit TCAM

The previous simulation result shows the output for the extracted view of 2x4 bit TCAM, where the data stored in first word line is 0000 and that in second word line is 1111. The searched data is 0000. Thus ML_1 is set as high.

PAD FRAME OUTPUT:

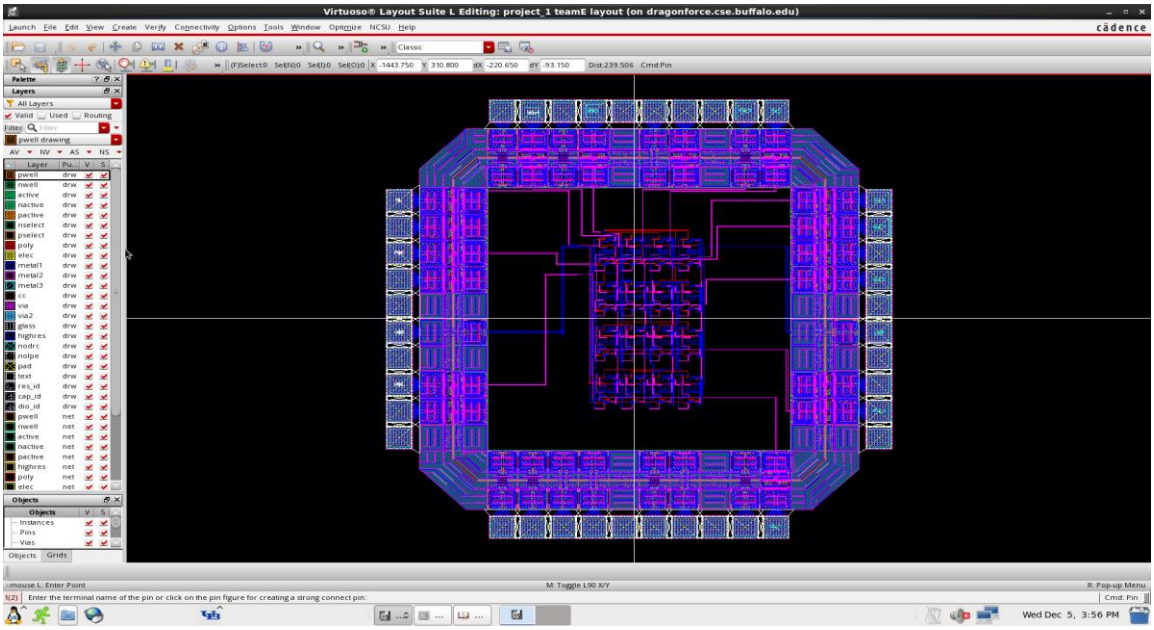

Fig 13: Pad frame layout for 4x4 bit TCAM

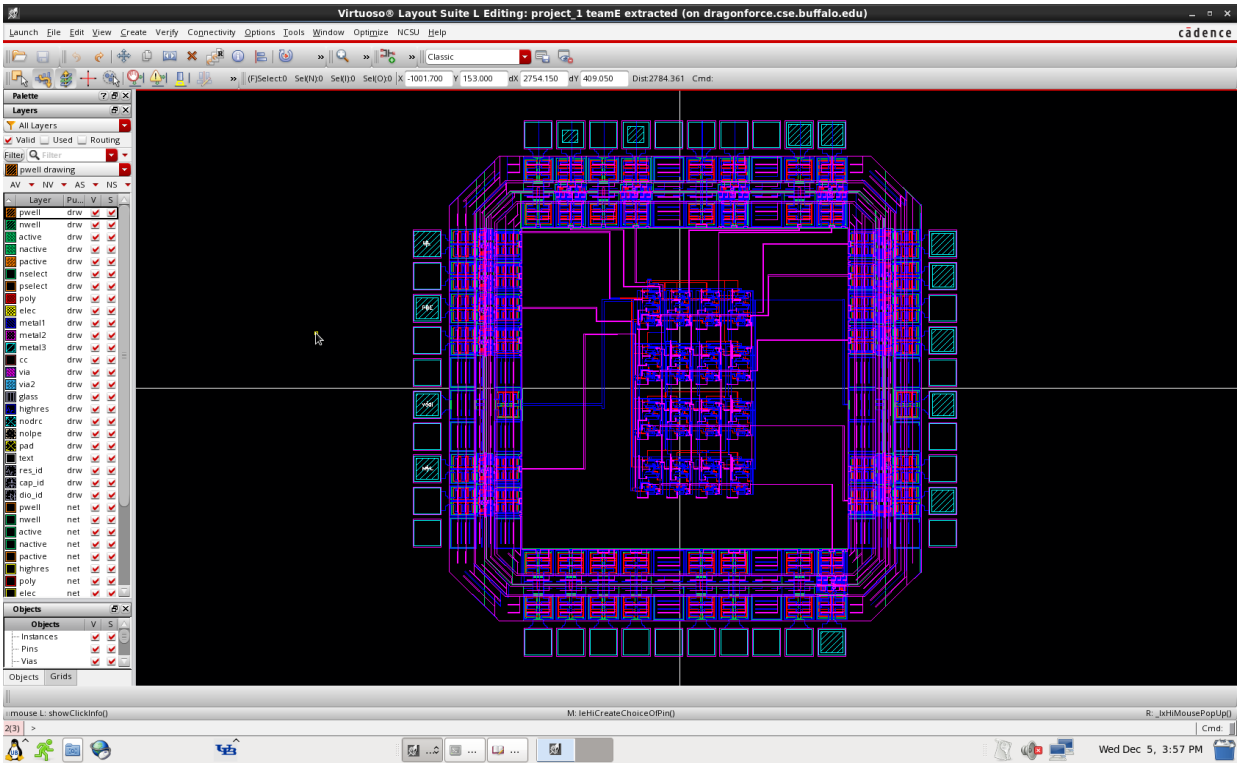

Fig 14: Pad frame extracted view for 4x4 bit TCAM

Fig 15: Pad frame output for 4x4 bit TCAM

Advantages of TCAM over software approaches

- Software based approaches eg: Binary Search
  Drawbacks: Look up table must be ordered
  Complexity : ***O(log n)*** where n is number of total bits
- CAM can be of two types Binary CAM and TCAM
  The max complexity is : ***O(l)*** where l is the length of word line
  TCAM has an evaluation circuit reducing the search time.

Future scope and Conclusion

- TCAM can highly be used in industries where speed is the major concern. For example in routers, switches, and IOT devices
- In order to reduce the power consumption of TCAM for its profound use in hardware:
  - Selective pre-charging of match line
  - By minimizing the signal swing in the match line either by reducing the pre-charge and discharge levels
  - Implementing various architectures such as Butterfly TCAM , Ripple pre-charge TCAM to decrease the power consumption

References

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[2] D. Brooks, P. Bose, V. Srinivasan, M. Gschwind, P. G. Emma, and M. G. Rosenfield. New methodology for early-stage, micro architecturelevel power-performance analysis of microprocessors. IBM Journal of Research and Development, 47(5/6), 2003.

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