**COA LAB 28-08-2023 Monday**

**Assignment Number :** Verilog\_Assgn\_3 **Problem Number :** 1

**Group Number :** 9 **Semester :** AUTUMN 2023

**Group Members :**

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**ALU :**

* Top-level module with 3 inputs : operand1 (r1), operand2 (r2), operator (op) & output (out).
* All 8 each of the eight functions, are instantiated.
* Based on input operator (op) using a switch-case output will be taken from respective functions.

**ADD :** Implemented 8-bit carry look ahead full adder using 4-bit carry look ahead adders.

**SUB :** Implemented subtractor by adding subtrahend’s (i.e., operand2 => r2) 2’s compliment to the minuend (i.e., operand1 => r1).

**INIT :** Outputs the given operand.

**LEFT SHIFT :** Shifts every bit by 1 towards left => effectively multiplies by 2.

**RIGHT SHIFT :** Shifts every bit by 1 towards right => effectively divides by 2.

**AND :** Computes bitwise AND of operand1 (r1) and operand2 (r2).

**OR :** Computes bitwise OR of operand1 (r1) and operand2 (r2).

**NOT :** Computes bitwise compliment of given operand.

**TEST BENCH DATA :**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **r1** | **r2** | **op** | **out** | **Actual Output** |
| 5 | 20 | 0 | 25 | 25 |
| 170 | - | 6 | 85 | 85 |
| 96 | 69 | 1 | 27 | 27 |
| 33 | - | 2 | 33 | 33 |
| 255 | - | 3 | 254 | 254 |
| 255 | - | 4 | 127 | 127 |
| 8 | 7 | 5 | 0 | 0 |
| 8 | 7 | 7 | 15 | 15 |