**COA LAB 30-08-2023 Wednesday**

**Assignment Number :** Verilog\_Assgn\_4 **Problem Number :** 1

**Group Number :** 9 **Semester :** AUTUMN 2023

**Group Members :**

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**Top level module:**

1. Used four states based on **LSB** and **Q-1**namely **oz** (for 10)**, zo** (for 01)**, shift** (for 00),and **shift** (for 11) and a looping accept state when **n** (here 8 bits) shift operations are done.
2. If state = 00 or 11 just called shifter function.
3. If state = 01, called Adder function on **A** (i.e., out[15:8]) and **M** and then changed state to **shift**.
4. If state = 10, called Adder function on **A** (i.e., out[15:8]) and 2’s compliment of **M** (~M) and then changed state to **shift**.