**COA LAB 11-09-2023 Wednesday**

**Assignment Number :** Verilog\_Assgn\_6 **Problem Number :** 1

**Group Number :** 9 **Semester :** AUTUMN 2023

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Implemented 8, 4 bit registers using 3 bit register codes. Initialised memory block with 16, 4 bit numbers using Single Port DRAM.

Top Module has input ports 2 bit opcode, 3 bit regcode, 4 bit memloc, 4 bit data, clock and out for operation code, register to read from/write to, memory location to read from/write to.

Using a 4 bit opcode to operate the given 4 operations:

1. For opcode = 0: We load data into memloc by mapping them to appropriate variables of mem\_block module and setting both ena (enable) and wea (write enable) to 1 each.
2. For opcode = 1: We load data from regcode into meloc by mapping them to appropriate variables of mem\_block module and setting both ena (enable) and wea (write enable) to 1.
3. For opcode = 2: We load data from memloc into regcode by mapping them to appropriate variables of mem\_block module and setting ena (enable) to 1 to read from and wea (write enable) to 0, so that we don’t change the value in the memloc by accident to some arbitrary value in data.
4. For opcode = 3: We load data from memloc by mapping it to appropriate variable of mem\_block module and setting ena (enable) to 1 to read from and wea (write enable) to 0, so that we don’t change the value in the memloc by accident to some arbitrary value in data.

out of top module (reg2mem) is passed as out into mem\_block module as well so as soon as mem\_block returns an output out top module shows it in the wave simulator.