HARSHITH REDDY

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EDUCATION

Birla Institute of Technology and Science, Pilani, India **Aug 2022 – Present**

Bachelor of Engineering, Electronics and Communication Engineering, **CGPA: 8.99 /10**

Relevant Courses: RF Microelectronics, Advanced Analog & Mixed Signal Design, Analog & Digital VLSI Design, Analog Electronics, Digital Design, Microelectronic Circuits.

RESEARCH INTERESTS

Analog, RF and Mixed-Signal IC Design, RF/mm-Wave/THz Transceivers, Radar & Biomedical Imaging and Sensing

SKILLS

CAD Tools: Virtuoso-L/XL/GXL/ADE Assembler, Altium-PCB-Designer, KiCAD, LTspice, Ansys RaptorX
Software/Languages: Python, C, Unix, MATLAB, Verilog, AWS/Azure, SPICE
Technology Nodes: UMC-28/65/90nm, TSMC/SCL-180nm

EXPERIENCE

Analog Design Intern - Texas Instruments, Bengaluru, INDIA **May 2025 – July 2025**

Project: Input Bandwidth Extension and Impedance Matching Network Design (on die) for a high-speed ADC

- Designed a bridged T-Coil (on-die) for a 6-GSPS interleaved ADC, that improved the input bandwidth from 4.5GHz to 8.8GHz with an S11 under -14 dB, utilizing less than 0.015 mm^2 area (differential). Used *Ansys RaptorX* for electromagnetic extraction and optimized the T-Coil for an FCBGA package.
- Designed and optimized a Matching Network and a T-Coil to account for wire bond parasitics for a 6-GSPS ADC with QFN package, which increased the input bandwidth from 3.8GHz to 8.2GHz, and S11 under -12dB.
- Designed a robust and simple Matching Network (on die) to suppress impedance ripples caused by FCBGA substrate routing and die bump parasitics for a 12-GSPS time-interleaved ADC.
- Secured a 6-month internship extension from January to June 2026 in the high-speed ADC group.

System Design Intern - PNT Robotics & Automations Solutions LLP, INDIA **May 2024 – July 2024**

Project: Industrial Water Tank Monitoring System

- Designed a Water Tank Monitoring System with an STM32 Microcontroller, Buoyancy Sensor, Real-Time Clock (RTC), relay switches and a Global System for Mobile Communication (GSM) Module.

ACADEMIC PROJECTS

Design of a Capacitor flip-over Multiplying Digital-to-Analog Converter (MDAC) **Oct 2025 – Nov 2025**

- Designed a fully differential two-stage folded cascode Op-Amp with gain-boosting in 45-nm CMOS, with DC gain = 82 dB, GBW = 530 MHz, Phase Margin = 61°.
- Utilized switched-capacitor common-mode feedback and bootstrapped switches to design an x2 gain MDAC, with sample rate = 100 MSPS, settling time = 3.1 ns, power = 9.3 mW.

Design of a Low Dropout Regulator (LDO) **Sept 2025 – Oct 2025**

- Designed a PMOS pass transistor LDO in 180-nm TSMC with V_{out}= 1.5 V and max. load current of 21 mA.
- Loop Gain = 55 dB, Phase Margin = 87°, PSRR = -58 dB, Load Regulation = 0.36 mV/mA, Transient Peaking when load is switched for Full Swing = 84 mV, Power = 0.9 mW.

Design of a Zero-IF Double-Balanced Active Down Conversion Mixer **Mar 2025 – Apr 2025**

- Designed a 2.4 GHz zero-IF double-balanced gilbert cell mixer in UMC 28-nm CMOS.
- Conversion Gain = 10.6 dB, IIP3 = 3.0 dBm, NF = 9.7 dB, Power = 2.9 mW.

Design of a mm-Wave Low-Power and Variable-Gain Low Noise Amplifier **Feb 2025 – Sept 2025**

- Designed a 4.5 mW two-stage cascode common-source LNA in UMC 28-nm CMOS, using gate-to-source magnetic coupling feedback for input & noise matching, forward body-biasing, and a unique approach to gain variation using an AC-coupled transistor.
- At highest gain: Gain: 21 dB @ 40 GHz, IIP3 = -7.8 dBm, P_{1dB} = -21 dBm, NF = 2.8 dB.
- At lowest gain: Gain: 15 dB @ 40 GHz, IIP3 = 1.2 dBm, P_{1dB} = -14.8 dBm, NF = 5.5 dB.

Design Projects as part of the course, Analog and Digital VLSI Design – ECE F313 **Sept 2024 – Nov 2024**

- Designed a 1.8V Miller-compensated Operational Amplifier in TSMC 180 nm, with C_L=2 pF, achieving DC gain = 65 dB, Phase Margin = 60°, GBW = 35 MHz, CMRR = 70 dB, Slew Rate = 30 V/µs, and consuming 430 µW.
- Implemented a 1-bit full adder in TSMC 180 nm, using transmission-gate logic to reduce footprint to 320 µm^2.

Design of a Novel Low TC and Low-Voltage CMOS Voltage Reference **Aug 2024 – Mar 2025**

- Designed a fully integrated CMOS voltage reference in 90-nm process, utilizing low threshold voltage (LVT) transistors in subthreshold region to reduce supply voltage to 0.5V and power to 0.67 µW.
- Utilized a novel curvature compensation to reduce temperature coefficient to 16.28 ppm/°C (-40 °C to 130 °C).
- V_{ref} = 205 mV, Supply Voltage Sensitivity = 1.65 %/V, PSRR = -50 dB

PUBLICATIONS

1. **Harshith Reddy** and Pankaj Arora, "A 40 GHz Low-Power Variable-Gain Low Noise Amplifier in 28-nm CMOS Process," in *Proceedings of the 13th IEEE International Conference Intelligent Embedded, MicroElectronics, Communication and Optical Networks (IEMECON)*, Jaipur, December 2025. - https://arxiv.org/pdf/2512.00443

2. **Harshith Reddy** and Pankaj Arora, "A 16.28 ppm/°C Temperature Coefficient, 0.5 V Low-Voltage CMOS Voltage Reference with Curvature Compensation," in Proceedings of the 29th International Symposium on VLSI Design and Test (VDAT), Chandigarh, August 2025. - https://arxiv.org/pdf/2508.15729

EXTRA-CURRICULAR / VOLUNTEERING

Teaching Assistant – ECE F434 Digital Signal Processing **Aug 2025 – Dec 2025**

- Assisted in conducting lab sessions with a course strength of 150 students, guiding them to implement DFT, IIR/FIR filters, Windowing etc. in MATLAB, and, FFT and simple filters using Verilog and TI DSP kits with C.

Teaching Assistant – ECE F244 Microelectronics Circuits **Jan 2025 – May 2025**

- Assisted in conducting two demonstrative sessions for LTspice and a lab exam with a course strength of 350.
- Clarified students doubts regarding their project-based assignments and evaluated the assignments.

Electrical Subsystem Lead, **CRISS Robotics** **April 2023 – Mar 2025**

- Led a team of 6 members in designing and implementing the electrical system for a Mars Rover prototype, competing in international Rover building competitions like IRC, IRDC, and URC.
- Designed, fabricated, and tested full-fledged PCBs (Printed Circuit Boards) using Altium for robust and modular *Power*, *Arm,* and *Drive* of the rover, controlled by *ESP32* and *Raspberry Pi*.
- Implemented an intra-rover communication network using CAN bus and rover-base station communication using *Ubiquiti's airMAX 2.4 GHz* omni and sector antennas with Python, *sockets,* and *SSH*.

Other Interests/Hobbies:- Acoustic Drums (musical instrument), Basketball, hiking/trekking, Robotics.