A 16.28 ppm/°C Temperature Coefficient, 0.5V Low-Voltage CMOS Voltage Reference with Curvature Compensation

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Abstract—This paper presents a fully-integrated CMOS voltage reference designed in a 90 nm process node using low voltage threshold (LVT) transistor models. The voltage reference leverages subthreshold operation and near-weak inversion characteristics, backed by an all-region MOSFET model. The proposed design achieves a very low operating supply voltage of 0.5 V and a remarkably low temperature coefficient of 16.28 ppm/°C through the mutual compensation of CTAT, PTAT, and curvature-correction currents, over a wide range from -40 °C to 130 °C. A stable reference voltage of 205 mV is generated with a line sensitivity of 1.65 %/V and a power supply rejection ratio (PSRR) of -50 dB at 10 kHz. The circuit achieves all these parameters while maintaining a good power efficiency, consuming only 0.67 μW.

Index Terms—CMOS voltage reference, temperature compensation, Subthreshold, power efficient.

I. INTRODUCTION

In most system-on-a-chip (SoCs) systems, a voltage reference insensitive to temperature, supply voltage, process, and mismatch variations is crucial [1]. They are essential components in multiple analog circuit applications such as Analog-to-Digital Converters (ADCs), linear regulators, power management systems, sensors, Internet of Things (IoT), and wearable devices [2]. Most voltage references work by generating two types of currents, namely PTAT (proportional to absolute temperature) and CTAT (complementary to absolute temperature), and summing them to develop a temperature invariant voltage at the output [3]. The most used bandgap voltage reference circuits use lateral BJTs or parasitic BJTs in CMOS process, and op-amps. In a conventional bandgap voltage reference, the base-emitter voltage (V_{BE}) of a bipolar transistor decreases linearly with temperature, exhibiting a CTAT characteristic. A PTAT voltage is generated by the difference in V_{BE} between two bipolar transistors operating at different current densities. A bandgap reference circuit combines these CTAT and PTAT voltages to produce a stable reference voltage (V_{REF}) close to the silicon bandgap voltage of 1.2 V [4]. As CMOS technology advances, ADCs and other circuits require lower operating voltages and power-efficient performance. The start-up voltage of low-power ADCs is constrained by the minimum voltage needed for the voltage reference operation. Lowering its supply voltage extends ADC runtime and allows operation with harvested voltages as low as 0.5 V [3].

This work presents a purely CMOS-based voltage reference architecture that achieves an excellent temperature coefficient, with a good line sensitivity and a distinctively low operating supply voltage while maintaining power efficiency. Being purely CMOS based makes this design better compatible with a larger set of process technologies and helps achieve operating voltage by the use of low threshold transistor models and subthreshold operation. This paper is divided into four sections. Section II analyzes in detail the working of the proposed architecture. This section is subdivided into four parts to describe the different segments of the circuit – PTAT, CTAT, curvature compensation, and output reference generator. Section III discusses the simulation results achieved in this paper. Concluding remarks are made in Section IV.

II. PROPOSED DESIGN

A. PTAT Circuit

The core part of the PTAT circuit as shown in Fig. 1 that generates the PTAT current are two MOSFETs, M_1 and M_2, operating in subthreshold region, having a similar I-V characteristics to that of a BJT, and also because of which power efficiency is significantly improved. The aspect ratios of M_1 and M_2 are such that, M_2 is N_p times larger than M_1 as marked in the schematic Fig. 1, and the leakage currents, that can be defined by equation (1), of transistors M_1 and M_2 are set equal by the cascode current mirrors M_3, M_4, M_5, and M_6. Cascode current mirror helps in improving the line sensitivity of the voltage reference and reduces the voltage drop across MOSFETs M_1 and M_2, for them to persist in the subthreshold region across large temperature and power supply variations. The resistor R_1 is necessary for maintaining a voltage drop between the gate voltages of M_1 and M_2 as a
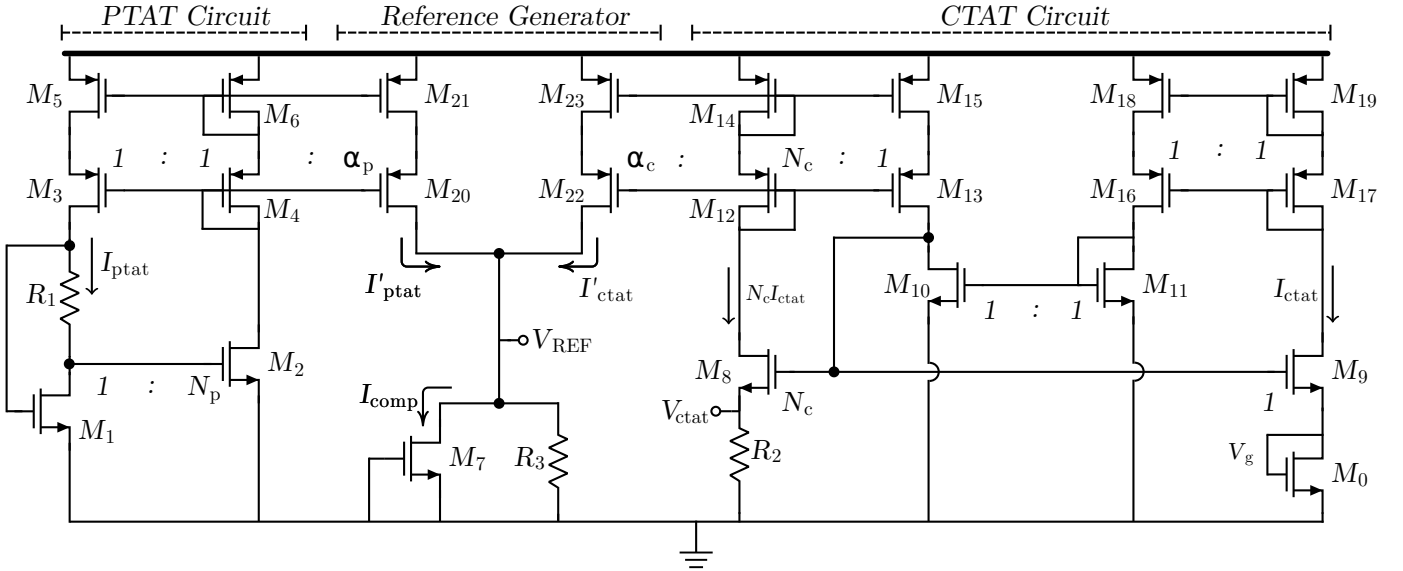
Fig. 1: Schematic diagram of the proposed voltage reference circuit

function of temperature. The subthreshold leakage current I_{ds} can be given as [5]

$$I_{ds} = I_{ds0} e^{\frac{V_{gs} - V_{th}}{n v_T}} \left(1 - e^{-\frac{V_{ds}}{v_T}}\right) \quad (1)$$

where n is a process dependent factor caused by the depletion region characteristics and is typically in the range of 1.3 – 1.7 [5]. The gate to source voltage is indicated as V_{gs}, V_{ds} is the drain to source voltage, and V_{th} is the threshold voltage. The last term, i.e. $\left(1 - e^{-\frac{V_{ds}}{v_T}}\right)$, can be approximated to 1 as the V_{ds} of M_1 and M_2 will be biased at a voltage of at least 150 mV which is a few multiples greater than v_T even at higher temperatures (34.6 mV at 130°C). The ηV_{ds} term in the equation 2.42 from [5] caused due to drain-induced barrier lowering has been neglected to make calculations simpler, which can later be curvature compensated including other non-linearities. The coefficient I_{ds0} is given as [5]

$$I_{ds0} = u_n C_{ox} \frac{W}{L} v_T^2 e^{1.8} \quad (2)$$

μ_n, C_{ox}, v_T and $\frac{W}{L}$ are as usual the electron mobility, per unit area gate oxide capacitance, thermal voltage and the aspect ratio of the MOSFET respectively. Now, as both the drain currents of M_1 and M_2 are set equal, we can say

$$\frac{I_{ds0,2}}{I_{ds0,1}} = e^{\frac{V_{gs1} - V_{gs2} - (V_{th1} - V_{th2})}{n v_T}} \quad (3)$$

If we can assume that the two threshold voltages are approximately equal (although practically they would be slightly off, which would just result in an additional constant close to 1 multiplied to our final expression), the numerator in the exponent will just result in $V_{gs1} - V_{gs2} = I_{ds1} R_1$. Take natural log on both sides in equation (3) we get

$$ln\left[\frac{(\frac{W}{L})_2}{(\frac{W}{L})_1}\right] = \frac{I_{ptat} R_1}{n v_T} \quad (4)$$

if we can call $I_{ds1} = I_{ds2} = I_{ptat}$. As discussed earlier, if $(\frac{W}{L})_2 : (\frac{W}{L})_1 :: N_p : 1$, the final expression for I_{ptat} can be derived as

$$I_{ptat} = \frac{n v_T}{R_1} ln N_p \quad (5)$$

Hence we can say that the leakage currents of M_1 and M_2 have a PTAT nature, whose strength and the slope can be adjusted by altering N_p or the ratio of the sizes of M_1 and M_2, and R_1 as can be seen in Fig. 2.

B. CTAT Circuit

The CTAT architecture, as shown in Fig 1, is a modified version of the voltage reference design proposed by F. Olivera and A. Petraglia [1], which exploits the multi-threshold characteristics of a MOS transistor. The unified current control model (UICM) accurately describes transistor behavior across all inversion levels that the conventional square law based models are unable to predict [1]. The core part of the CTAT circuit is the nature of the gate voltage of the MOS transistor M_0, which is copied across the resistor R_2 (labeled V_{ctat}) with N_c times higher current flowing in that branch. The transistors $M_8 : M_9$ and $M_{12}, M_{14} : M_{13}, M_{15}$ are sized in the ratio $N_c : 1$ and, $M_{10} : M_{11}$ and $M_{16}, M_{18} : M_{17}, M_{19}$ are equally sized pairs to realize a CTAT current generator from a CTAT voltage.

The M_0 MOSFET, being diode connected, will operate mostly in forward saturation, and its drain current I_D can be given as [7]

$$I_D = I_S i_f \Rightarrow i_f = \frac{I_D}{I_S} \quad (6)$$

where i_f is the forward inversion level. Weak inversion is indicated by $i_f < 1$, and similarly $1 < i_f < 100$ and $i_f > 100$ for moderate and strong inversion. I_S is the specific current defined by [8]

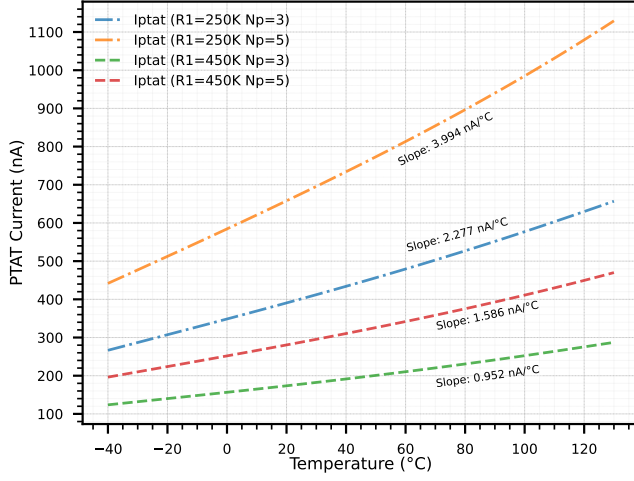$$I_S = 2 n \mu_n C_{ox} \frac{W}{L} v_T^2 \quad (7)$$

Fig. 2: Drain currents of M_1 and M_2 (PTAT) for different R_1 and N_p, vs. temperature

and n is the slope factor. The I-V relationship using UICM can be modeled by [7]

$$V_P - V_S = v_T[\sqrt{1+i_f} - 2 + ln(\sqrt{1+i_f} - 1)]$$
$$= v_T F(i_f) \qquad (8)$$

where, Vp the pinch-off voltage is

$$V_P = \frac{(V_G - V_{th0})}{n} \qquad (9)$$

V_S and V_G are the source and gate voltages w.r.t bulk (gnd), and V_{th0} is the threshold voltage at $V_S = 0$. Equation (8) can be re-written as

$$V_G = V_{th0} + n\frac{k_B}{q}F(i_f) \cdot T \qquad (10)$$

where k_B, q, and T are the Boltzmann constant, electron charge, and absolute temperature, respectively. The first term being the threshold voltage of the MOS transistor expresses a CTAT behavior of approximately -0.43 mV/°C. The sign and magnitude of the function $F(i_f)$ determines the slope of the CTAT voltage across M_0, which is replicated across R_2, with N_c-fold higher current as compared to M_0 drain current. Hence, we can say that $V_{ctat} = R_2 N_c I_{ctat}$. By solving this equation for W/L of M_0, we get [1]

$$\left(\frac{W}{L}\right)_{M_0} = \frac{1}{2N_c R_2} \frac{V_{th0} + n\frac{k_B}{q}F(i_f) \cdot T}{n\mu_n C_{ox} \frac{k_B^2 T^2}{q^2} i_f} \qquad (11)$$

Thus, varying the aspect ratio of M_0 affects the inversion level i_f and the function $F(i_f)$, giving the flexibility to alter the CTAT voltage slope, as shown in Fig. 3(a). In this design, a trade-off between linearity and power efficiency has to be done, but because of the presence of curvature compensation, a lower inversion level can be preferred to reduce power consumption. Additionally, the CTAT current ratio mirrored to the output branch can also be altered by adjusting the value of α_c and N_c, following the proportionality $I'_{ctat} \propto \alpha_c$ and $I'_{ctat} \propto \frac{1}{N_c}$, as also shown in Fig. 3(b).
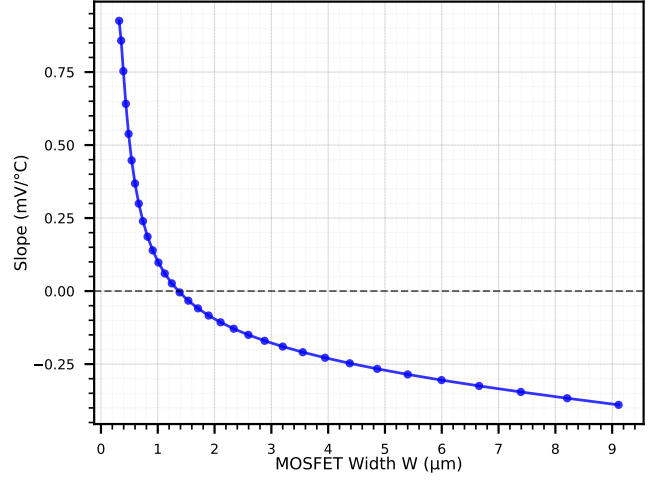
(a)
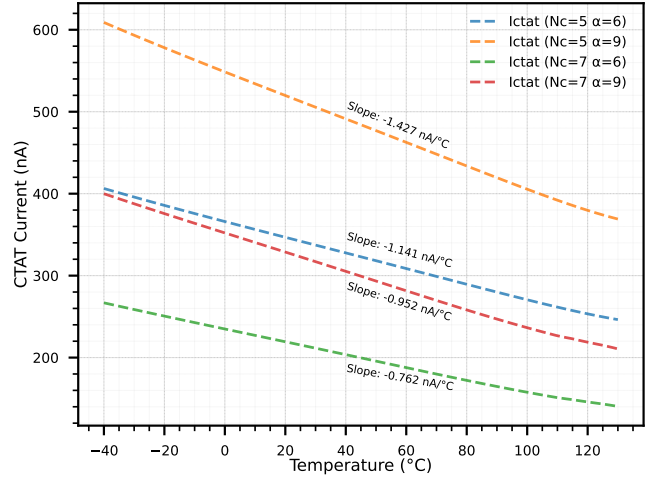
(b)

Fig. 3: CTAT Current characteristics (a) slope of CTAT gate voltage of M_0 vs. width of M_0 with L=10μm (b) CTAT current generated at output branch for different α_c and N_c, vs. temperature

C. Curvature Compensation

To better improve the temperature coefficient performance and extend the operational temperature range, curvature compensation is a widely used technique to reduce the deviation of the output voltage caused due to non-linear effects. The technique used in this design exploits the characteristics of subthreshold leakage current, which has an exponential-like property w.r.t. temperature as can be seen in Fig. 4 because of the CTAT nature of the threshold voltage in the numerator of the exponent term in equation (12). The strength of the curvature compensation can easily be adjusted by varying the aspect ratio of M_7. The subthreshold leakage current can be given by [6]

$$I_{Leak} = \mu_n C_{ox} \frac{W}{L}(\eta - 1)\left(\frac{k_B T}{q}\right)^2 \exp\left(-\frac{q V_{th}}{\eta k_B T}\right) \quad (12)$$
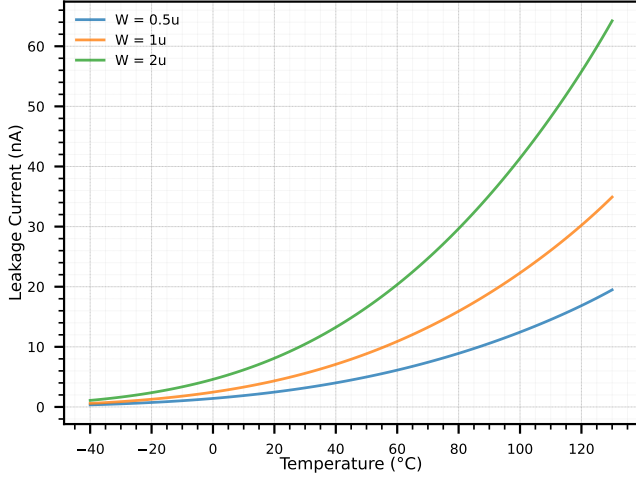
Fig. 4: Subthreshold leakage current of M_7 vs. temperature

Fig. 5: PTAT, CTAT and curvature compensation currents

where η is the subthreshold swing coefficient. The M_7 transistor is placed in parallel to R_3 such that it drains out current exponentially as temperature increases, thereby decreasing the output reference voltage across R_3 and reducing the overall temperature deviation. By carefully choosing the strengths of PTAT, CTAT, and curvature compensation, an excellent temperature coefficient can be achieved.

D. Output Reference Generator

The output voltage generator circuit, as shown in Fig. 1, is realized using cascode current mirrors to enhance its current mirroring capabilities - to improve line sensitivity (i.e., reference voltage variation w.r.t. V_{DD} supply) and power supply rejection [10]. The PTAT and CTAT currents are mirrored and summed to the output branch by ratios of α_p and α_c respectively, through the resistor R_3, generating a voltage that can be given by

$$V_{REF} = R_3(\alpha_p I_{ptat} + \alpha_c I_{ctat} - I_{comp}) \quad (13)$$

The value of V_{REF} is not fixed and variable by adjusting the values of R_3 and current mirror ratios. The proposed circuit was designed to produce a reference voltage of 205 mV.

III. Results Obtained

The voltage reference proposed in this paper has been implemented on a 90 nm CMOS process with the circuit schematic given in Fig. 1. The circuit has been optimized to give an excellent temperature coefficient while being power efficient, with a Quiescent current of 1.3 μA at room temperature. The power consumption ranges from 0.67 μW with a supply of 0.5V to 4.3μW with a supply of 3.3V. The different components of the output current generated, i.e., the CTAT, PTAT, and the curvature compensation current, can be seen in Fig. 5. CTAT current has a slope of -0.549 nA/°C, PTAT has a slope of 0.731 nA/°C, and the curvature compensation current has a best fit slope of 0.194 nA/°C. The slope of the net current I_{REF} flowing through R_3 can be calculated as
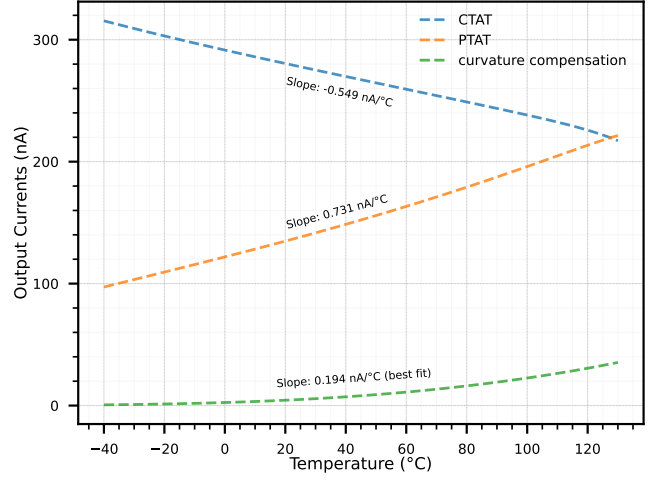
$$I_{REF} = I'_{ptat} + I'_{ctat} - I_{comp}$$

$$\text{Slope}(I_{REF}) = 11 \text{ pA/°C} \approx 0$$

Fig. 6 shows the variation of output voltage V_{REF} versus a wide range temperature of -40°C to 130°C with and without curvature compensation. Without compensation, the circuit has a temperature coefficient of 137 ppm/°C with a maximum deviation of 4.69 mV. However, with compensation, the proposed circuit achieves a brilliant temperature coefficient of 16.28 ppm/°C with a maximum deviation of just 0.57 mV or 570 μV. The reference voltage produced at room temperature (27°C) is 205.5 mV, with a minimum V_{REF} of 205.44 mV at 8°C and a maximum V_{REF} of 206.01 mV at 92°C. Fig. 7(a) shows the voltage supply characteristics of the voltage reference with and without cascode current mirror modification. It can
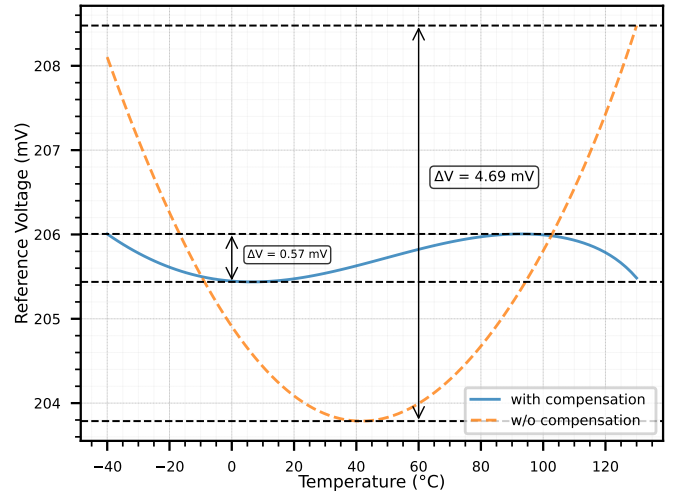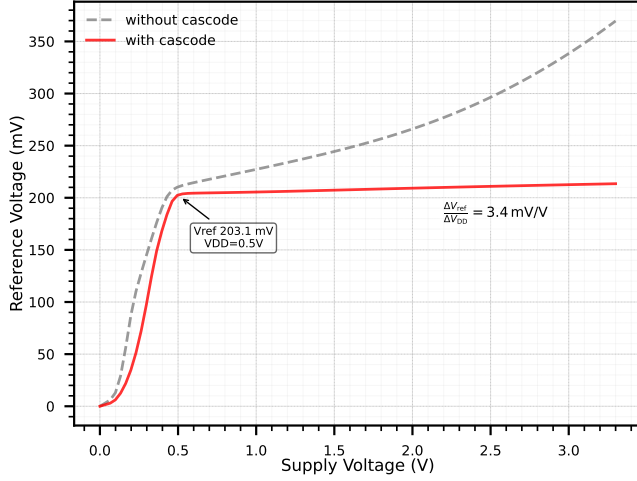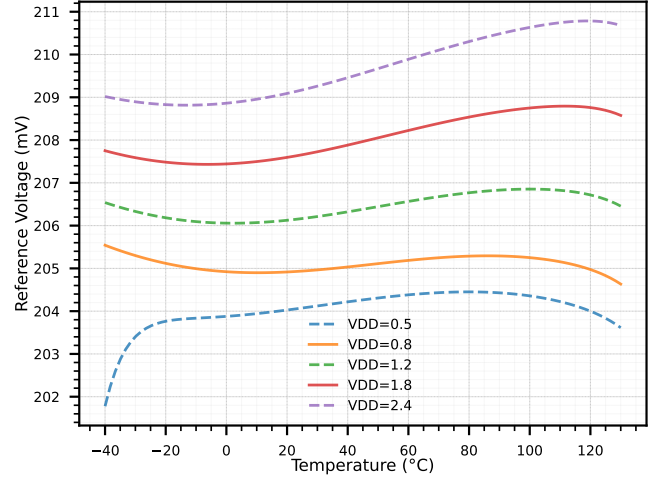

Fig. 6: Variation of output reference voltage (V_{REF}) over a wide temperature from -40°C to 130°C

Fig. 7: V_{REF} vs supply and temperature variation (a) Output reference voltage V_{REF} as a function of supply voltage (with and without cascode) (b) Temperature variation of V_{REF} at different supply voltages

be seen that the modification has significantly lowered the voltage supply sensitivity to having a line sensitivity of just 1.65%/V, which is only about a 3.4 mV increase in V_{REF} voltage for each volt of increase in supply voltage which can also be seen in Fig. 7(b). The voltage reference reaches its nominal value of 205 mV (with less than 1% error) for a tremendously low minimum supply voltage of 0.5 V. The voltage reference nominal supply voltage is 1V and has a wide range of operational voltage starting from 0.5 V to over 3.3 V. Fig. 8 shows the plot of power supply rejection of the proposed voltage reference with and without cascode current mirror modification. From a PSRR of -30 dB, the voltage reference achieves a PSRR of -50 dB up to a frequency of 10 kHz with the modification. The circuit also achieves a PSRR of -41 dB at a high frequency of 100 kHz.

Fig. 9, 10, and 11 demonstrate the Monte-Carlo simulation results of 100 samples to predict the voltage reference performance under PVT variations. Fig. 9 depicts the reference voltage variation, with a mean μ of 204.85 mV and a standard derivation σ of 9.06 mV. In Fig. 10, the average temperature coefficient is 16.28 ppm/°C with a standard derivation of 7.23 ppm/°C. The minimum of all samples is as low as 6.3 ppm/°C. Fig. 11 shows an average line sensitivity of 1.65 %/V with a minimum of 1.43 %/V for the supply voltage range between 0.5 V and 3.3 V.

IV. CONCLUSION

This paper presents a fully-integrated CMOS voltage reference using low voltage threshold transistors in a 90 nm process node. The reference voltage attains independence of temperature variation by the mutual compensation of PTAT, CTAT, and curvature compensation currents. By exploiting subthreshold and weak inversion characteristics of MOSFETs, the design achieves a very low temperature coefficient, line sensitivity, and power consumption. Monte-carlo simulations
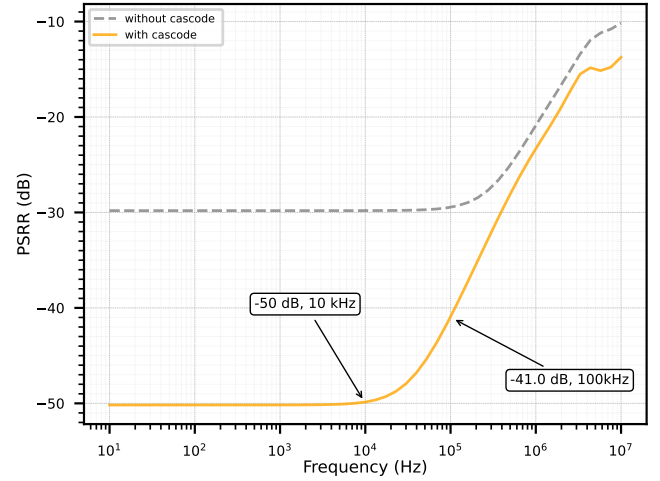

Fig. 8: Power Supply Rejection (PSRR) of the voltage reference (with and without cascode)

show a reference voltage of 204.85 mV with a temperature coefficient of 16.28 ppm/°C in wide range of -40 °C to 130 °C, consuming just 0.67 μW at a 0.5 V supply and 1.3 μW at a 1 V supply. The performance summary and comparison with recent works are given in Table 1.

Parameter	Ref. [1]	Ref. [3]	Ref. [6]	Ref. [10]	**This Work**
CMOS Process	0.18 μm	65 nm	0.18 μm	0.25 μm	90 nm
Min. Supply Voltage (V)	1.2	0.7	1	2.5	0.5
Supply Range (V)	1.2–1.8	0.7–3	1–2.4	2.5–4.5	0.5–3.3
Ref. Voltage (mV)	512.8	223	575	1184	205
Power Consumption (μW)	5.64	0.075	1.212	122	0.67
Line Sensitivity (%/V)	0.28	2.54 (>0.7V)	0.1	-	1.65
PSRR (dB)	-42 dB @ 100Hz	-62 dB @ 1kHz	-	-80 dB @ 1kHz	-50 dB @ 10kHz
Temp. Range (°C)	0 to 100	-60 to 160	-30 to 120	-40 to 130	-40 to 130
Temp. Coefficient (ppm/°C)	41	19.47	52.1	15.23	16.28

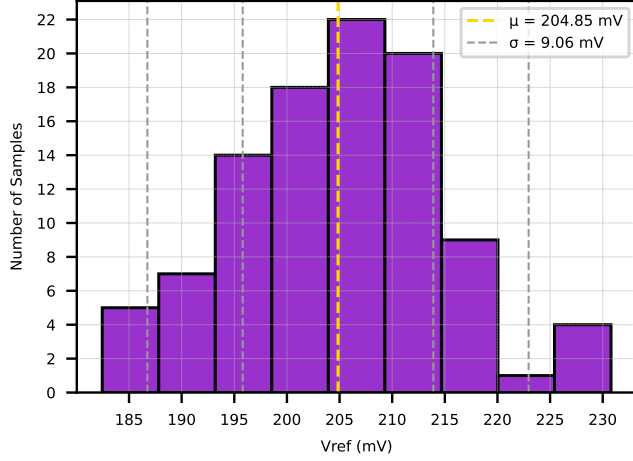TABLE I: Performance comparison with state-of-the-art voltage references

Fig. 9: Process Variation of reference voltage V_{REF} for 100 samples (Monte-Carlo)
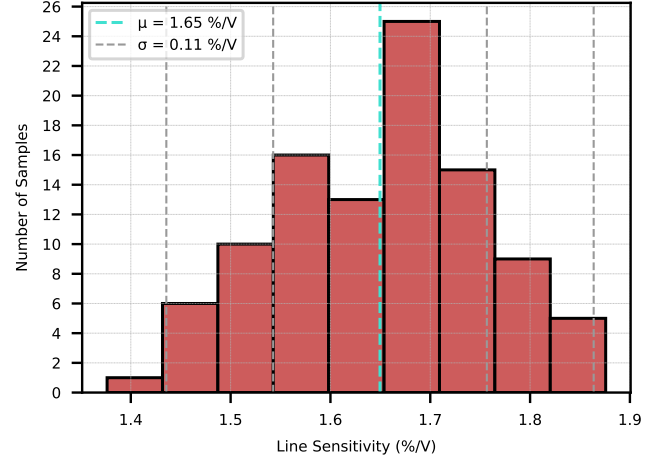

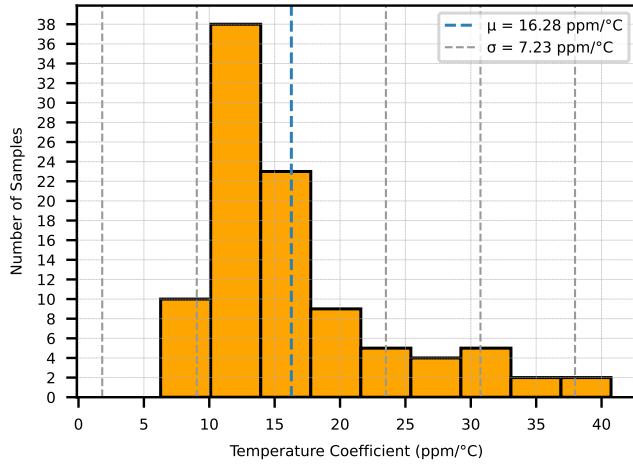Fig. 11: Process Variation of line sensitivity for 100 samples (Monte-Carlo)

Fig. 10: Process Variation of temperature coefficient for 100 samples (Monte-Carlo)

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